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# A 175 GHz HBV Frequency Quintupler With 60 mW Output Power

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**Abstract**—In this letter, we present a fixed tuned 175 GHz frequency quintupler with 60 mW output power. The peak efficiency is 6.3% and the 3-dB bandwidth is 8 GHz. The multiplier is based on a single Heterostructure Barrier Varactor (HBV) diode that is flip-chip soldered into a microstrip matching circuit. All the matching is done “on-chip” and there is no need for DC bias. The multiplier block is very compact (25 x 9 x 8 mm<sup>3</sup>).

**Index Terms**—Frequency multipliers, HBV, millimeter wave, Terahertz sources, harmonic generation, varactors

## I. INTRODUCTION

FREQUENCY multiplication is the standard solution to produce power at millimeter wave frequencies [1] where the fabrication and phase-locking of fundamental oscillators is difficult. Typically, a number of separate multipliers are cascaded to reach frequencies beyond 100 GHz. The workhorse of these multiplier chains are Schottky diode multipliers (x2, x3) that can be used up to, and even beyond, 1 THz [2]. Transistor based MMIC multipliers are rapidly improving and have been demonstrated at millimeter wave frequencies [3].

In this letter, we present a multiplier module with high multiplication factor (x5) that in a single step produces 60 mW of output power at 175 GHz, starting from 35 GHz - a microwave frequency that is readily commercially available. The module operates without any bias and consequently there is no DC-connection between the circuit and the outside world, which virtually eliminates the sensitivity towards ESD. The combination of high multiplication factor, high output power and a compact package makes this design competitive with respect to Schottky or MMIC technology for applications where the limited 3-dB bandwidth (4.6%) can be accepted.

The non-linear element used for the frequency multiplication is a heterostructure barrier varactor (HBV) diode [4], with a layout that is tailored for high output power.

Special attention has been paid to the thermal design of the device to ensure proper heat-sinking [5],[6]. To further improve the thermal properties, the microstrip circuits are fabricated from AlN, a material that has good thermal conductivity ( $\sim 170 \text{ W m}^{-1} \text{ }^\circ\text{C}^{-1}$ ).

## II. HBV DEVICES

The HBV diode fabrication consisted of three major process steps: First, the ohmic contacts were defined using an optical lithography and lift-off process. The metal-stack for the ohmic contacts was: Ni/Ge/Au/Ti (10nm/50nm/250nm/200nm). The Ti-layer was used as an etch-mask when the diode mesas were defined in a CH<sub>4</sub> dry-etch process. Secondly, by wet etching in a H<sub>2</sub>O<sub>2</sub>:H<sub>3</sub>PO<sub>4</sub>:DI (1:1:25) solution, the diodes were isolated. The last process step was to form air bridges. The air bridges were plated in a gold solution to a thickness of 2.5  $\mu\text{m}$ . Finally, the diodes were diced and flip-chip soldered onto the circuits. In Fig. 1, a scanning electron microscope picture of an HBV diode is shown. The device consists of 4 diode mesas connected in series with a total of 12 barriers (3 barriers per mesa) and 500  $\mu\text{m}^2$  device area per mesa. A single barrier layer consist of an InGaAs/InAlAs/AlAs/InAlAs/InGaAs (5nm/5nm/3nm/5nm/5nm) structure. The undoped barriers are separated by a Si doped ( $1 \times 10^{17} \text{ cm}^{-3}$ ) InGaAs modulation layer, details of the epi structure can be found in [7]. The DC measurements showed a maximum capacitance of 0.87 pF/barrier and a breakdown voltage of 50 V. The current-voltage and capacitance-voltage characteristics of a measured device are presented in Fig. 2.

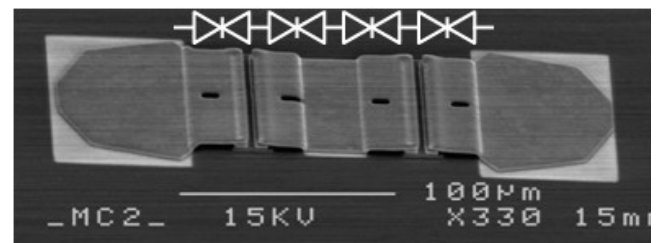


Fig. 1. SEM picture of an HBV diode on chip. The 4 diode mesas, each with an area of 500  $\mu\text{m}^2$ , are contacted by air bridges. The pads are 100  $\mu\text{m}$  x 65  $\mu\text{m}$  in size and are used to flip-chip solder the device onto a microstrip circuit.

## III. CIRCUIT DESIGN

A non-linear device typically produces harmonics of the fundamental frequency that is used to drive the device. This

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means that the circuit design becomes more complex with higher multiplication factor, since all the intermediate harmonics must be terminated in proper impedances in order for the multiplier to operate well [8],[9]. The HBV device has a symmetric capacitance-voltage characteristic (Fig. 2), which intrinsically generates only odd harmonics – this simplifies the circuit design and allows for the design of higher-order multipliers [10]-[13].

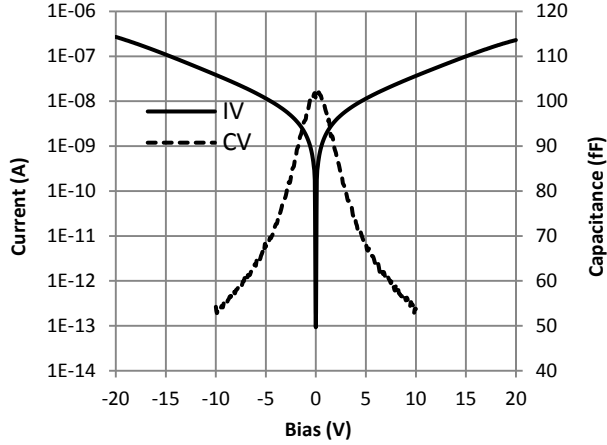


Fig. 2. Measured current-voltage characteristic and capacitance-voltage characteristic of a device with the layout shown in Fig. 1.

The HBV device model used in the circuit design is a quasi-empirical electro-thermal model developed at Chalmers [6]. This device model is implemented in Agilent ADS and is used together with the harmonic balance simulator to calculate the optimum embedding impedances for the diode and to do the final simulations of the multiplier performance.

The optimum embedding impedances for the HBV diode chip are calculated by first simulating a 3D model of the diode chip in Ansoft HFSS, to create an S-parameter file for the diode chip. This S-parameter file is then used together with the electro-thermal diode model to calculate the embedding impedances, using an optimization routine in the harmonic balance simulator. The optimum embedding impedances for the diode, calculated with reference planes at the start of the airbridges, are:  $Z_1=27+95i$  Ohm,  $Z_3=0+15i$  Ohm,  $Z_5=20-30i$  Ohm.

The multiplier circuit is implemented as a microstrip circuit with open waveguide probes to couple the signal to the input and output waveguides. All the impedance matching is done in the microstrip circuit. The input matching structure for the fundamental frequency consists of a quarter-wavelength transformer, to match the low real impedance of the HBV diode, in series with an inductive line to resonate out the capacitance of the diode. The symmetric pair of open radial stubs is used to provide an RF ground termination for both the 3<sup>rd</sup> and the 5<sup>th</sup> harmonic at the input side. At the output side, there is a coupled-line band-pass filter with a center frequency of 175 GHz and another pair of stubs to fine-tune the impedance matching. The output matching network provides an RF ground at the fundamental frequency, while the impedances at the 3<sup>rd</sup> and 5<sup>th</sup> harmonic are optimized for high

conversion efficiency. The coupled-line band-pass filter has better than 15 dB return-loss over a 20 GHz bandwidth and is not the limiting factor for the final multiplier bandwidth. The output waveguide is WR5 with a cut-off frequency of ~116 GHz, which will effectively suppress any power at the 3<sup>rd</sup> harmonic that leaks through the band-pass filter. The microstrip circuit and the waveguide probes were designed using Ansoft HFSS.

The waveguide block is designed to be very compact ( $25 \times 19 \times 8$  mm<sup>3</sup>) and is shown in Fig. 3. The microstrip circuit is mounted in a channel between the input and output waveguide and a photograph showing the central part of the chip, with the flip-chip soldered HBV diode, is presented in Fig. 4.

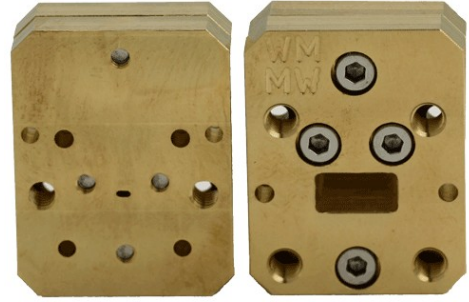


Fig. 3. Photograph of the waveguide block (rear view and front view). The rectangular openings are the output and input waveguides respectively.

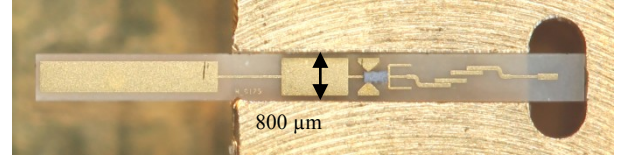


Fig. 4. Photograph of the chip after assembly in the waveguide block. The HBV diode is seen in the center, flip-chip soldered onto the circuit. At the input side, the pair of radial stubs and the quarter wave transformer can be seen, while the pair of tuning stubs together with the band-pass filter are visible at the output side. Open waveguide probes are used to couple the signal into and out from the chip.

#### IV. RESULTS

We have measured the output power and the efficiency as a function of input power at the center frequency. The input signal was supplied by a synthesizer followed by a Spacek power amplifier. The input power was sampled in real-time using a 10 dB directional coupler and a HP 8487A power sensor to ensure accurate results. The result is shown in Fig. 5 and features a maximum output power of 60 mW at an efficiency of 6.3%.

Since a single x5 multiplier unit can substitute two cascaded frequency doublers, or a doubler and a tripler, the efficiency of 6.3% is quite competitive. The efficiency of the cascaded multipliers should be better than 25% to accomplish the same overall efficiency (not taking any extra loss into account). A plot of the measured output power as a function of frequency is shown in Fig. 6, and the result is compared with the simulated performance. The agreement between the simulated and the measured results is overall good but the results are

sensitive to the assembly technique used. It is important to assemble the circuit flat in the circuit channel, without any airgap or excess mounting media (glue or wax) below. Since the circuit channel will act as the ground plane for the circuit, any spacing between the circuit and the circuit channel will affect the characteristic impedance of the microstrip lines and thereby the circuit performance. The most prominent effect will be a shift upwards in frequency for the circuit. The simulations in Fig. 6 include a 5  $\mu\text{m}$  thick layer of wax ( $\epsilon_r = 3$ ) between circuit and ground plane. This layer results in a shift in center frequency of approximately 3%, based on simulations. The thickness of the mounting media (wax or glue) was characterized using a high resolution optical microscope and was confirmed to be on the order of 5  $\mu\text{m}$ .

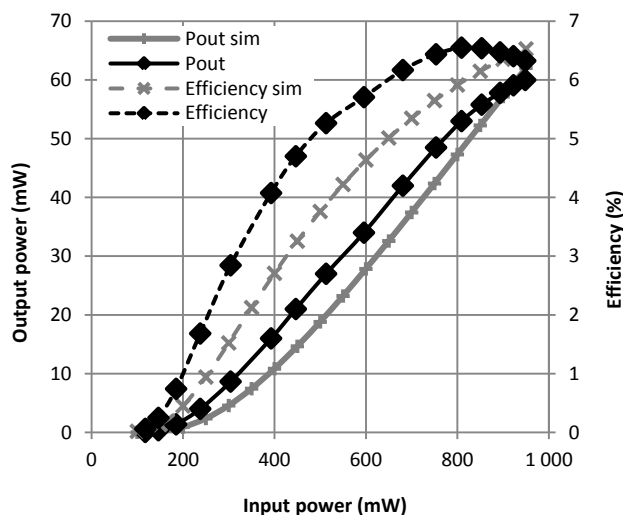


Fig. 5. Measured and simulated output power and efficiency as a function of input power at 173 GHz. The simulated data includes a 0.5 dB input mismatch and a 1 dB loss at the output. The maximum measured output power is 60 mW at an efficiency of 6.3%.

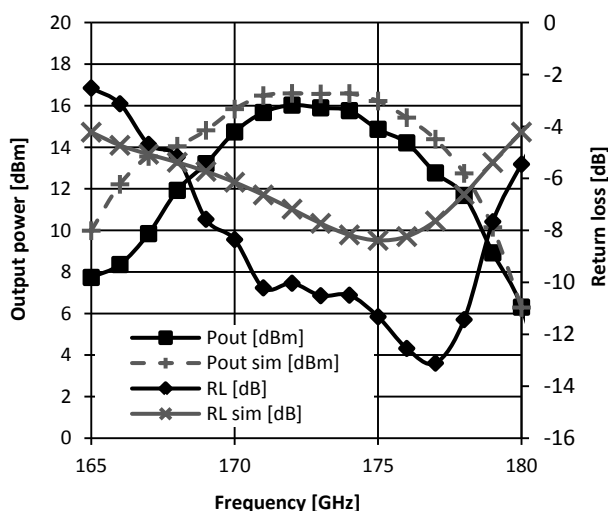


Fig. 6. Measured and simulated output power and input return-loss (RL) as a function of frequency at an input power of 700 mW; the measured 3-dB bandwidth is 8 GHz. The simulated data includes a 0.5 dB input mismatch and a 1 dB loss at the output. The waveguide to microstrip transitions are not included in the simulation.

Included in Fig. 6 is also a plot of the input return-loss as a function of frequency. The measured return-loss is better than the simulated which may indicate that there is some additional loss at the input side; this would also explain the slightly lower measured output power.

## V. CONCLUSION

We have demonstrated a frequency multiplier with 60 mW output power at a center frequency of 173 GHz. The high multiplication factor (x5) means that the module translates from an accessible microwave frequency ( $\sim 35$  GHz) to a frequency deep in the millimeter wave frequency band. The 3-dB bandwidth of the module is 8 GHz (4.6%). The module is suitable as a drive-stage for a multiplier chain to higher frequencies, or as a powerful transmitter in, e.g., a radar application.

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