Thesis for The Degree of Licentiate of Engineering

Design and Evaluation of Antenna-Integrated Down-Converters for THz Applications

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Abstract

Terahertz imaging is increasingly interesting for security applications. Rather than reconstructing 2-D images as in passive imagers, active imagers, which record the phase as well as amplitude of the returned signal by using a coherent radar principle, allow a 3-D image reconstruction. For a reduced scanning time, multipixel is advised. A straightforward way designing such systems is to stack identical receivers in a linear array. The aim of this work is to find suitable frequency down-converter designs for such a receiver array.

In this thesis, down-converters are not designed to operate at THz frequencies directly but scaled down to GHz range to verify different topologies. At 24 GHz, a balanced self-oscillating mixer (SOM) with integrated 4×4 patch array antenna in hybrid integrated circuit technology is investigated. This topology is rather simple when compared to a mixer integrated with an LO chain. Within a 3-dB bandwidth of 800 MHz, the SOM alone achieves a conversion gain better than -15 dB. If the gain of the integrated receiver is defined as a sum of the SOM's conversion gain and the antenna gain referred to an isotropic antenna, it peaks at 5.9 dB from the measurement. The double-slot antenna integrated resistive mixer at 200 GHz is then presented. With the help of a focusing Si lens, the antenna directivity is largely improved to ∼24.5 dBi. In a frequency range of 185 GHz to 202 GHz, a conversion loss of 8.0 dB and 12.2 dB is measured for the single-ended resistive mixer and the single-balanced mixer, respectively.

To evaluate the noise figure of the presented 200 GHz down-converter, the single generator N-times power method is proposed and validated experimentally. It is especially suitable for high noise figure system at millimeter wave range.

Keywords: down-converter, receiver, self-oscillating mixer, resistive mixer, patch array, double-slot antenna, lens, imaging, THz, millimeter wave, microwave, MMIC, noise figure.

List of Publications

Appended papers

This thesis is based on the work contained in the following papers:

[A] Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, H. Zirath "24 GHz balanced self-oscillating mixer with integrated patch antenna array," in *European Microw. Conf. (EuMC)*, Oct. 2011, pp. 404-407.

[B] Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, B. M. Motlagh, S. Cherednichenko, I. Kallfass, A. Leuther, and H. Zirath "Monolithically integrated 200-GHz double-slot antenna and resistive mixers in a GaAs-mHEMT MMIC process," in *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2494-2503, Oct. 2011.

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Abbreviations

2-D	2-Dimensional
3-D	3-Dimensional
CW	Continuous Wave
CPW	Coplanar Waveguide
DUT	Device Under Test
FET	Field-Effect Transistor
FMCW	Frequency Modulated Continuous Wave
FSL	Free Space Loss
FTIR	Fourier Transform Infrared
GHz	Gigahertz
GSG	Ground-Signal-Ground
HEB	Hot Electron BOlometer
IF	Intermediate Frequency
LIBS	Laser-Induced Breakdown Spectrometry
LNA	Low Noise Amplifier
LO	Local Oscillator
mHEMT	Metamorphic High Electron Mobility Transistor
MMIC	Monolithic Microwave Integrated Circuit
mm-wave	millimeter-wave
NF	Noise Figure
NFA	Noise Figure Analyzer
NQR	Nuclear Quadrupole Resonance
NMR	Nuclear Magnetic Resonance
PCB	Printed Circuit Board
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
SOM	Self-Oscillating Mixer
STJ	Superconducting Tunnel Junction
THz	Terahertz
T/R	Transmitter/Receiver

Notations

f_{t}	current gain cutoff frequency
$f_{\max}$	power gain cutoff frequency
f_{RF}	RF frequency
f_{LO}	LO frequency
f_{IF}	IF frequency
f_{out}	output frequency
$G_{\mathrm{p}}(\theta, \varphi)$	far-field function of single patch
$G_{\mathrm{A}}(\theta, \varphi)$	far-field function of the patch array
l	patch length
w	patch width
h	substrate height
θ	polar angle
φ	azimuth angle
Δ	element spacing of patch array
k	propagation constant (section 2.1.2)
	Boltzmann constant (Chapter 3)
V	voltage
R	resistance
C	capacitor
L_{c}	conversion loss
G	gain
P	power
T_0	standard room temperature (290 K)
F	noise factor
T_{e}	equivalent noise temperature
B	bandwidth
T	temperature
Y	Y-factor

Chapter 1

Introduction

Spectroscopic detection has seen a large interest in such various fields for military, industrial, medical and geological applications. To meet a variety of application areas, the imaging techniques developed thus far include: acoustic waves, induction metal detectors, nuclear resonance, lasers, X-rays, electromagnetic waves. In recent years, a lot of attention has been drawn to the area of concealed weapon and hidden explosive detection. For such standoff-imaging applications, a suitable technology need to be able to penetrate most of the common barriers and must be non-ionizing for safety reasons.

1.1 Imaging techniques overview

The acoustic wave is commonly used in a variety of sensor fields because it is highly sensitive and inherently capable of measuring different quantities [1]. However, acoustic waves cannot penetrate heavy clothing due to the severe reflection and attenuation. X-ray spectroscopy techniques, commonly used for medical imaging, are always controversial due to adverse effects. Evidences have shown that X-ray can be an inducer of cancer [2]. So far, most of the weapons are detectable by metal detectors. However, the existence of ceramic knifes and

plastic explosives, for example, should also be kept in mind as threats. Chemical-based explosives are predominantly identified with spectrometry. Techniques such as Fourier transform infrared (FTIR) and nuclear magnetic resonance (NMR) are widely used in laboratories [3]. By contrast, laser-induced breakdown spectroscopy (LIBS) and γ-spectroscopy are available for outdoor applications but suffers from insufficient accuracy and ionization radiation, respectively [3, 4]. Besides, the nuclear quadrupole resonance (NQR) takes the advantage that a magnet is not required compared to NMR, but its poor sensitivity limits the outdoor applications.

Electromagnetic techniques, which make use of microwave (λ=10$\sim$1000 mm), millimeter-wave (λ=1$\sim$10 mm) and even terahertz-wave (λ=0.1$\sim$1 mm), not only penetrate most of the common barriers but also meet the safety requirement of non-ionizing radiation. Furthermore, Terahertz (THz) spectra offer the capability of identifying certain hidden substances from their characteristic spectra [5]. Therefore, the electromagnetic techniques, especially the THz, are promising for security applications.

1.2 Terahertz imaging system

In the THz regimes, some passive direct detect technologies, like NbN hot electron bolometer (HEB), superconducting tunnel junction (STJ), and microbolometers, have been successfully applied to imaging at a cryogenic environment [6–8]. In monolithic integrated circuit technology, a 0.65 THz focal-plane array which consists of antennas and detectors demonstrates the imaging successfully without cooling [9].

Rather than reconstructing two-dimensional (2-D) images by using the direct detect technologies, coherent radar, which records the phase as well as amplitude of the returned signal,

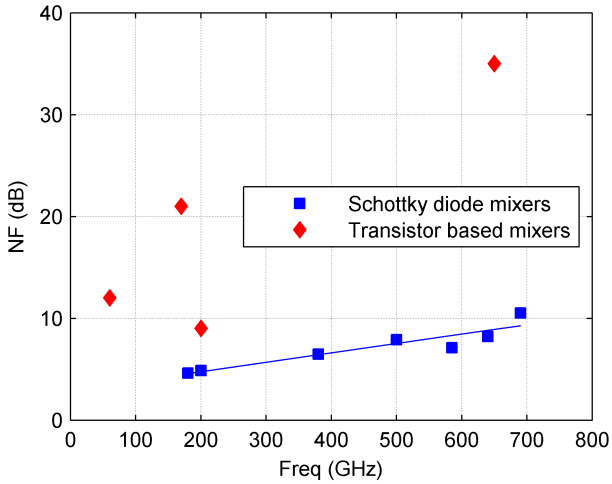


Fig. 1.1: Comparison of noise figures versus frequency between Schottky diode mixers and transistor-based mixers.

allows a three-dimensional (3-D) image formation [10]. By employing frequency modulated continuous wave (FMCW), Jet Propulsion Laboratory demonstrated a 660-690 GHz 3-D imager at room temperature, which is based on Schottky diode technology [11–13].

Schottky diodes are well known for the low noise performance compared to transistors. As can be seen from Fig. 1.1, the transistor based mixers [14–16] in the monolithic microwave integrated circuit (MMIC) technology report higher NF than Schottky diode mixers [17–22]. However, MMICs possess a possibility of fully integration. By cascading a well designed RF low noise amplifier (LNA) before the mixer, the integrated receiver front-end could achieve not only comparable NF but also higher conversion efficiency compared that of Schottky diode technology [23–25]. In the past, MMIC technology has been successfully applied to solid-state devices and systems below 100 GHz. In recent years, the continuously development of

semiconductor manufacturing processes has pushed the current gain cutoff frequency (f_t) and the power gain cutoff frequency (f_{max}) of transistors into THz range [26–28]. It opens up opportunities for terahertz monolithic integrated circuits [29–31].

1.3 Goal of this work

In an active imaging system, a multipixel receiver is highly desired for reduced scanning time. A straightforward way is to stack identical receivers to build a linear array. Using traditional building practice, the microwave integrated circuits and antennas are optimized individually in different technologies and connected afterwards. This becomes increasingly difficult with increasing frequency since the interconnecting wires will deteriorate the system performance. It is desirable to integrate the antenna with circuits in the same technology. Thus, the goal of this thesis is to investigate different down-converter topologies with an integrated antenna which would are suitable for constructing linear arrays in the mm-wave and THz range.

Chapter 2

Two Common Down-Converter Topologies

The frequency down-converter plays a key role in receivers. It converts the RF signals down to the intermediate frequency (IF) band for signal processing. In this chapter, two different types of down-converters are analyzed and investigated experimentally.

2.1 Self-oscillating mixer (SOM) with integrated patch antenna array

2.1.1 Motivation and limitation of SOM

A traditional receiver front-end, as is shown in Fig. 2.1, typically consists of antenna, RF low noise amplifier (LNA), down-converter mixer, local oscillator (LO), IF filter and IF amplifier. As the frequency increases, the LO signal is normally generated by an oscillator followed by a frequency multiplier.

The SOM is a neat solution to avoid the redundant LO

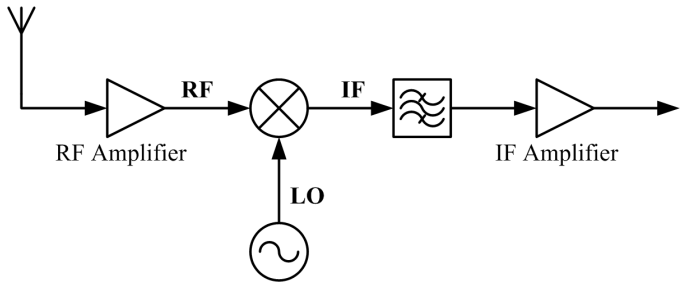


Fig. 2.1: Comparison of noise figures versus frequency between Schottky diode mixers and transistor-based mixers.

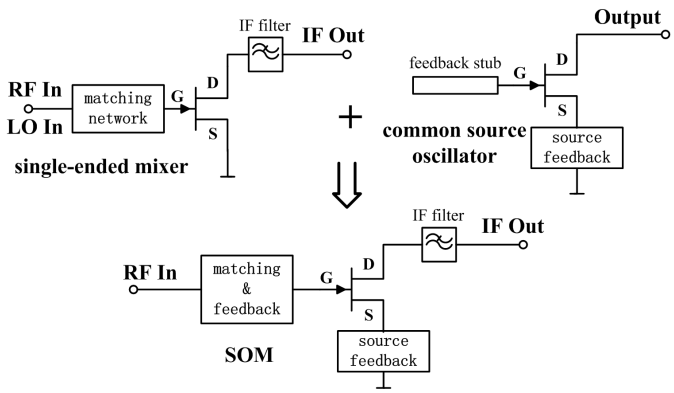


Fig. 2.2: Schematic of a single-ended SOM

multiplication chain, because the self-oscillation applies the desired LO signal as in a standard mixer [32]. Fig. 2.2 shows the so called gate mixer as an example. It is a combination of a gate mixer and a common source oscillator. Since the function of frequency conversion and oscillation is accomplished by the same nonlinear device, smaller size and lower power consumption can be achieved.

In a common source oscillator, series feedback at the source terminal and the network at the gate terminal are designed to

fulfill the oscillation condition at the desired frequency [33]. For stable SOM operation, the oscillation should not be sensitive to the input RF signal.

The main limitation of a SOM down-converter is the lower end of the IF frequency. When the input RF frequency is very close to the self-oscillation one, frequency synchronization may occur and the mixing process will be prevented [34]. Therefore, SOM designs may not be efficient when low IF is needed. Because the biasing and matching of a SOM is tradeoff between the optimal designed oscillator and mixer, other figures of merit, such as conversion gain and phase noise, are worse when compared to traditionally designed receivers. However, in applications where size, power consumption and cost are more concerned, the SOM would still be a good choice [35–37].

2.1.2 24 GHz balanced SOM with integrated patch array

When functioning as an active imager, the down-converter aims to receive signals at a frequency of several hundred gigahertz (GHz). Hence, the SOM should apply the LO frequency at the same order from its self-oscillation. However, the highest frequency that can be achieved from an oscillator is limited by the cut-off frequency of the used transistor technology. It is possible to use higher harmonics of the oscillation frequency in the mixing process in order to circumvent this problem.

A 24 GHz balanced SOM with integrated 4×4 patch array antenna is designed and evaluated mainly to verify the topology. It is fabricated in hybrid integrated circuit technology to enable on-board trimming. Fig. 2.3 shows the topology of the proposed balanced SOM, which contains two identical single-ended SOMs. This fully symmetric arrangement leads to a virtual ground at the middle of the gate transmission line [33].

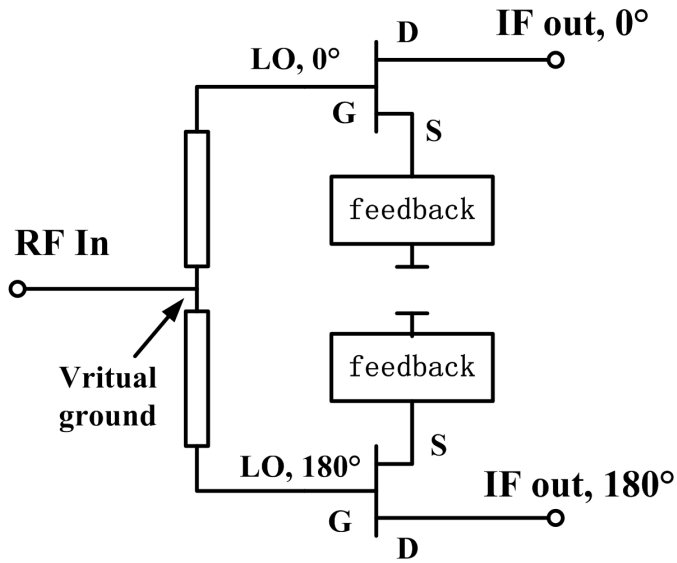


Fig. 2.3: Topology of the balanced SOM.

Therefore, the signals generated by the two branches will be 180° out-of-phase.

Fig. 2.4 shows the schematic of the 24 GHz balanced SOM. The quarter wavelength short-circuited stub (at 24 GHz) is connected at the source to enable a DC ground path of the transistor. The resonant circuit which mainly determines the oscillating frequency incorporates the gate transmission line as an inductive element and the capacitor "C1". Values of these components are tuned in simulations to achieve the fundamental oscillating frequency at 12 GHz. The RF port which is inserted at the center point does not affect the oscillation condition due to the virtual ground property at this node. Furthermore, the anti-phase condition offered by the topology will cancel the fundamental frequency (here is 12 GHz) and all odd harmonics at both RF and IF ports, while the even harmonics are in phase and will thus be added constructively.

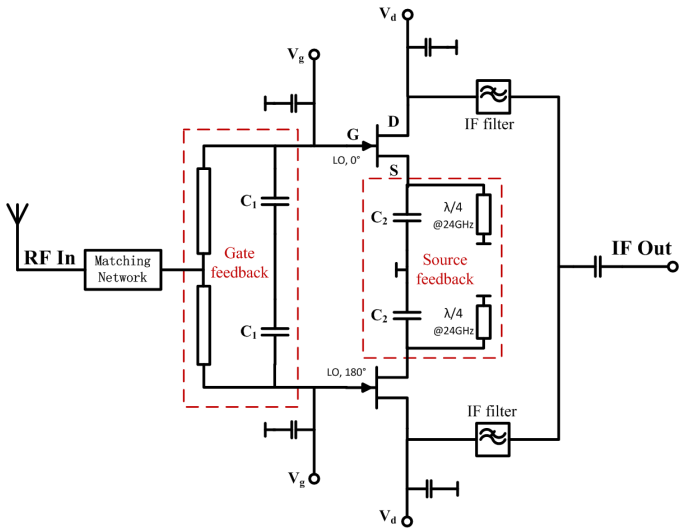
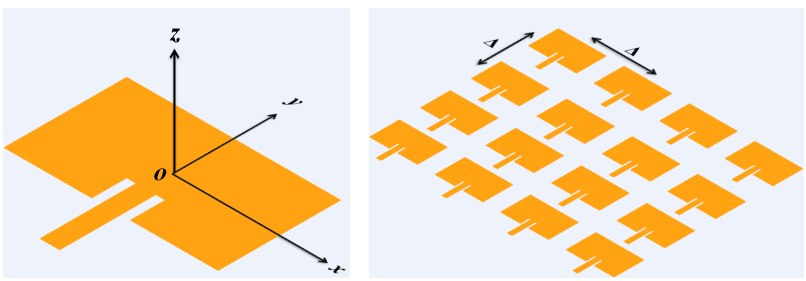


Fig. 2.4: Schematic of the balanced SOM.

When connecting a SOM with an antenna, it is beneficial to have both of them integrated in the same planar technology. Since only single metal layer PCB (Rogers3003) is used, the patch array antenna with uniform amplitude and phase feeding network is selected for easy integration with microstrip.



(a) (b)

Fig. 2.5: Sketch of (a) a single patch and (b) 4×4 patch array.

According to [38], the far-field function of a quadratic patch array with equal spacing in both x- and y- direction can be analytically calculated in two steps:

I. By choosing the origin of the coordinate system to the center of a single patch, as shown in Fig. 2.5 (a), the far-field function of one patch can be calculated as:
• when $\theta \leq \pi/2$

$$G_p(\theta,\varphi) = \frac{j \cdot 4E_0 h}{\pi} \cdot \left[\frac{sin\left(k\frac{w}{2}sin\theta cos\varphi\right)}{sin\theta cos\varphi}\right] \cdot \left[cos\left(k\frac{l}{2}sin\theta cos\varphi\right)\right] \cdot \left[sin\varphi\hat{\theta} + cos\theta cos\varphi\hat{\varphi}\right] \tag{2.1}$$

• when $\theta > \pi/2$

$$G_p(\theta,\varphi) = 0 \tag{2.2}$$

where l and w are the length and the width of the patch, respectively; k is the propagation constant; h is the height of the substrate.

II. For a quadratic patch array with equal spacing in both x- and y- direction, as shown in Fig. 2.5 (b), the far-field function from the element-by-element sum technique can be written as:

$$G_A(\theta,\varphi) = \sum_{m=1}^{N}\sum_{n=1}^{N} G_p(\theta,\varphi) \cdot e^{jk\Delta sin\theta\left[\left(m-\frac{N+1}{2}\right)cos\varphi + \left(n-\frac{N+1}{2}\right)sin\varphi\right]} \tag{2.3}$$

where Δ is the element spacing in both x- and y- direction; and N is the maximum number of elements at each direction (N=4).

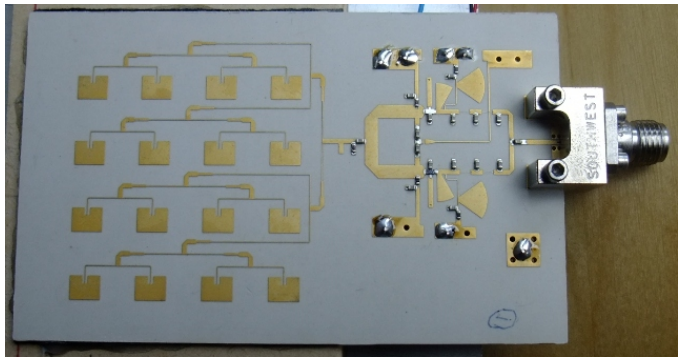


Fig. 2.6: Photo of the 24 GHz SOM with integrated 4×4 patch array antenna.

Fig. 2.6 shows the photo of the integrated 24 GHz down-converter. The SOM and the antenna are matched to 50 Ω and connected directly. It occupies a board size of 75×45 mm^2.

2.1.3 Experimental results

In order to characterize the integrated SOM with the patch array, a complete transmitter/receiver (T/R) link is setup as shown in Fig. 2.7. The horn antenna and the patch array antenna are aligned on axis with the same polarization. A distance of 4 m between the antennas guarantees the far-field condition.

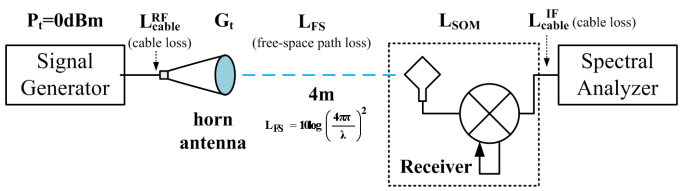


Fig. 2.7: Measurement setup.

From the link budget, assuming 0 dBm RF power (P_t) from the generator, the measured and simulated IF output power is

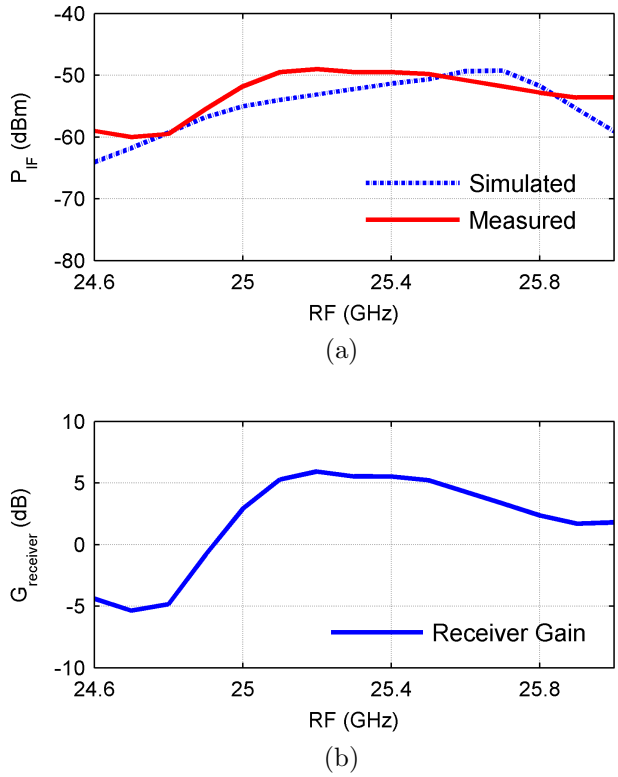


Fig. 2.8: (a) Measured and simulated IF output power, (b) estimated isotropic gain of the receiver.

shown in Fig. 2.8 (a). Then, the estimated isotropic receiver gain, which incorporates the SOM's conversion gain and the antenna's isotropic gain, is estimated from the measurement and shown in Fig. 2.8 (b). As can be seen from Fig. 2.8 (b), the integrated down-converter (SOM+patch array) achieves a peak isotropic gain of 5.9 dB and a 3 dB-bandwidth of 800 MHz.

2.1.4 Conclusion about the self-oscillaing mixer topology

For an ideal SOM, we prefer a high self-oscillation power to drive the mixing efficiently while the transistor is better to be biased under the condition as an ideal switch. However, the DC bias for an optimal oscillation conflicts with the best bias for optimal mixing. Therefore, a SOM does not compete a well designed mixer in terms of the electrical performance. But the SOM possesses the properties of simplicity and compactness. The SOM could therefore be attractive in applications where the size and cost of the overall system is the prime concern.

2.2 Resistive mixer with integrated double-slot antenna

2.2.1 Theory of the resistive mixer

Frequency conversion due to frequency mixing occurs with any nonlinear element. In a down converter mixer, two independent frequencies, f_{RF} and f_{LO}, are multiplied to produce a number of mixing products:

$$f_{out} = mf_{RF} + nf_{LO} \tag{2.4}$$

where m and n are integers or zero (0, ±1, ±2, ±3, $\cdots$). However, only the IF frequency, $f_{IF} = |f_{RF} - f_{LO}|$, is the desired.

The resistive FET mixer was first proposed by Stephen A. Maas in 1987 [39]. The topology is shown in Fig. 2.9. The LO signal along with a DC bias is applied at the gate while the RF signal is applied to the drain. Then, the IF frequency is filtered from the drain.

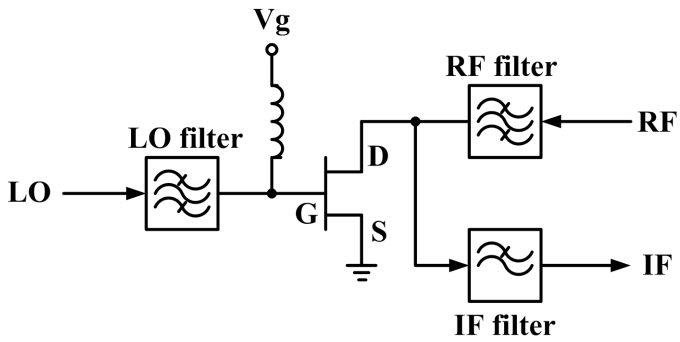


Fig. 2.9: Topology of the resistive FET mixer.

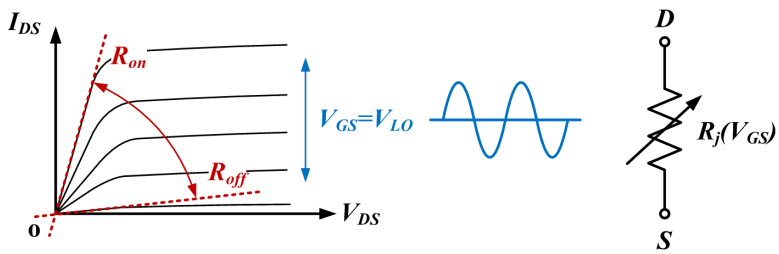


Fig. 2.10: Simplified model of the resistive mixer.

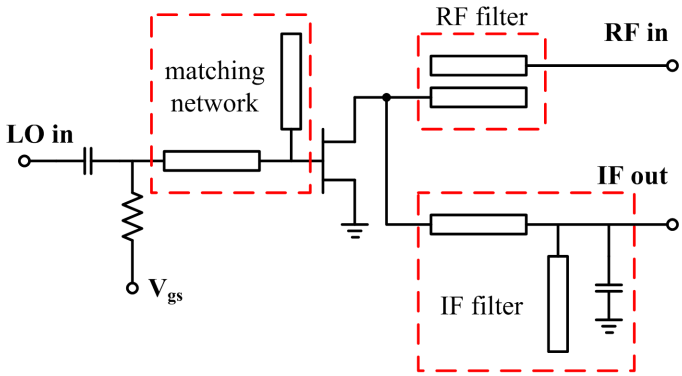
As can be seen from the typical I-V curve of a field-effect transistor (FET), shown in Fig. 2.10, the channel can be approximated with a variable resistor when the drain-to-source voltage (V_{DS}) is small, and channel resistances can be denoted by the IV-slopes which depend on the gate voltage. In a resistive mixer, no DC bias is applied to the drain. Hence, it can be modeled as a variable resistance which is controlled by the LO signal. In one LO cycle, the channel resistance increases to virtually infinity (R_{off}) when the gate voltage drops below the threshold voltage (V_{t}), and it decreases to a very low value (R_{on}) when the gate voltage reaches to the maximum. For the optimal operation, the gate is biased at V_{t} while the LO power is chosen for lowest conversion loss [40].

2.2.2 Design of 200 GHz resistive mixer with integrated double-slot antenna

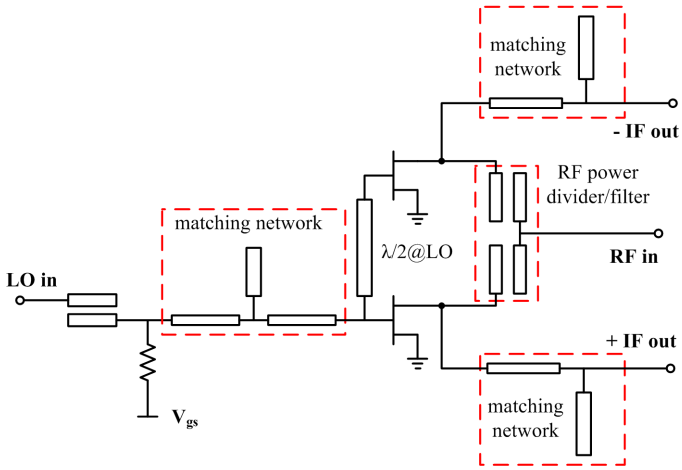
In Paper [B], based on the 100-nm metamorphic HEMT (mHEMT) technology, two resistive mixers with an integrated double-slot antenna at ∼200 GHz are designed. Fig. 2.11 shows the schematic of the two resistive mixers. In both cases, the LO is connected to the gate in order to vary the channel resistance. The principal attraction of a single-ended mixer is the simple topology, but there may be poor LO-to-RF isolation (e.g. 9.3 dB isolation obtained from the single-ended mixer of this work [41]). By contrast, the LO leakage in a single-balanced mixer is suppressed intrinsically because the LO signals at the two gates are 180° out-of-phase (e.g. better than 39 dB isolation achieved from the single-balanced mixer of this work). However, since two transistors are working for frequency conversion in the single-balanced mixer, higher LO power would be needed compared to the single-ended design.

The choice of MMIC-based antenna is often limited by the layer topology. In the given HEMT process with two metal layers (including the ground layer at backside), antenna structures such as dipoles, folded dipoles, microstrip fed patch and slots are possible to realize. Due to the thin substrate, the patch antenna would unfortunately have poor efficiency and dipoles would exhibit low input impedance (a few ohms) which is difficult to match [42, 43]. By contrast, the slot antenna is preferred, especially at millimeter-wave frequencies since its radiation can be coupled to a focusing ellipsoidal lens [44, 45].

Fig. 2.12 shows the geometry of the designed double-slot antenna with microstrip feed network on a ellipsoidal Si lens. Two slots are etched out in the backside metal layer while the microstrip feed network is located at top metal layer for further integration with resistive mixers. Center of the double slots should align to the center of the Si lens. With the help of the



(a)



(b)

Fig. 2.11: Schematic of (a) the single-ended resistive mixer and (b) the single-balanced resistive mixer.

focusing lens, a narrow beam with a directivity of ∼24.5 dBi is obtained.

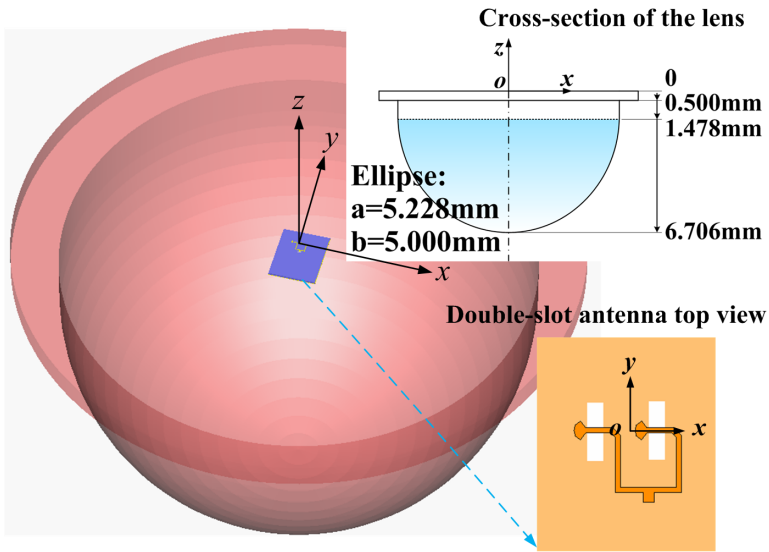
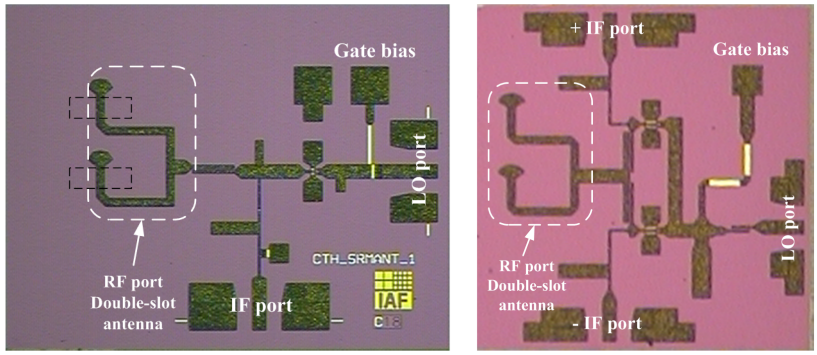


Fig. 2.12: Double-slot antenna with microstrip feed network on Si lens.

In this work, the RF ports of both the single-ended mixer and the single-balanced mixer are matched to 50 Ω for breakout measurements. The double-slot antenna is also matched to the same impedance and is directly coupled to the RF port of mixers. The chip photos are shown in Fig. 2.13. The double slots located at the back of the GaAs substrate beneath the coupler's arms are marked by the black dashed rectangles. Chip dimensions are 1100×700 μm^2 and 900×950 μm^2, respectively.

2.2.3 Experimental results

To evaluate the two integrated receiver front-end, a complete T/R link at G-band (140-220 GHz) is set up, as shown in



(a) (b)

Fig. 2.13: Chip photos of (a) double-slot antenna integrated with single-ended resistive mixer and (b) double-slot antenna integrated with single-balanced resistive mixer.

Fig. 2.14 and Fig. 2.15. The transmitter is an in-house manufactured ×6 frequency multiplier source module (output frequency band: 163-202 GHz) with a G-band corrugated horn antenna. The MMIC chip is glued on the Si lens with center aligned between the lens and the double slots. The transmitter horn is aligned around 200 mm underneath the Si lens with the same polarization. On-chip coplanar waveguide (CPW) pads at LO and IF ports enable an on-wafer probing through ground-signal-ground (GSG) probes.

In order to evaluate the receiver, we define that the receiver gain (G_{RX}) incorporates the antenna gain referred to an isotropic antenna (G_{r}) and the conversion loss of mixer (L_{c}). From the link budget, the G_{RX} can be represented by:

$$G_{RX} = P_{out} - G_{LNA} + L_{cable} + L_{probe} + FSL - G_t - P_t \quad (2.5)$$

where the power values are measured in dBm and the gain/loss are given in dB.

- P_{out} is the measured IF power;
- G_{LNA} represents the gain of the IF LNA;
- L_{probe} and L_{cable} are the losses of the IF probe and the IF

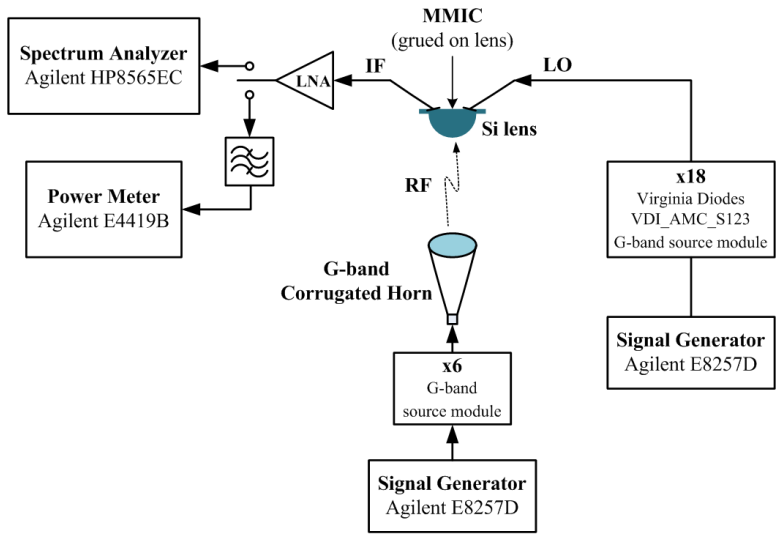


Fig. 2.14: Diagram of the measurement setup.

cable respectively;
• FSL is the free space loss which can be calculated by $FSL = 20 \cdot log\left(\frac{4\pi d}{\lambda}\right)$ dB and d is the distance between the transmitter and receiver;
• G_{t} is the gain of the corrugated horn and is obtained by EM simulation;
• P_{t} is the RF power from the $\times 6$ module. It was kept at -20 dBm for all the RF frequencies.

Because the double-slot antenna and the resistive mixers are matched, L_{c} can be deduced by:

$$L_c = G_r - G_{RX} \tag{2.6}$$

As is discussed before, the performance of a resistive mixer is a function of the gate bias and LO power. Thus, it is necessary to tune them prior to the measurements. In the measurement setup, the maximum available LO power is around +5 dBm. In both receivers, this is not high enough to achieve

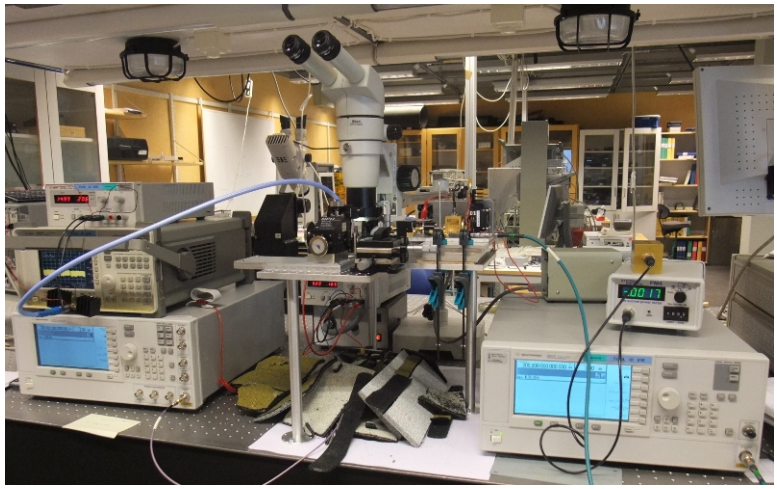
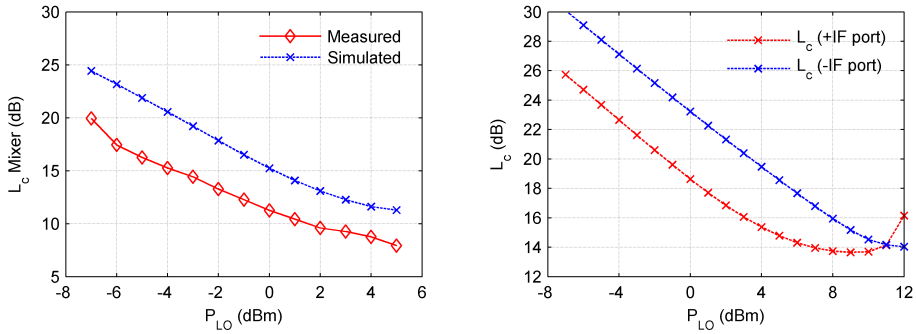


Fig. 2.15: Photo of the measurement setup.

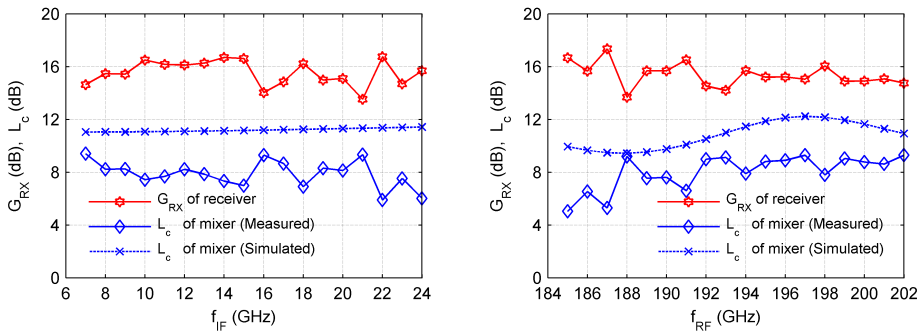
the lowest L_c, as shown in Fig. 2.16. Keeping +5 dBm LO power pumped, the G_{RX} of receiver and the L_c of mixer are estimated with a swept frequency, as shown in Fig. 2.17 and Fig. 2.18. With RF frequency varying from 185 GHz to 202 GHz, a typical L_c of 8.0 dB and G_{RX} of 15.4 dB is measured for the single-ended topology, while a typical L_c of 12.2 dB and G_{RX} of 11.2 dB is obtained from one of the two IF outputs for the single-balanced one.

Noise figure (NF) is an important indicator when evaluating a receiver. In this work, it is difficult to apply the traditional methods, such as the direct noise measurement method, the Y-factor method and the signal generator twice power method. A novel method, which is called the signal generator N-times power method, is proposed. It is suitable for evaluating moderate to high NF devices operating beyond 100 GHz. Limitations of the traditional methods and details of the proposed method will be clarified in Chapter 3. Fig. 2.19 shows the estimated NF of both mixers.



(a) (b)

Fig. 2.16: Conversion loss versus LO power for (a) the single-ended resistive mixer and (b) the single-balanced resistive mixer.



(a) (b)

Fig. 2.17: Conversion loss of the single-ended resistive mixer and estimated gain of the integrated receiver (a) fixed LO at 209 GHz (b) fixed IF at 1 GHz.

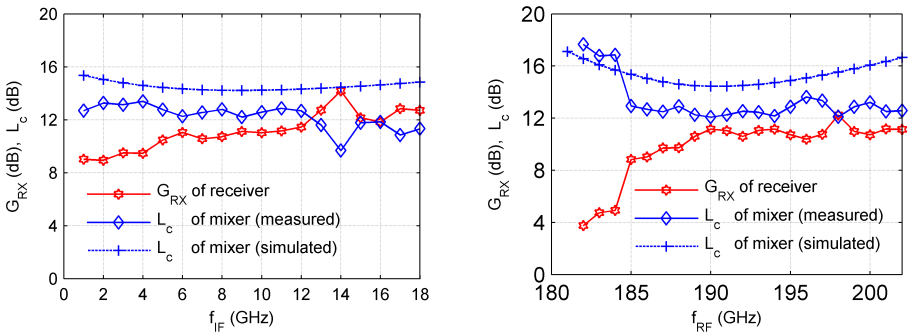


Fig. 2.18: Conversion loss of the single-balanced resistive mixer and estimated gain of the integrated receiver (a) fixed LO at 184 GHz (b) fixed IF at 1 GHz.

2.2.4 Conclusion about the resistive mixer

A resistive mixer uses the channel-resistance of FETs to achieve frequency conversion. Since the drain is not biased, DC consumption of a resistive mixer is virtually zero. The single-ended topology holds a simple structure at the expense of a poor LO-to-RF isolation. By contrast, the single-balanced mixer suppress the LO leakage intrinsically but requires more LO power to drive the transistors efficiently. In different applications, all those factors should be taken into consideration.

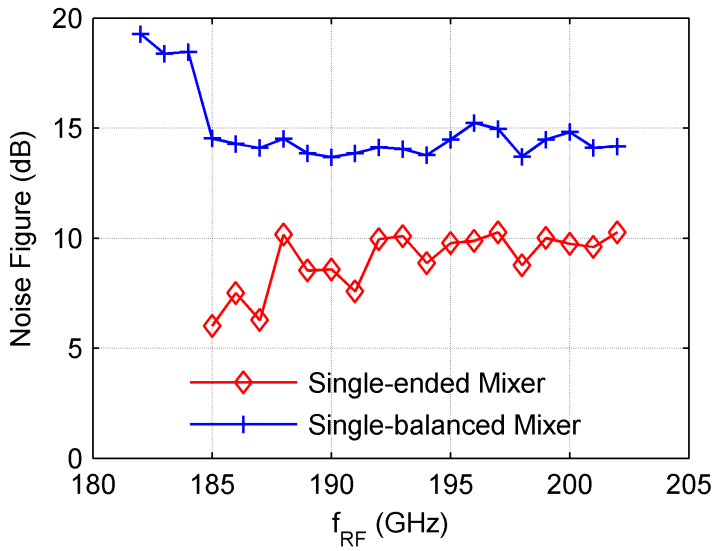


Fig. 2.19: Estimated NF of the single-ended mixer and the single-balanced mixer.

Chapter 3

Signal generator N-times power method for noise figure evaluation

The noise figure measures the amount of noise added by a component. It is defined by the ratio of the input signal-to-noise ratio (SNR) to the output SNR, or more often by the ratio of the total available noise power at the output (N_{o}) to the output available noise power (N_{i}) due to thermal noise originating from the input resistor at standard room temperature (T_0=290 K) [46]. Normally, the noise factor (F) is respected as a linear value while noise figure (NF) is respected as the same number in dB. Sometimes, the equivalent noise temperature (T_{e}) is used. Together, the three parameters describe the same property when evaluating a noise contribution and they can be converted between each other by using Eq. (3.2) and Eq. (3.3).

$$F = \frac{SNR_i}{SNR_o} = \frac{N_o}{N_i} \tag{3.1}$$

$$NF = 10 \log F \cdots (dB) \tag{3.2}$$

$$T_e = T_0 (F - 1) \tag{3.3}$$

3.1 Traditional noise figure measurement methods

In most modern receiving systems, it is essential to know the noise generated within receiver components. The most well-known methods are the direct noise measurement method, the Y-factor method and the signal generator twice-power method [47].

3.1.1 Direct noise measurement method

The direct noise measurement method is the most straightforward way and the diagram is shown in Fig. 3.1. Output noise power is measured directly when the input of the device-under-test (DUT) is terminated by a matched load at 290 K.

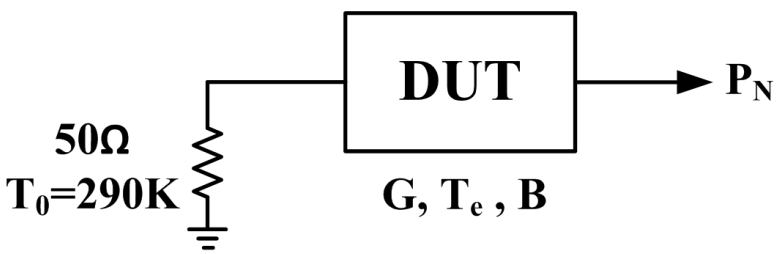


Fig. 3.1: The direct noise measurement method.

According to the noise power definition, the total available noise power at the output is written by:

$$P_N = kTBG \tag{3.4}$$

where
- k=1.38×10^{-23} J/K is the Boltzmann constant;
- B is the noise bandwidth;
- G is the gain;
- $T = T_0 + T_e$ is the total equivalent input noise temperature.

In direct noise measurement method, the noise bandwidth B and the gain G must be known. From Eq. (3.4), noise temperature T_{e} can be calculated as:

$$T_e = \frac{P_N}{kBG} - T_0 \tag{3.5}$$

or, by using Eq. (3.3), the noise factor F is written as:

$$F_{DUT} = \frac{P_N}{kT_0BG} \tag{3.6}$$

This direct noise figure measurement method is useful for high NF measurement, because a higher output power due to a higher NF of DUT will help to improve the accuracy of power measurement. However, for a lossy DUT, the output noise power can be difficult to be identified from the noise floor.

3.1.2 The Y-factor method

The concept of the Y-factor method is shown in Fig. 3.2. At the input of a DUT, the physical temperature of a matched resistor is changed between two distinct values T_{hot} and T_{cold}. Correspondingly, the output power is measured as P_1 and P_2. According to Eq. (3.4),

$$P_{hot} = k\left(T_{hot} + T_e\right)BG \tag{3.7}$$

$$P_{cold} = k\left(T_{cold} + T_e\right)BG \tag{3.8}$$

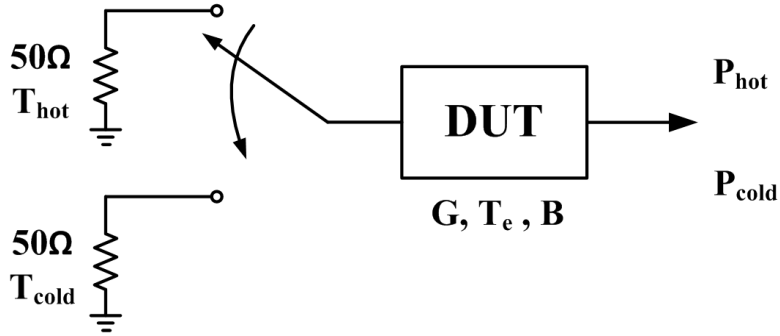


Fig. 3.2: The Y-factor method.

The Y-factor is defined as:

$$Y = \frac{P_{hot}}{P_{cold}} \tag{3.9}$$

or in dB value as:

$$Y_{dB} = 10 \log Y \tag{3.10}$$

Thus, from Eq. (3.7)∼(3.9), we can write:

$$Y = \frac{T_{hot} + T_e}{T_{cold} + T_e} \tag{3.11}$$

$$T_e = \frac{T_{hot} - YT_{cold}}{Y - 1} \tag{3.12}$$

or

$$F_{DUT} = \frac{T_{hot} - YT_{cold}}{(Y - 1)\, T_0} + 1 \tag{3.13}$$

The Y-factor method is commonly used by commercial noise figure analyzers (NFAs), where abundant noise power coming

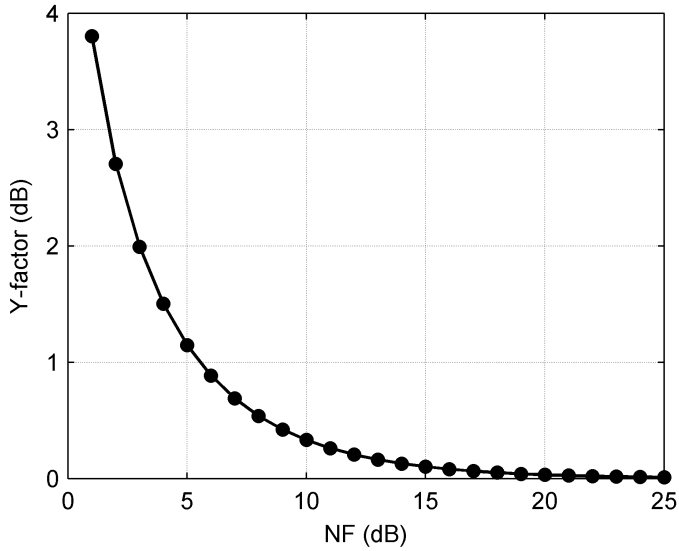


Fig. 3.3: Analytical curve of the Y-factor as a function of noise figure (T_{hot}=290 K and T_{cold}=77 K).

from a noise source serves as the hot load and a matched load at room temperature serves as the cold load. Due to the limited bandwidth of noise sources, so far the commercial NFAs only work up to tens of GHz. As frequency increases above 100 GHz, a matched load at room temperature and liquid nitrogen (77 K) are usually chosen as the hot load and cold load, respectively [23]. In this method, the Y-factor is a relative value, its accuracy is import. At millimeter wave range, when 290 K/77 K serves as hot/cold temperature, the Y-factor as a function of noise figure is shown in Fig. 3.3. For a high NF system, the Y-factor will be very small and difficult to measure accurately. Fig. 3.4 shows the analytical error of NF when the measured Y-factor is ±0.05 dB away from the true value. At the low noise range, such small error can be ignored. But as the true NF increasing, this small Y-factor error contributes more and more to the measured NF. Therefore, at frequencies above

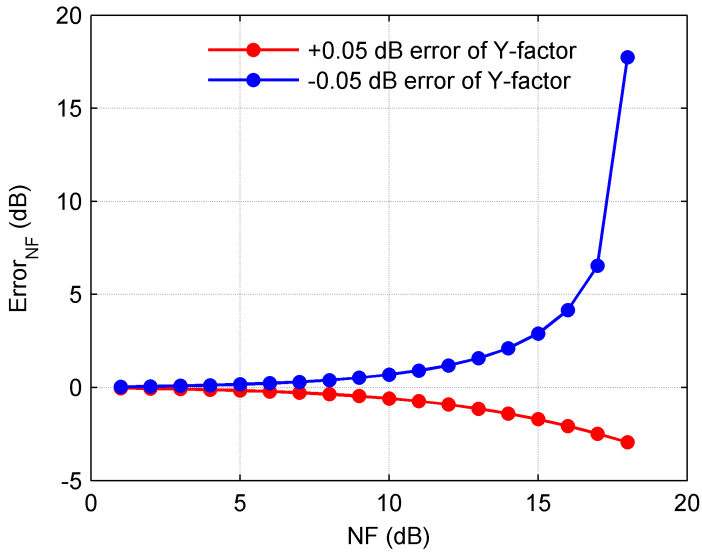


Fig. 3.4: Analytical noise figure error introduced by ±0.05 dB Y-factor error (T_{hot}=290 K and T_{cold}=77 K).

100 GHz, the Y-factor method is only suitable to evaluate low to moderate NF devices.

3.1.3 Signal generator twice-power method

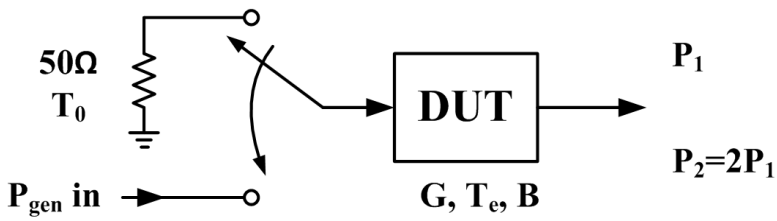


Fig. 3.5: The signal generator twice-power method.

Similar like the direct noise measurement method, the signal generator twice-power method is also useful for devices

with high NF. As can be seen from Fig. 3.5, the output power is firstly measured (P_1) when the input is terminated with a matched load at room temperature. Then, a continuous wave (CW) signal generator is connected and its power (P_{gen}) is adjusted to produce a 3-dB increase at the output (P_2). According to Eq. (3.4):

$$P_1 = k\,(T_0 + T_e)\,BG \tag{3.14}$$

$$P_2 = k\,(T_0 + T_e)\,BG + P_{gen}G \tag{3.15}$$

Because $P_2 = 2P_1$, from Eq. (3.14) and Eq. (3.15):

$$T_e = \frac{P_{gen}}{kB} - T_0 \tag{3.16}$$

or

$$F_{DUT} = \frac{P_{gen}}{kT_0B} \tag{3.17}$$

Compared with the direct noise measurement method, gain of the DUT is ignored. In this method, an accurate measurement of P_{gen} is the most critical and error prone part. Depending on the dynamic range of the power meter at millimeter wave range, the P_{gen}, which results in only 3 dB increases at the output, could be too weak to measure accurately.

3.2 Signal generator N-times power method

In Section 2.2, two resistive mixers with integrated double-slot antenna are designed for G-band operation. However, the above NF measurement methods are difficult to be applied here

due to the limitation and consideration which is discussed in section 3.1. Based on the signal generator twice-power method, the signal generator N-times power method is proposed. It avoids measuring a very weak P_{gen}.

3.2.1 Working principle

The working principle of the single generator N-times power method is similar to the signal generator twice-power method, as shown in Fig. 3.6.

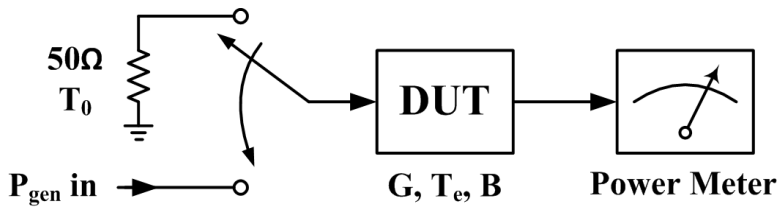


Fig. 3.6: The signal generator N-times power method.

When the input is terminated with a matched load at room temperature, the measured output power (P_1) can be written as:

$$P_1 = k\,(T_0 + T_e)\,BG \tag{3.18}$$

Then a CW signal generator is connected to the input port where the CW signal should be within the bandwidth of DUT. With an input power of P_{gen}, an output power of P_2 is measured and is written as:

$$P_2 = k\,(T_0 + T_e)\,BG + P_{gen}G \tag{3.19}$$

If the N factor is defined by:

$$N = \frac{P_2}{P_1} \tag{3.20}$$

Then the equivalent noise temperature of the DUT can be calculated from Eq. (3.18)∼(3.20) as:

$$T_e = \frac{P_{gen}}{kB\,(N-1)} - T_0 \tag{3.21}$$

or

$$F_{DUT} = \frac{P_{gen}}{kT_0B\,(N-1)} \tag{3.22}$$

Theoretically, one can apply arbitrary amount of power for P_{gen}. This especially benefits at the millimeter wave range where the dynamic range of a power meter is limited.

3.2.2 Experimental validation

At lower frequency, three simple networks are characterized by the signal generator N-times power method and by a commercial NFA (Agilent N8975) as an experimental validation. As is shown in Fig. 3.7, three networks are used to apply low NF (<5 dB), moderate NF (5∼10 dB) and high NF (>10 dB). By using the signal generator N-times power method, a large range of the ratio N is applied in the measurement. As can be seen from Fig. 3.8, the estimated NF for each network agrees well with the results by the NFA.

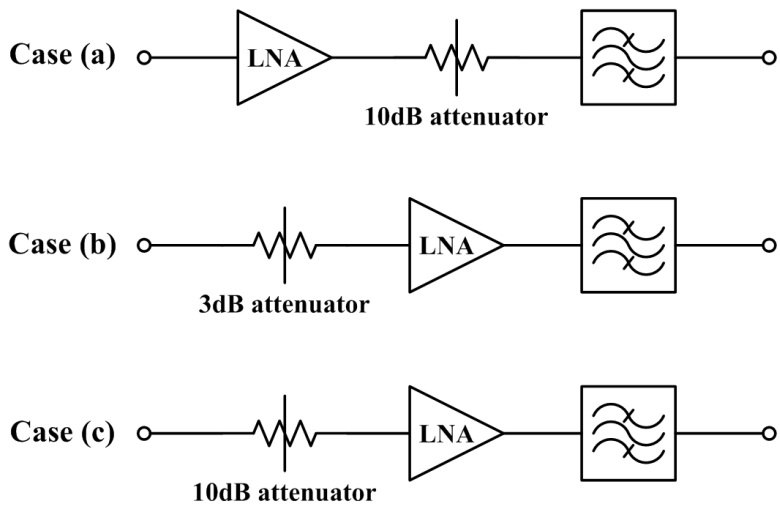


Fig. 3.7: Three networks with (a) low NF; (b) medium NF; (c) high NF.

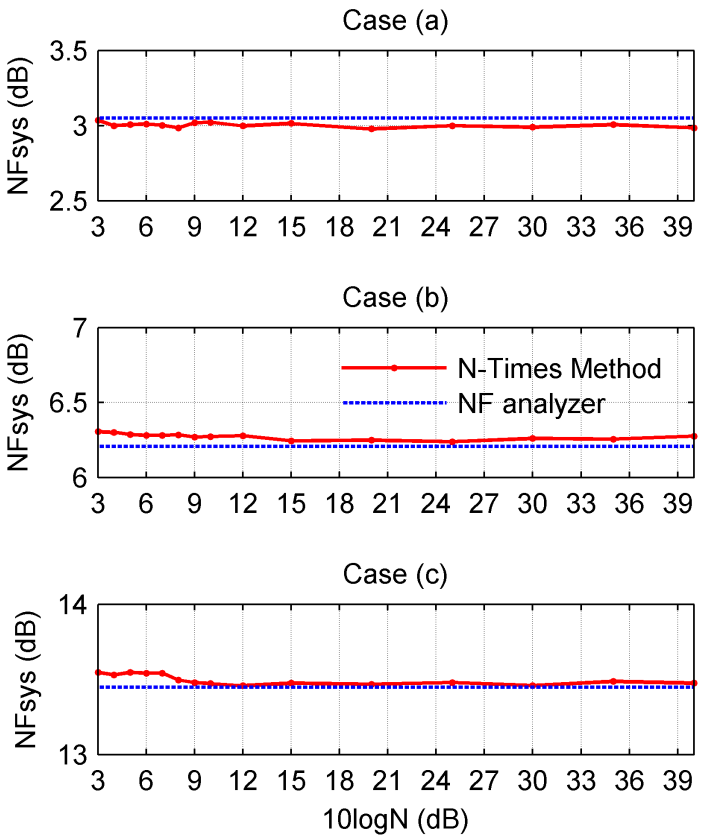


Fig. 3.8: NF comparison with different measurement.

Chapter 4

Summary and future work

Aiming for the THz linear receiver array, different types of antenna integrated down-converters are investigated as possible candidates. In the initial designs, operating frequencies are not designed at the THz range but scaled down to lower frequencies for on-board trimming or easier measurements. In the hybrid integrated circuit technology, a 24 GHz balanced self-oscillating mixer with integrated 4×4 patch array antenna is designed and fabricated. The most attractive feature of the SOM is that no external LO needs to be applied. This would largely simplify a fully integrated receiver array, since the LO multiplication chain and distributed network tend to be bulky as frequency increases. Furthermore, a balanced topology utilizes the second harmonic. Compared to a fundamental operation, the highest working frequency of the balanced design is doubled. Drawbacks of the SOM are mainly because of the non-optimal bias for either an oscillator or a mixer. Therefore, a SOM cannot be better than a well designed mixer in terms of the electrical performance.

In the 100 nm GaAs mHEMT MMIC technology, resistive FET mixers with integrated double-slot antenna are designed. Since no bias is applied to the drain, the DC consumption of a resistive mixer is virtually zero. The single-ended mixer

achieves a good conversion loss at frequencies of ∼200 GHz. The single-balanced topology possesses very good capability of LO leakage suppression at the expense of higher LO power requirement. At millimeter wave range, high power becomes precious and thus the power budget must be taken into consideration. The on-chip double-slot antenna is aligned on an ellipsoidal Si lens for beam focusing. With the help of the Si lens, the antenna directivity is largely improved to ∼24.5 dBi.

In order to characterize the noise figure of the designed 200 GHz mixers, the signal generator N-times power method is presented. It can be a suitable method to estimate a high noise figure at millimeter wave range.

In the future, more topologies of down-converters (e.g. Gilbert mixer, transconductance mixer) will be look into. Simultaneously, the operation frequency will be pushed to around 340 GHz and a fully integrated 340 GHz receiver front-end is aimed for single pixel.

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Paper A

24 GHz balanced self-oscillating mixer with integrated patch antenna array

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24 GHz Balanced Self-Oscillating Mixer with Integrated Patch Antenna Array

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Abstract—**Design and performance of a balanced self-oscillating mixer (SOM) co-designed and integrated with a 16 element quadratic microstrip patch array is presented in this paper. The oscillation frequency of the SOM is 24 GHz and the conversion gain is better than -15 dB. The patch antenna array has a gain better than 16dB. The integrated receiver has a 3dB-bandwidth of 800 MHz and a peak receiver gain of 5.9 dB.**

Keywords- Self-Oscillating Mixer, Microstrip Patch Array

I. INTRODUCTION

The allocated industrial, scientific and medical (ISM) band around 24 GHz is one of attractive bands for the short range radar applications varying from high-tech automotive collision avoidance and healthcare sensors to low-tech door openers. In order to be more commercially competitive in all applications, high performance, low cost and compact size are always of large interest. A traditional receiver front-end is typically composed of antenna, mixer, and a local oscillator (LO). As the operating frequency increases, high output power LO multiplication chain tends to become bulky but is necessary in order to drive the mixer efficiently.

The first FET SOM was reported in [1] where the function of mixer and oscillator are realized by the same transistor without any external LO feed. Since the oscillating frequency is limited by device's f_{max}, sub-harmonic SOM [2] and balanced SOM [3] where the input RF signal will mix with higher order LO harmonics are good solutions to extend the frequency range of operation.

For a cost-effective overall solution, it is beneficial if both the mixer and the antenna are integrated in the same planar technology. Planar dipoles are not considered in this work due to the matching problem in the chosen technology with thin substrate. Even though planar slots are feasible, they require opening in the ground planes when fed by microstrip lines. Hence, for easy integration with microstrip, a patch array is selected as suitable candidate.

In this paper, a balanced SOM integrated with a patch antenna is designed for 24 GHz application. The overall design was integrated on standard Rogers3003 with ε_r=3, [4]. The surface mount active devices are standard VMMK-1225 HEMTs offered by Avago Technologies, [5]. The proposed topology performs well as a receiver and can be further modified for FMCW application.

II. BALANCED SOM DESIGN

The SOM can be designed as a simple combination of a single-ended mixer and a common source oscillator, as shown in Fig. 1. Because of the source and gate feedback, the transistor oscillates at a frequency determined by the oscillation condition. The RF input signal from the gate is mixed with the oscillating frequency, and an IF output signal is extracted by a low-pass filter from the drain.

The balanced SOM contains two identical SOMs shown in Fig. 1, which are connected by a transmission line at the gate, as shown in Fig. 2. According to the analysis in [3], such fully symmetric topology forces the middle point of the gate transmission line as virtual ground. In this case, once the two transistors start oscillating, signals generated by these two branches will be 180-degree out-of-phase.

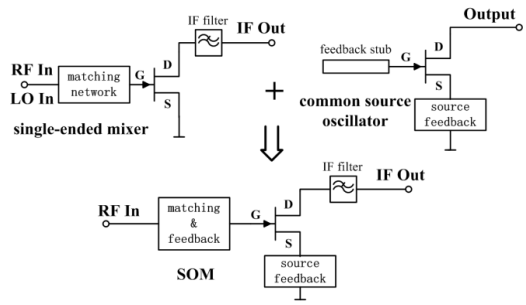

Fig. 1. Combine single-ended mixer and common source oscillator into a SOM.

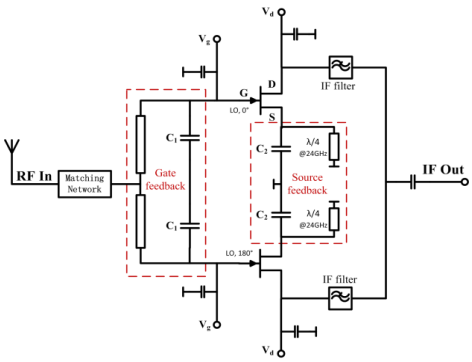

Fig. 2. Schematic of balanced SOM.

Fig. 2. shows the schematic of the balanced SOM in this work. Both the gate transmission line and the shunt capacitance 'C_1' serve as the gate feedback. The oscillating frequency can be tuned by varying the length of the transmission line or by varying the capacitance 'C_1'. Negative resistance at the gate is introduced by the source feedback capacitor 'C_2'. The fundamental oscillating frequency of 12 GHz is achieved by tuning the value of C_1, C_2 and the length of the gate transmission line in ADS simulation. A quarter wavelength short-circuited stub (at 24 GHz) is connected at the source to complete DC ground path of the transistor. The synthesized low-pass filter needs inductances in the order of nH. The high-Q inductors are realized with bond wires instead of surface-mount inductors with low-Q factor. The RF port when inserted at the centre point does not affect the oscillation condition due to the virtual ground property.

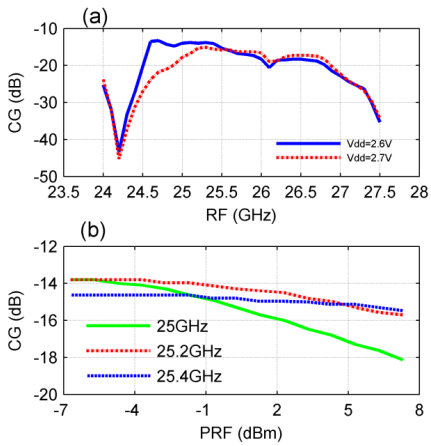

Fig. 3. (a) Measured conversion gain under different drain bias. (b) Measured input 1dB compression

The anti-phase conditions offered by the topology will cancel the fundamental frequency and all the odd harmonics at both RF and IF ports, while the even harmonics are in phase. Thus, when RF is applied, it splits in phase to both gates and mixed with 2nd harmonic and further gets added at the IF port.

The stand-alone SOM is manufactured and measured. The LO applied by the 2nd harmonic of the self-oscillation frequency is around 24 GHz. Then the measured conversion gain of the balanced SOM is shown in Fig. 3(a). A peak conversion gain of -13.3 dB @ 24.7 GHz is achieved with an optimum bias point of V_d=2.6 V and V_g=0.4 V. Sweeping RF frequencies from 24.6 GHz to 25.5 GHz, better than 15 dB conversion loss is achieved. The deep drop at 24.2 GHz is caused by resonance of drain bias network at 200 MHz IF, and it can be shifted down towards lower IF frequency by adding a serial connected inductor. As can be seen from Fig. 3(b), the input 1 dB compression point is around 0 dBm.

III. ANTENNA DESIGN

The patch antennas being resonant, offers limited bandwidth and it strongly depends upon the thickness and dielectric constant of the substrate. For wide bandwidths, low ε_r and thick substrates are suggested [6]. The wideband patch arrays even though having excellent crosspol characteristics requires multiple PCB layers to achieve aperture coupling [7]. Also bandwidth of the patch can be enhanced by using inset feed or making openings in the ground plane of the patch [8]. But for current application, to achieve low cost solution, only single metal layer is used for the design. With such a constraint, series fed microstrip patches integrated with MMIC receiver in mm wave band are demonstrated in [9],[10]. Integration of such an array with sub-harmonic mixer is demonstrated in [11].

Even though, series fed patch array is simpler in layout, the phase shift offered by the patch and the series line becomes frequency dependent, which results in beam scanning. Hence, for this work, broadside beam with 20dBi directivity using uniform amplitude and phase feeding network is selected.

A. Analytical Far-field function of Patch Array

Microstrip patch antennas inherently have broad beamwidths. So for higher directivity, uniformly excited patch array is unavoidable. The far-field function of single patch by using transmission line model is discussed in [12],[13]. By choosing the origin of coordinate system to center of the patch the far-field function is written as,

$$G_p(\theta,\varphi)=\frac{j\cdot 4E_o h}{\pi}*\left\{\frac{\sin\left(k\frac{w}{2}\sin\theta\cos\varphi\right)}{\sin\theta\cos\varphi}\right\}$$

$$*\left\{\cos\left(k\frac{l}{2}\sin\theta\sin\varphi\right)\right\}*\left[\sin\varphi\hat{\theta}+\cos\theta\cos\varphi\hat{\varphi}\right]\cdots\theta\le\frac{\pi}{2}$$

$$\frac{\sin\left(k\frac{w}{2}\sin\theta\cos\varphi\right)}{\sin\theta\cos\varphi}=k\frac{w}{2}\cdots\sin\theta\cos\varphi\to 0$$

$$G_p(\theta,\varphi)=0\cdots\cdots\cdots\theta>\frac{\pi}{2}$$

where

- l=length of the patch;
- w= width of the patch;

- k=propagation constant;
- h=height of the substrate.

The far-field function of whole array is then achieved by element-by-element sum technique. To get equal beamwidths in E- and H- planes quadratic array with equal spacing in x-y direction is chosen. The requirement of 20dBi directivity gets satisfied by choosing 4 x 4 elements with spacing of ~0.75λ. The complete analytical far-field function of array is then written as,

$$G_A(\theta,\varphi)=\sum_{m=1}^{N}\sum_{n=1}^{N} G_p(\theta,\varphi)e^{jk\Delta\sin\theta\left\{\left(m-\frac{N+1}{2}\right)\cos\varphi+\left(n-\frac{N+1}{2}\right)\sin\varphi\right\}}$$

where

- Δ=element spacing in x-y direction (9000μm);
- N=max. number of elements (N=4).

B. Simulated & Measured Performance of Patch Array

For practical array, feeding network made up of microstrip lines and finite ground plane size is needed. Once the array geometry is selected, the initial patch dimensions are calculated using [13]. The microstrip feed network for 4 x 4 elements is designed using [14]. Finally, the whole geometry was simulated and optimized in [15]. The comparison between analytical patch array with infinite ground plane and simulated patch array with feeding network and finite ground plane size of 42 x 40 mm^2 is shown in Fig. 4.

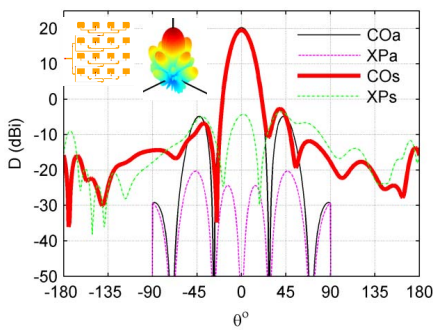

Fig. 4. Comparison between Analytical and Simulated pattern @ 25 GHz.

The φ=45º copolar and crosspolar patterns seen in Fig.4 clearly shows the high crosspolar levels due to unwanted radiations from microstrip lines. This spurious radiation reduces directivity and destroys on-axis null for crosspol. The 3-D radiation pattern along with array geometry is shown at the top left corner in Fig. 4.

The patch array is characterized by input reflection coefficient and radiation pattern measurements ins anechoic chamber. The performance of the array considering directivity and gain and S_{11} are shown in Fig. 5(a) and (b). The discrepancy in simulated and measured S_{11} is due the fact that there exist connectors/adaptors between calibrated reference plane and microstrip antenna port. Also the radiation pattern measurements are influenced by imperfections in the anechoic chamber and limited dynamic range (<50dB) due to high cable losses. The main beam is in well agreement with simulations. Similar observations are noted over various measured frequencies. The simulated and measured E-, H-plane radiation patterns are shown in Fig. 6(a) and (b), similar agreement has been observed for other frequencies in the band of 24~26 GHz.

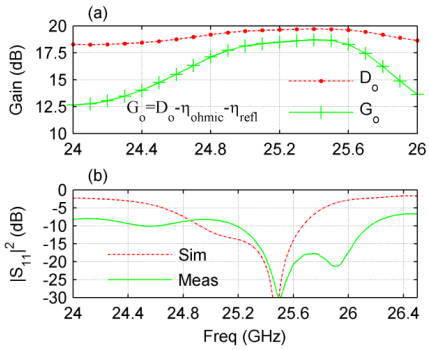

Fig. 5. (a) Simulated gain, (b) simulated and measured S11.

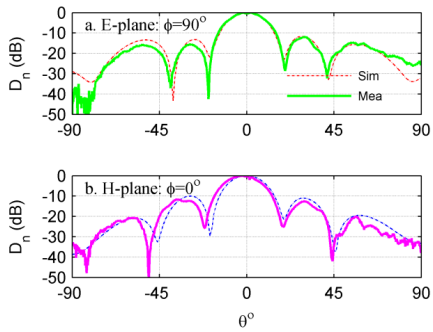

Fig. 6. Simulated and measured (a) E-plane and (b) H-plane @ 25 GHz.

IV. RECEIVER CHARACTERISTICS

The 24 GHz balanced SOM integrated with 16 element quadratic microstrip patch array was fabricated and mounted as shown in Fig.7.

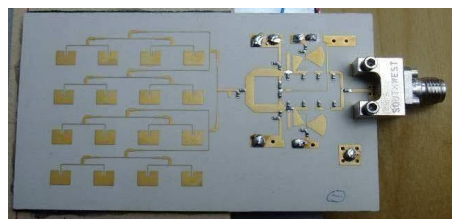

Fig. 7. Fabricated 24 GHz SOM with integrated 16-element patch antenna, board size 75x45mm.

For the characterization of the SOM with integrated antenna, a measurement setup according to Fig. 8 was

arranged. The horn antenna and receiver SOM are aligned for horizontal polarization at a range of 4 m, which guarantee the far field condition.

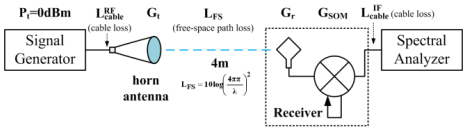

Fig. 8. Measurement setup and link calculations.

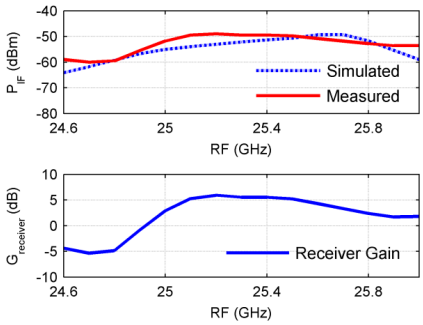

Fig. 9. (a) Measured & simulated IF power, (b) Measured receiver gain

The IF power can be calculated by Eq. (1).

$$P_{IF} = P_t + G_t - L^{RF}_{cable} - L_{FS} + G_r + G_{SOM} - L^{IF}_{cable} \quad (1)$$

where the power values are measured in dBm, and the gain/loss are given in dB:

- P_t=power from generator;
- G_t=gain of horn antenna;
- L^{RF}_{cable}=loss of RF cable;
- $L_{FS} = 20log\left(\frac{4\pi df}{c}\right)$ (free-space path loss);
- G_r=gain of patch array;
- G_{SOM}=conversion gain of SOM;
- L^{IF}_{cable}=loss of IF.

The simulated and measured IF power is shown in Fig. 9(a). The gain of the integrated receiver, which incorporates the antenna gain and the conversion loss of the SOM ($G_{receiver} = G_r + G_{SOM}$ in dB), can be extracted from the measurement, and the result is shown in Fig. 9(b). The peak gain of the receiver achieves 5.9 dB at 25.3 GHz RF. A 3dB-bandwidth of 800 MHz is obtained with a power consumption of 52 mW.

V. Conclusion

A balanced self-oscillating mixer integrated with 16 element quadratic microstrip patch array is designed, fabricated and measured for 24 GHz receiver application. Inherent symmetry of balanced SOM guarantees the anti-phase performance and amplitude balance, which further suppress the fundamental oscillation efficiently. RF signals mix with the 2nd harmonic of the oscillating frequency and a better than -15 dB conversion gain is achieved with 900 MHz bandwidth. The measured patch array performance is in agreement with simulations. The bandwidth for VSWR<2.0 is about 1GHz and can be improved with appropriate choice of substrate. Also the simulated and measured system performance agrees well. The integrated receiver achieves a peak gain of 5.9 dB and a 3dB-bandwidth of 800 MHz.

Acknowledgment

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Paper B

Monolithically integrated 200-GHz double-slot antenna and resistive mixers in a GaAs-mHEMT MMIC process

Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, B. Motlagh, S. Cherednichenko, I. Kallfass, A. Leuther, and H. Zirath

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Monolithically Integrated 200-GHz Double-Slot Antenna and Resistive Mixers in a GaAs-mHEMT MMIC Process

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***Abstract*—This paper presents the design and characterization of two resistive mixers integrated with a double-slot antenna in a 100-nm GaAs mHEMT technology. With RF frequency varying from 185 to 202 GHz, a typical conversion loss (L_c) of 8.0 dB is measured for the single-ended mixer and a typical L_c of 12.2 dB is obtained from one of the two IF outputs for the single-balanced mixer. Each mixer is integrated with a double-slot antenna and mounted on an Si lens. Incorporating the antenna gain and the conversion loss of the mixer, a typical receiver gain of 15.4 dB is achieved for the integrated antenna with single-ended mixer, and a typical receiver gain of 11.2 dB is obtained for the integrated antenna with single-balanced mixer by measuring one of the two IF outputs.**

In this paper, a novel method is also proposed and proved to evaluate a moderate to high noise figure (NF) device in millimeter/submillimeter frequency band. The result shows that the single-ended mixer in this paper has an NF around 1.0 dB higher compared to its L_c, and the single-balanced one has an NF about 1.6 dB higher than its L_c at room-temperature operation.

***Index Terms*—Conversion loss, double-slot antenna, GaAs, G-band, metamorphic HEMT (mHEMT), monolithic microwave integrated circuit (MMIC), noise figure (NF), N-times, resistive mixer, system gain.**

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I. Introduction

MILLIMETER-WAVE (30–300 GHz) systems are playing an increasingly important role in many scientific and military applications, such as remote sensing, radio astronomy, radar, and communication. Compared with microwave systems at lower frequencies, millimeter-wave remote sensing (imaging) systems have higher spatial resolution ability and more compact size. Furthermore, they are less sensitive to the atmospheric attenuation (water vapor absorption and particles scattering) when compared with terahertz (300 GHz–3 THz) systems [1].

Using traditional building practice, the monolithic microwave integrated circuit (MMIC) and the antenna are optimized individually in different technologies and connected through bond or ribbon wires. This becomes increasingly difficult with increasing frequency since the interconnecting wires will deteriorate the performance of the system. At frequencies beyond 100 GHz, a good solution could be to integrate the antenna on the MMIC itself [2], [3], as a necessary step in optimizing the performance of transmit/receive (T/R) components. With the present state of the performance at microwave frequencies, a mixer is commonly preceded by a low-noise amplifier (LNA) to minimize the noise figure (NF). However, due to the limitation in f_t and $f_{\max}$ of the active devices, it is challenging to design LNAs at the higher millimeter- and submillimeter-wave frequencies. Therefore, a monolithic receiver that integrates a planar antenna [4] directly with a resistive mixer is an attractive and convenient solution at these frequencies.

This paper presents an integrated design of a double-slot antenna with two resistive mixers at G-band (140–220 GHz), based on the 100-nm metamorphic HEMT (mHEMT) technology from the Fraunhofer Institute of Applied Solid-State Physics (FHG-IAF), Freiburg, Germany.[1] In order to evaluate the NF of the designed mixers, a novel method is also proposed and proven in this paper.

II. Technology

For high-frequency and ultra-low-noise applications, the HEMT based on InGaAs/InAlAs heterostructures with high In-content in the electron transport channel is a well-proven device [5], [6]. These heterostructures can either be grown directly on InP substrates or by using a metamorphic buffer to adapt the lattice constant on GaAs wafers. The advantages of

[1][Online]. Available: http://www.iaf.fraunhofer.de

TABLE I
DC AND RF PARAMETERS OF A 2×30 μm GATE-WIDTH 100-nm mHEMT

R_c	0.07 Ω
R_s	0.25 Ω
$g_{m,max}$	1400 mS/mm
$I_{D,max}$	900 mA/mm
f_t	200 GHz
f_{max}	300 GHz

the metamorphic approach are the price and quality of the GaAs wafers. The material is less brittle than InP, and wafers with high crystal quality are available up to 150-mm wafer diameter. In addition, metamorphic buffers with lattice constants larger than InP enable even InAs channels [7]. The disadvantage of the mHEMT is the additional growth effort.

The mHEMT layers are grown on 4-in semi-insulating GaAs wafers by molecular beam epitaxy (MBE). For the metamorphic buffer, a linear $In_xAl_{0.48}Ga_{0.52x}As$ $(x = 0 \rightarrow 0.52)$ transition is used. Electron beam evaporated GeAu layers are used for the ohmic contacts, which are alloyed at 300 °C on a nitrogen purged hot plate. The 100-nm T-gate is defined by 100-kV electron beam lithography. The devices are passivated with a 250-nm-thick chemical vapor deposition (CVD) deposited SiN layer used as a dielectric layer for the metal–insulator–metal (MIM) capacitors. Further passive elements are NiCr thin-film resistors, an electron beam evaporated Au based interconnection layer, and a 2.7-μm-thick plated Au layer in air-bridge technology.

For MMICs operating in the G-band and beyond, a backside process was developed to suppress substrate modes within the circuits. After front side processing, the 4-in GaAs wafers are glue bonded to sapphire substrates in a vacuum chamber. The GaAs substrates are thinned to a final thickness of 50 μm. Through-substrate vias are etched in a chloride based ICP etching process using resist as etching mask. The via diameter at the etch stop layer on the front side is 30 μm. An additional lithography layer defines the dicing streets on the Au plated wafer backside. Subsequently the 50-μm GaAs wafer is separated from the sapphire substrate by dissolving the glue in an organic solvent. The wafers are rinsed, dried, and subsequently carefully transferred to glue tape for final measurements and dicing.

Typical electrical dc and RF parameters of a 2×30 μm gate width 100-nm mHEMT are shown in Table I.

III. TOPOLOGY AND DESIGN

A. Mixers

A resistive field-effect transistor (FET) mixer uses the channel-resistance of the FET to achieve frequency mixing [8]. Although it is not competitive with the Schottky diode mixer in terms of NF at very high frequencies, the resistive FET mixer is preferred in many applications, like communication, due to the advantages of low dc consumption (virtually zero), superior linearity, and high dynamic range.

Fig. 1 shows the schematic of the single-ended resistive FET mixer. The RF signal is applied to the drain through a single-section coupled line filter, and the LO is applied through a single-stub matching network to the gate of the FET. The IF signal is extracted by an IF filter from the drain. As a resistive mixer, the drain remains unbiased, and the gate voltage, applied through a large resistor, biases the transistor close to pinch-off for enhanced L_c and distortion characteristic. A breakout of the single-ended resistive mixer, without the double-slot antenna, was presented in [9].

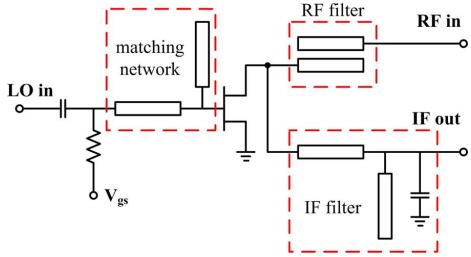

Fig. 1. Schematic of the single-ended resistive mixer.

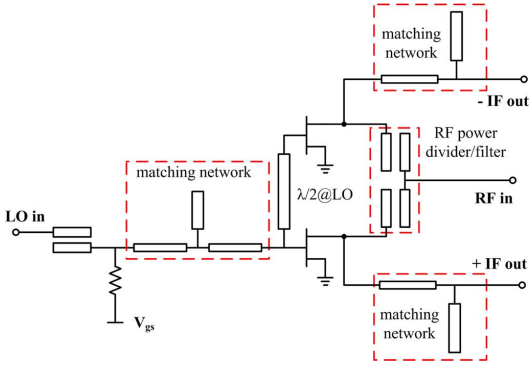

Fig. 2. Schematic of the single-balanced resistive mixer.

A drawback of the single-ended topology is that the LO-to-RF isolation is poor. According to [9], only 9.3-dB isolation was achieved by the single-ended mixer. To suppress this unwanted LO leakage, a balanced mixer topology could be used [10]. The second mixer presented in this paper is a 200-GHz single-balanced resistive mixer. The schematic of this mixer is shown in Fig. 2. A half-wavelength transmission line is used as an 180° phase shifter to apply differential LO signals at the gates of the FETs. Sufficiently low loss of this line ensures amplitude balance between the two branches. The residual out-of-phase LO signals will be combined in-phase and cancelled at the drain. Two 180° out-of-phase IF signals are extracted from the two drains and can be combined in an external balun.

B. Antenna Design

The choice of MMIC-based antenna is often limited by the layer topology of HEMT process. Since the MMIC cost in manufacturing is proportional to its size, small gain antennas are usually feasible. Different types of antenna structures such as

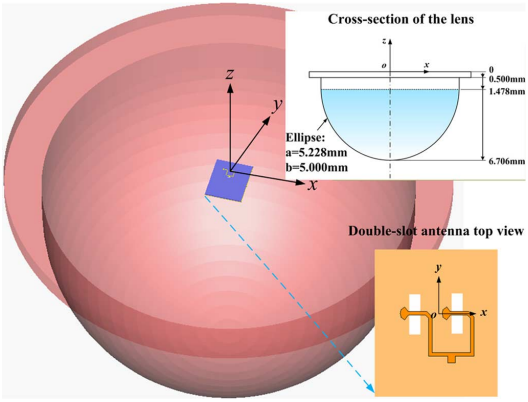

Fig. 3. Double slot antenna with microstrip feed network on Si lens.

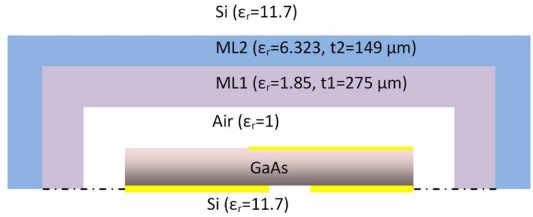

Fig. 4. Simulation setup for impedance matching.

dipoles, folded dipoles, microstrip fed patch, and slots are possible with the layers found in a typical HEMT process. Review on these types of antennas is given in [4].

Slot antennas are preferred in our case in comparison to patch or dipole since microstrip patches on thin substrates have poor ohmic efficiency, while dipoles on thin substrate exhibit low real part of input impedance (a few ohms), which makes them difficult to match.

Coplanar waveguide (CPW) fed double slot antennas are often used at millimeter-wavelengths since its radiation can be coupled to a focusing ellipsoidal lens, as presented in [11] and [12]. Two slot antennas separated by $\lambda_g/2$ make radiation pattern equal in the E- and H-plane. With CPW type of feeding, the slots radiate through the substrate and then further into the lens. If the substrate dielectric constant is matched with the lens, most of the radiation is focused by the lens and the problem of surface wave modes is overcome. It is also possible to use a folded slot antenna fed by CPW lines in this topology, as in [13] and [14].

GaAs, having a dielectric constant of 12.9, is not well matched to that of Si having $\varepsilon_r = 11.7$. Hence, the CPW fed double slot antenna should be modified to be fed with microstrips. Considering the layer topology of the process, slots can be etched out in backside metal layer with microstrip feeding them at top metal layer. The slots directly radiate in the Si lens beneath it. The feeding structure and topology is shown in the inset of Fig. 3.

The separation between the slots is a half-wavelength in silicon. The impedance properties of such microstrip fed slot are studied in [15]–[17], and improved matching of the folded slot using a via-hole is discussed in [18]. In this case, since the slot is at the interface of Si and GaAs, its resonant length is approximately chosen as $\lambda_{\mathrm{Si}}/2$ and the length, as well as radial stub, is optimized numerically for antenna input impedance of 50 Ω. In this work, the length of the slots and the separations are optimized as 180 and 190 μm, respectively. The microstrip lines are terminated with a radial stub and the output from two slots is combined with a microstrip tee.

The Si-lens used in this work has a diameter of 10 mm with ellipsoidal surface defined by semi-major and minor axes of 5.228 and 5 mm, respectively. High-resistivity Si is chosen as a material for fabrication along with the antireflection coating (ARC) of 210-μm thickness made from Stycast 1264 ($\varepsilon_r = 2.9$). Stycast is chosen because its dielectric constant is the closest to the optimum value required, which is 3.42. While mounting the chip on the lens, care is taken that the antenna center is aligned to the lens optical axis to maximize the directivity in broadside direction. The overall geometry of chip+lens is shown in Fig. 3.

The complete geometry presented in Fig. 3 has a large size, and full wave simulation on the whole geometry is time consuming. Hence, for faster simulation, the slots can be made to radiate in infinite Si medium without modeling the lens. Ideally, the slots should radiate in air for upper hemisphere and in infinite Si in lower hemisphere. The simulation tool used in this work, CST MWS [19], allows the complete volume to be filled with the same material, which means that we cannot model the volume as a combination of a semi-infinite Si medium and a semi-infinite air medium. This limitation is overcome by putting finite vacuum box with two Chebyshev quarter-wave matching layers [20] on the microstrip network side, i.e., upper hemisphere, while the rest of the volume is filled with Si. This is illustrated in Fig. 4. By making use of these matching layers, the slot impedance can be optimized much faster as compared to simulating with a whole lens. The double slot antenna input reflection coefficient at microstrip port, optimized for $Z_{\mathrm{ref}} = 50\ \Omega$, using this method is shown in Fig. 5 along with the input reflection coefficient obtained after simulating the entire structure with ellipsoidal lens. The difference between two input reflection coefficients is due to the fact that the ARC made by Stycast is not the ideal one. This results in the small ripples in S_{11}, as seen in Fig. 5.

The simulated antenna (together with Si Lens+ARC) radiation patterns at 200 GHz are shown in Fig. 6 (*top*). The sidelobe level is ~ -19 dB down. This result is similar to that of [12, Fig. 4] with an extension length of 2600 μm for extended hemispherical lens. The variation of the E-plane pattern for different frequency points is shown in Fig. 6 (*bottom*). Altogether, this antenna design achieves directivities of $\sim$24.5 dBi and matching of -10 dB over 190–205 GHz.

IV. Integration of Antenna and Mixer

The RF ports of both the single-ended mixer and single-balanced mixer are matched to 50 Ω for breakout measurements. The double-slot antenna is also matched to the same impedance

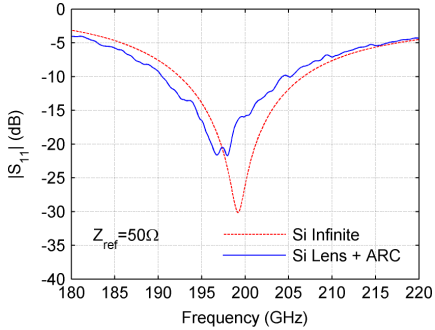

Fig. 5. Simulated antenna input reflection coefficient.

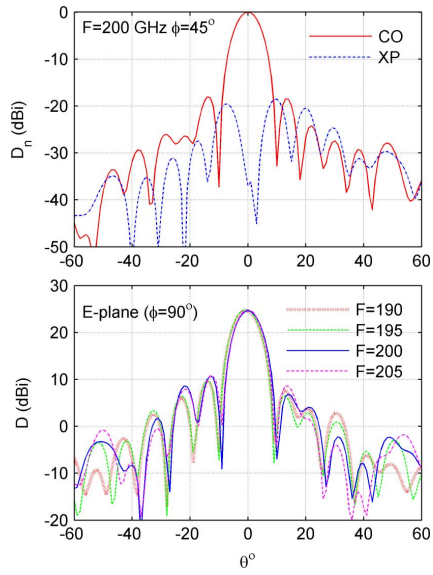

Fig. 6. (*top*) Simulated normalized co- and cross-pol directivity at $f = 200$ GHz, $\varphi = 45^\circ$ plane. (*bottom*) Simulated E-plane patterns for various frequencies.

and is directly coupled to the RF port of the mixer. Chip photographs are shown in Fig. 7. The double slots located at the back of the GaAs substrate beneath the coupler's arms are marked by the black dashed rectangles. The chip dimensions are 1100×700 μm^2 and 900×950 μm^2, respectively.

V. Measurements

Fig. 8 shows the measurement setup. The transmitter is an in-house manufactured $\times 6$ frequency multiplier source module (output frequency band: 163–202 GHz) with a G-band corrugated horn antenna. The transmitter is aligned around 200 mm underneath the Si lens. The local oscillator (LO) signal is applied by a Virginia Diodes Inc. (VDI) $\times$ 18

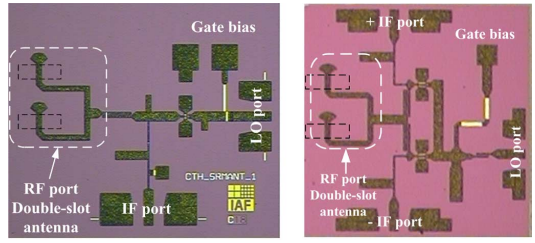

Fig. 7. Chip photograph of: (a) antenna integrated with single-ended resistive mixer and (b) antenna integrated with single-balanced resistive mixer.

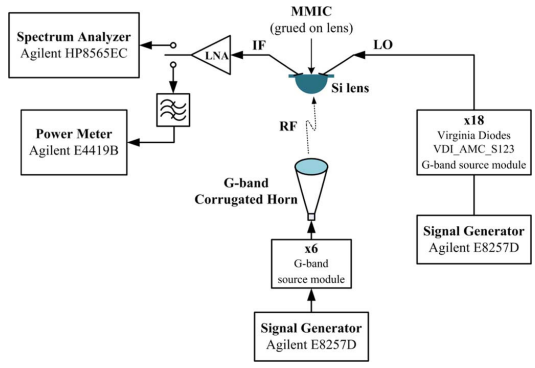

Fig. 8. Measurement setup.

source module[2] together with a signal generator, and further pumped into the mixer's LO port through a G-band on-wafer ground–signal–ground (GSG) probe. The IF output signal is then amplified by an LNA[3] (with 29-dB gain and 4-dB NF) and finally measured by a spectrum analyzer or power meter.

The gain (G_{RX}) of the integrated receiver, which incorporates the antenna gain referred to an isotropic antenna and the conversion loss of the mixer, can be represented by

$$G_{\mathrm{RX}} = P_{\mathrm{out}} - G_{\mathrm{LNA}} + L_{\mathrm{cable}} + L_{\mathrm{probe}} + \mathrm{FSL} - G_t - P_t \tag{1}$$

where the power values are measured in dBm, and the gain/loss are given in decibels.

- P_{out} is the measured IF power.
- G_{LNA} represents the gain of the IF LNA.
- L_{probe} and L_{cable} are the losses of the IF probe and the IF cable, respectively.
- Free-space loss (FSL) can be calculated by $\mathrm{FSL} = 20 \cdot \log((4\pi d)/(\lambda))$ dB and d is the distance between the transmitter and receiver.

[2]VDI, Charlottesville, VA. [Online]. Available: http://www.virginiadiodes.com

[3]B&Z Technologies Inc., Stony Brook, NY. [Online]. Available: http://www.bnztech.com

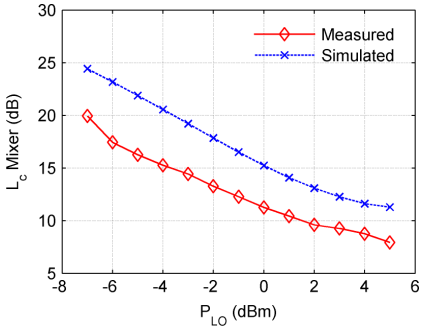

Fig. 9. Conversion loss versus LO power for the single-ended mixer ($f_{\rm LO} = 202$ GHz, $f_{\rm RF} = 201$ GHz).

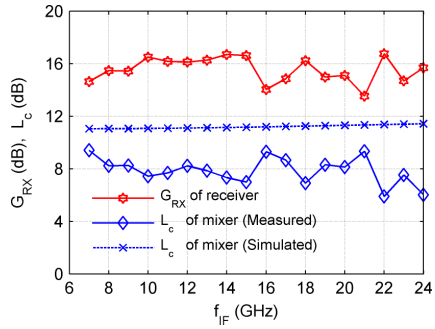

Fig. 10. Conversion loss of the single-ended resistive mixer and measured gain of the integrated receiver with single-ended mixer ($f_{\rm LO} = 209$ GHz).

- G_t is the gain of the corrugated horn and is obtained by electromagnetic (EM) simulation.
- P_t is the RF power from the $\times 6$ module. It was kept at -20 dBm for all the RF frequencies.

Considering the double-slot antenna and the resistive mixers are impedance matched, the mixer's conversion loss L_c can be deduced by

$$L_c = G_r - G_{\rm RX} \tag{2}$$

where the gain (G_r) of the antenna with lens is derived from EM simulation.

A. Measured Results of the Receiver With Single-Ended Resistive Mixer

The gate voltage of the device is tuned prior the measurements to determine the optimum bias that gives the minimum L_c. This tuning is repeated at different LO and RF frequencies and 0 V is chosen as the optimum gate voltage.

Fig. 9 shows the measured L_c versus applied LO power, which is limited by the power from the VDI $\times$ 18 source module. With a maximum applied $+5$-dBm LO power (probe loss has been accounted for), the single-ended mixer is not yet saturated.

Fig. 10 shows the $G_{\rm RX}$ of the system and estimated L_c of the mixer with fixed LO at 209 GHz and a LO power of $+5$ dBm. Within the measured bandwidth, the $G_{\rm RX}$ is higher than 13.5 dB while the typical L_c is 8.0 dB. The measured IF bandwidth is limited by the bandwidth of the $\times 6$ source module, which can only generate signals up to 202 GHz. However, nothing suggests that the IF bandwidth is limited to the shown 6–24 GHz. In the measurement setup, the signal radiated from the transmitting horn not only illuminates the double-slot antenna with Si lens. The rest of the signal power is also reflected by any materials on its way. Some significant fluctuations (e.g., 3.5 dB jumps from 21 to 22 GHz) that are caused by multipath effect can be seen from the curves. The results have been improved significantly by placing absorbing material in a wide area around the transmitting antenna.

The $G_{\rm RX}$ of the receiver and the L_c of the mixer are also measured at fixed IF of 1 GHz by tuning the LO and RF frequencies at the same time, as shown in Fig. 11. At each LO frequency,

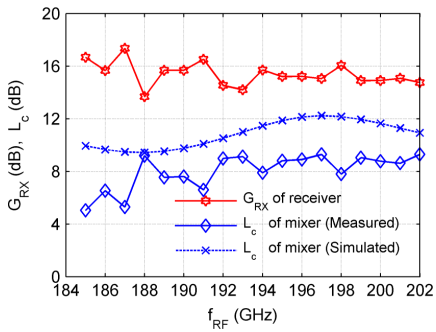

Fig. 11. Conversion loss of the single-ended resistive mixer and measured gain of the integrated receiver with single-ended mixer ($f_{\rm IF} = f_{\rm LO} - f_{\rm RF} = 1$ GHz).

the highest output power (3–5 dBm after probe loss correction) from the LO module is applied to the mixer. A typical system gain of 15.4 dB is achieved, and the typical L_c is 8.0 dB.

B. Measured Results of the Receiver With Single-Balanced Resistive Mixer

The single-balanced mixer has two differential IF outputs that are not combined on-chip. During the measurements, only one of the IF output signal is measured while the other one is terminated with a 50-Ω load. As the input LO power is split into two equal parts to feed the balanced topology, lower LO power to each branch will see a higher L_c of the individual mixer cells compared to the single-ended mixer.

The same measurements have been performed on the receiver with single-balanced mixer as for the single-ended design. -0.2 V is chosen to be the optimal gate voltage.

In the measurement, we found that the outputs from the two IF ports are not equal, but possesses a 4-dB difference. When resimulating the design, this unequal performance from the two IF ports can be observed. As can be seen from the simulated conversion loss as a function of LO power in Fig. 12, L_c derived from the "IF+" port, referred to Fig. 7(b), is better than that from "IF$-$" port unless the transistors are saturated by sufficient LO power. Further simulation indicates that this effect

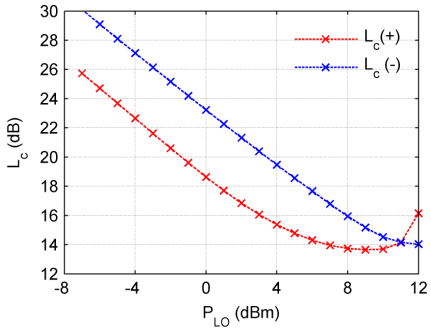

Fig. 12. Simulated conversion loss from two IF ports as a function of LO power for the single-balanced mixer ($f_{\rm LO} = 186$ GHz, $f_{\rm RF} = 187$ GHz).

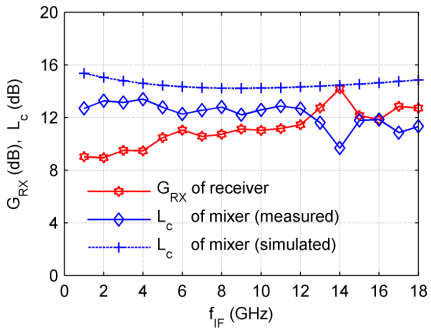

Fig. 13. Conversion loss of the single-balanced resistive mixer and measured gain of the integrated receiver with single-balanced mixer ($f_{\rm LO} = 184$ GHz).

originates from the on-chip LO balun, which is shorter than a desired length of $\lambda_{\rm LO}/2$, and results in an unequally pumped LO power at the gates of the two transistors. The performance of this mixer could thus be improved by a properly designed LO balun. The following results will present the performance obtained from the "IF+" port.

Keeping the maximum LO power (3–5 dBm over frequency after probe loss correction) from the LO source, the $G_{\rm RX}$ of the receiver and the L_c of the single-balanced mixer are measured with fixed LO (=184 GHz) and fixed IF (=1 GHz), respectively, as shown in Figs. 13 and 14. The receiver achieves a typical gain $(G_{\rm RX})$ of 11.2 dB and the resistive single-balanced mixer achieves a typical L_c of 12.2 dB.

C. NF Estimation

For the measurement of NF, we propose a novel method, called the signal generator N-times power method, which is suitable for evaluating moderate to high NF devices operating beyond 100 GHz. According to this method, the noise factor can be calculated as

$$F_{\rm sys} = \frac{P_{\rm gen}}{k \cdot T_0 \cdot B \cdot (N-1)} \tag{3}$$

where

- $F_{\rm sys}$ is the noise factor to be determined;

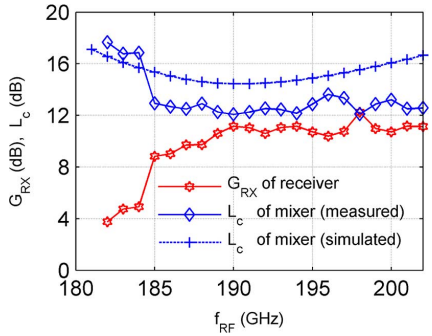

Fig. 14. Conversion loss of the single-balanced resistive mixer and measured gain of the integrated receiver with single-balanced mixer ($f_{\rm IF} = 1$ GHz).

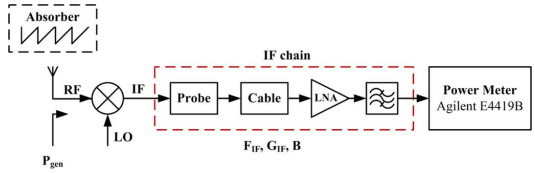

Fig. 15. IF chain for NF measurement.

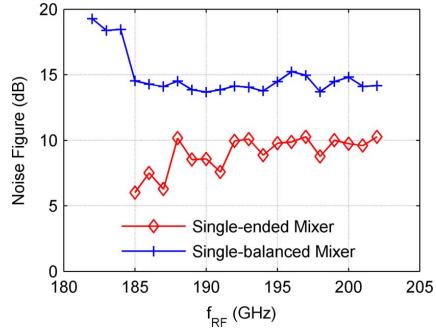

Fig. 16. Measured NF of the single-ended mixer and single-balanced mixer.

- k is the Boltzmann constant;
- T_0 is the room temperature in Kelvin;
- B is the noise bandwidth in hertz;
- N is the ratio between two output powers;
- $P_{\rm gen}$ is the input power in watt.

More details of the signal generator N-times power method is clarified in the Appendix.

The NF measurement setup is similar to the setup shown in Fig. 8, but a low-pass filter is added in the IF chain, as shown in Fig. 15. The NF of the receiver cascaded with the IF chain is evaluated by the signal generator N-times power method. For the measurement without continuous wave (CW) signal input, the matched load is replaced by absorbers at room temperature facing the receiver antenna. Certain power is then received from the transmitting antenna and $P_{\rm gen}$ should be the calculated RF power right at the RF port of mixer. Once the NF of the cascaded

TABLE II
COMPARISONS TO OTHER RECEIVER WITH ON-CHIP ANTENNA

f_{RF} (GHz)	*G_c (dB)	NF (dB)	DC Consumption (mW)	Size (mm^2)	Antenna Topology	Technology	Reference
140	-43	N/A	120	0.58×0.7	Tapered Slot	65 nm CMOS	[25]
170	-30	21	800	1.52×0.84	Tapered Dipole (with metal fill)	120 nm SiGe BiCMOS HBT	[26]
200	15.4	9	0	1.1×0.7	Double-Slot	100 nm GaAs mHEMT	This Work
200	11.2	13.8	0	0.9×0.95	Double-Slot	100 nm GaAs mHEMT	This Work
220	2 (without antenna)	8.4	40	3.0×1.0	Square Slot	100 nm GaAs mHEMT	[2]
220	3.5 (without antenna)	7.4	110	2.75×1.75	Square Slot	100 nm GaAs mHEMT	[24]
650	-13	42	433	1.2×0.6	Folded Dipole	130 nm SiGe:C BiCMOS HBT	[3]
823	-22	47	1200	2.3×0.57	2×2 patch array	250 nm SiGe BiCMOS HBT	[27]

*G_c is the receiver gain including the gain of receiver chain and the antenna gain referred to the isotropic antenna.

subsystem is found, the NF of the IF chain is de-embedded by Friis' formula to obtain the NF of the mixers.

In order to make the measurement easier and compatible with the previous L_c measurements, the IF is fixed at 1 GHz and RF and LO frequencies are swept. Fig. 16 shows the calculated NF of the single-ended mixer and the single-balanced mixer. Note that the NF curves have the same trend as the conversion loss, including certain multipath effect. This is reasonable, because for both L_c and NF measurement, we choose the same frequencies and use the same measurement setup, thus, the multipath effect will be the same. Comparing the NF with the L_c shown in Figs. 11 and 14, respectively, the single-ended mixer has an NF around 1.0 dB higher than its L_c, and the single-balanced mixer shows an NF of 1.6 dB higher than its L_c.

VI. COMPARISON TO OTHER REPORTED MONOLITHIC RECEIVER WITH ON-CHIP ANTENNA

The performance of the two receivers described in this paper is compared to the state-of-art monolithic integrated receiver with an on-chip antenna operating above 100 GHz. As can be seen from Table II, the integrated receiver in GaAs HEMT technologies performs better than those in silicon technologies in terms of conversion gain and NF. Two integrated single-chip receivers at similar frequencies and using the same MMIC technology are reported in [2] and [21]. These chips achieve better NF performance compared to the MMICs presented in this work. However, both of them integrate a three-stage LNA between the antenna and the mixer, which improve the system NF at the cost of a larger, and thus, more expensive solution in terms of manufacturing and dc power consumption. Therefore, the work presented in this paper with an antenna integrated with a resistive mixer is preferred where simplicity and low power consumption are critical issues.

VII. CONCLUSION

In this paper, design and characterization of two resistive mixers integrated with a double-slot antenna on an Si lens have been presented. With +5-dBm LO power, a typical gain of 15.4 dB is achieved for the receiver with a single-ended mixer, and typically 8.0-dB conversion loss is obtained for the single-ended mixer. For the single-balanced topology, a typical gain of 11.2 dB is achieved for the receiver with one of the two IF outputs being measured, and a typical conversion loss of 12.2 dB is measured from one of the two IF outputs for the single-balanced mixer. 3–4-dB deviation between the simulated and measured results might be because that the large-signal model of the transistor is not accurate enough.

In order to evaluate the NF of the resistive mixers, a novel method is proposed and evaluated in this paper. This method is suitable for moderate-to-high NF circuits operating beyond 100 GHz, where commercial noise sources are difficult to find and the Y-factor is small with loads at 77/295 K. Using the signal generator N-times power method, the calculated results show that the NF of the single-ended mixer is around 1.0 dB higher than its conversion loss, and the NF of the single-balanced mixer is about 1.6 dB higher than its conversion loss.

APPENDIX
SIGNAL GENERATOR N-TIMES POWER METHOD

The NF is an important factor when evaluating the performance of a communication system. The Y-factor method is commonly used by commercial noise figure analyzers (NFAs) [25], where abundant noise power coming from a noise source serves as the hot load and a matched load at room temperature (295 K) serves as the cold load. As frequency increases beyond 100 GHz, a matched load under room temperature and liquid nitrogen (77 K) are usually chosen as the hot load and cold load, respectively [2]. For a high NF system, the Y-factor will be very small, and thus difficult to measure accurately. On the contrary, the signal generator twice-power method [26] is useful for devices with high NF. The output power is firstly measured when the input is terminated with a matched load at room temperature. A CW signal generator is then connected and its power (P_{gen}) is adjusted to produce a 3-dB increase at the output. An accurate measurement of P_{gen} is the most critical and error prone part of this method. As the CW input frequency increasing above 100 GHz, the P_{gen}, which results in only 3-dB increases at the output, could be difficult to measure

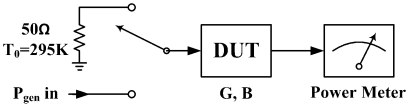

Fig. 17. Block diagram of the signal generator N-times power method.

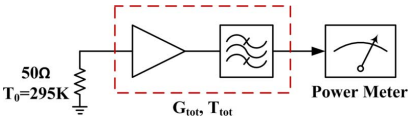

Fig. 18. Method of finding out equivalent noise bandwidth.

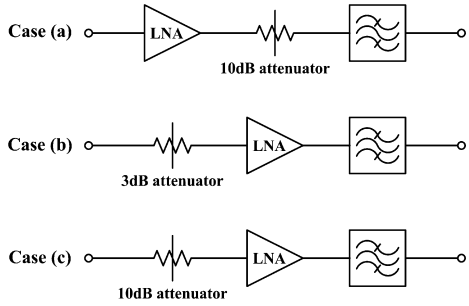

Fig. 19. Case (a): low NF. Case (b): medium NF. Case (c): high NF networks for measurement comparison.

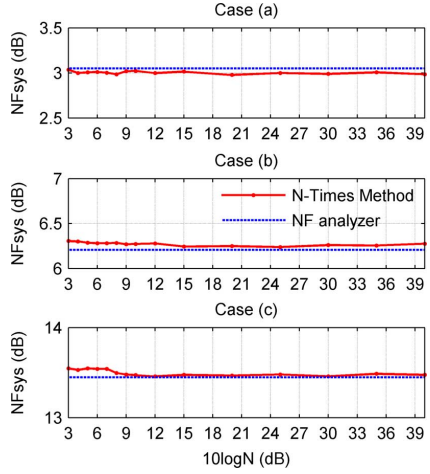

Fig. 20. NF comparison with different measurement.

accurately depending on the dynamic range of the power meter. Therefore, a more accurate measurement will be achieved if a higher $P_{\rm gen}$ can be applied. Based on the signal generator twice-power method, we propose the signal generator N-times power method.

Referring to Fig. 17, $T_0 = 295$ K is room temperature, assuming the device-under-test (DUT) has a bandwidth of B Hz and a linear gain of G. We assume the DUT has an equivalent noise temperature of $T_{\rm sys}$ (which is unknown). The input is first terminated by a load at the room temperature T_0, and the output power is measured to be P_1. According to noise power definition [27],

$$P_1 = k \cdot (T_0 + T_{\rm sys}) \cdot B \cdot G \tag{4}$$

where $k = 1.38 \times 10^{-23}$ is the Boltzmann constant.

Next, a CW signal generator is connected to the input port, where the CW signal should be within the bandwidth of the DUT. With an input power of $P_{\rm gen}$, an output power of P_2 is obtained, where P_2 is the mix of noise power and amplified CW signal. It can be written as

$$P_2 = k \cdot (T_0 + T_{\rm sys}) \cdot B \cdot G + P_{\rm gen} \cdot G. \tag{5}$$

By dividing (5) by (4), we will achieve

$$T_{\rm sys} = \frac{P_{\rm gen}}{k \cdot B \cdot (N-1)} - T_0 \tag{6}$$

where $N = P_2/P_1$ is the ratio of the measured power in the two cases.

The noise factor now becomes

$$F_{\rm sys} = 1 + \frac{T_{\rm sys}}{T_0} = \frac{P_{\rm gen}}{k \cdot T_0 \cdot B \cdot (N-1)}. \tag{7}$$

According to (7), the gain is not needed to determine $F_{\rm sys}$, but the noise bandwidth, B, must be known. Practically speaking, bandwidth can be confined by a bandpass filter (BPF) connected before the power meter. The value of B should be a calculated equivalent noise bandwidth with rectangular and "flat-top" frequency response spectral. Fig. 18 shows one way to determine the equivalent noise bandwidth. The input of the IF chain is terminated with a 50-Ω load at room temperature. The output power, P_N, is measured by the power meter and can be expressed as

$$P_N = k \cdot (T_0 + T_{\rm tot}) \cdot B \cdot G_{\rm tot} \tag{8}$$

where the IF gain $G_{\rm tot}$ and the noise temperature $T_{\rm tot}$ are obtained from a separate calibration with the NFA. The equivalent noise bandwidth is then

$$B = \frac{P_N}{k \cdot (T_0 + T_{\rm tot}) \cdot G_{\rm tot}}. \tag{9}$$

Three simple networks have been characterized by the proposed method and by a commercial NFA (Agilent N8975A) as an experimental validation. As is shown in Fig. 19, network (a) has been used to apply low NF (<5 dB) and (b) with moderate NF (5–10 dB) and high NF (>10 dB) for network (c). NF at 14.25 GHz,, which is the center frequency of the BPF, is evaluated by the signal generator N-times power method at different ratio N. As can be seen from Fig. 20, results obtained by the signal generator N-times power method coincide very well with the one measured by the commercial NFA.

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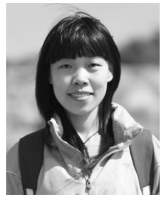

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