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Charge carrier velocity in graphene field-effect transistors

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To extend the frequency range of transistors into the terahertz domain, new transistor technologies, materials, and device concepts must be continuously developed. The quality of the interface between the involved materials is a highly critical factor. The presence of impurities can degrade device performance and reliability. In this paper, we present a method that allows the study of the charge carrier velocity in a field-effect transistor vs impurity levels. The charge carrier velocity is found using high-frequency scattering parameter measurements followed by delay time analysis. The limiting factors of the saturation velocity and the effect of impurities are then analysed by applying analytical models of the field-dependent and phonon-limited carrier velocity. As an example, this method is applied to a top-gated graphene field-effect transistor (GFET). We find that the extracted saturation velocity is ca. $1.4 \times 10^7$ cm/s and is mainly limited by silicon oxide substrate phonons. Within the considered range of residual charge carrier concentrations, charged impurities do not limit the saturation velocity directly by the phonon mechanism. Instead, the impurities act as traps that emit charge carriers at high fields, preventing the current from saturation and thus limiting power gain of the GFETs. The method described in this work helps to better understand the influence of impurities and clarifies methods of further transistor development. High quality interfaces are required to achieve current saturation via velocity saturation in GFETs. © 2017 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).

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The frequency range of electronic components is continuously being pushed towards higher frequencies. Particular interest is focused on the terahertz domain, due to the potential applications in imaging for medicine or security, spectroscopy, and wireless communication.

To increase the performance of high-frequency transistors regarding the figures of merit, namely, the transit frequency ($f_T$) and the maximum frequency of oscillation ($f_{\text{max}}$), new materials and technologies are still being explored. A critical factor is the interface between different materials. Impurities degrade the performance and reliability of a device. It is important to find characterization methods to study the origin of impurities and to understand how they affect device performance.

The saturation velocity of charge carriers in a transistor channel at high fields is an important material property for achieving high $f_T$ and $f_{\text{max}}$ values. Because of the large intrinsic charge carrier mobility and intrinsic saturation velocity of graphene, many efforts have been made to apply this fairly new material in high-frequency transistors. Therefore, in the following paragraph, graphene field-effect transistors (GFETs) are considered.

In previous investigations on the charge carrier velocity in GFETs using dc drain current measurements, pulsed current-voltage (I-V) measurements or transit frequencies were employed. The dc drain current method does not separate velocity and concentration, and hence, the evaluated velocity is affected by trapping/de-trapping. The pulsed I-V method avoids the slow trapping mechanisms and measures intrinsic velocity; hence, it does not allow the effects of impurities to be studied. Furthermore, the rapid (nanosecond) pulses drive charge carriers on a time scale that is much faster than that on which the energy coupling to the adjacent gate and substrate dielectrics can occur. This deviates from the velocity saturation effects in GFET structures. Under real application conditions, the saturation velocity is believed to be limited by intrinsic graphene optical phonons (OPs), surface optical phonons (SOPs) in the dielectrics, and self-heating. The transit frequency method, as published, provides velocity only, i.e., without concentration.

In this work, a method is introduced to study the charge carrier velocity in top-gated chemical vapour deposited (CVD) GFETs without the need to use a pulsed I-V measurement technique, thus allowing the study of charge carrier velocity under real application conditions. We analyze GFETs with typical top-gate design developed for high frequency applications since it allows for direct association of the evaluated carrier velocity with the GFET design and material features and their further development. Microwave measurements of high-frequency scattering parameters (S-parameters) and dc I-V characteristics are combined to determine the charge carrier velocity and charge carrier concentration independently. This allows us to demonstrate how the carrier generation from traps limits the drain current saturation. Transit frequencies are calculated from the S-parameters and are used to find the velocity of the charge carriers directly from the transit time via delay time analysis. Knowing the velocity of the charge carriers allows us to find...
the concentration of the charge carriers from the dc I-V characteristics, which is used in the analysis of phonon-limited saturation velocity. Through the use of the proposed method, the limiting factors of the saturation velocity in top-gated GFETs can be analysed. Furthermore, the effects of impurities on the mobility, the saturation velocity, and the current saturation are investigated.

Details and sequences of the fabrication steps and the characterization are given in the supplementary material. Sets of GFETs with gate length \( L = 1.0 \mu m \) and different total gate width \( W \) values of 2.5, 5, 10, and \( 20 \mu m \) are fabricated and characterized. In the analysis below, if not mentioned specifically, the GFETs with total gate width \( W = 20 \mu m \) are used. The variation in the concentration of impurities between samples is inherent to the fabrication process and is used to study the effect of impurities on the charge carrier velocity in the GFETs. Figure 1 shows a typical optical micro-photo with two gate fingers connected in parallel and a schematic 3D view of the gate stack of the GFETs.

The general outline of the developed method of analysis of the charge carrier velocity in GFETs is as follows. The transfer characteristics are used to extract the residual charge carrier concentration, the low-field mobility, and the contact resistance. Transit frequencies are calculated from the measured S-parameters, \( \tau_{int} \) is the transit delay, \( \tau_{ext} \) is the delay time required to charge the parasitic parts of the active device region, \( \tau_{pad} \) is the delay time associated with charging the gate pad capacitance \( (C_{pad}) \), and \( g_{m,ext} \) is the extrinsic trans-conductance normalized per unit width. Since the GFETs operate in the linear regime, we assume that \( C_{gs} = C_{gd} = C_g \cdot W / L / 2 \), where \( C_{gs} \) and \( C_{gd} \) are the gate-source and gate-drain capacitances, respectively, and \( C_g \) is the gate capacitance per unit area. Here, we neglect the fringing field effect. \( \tau_{pad} \) is de-embedded by extrapolating the dependence \( \tau_{tot}(1/W) \) to \( 1/W = 0 \). With the aim of de-embedding and finding \( \tau_{pad} \), we have selected and measured a set of GFETs with different widths but similar \( n_0 \approx 1.7 \times 10^{12} \ cm^{-2} \). Depending on \( V_d \), the total delay \( \tau_{tot} \) can change up to 10 ns in the studied range of \( W \). Subtracting the measured and de-embedded delay times allows us to find \( \tau_{pad} \). We assume that \( \tau_{pad} \) does not depend on the graphene quality and use it for GFETs with different \( n_0 \) values in the subsequent analysis. Knowing \( C, R, R_c, \) and \( \tau_{pad} \), the intrinsic transit delay \( \tau_{int} \) is then calculated using Eq. (1). Finally, the intrinsic transit time is used to calculate the intrinsic transit frequency

\[
\tau_{tot} = \frac{1}{2 \pi f_{T,ext}} = \tau_{int} + \tau_{ext} + \tau_{pad}
\]

\[
= \tau_{int} \left( 1 + \frac{R_c}{R - R_c} \right) + \frac{C_g \cdot W \cdot L}{2} + \frac{C_{pad}}{g_{m,ext}} \frac{1}{W},
\]

where \( f_{T,ext} \) is the transit frequency calculated from the measured S-parameters, \( \tau_{int} \) is the transit delay, \( \tau_{ext} \) is the delay time required to charge the parasitic parts of the active device region, \( \tau_{pad} \) is the delay time associated with charging the gate pad capacitance \( (C_{pad}) \), and \( g_{m,ext} \) is the extrinsic trans-conductance normalized per unit width. Since the GFETs operate in the linear regime, we assume that \( C_{gs} = C_{gd} = C_g \cdot W / L / 2 \), where \( C_{gs} \) and \( C_{gd} \) are the gate-source and gate-drain capacitances, respectively, and \( C_g \) is the gate capacitance per unit area. Here, we neglect the fringing field effect. \( \tau_{pad} \) is de-embedded by extrapolating the dependence \( \tau_{tot}(1/W) \) to \( 1/W = 0 \). With the aim of de-embedding and finding \( \tau_{pad} \), we have selected and measured a set of GFETs with different \( n_0 \) values in the subsequent analysis. Knowing \( C, R, R_c, \) and \( \tau_{pad} \), the intrinsic transit delay \( \tau_{int} \) is then calculated using Eq. (1). Finally, the intrinsic transit time is used to calculate the intrinsic transit frequency

\[
f_{T, int} = \frac{1}{2 \pi \tau_{int}}.
\]

Figure 2(a) shows the extrinsic transit frequency \( (f_{T,ext}) \) vs the drain voltage \( (V_d) \) and the intrinsic transit frequency \( (f_{T, int}) \) vs the intrinsic electric field in the channel

\[
E_{int} = -\frac{V_d}{L} \left( 1 - \frac{R_c}{R} \right)
\]

for devices with \( n_0 = (1.7, 1.9, 2.8) \times 10^{12} \ cm^{-2} \) (circles, squares, and diamonds). The extrinsic delay and the pad delay are responsible for the reduced \( f_{T, ext} \) compared to \( f_{T, int} \). Additionally, a larger \( n_0 \) seems to decrease the transit frequency.

Under the condition of \( V_{d, int} < V_{d, sat} = |V_g - V_{Dir}| + en/C \), where \( V_{d, int} = E_{int} \times L \) and \( n \) is the charge carrier concentration, we assume that the current regime is unipolar and that the velocity of the charge carriers and the field-dependent mobility are calculated as

\[
v = \frac{L}{\tau_{int}} \quad \text{and} \quad \mu_T = \frac{L}{\tau_{int} E_{int}}.
\]

The velocity of the charge carriers, which is calculated using Eq. (4), is presented in Fig. 2(b) for the device with \( n_0 = 1.7 \times 10^{12} \ cm^{-2} \). It can be seen that the velocity saturates for the fields above \( E_{int} = 1–1.5 \ V/\mu m \), which corresponds well to the results reported in Ref. 12. To evaluate the saturation velocity \( (v_{sat}) \), we fitted the carrier velocity calculated from the transit delay using Eq. (4) with an analytical expression of the field-dependent carrier velocity in the range \( E_{int} = 0–1.3 \ V/\mu m \) to avoid the effect of self-heating.
We assume that an effective saturation velocity ($v_{sat}^{eff}$) defined by several different OP mechanisms and Matthiessen's rule$^{29}$ in terms of velocity can be applied as

$$v_{sat}^{eff} = \frac{1}{\varepsilon_0} \frac{1}{\varepsilon_{SiO2}} \frac{1}{\varepsilon_{Al2O3}} \frac{1}{\varepsilon_{SiO2}} \frac{1}{\varepsilon_{Al2O3}} \frac{1}{\varepsilon_{SiO2}} \frac{1}{\varepsilon_{Al2O3}}$$

where $h\omega_{OP}$ is the OP energy and $N_{OP} = 1/\exp(h\omega_{OP}/k_B T) - 1$ is the phonon occupation. Since the channel is unipolar, the charge carrier concentration is calculated as

$$n = \frac{L}{\omega} \frac{1}{\varepsilon_0} \frac{1}{\varepsilon_{SiO2}} \frac{1}{\varepsilon_{Al2O3}}$$

We assume that an effective saturation velocity ($v_{sat}^{eff}$) defined by several different OP mechanisms and Matthiessen's rule$^{29}$ in terms of velocity can be applied as

$$v_{sat}^{eff} = \frac{1}{\varepsilon_0} \frac{1}{\varepsilon_{SiO2}} \frac{1}{\varepsilon_{Al2O3}} \frac{1}{\varepsilon_{SiO2}} \frac{1}{\varepsilon_{Al2O3}} \frac{1}{\varepsilon_{SiO2}} \frac{1}{\varepsilon_{Al2O3}}$$

FIG. 2. (a) Intrinsic transit frequency vs electric field in the channel for devices with $n_0 = (1.7, 1.9, 2.8) \times 10^{12}$ cm$^{-2}$ (circles, squares, and diamonds) at $V_g = -2$ V. The extrinsic transit frequency vs drain voltage for the device with $n_0 = 1.7 \times 10^{12}$ cm$^{-2}$ is indicated in the same graph by open circles. Dashed lines are polynomial fitting curves and serve as a guide to the eye. (b) The carrier velocity for the device with $n_0 = 1.7 \times 10^{12}$ cm$^{-2}$ was calculated using Eq. (4) and fitted by the empirical expression of Eq. (5) (solid line) using $\gamma = 3$, $\mu_0 = 1920$ cm$^2$/V s, and $v_{sat} = 1.4 \times 10^7$ cm/s vs the electric field in the channel. The effective saturation velocities calculated using Eq. (8) for graphene with Al$_2$O$_3$ OPs (dotted), graphene with SiO$_2$ OPs (dashed), and graphene with SiO$_2$ and Al$_2$O$_3$ OPs are also shown (dashed-dotted).
the channel is determined by the applied gate voltage and drain voltage. Comparing the charge carrier concentration for different devices at $|V_G - V_{Dir}| = 4.7$ V, far away from the Dirac point to avoid the influence of puddles, and $E_{int} = 1.5$ V/μm indicates that the decrease in $v_{sat}$ with $n_0$ can possibly be explained by the emission of electrons from traps (impurities) at high fields. Larger $n_0$ values correlate with a higher trap concentration and lead to additional charge carriers [Fig. 3(b)], which, according to Eq. (6), decreases the saturation velocity.

In conclusion, we presented a method for the analysis of the charge carrier velocity in the transistor channel and demonstrated its application using the example of top-gated CVD GFETs with different impurity concentrations. In general, the proposed method can be applied for field-effect transistors based on materials other than graphene, including transition metal dichalcogenides, such as black phosphorus, and common semiconductors. However, in these cases, the distribution of the electric field and, hence, of the charge carrier concentration and velocity along the channel should be taken into account.

In this work, the GFET with the lowest residual carrier concentration ($n_0$), i.e., the lowest impurity level ($n_{imp}$), of $n_0 = 1.7 \times 10^{12}$ cm$^{-2}$ affords a saturation velocity $v_{sat} = 1.4 \times 10^7$ cm/s and an intrinsic transit frequency $f_{t,intr} = 22$ GHz at a gate length of 1 μm. Analysis using a model based on optical phonon scattering at the two interfaces in the vicinity of graphene indicates that at this impurity concentration, the effective $v_{sat}^{eff}$ is limited mainly by the SiO$_2$ and graphene OPs. However, the impurity concentration and the accompanying emission of charge carriers at high fields are too high to allow saturation of the drain current to be achieved. Employing technological processes that result in a reduction in the impurity concentration and hence a reduction in the emission of charge carriers at high fields is a possible way to achieve drain current saturation via velocity saturation and thus obtain higher power gain of the GFETs. In addition, replacing the SiO$_2$ substrate and Al$_2$O$_3$ top dielectric with materials with higher OP energies, e.g., sandwiching graphene between hexagonal boron nitride, allows us to increase the saturation velocity up to $3 \times 10^7$ cm/s or $5 \times 10^7$ cm/s and the intrinsic transit frequency up to 48 GHz or 80 GHz at a gate length of 1 μm.

See supplementary material for a detailed description and discussion of device fabrication and characterization.

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