SUBSTRATE NOISE COUPLING IN MIXED-SIGNAL INTEGRATED CIRCUITS

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Substrate Noise Coupling in Mixed-Signal Integrated Circuits

Compact Modeling and Grounding Strategies

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CHALMERS

Department of Microtechnology and Nanoscience
Physical Electronics Laboratory
CHALMERS UNIVERSITY OF TECHNOLOGY
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Cover: Exact and modeled spreading resistance between a circular contact and a groundplane (Fig. 6 in Paper H).

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Abstract

Integration of digital and analog circuits on the same chip is the result of the microelectronic industry's strive for low-cost, small, hand-held products. However, these mixed-signal circuits can experience interference problems; digital circuits inject noise into the substrate which is transmitted throughout the chip and received by sensitive analog circuits. This substrate noise can therefore degrade the performance of the chip.

When performing noise coupling analysis, accurate substrate models are needed. Previous compact models were either based on two dimensional simulations, which is not sufficient since the substrate problem is inherently three dimensional, or required extraction of empirical parameters, which makes the models less predictable.

This thesis presents accurate compact substrate models which can predict the noise coupling of integrated circuits. A physics-based modeling approach has been employed to yield scalable and predictive three dimensional models. Such models for uniformly doped substrates have been considered in detail since most models presented in the research literature are for epitaxial substrate types. Furthermore, general models for multi-layer substrates and arbitrary aggressor and victim geometries are presented as well.

The substrate models have been utilized for investigating the efficiency of several substrate biasing methods, such as guard bands, guard rings, and distributed ground contacts. It was concluded that distributed grounding was the most effective. The performance of an active decoupling circuit has also been studied applying our substrate models. It was shown that dc grounding is equally good as active decoupling, for all reasonable values of the substrate resistivity.

Keywords: Mixed-signal integrated circuits, substrate noise coupling modeling, surface potential, substrate resistance, z-parameter, active noise reduction, grounding resistance, elliptic integrals.

List of Appended Papers

This thesis is based on the work contained in the following appended papers, listed in chronological order:

A. Substrate Resistance Modeling for Noise Coupling Analysis

Simon Kristiansson, Shiva P. Kagganti, Tony Ewert, Fredrik Ingvarson, Jörgen Olsson, and Kjell O. Jeppson
Presented at the IEEE International Conference on Microelectronic Test Structures, 2003.

B. Resistance Modeling in 1D, 2D, and 3D for Substrate Networks

Shiva P. Kagganti, Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson
Physica Scripta, vol. T114, pp. 217–222, 2004.

C. A Comparison of the Exact and an Approximate Solution for the Resistance Between Two Coplanar Circular Discs

Simon Kristiansson, Shiva P. Kagganti, Fredrik Ingvarson, and Kjell O. Jeppson
Solid-State Electronics, vol. 49, no. 2, pp. 275–277, 2005.

D. A Surface Potential Model for Predicting Substrate Noise Coupling in Integrated Circuits

Simon Kristiansson, Fredrik Ingvarson, Shiva P. Kagganti, Nebojša Simić, Marinel Zgrda, and Kjell O. Jeppson
IEEE Journal of Solid-State Circuits, vol. 40, No. 9, pp. 1797–1803, Sept. 2005.

E. Modeling of Rectangular Contacts for Noise Coupling Analysis in Homogeneous Substrates

Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson
Presented at the 23rd Norchip Conference, 2005.

F. Properties and Modeling of Ground Structures for Reducing Substrate Noise Coupling in ICs

Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson
Presented at the IEEE International Symposium on Circuits and Systems, 2006.

G. Evaluation of Using Active Circuitry for Substrate Noise Suppression

Rashid Farivar, Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson
Presented at the ACM Great Lakes Symposium on VLSI, 2007.

H. Compact Spreading Resistance Model for Rectangular Contacts on Uniform and Epitaxial Substrates

Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson
IEEE Transactions on Electron Devices, vol. 54, No. 9, pp. 2531–2536, Sept. 2007.

Contents

Acknowledgement

It is now four weeks until I will defend my thesis, and it is due time to finish writing. What better way to do this, than to acknowledge people that have helped me on my way.

First, I want to warmly thank my supervisor Professor Kjell O. Jeppson for accepting me as a Ph.D-student, guiding and supporting my work, and for improving my writing.

My second supervisor Dr. Fredrik Ingvarson deserves many thanks for fruitful discussions and clever insights, for implementing our substrate models in Mathematica, for always being available for proof-reading papers in the last shivering minutes before deadlines (including this thesis), and for providing nice company during coffee-breaks.

My coworker Shiva P. Kagganti is recognized for his contributions, ranging from designing test circuits, performing measurements, and initiating and writing Paper B.

Tony Ewert and Jörgen Olsson from the Ångström Laboratory, Uppsala University are acknowledged for performing the three dimensional device simulations in Paper A. Our master thesis students, Nebojša Simić and Marinel Zgrda, are acknowledged for the nice work of implementing our substrate models in Matlab, and for investigating the Cadence tool SubstrateStorm. Our project student Rashid Farivar is acknowledged for the exhaustive work of running ADS simulations of the active decoupling method in Paper G.

All my colleagues affiliated to the coffee-room on the fifth floor, building B, at MC2, are acknowledged for contributing to a nice working atmosphere. This work was funded by Stiftelsen för Strategisk Forskning and by Vetenskapsrådet.

Slutligen vill jag ge tusen tack till min familj, speciellt till min fru Anna för stöd och tålamod under min tid som doktorand, och mina barn Jonatan och Filip för att de påminner mig om att livet inte bara består av arbete.

Simon Kristiansson Göteborg, 2007-09-14

1
Introduction

This thesis deals with substrate noise coupling in integrated circuits (ICs). More specifically, modeling the transmission of interference through the silicon substrate between digital and analog circuits in mixed-signal ICs. The presented substrate models are applied to the problem how to efficiently bias the substrate. Also, a proposed method of using active circuits for decreasing the transmission of noise through the substrate is briefly discussed.

This chapter begins with explaining the broader scope into which the work belongs and identifying the thesis topic in Sections 1.1 and 1.2. Then the injection, transmission, and reception of substrate noise is discussed in Section 1.3. The chapter ends with a brief outline, and a clarification of the research contributions of the thesis in Section 1.4.

1.1 Mixed-Signal Integrated Circuits

The trend in microelectronics ever since Kilby and Noyce invented the integrated circuit in 1958,[1] has been to continually make the integrated devices smaller and smaller. With this evolution the complexity and operating frequency of the microchips have steadily increased. This is called down-scaling and has made it possible to integrate many different types of circuits on the same silicon substrate.

The miniaturization has even made it possible to create complete systems on the same silicon chip. These integrated circuits are popularly called systems-on-chips (SoCs), and can include e.g. digital, analog, and radio frequency circuits on the same chip. Circuits with both continuous analog signals and discrete digital signals are called mixed-signal ICs, and these are common in consumer products such

[1] Kilby gives his recollection of the early days of the IC in [1] and in his Nobel lecture [2] (Kilby received the Nobel Prize for the invention of the IC in 2000). A thorough account on the history of the microchip is also given in [3].

as cellular telephones, personal digital assistants, and other hand-held devices. Typically mixed-signal circuits include analog circuits to communicate with the outer analog world, and digital circuits to process signals. More specifically, circuits such as low noise amplifiers and analog-to-digital and digital-to-analog converters are common.

The main driving force behind the integration of digital and analog circuits is cost; it is cheaper to manufacture a single-chip solution than a multi-chip solution. But this is not the only benefit of integration; the power dissipation and the size of the system are reduced in a one-chip solution, and the circuits can generally operate faster when they are on the same chip [4, Ch. 1].

For consumer products the mixed-signal content is increasing. As stated in the 2005 edition of the International Roadmap for Semiconductors (ITRS) [5]:

> Radio frequency and analog/mixed-signal (RF and AMS) technologies now represent essential and critical technologies for the success of many semiconductor products. Such technologies serve the rapidly growing wireless communications market.

Thus, the co-integration of analog and digital circuits is likely to become even more common in the future. However, it should be mentioned that there is the option to integrate different circuits not on the same chip, but in the same package. Such solutions are called system-in-a-package (SIP), and has its advantages over SOCs in certain situations. Early in the product development the decision whether to opt for a system-on-chip or a system-in-package solution has to be made [6]. This decision is ultimately based on a tradeoff between performance and cost. This is not a simple matter to settle, and there have been papers published on how to make such decisions early in the design phase [7]. Such questions will however not be treated here. This thesis is restricted to problems related to placing analog and digital circuits on the same silicon chip.

1.2 Substrate Noise Coupling in Mixed-Signal ICs

Unfortunately, putting both digital and analog circuits on the same chip can be problematic. The digital circuits can disturb the sensitive analog circuits in several ways. However, the interference of analog circuits is mainly caused by switching of digital circuits on the chip

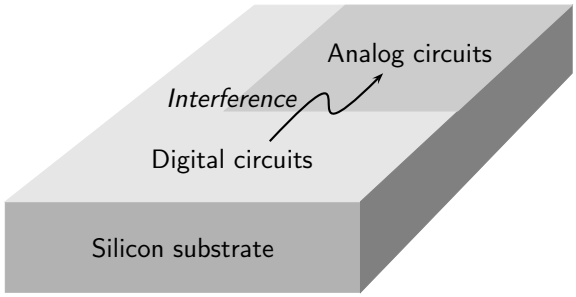


Figure 1.1 Schematic top-view of a mixed-signal IC. The figure illustrates parasitic coupling from the digital to the analog circuits.

(creating what is called simultaneous switching noise) [8]. The coupling problem is illustrated in Fig. 1.1.

Basically, the parasitic interactions between circuits on chip can be divided in two types; thermal and electrical. Thermal coupling can occur when the chip substrate heats up due to the operation of for example power amplifiers, and this elevated temperature can degrade the performance of other devices on the chip [9, 10][2]. The electrical coupling can be resistive, capacitive, or inductive by nature. These interaction mechanisms are all present in a chip, but some can be more important than others depending on the circuits on the chip.

The disturbances can also be discussed in relation to which part of the mixed-signal circuit they originate in. There can be disturbances related to the chip package, which can be of both capacitive and inductive nature. Switching of the digital circuits will cause inductive and capacitive coupling between the interconnects on chip (commonly called crosstalk, see [11] and [12, Ch. 1]). The switching of the digital circuits also creates disturbances on the power and ground networks of the chip, and this can couple to the analog parts. These noise coupling mechanisms have all attracted much attention in the literature.

Another important electrical coupling in mixed-signal circuits, the topic of this thesis, occurs through the common chip substrate [8]. Since this interaction is unwanted, it is called substrate coupled noise. This "noise" is not random in nature, and should not be confused with intrinsic device noise, such as thermal noise. In that sense, it would be more appropriately called something like "substrate coupled interference". The terminology is however settled now. A definition of substrate noise suitable for us, is *any unwanted variation of the substrate potential over time.* The noise coupled through the substrate can be orders of magnitude larger than the intrinsic device noise [13],

[2]Thermal coupling will not be addressed further in this thesis, therefore all coupling discussed will be electrical.

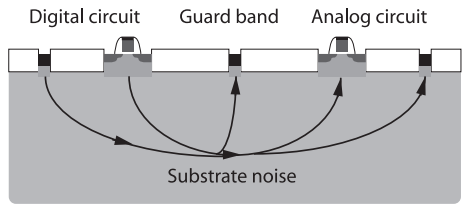


Figure 1.2 Cross-sectional view of a mixed-signal IC. The noise couples from the digital circuit to the analog circuit through the common substrate.

and is therefore a major concern in mixed analog-digital circuits. See Fig. 1.2 for an illustration of substrate noise coupling.

Noise coupling can occur between circuit blocks in purely analog or digital circuits, but it is especially troublesome in mixed-signal circuits. The ITRS concisely summarizes the challenges [5]:

> Signal isolation, especially between the digital and analog regions of the chip, is a particular challenge for scaled technologies and for increased integration complexity. Noise coupling may occur through the power supply, ground, and shared substrate. The difficulty of integrating analog and high-performance digital functions on a chip increases with scaling in both device geometry and supply voltage. Signal isolation is critical for success in co-integrating high performance analog circuits and highly complex digital signal processing (DSP) functions on the same die or substrate. Such co-integration is required in many modern communication systems to reduce size, power, and cost.

There are two sides to the noise coupling problem. Firstly, the mechanisms behind the creation, transmission, and reception of substrate noise must be well understood. This knowledge can then be utilized for designing more robust mixed-signal ICs, in which the noise received by sensitive circuit blocks has been reduced. Secondly, noise coupling models which can be implemented in a circuit simulator such as SPICE (Simulation Program with Integrated Circuit Emphasis) must be developed. When designing a mixed-signal IC, circuit simulations can then be performed to see if the noise coupling is a problem or not. When the simulations show that the chip functions as required, the IC can be fabricated. The use of noise coupling models will then hopefully increase the chances for first-time success, avoid a costly trial-and-error approach, and reduce the need for several test runs.

In the next section, the injection, transmission, and reception mechanisms of substrate noise will be outlined, together with a short history of the substrate noise coupling field. This will serve as a back-

ground for the main topic of the thesis—modeling the substrate for noise coupling analysis—as presented in Chapters 2 and 3, and the appended papers.

1.3 A Closer Look at Substrate Noise Coupling

Substrate noise was discussed in early works by Olmstead and Vulih [14], and Warren and Jungo [15] in the late 1980s. Substrate noise coupling in memory circuits was briefly discussed by Yuan and Liou in 1990 [16]. After this the number of publications in the substrate noise field started to soar. The substrate noise coupling field is now very active, with a large number of papers published each year, it has also been included in textbooks, e.g. [17, Ch. 1] and [18, Ch. 18].

The substrate noise coupling problem is complex since it involves such a large number of circuit elements coupled to each other through the silicon substrate. Conceptually, however, it is rather simple and can be divided into three parts: noise injection, noise transmission through the substrate, and finally noise reception, see Fig. 1.3. Many different devices can inject noise into the substrate, for example transistors and substrate contacts (used for biasing the substrate so that the transistors have a well defined potential under the channel region). Transistors can inject noise into the substrate through impact ionization due to high-energy charge carriers near the drain. This was identified early as a contributor to substrate currents [19, 20]. Transistors can also inject noise through transistor-to-substrate capacitances. The substrate contacts can also inject noise into the substrate. This occurs when the digital circuits switch and draws current through the power supplies. Part of this current can be injected into the substrate [12, Ch. 2].

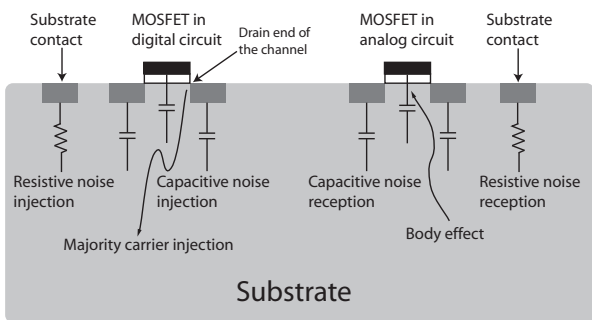


Figure 1.3 Cross-sectional view of the substrate illustrating the different noise injection and reception mechanisms.

The devices in the analog circuits can receive substrate noise in several ways. If the substrate potential varies under the transistors, these will be affected through the body-effect (the threshold voltage of the transistors increases with the voltage between the source and the substrate [18, Ch. 2]) and direct capacitive coupling. The substrate contacts in the analog circuits can also collect noise and couple it to the analog devices.

The injection and reception of substrate noise by the transistors on the chip are captured in the transistor models through the substrate node. But, for the injection of noise by different substrate contact shapes, and the transmission of noise through the substrate, models have to be developed in order to predict how much the digital circuits affect the analog circuits. This is the main objective of this thesis.

The amount of substrate noise created by digital circuits is very much dependent on the interconnections on the chip, and the packaging of the chip. This thesis will however not treat these matters, and will concentrate on the transmission of noise through the substrate, and on how the substrate can be biased to reduce the noise transmitted. For a detailed account on the parasitics of packaging of ICs, see [21]. For a review on packaging of ICs and its impact on substrate noise, see [22].

1.4 Outline and Contributions of the Thesis

The thesis can be read at four different levels; these are now described. The Abstract, Chapter 1, and Chapter 4, compose the first level. These give a good picture of the subject area, the research contributions of the thesis, and the conclusions derived from this research. The second level requires in addition reading Chapters 2 and 3. In these, more background is given to the chosen thesis topics. More detail is also given regarding the contributions of the thesis in these areas, including the main model equations and results. The third level adds reading the appended papers. Finally, the fourth, and most detailed reading level consists of reading the whole thesis together with the appendix.

The content and contributions of the thesis is briefly:

Chapter 2 introduce techniques for modeling the substrate in noise coupling analysis. The first section provides a background on common substrate modeling techniques. This is done in order to explain why

our work is needed and where it fits in the big picture. The other sections in this chapter summarize our modeling work as presented in Papers A-E and H. First, our surface potential based substrate noise coupling model is presented. Then it is discussed how the surface potential on the chip can be calculated by superposition. This chapter also discuss the resistance between two surface contacts and problems in representing the substrate by a network of lumped resistances. The chapter ends with presenting a model for the interaction of digital circuit blocks with the substrate.

Chapter 3 begins with giving a background on different methods presented in the literature for reducing substrate coupled noise. The next section present our work on substrate biasing. We also discuss modeling of the grounding resistance. Finally, a proposed method of using active circuits to reduce the substrate noise coupling is discussed. This work is presented in Paper G where we use an accurate substrate model to show that the active noise reduction method is not necessarily better than dc grounding.

Chapter 4 summarize and discuss the results of the thesis. Suggestions for future work are also presented.

Appendix The appendix collects the more detailed mathematical modeling, in order not to disrupt the flow of the main text.

Paper A presents our first surface potential based substrate model. It shows how the substrate coupling can be modeled for a specific case. The model matches measured results well, and it is also shown that the model can be directly implemented in a circuit simulator. Problems in representing the substrate as a resistor network are also discussed.

Paper B discusses the resistance between two surface contacts in detail. The resistance dependence on geometry is investigated and it is shown that both the qualitative and the quantitative behavior of the resistance differ significantly in one, two, and three dimensions. This is not surprising, but in many substrate noise coupling publications two dimensional device simulations are utilized for predicting noise coupling and for deriving resistance models. Paper B clearly indicates that two dimensional models can be very inaccurate compared with three dimensional models.

Paper C Our substrate noise coupling model is based on superposition of potentials. It is not obvious on before-hand that this superposition is accurate enough. This paper compares the superposition model with the exact solution for the interaction between two coplanar circular discs. It is shown that the superposition model is very accurate thus giving theoretical support for our superposition model.

Paper D presents our substrate noise coupling model based on superposition of surface potentials. The model can handle an arbitrary number of contacts. The contacts can have any shape and the substrate can be non-uniformly doped.

Paper E presents a compact analytical surface potential model for rectangular contacts on uniform substrates. The model is based on approximating rectangular contacts as elliptical contacts.

Paper F investigates how different configurations of substrate contacts affect the substrate noise coupling. It also introduces compact models for grounding resistances.

Paper G investigates a proposed method of using active circuits to reduce substrate noise coupling. By using a more accurate substrate model, it is shown that the efficiency of the proposed active noise reduction method is not more efficient than dc grounding.

Paper H presents a compact spreading resistance model for finite thickness uniform substrates with a grounded backplane. This model can also be applied to model the spreading resistance on epitaxial substrates.

2
Substrate Modeling

The main topic of this thesis, modeling the substrate for noise coupling analysis, is treated in this chapter, and in the appended Papers A-E, and H. The first section of this chapter provides a short overview of three different substrate modeling approaches: the finite difference, the boundary element, and the macro-model methods. Section 2.2 and onwards summarizes our modeling.

2.1 Substrate Modeling Methods

When studying noise coupled through the substrate in mixed-signal integrated circuits accurate models of the substrate are needed. One way of deriving an equation modeling the electrical phenomena in the substrate, is to start with Ampère's law in differential form [23, p. 246]

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}. \tag{2.1}$$

Here $\mathbf{H}$, $\mathbf{J}$, and $\mathbf{D}$, are the magnetic field, the current density, and the displacement field in the substrate, respectively. Taking the divergence of Ampère's law and applying the vector identity $\nabla \cdot (\nabla \times \mathbf{A}) \equiv 0$ ($\mathbf{A}$ being a vector field), results in [10]

$$0 = \nabla \cdot (\sigma \mathbf{E}) + \frac{\partial \nabla \cdot (\epsilon \mathbf{E})}{\partial t}, \tag{2.2}$$

where the constitutive relations $\mathbf{J} = \sigma \mathbf{E}$ (the point form of Ohm's law) and $\mathbf{D} = \epsilon \mathbf{E}$ have been used. In these relations, σ and ϵ are the conductivity and permittivity of the substrate, respectively, and $\mathbf{E}$ is the electric field. Equation (2.2) is actually the continuity equation for the charges in the substrate, which in the sinusoidal steady-state can be written as $\nabla \cdot [(\sigma + j\omega\epsilon)\,\mathbf{E}] = 0$. Equation (2.2) represents a

conductive current $\sigma\mathbf{E}$ and a displacement current $\partial(\epsilon\mathbf{E})/\partial t$ giving the total current flowing in each small part of the substrate.

Equation (2.2) can be solved by the finite difference method (FDM). The substrate is then divided into many small cubes (other shapes are also possible), see Fig. 2.1(a), and (2.2) can be approximated as [10]

$$\sum_{j=1}^{6}\left[G_{ij}\left(V_i - V_j\right) + C_{ij}\left(\frac{\partial V_i}{\partial t} - \frac{\partial V_j}{\partial t}\right)\right] = 0, \tag{2.3}$$

where the conductivity and the permittivity are assumed to be constant in each cube. In Eq. (2.3) the conductance G_{ij} and the capacitance C_{ij} are given by the simple block expressions

$$G_{ij} = \sigma\frac{A_{ij}}{L_{ij}}$$

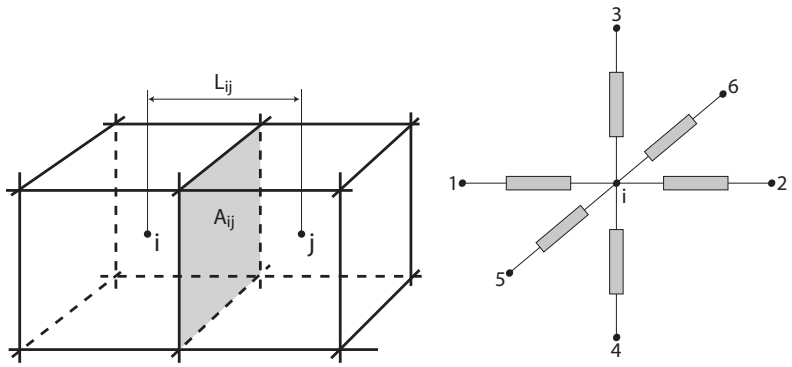
and

$$C_{ij} = \epsilon\frac{A_{ij}}{L_{ij}},$$

where A_{ij} is the surface area and L_{ij} the distance between nodes i and j, see Fig. 2.1(b). Equation (2.3) expresses that the total current flowing into cube number i is always zero (Kirchoff's current law) and that the ith node is connected to six other nodes through parallel connection of the conductance G_{ij} and the capacitance C_{ij}. This is illustrated in Fig. 2.1(b). Note that, since each cube can have different conductivities and permittivities, the substrate can have any resistivity profile, varying both laterally and depth-wise.

Thus, in the finite difference method the substrate is divided into many small pieces, and the circuit elements interacting with the substrate are connected to a very large mesh of resistances and capacitances connected in parallel. From the point of each device, the substrate can therefore be viewed as a very large, but sparse, matrix. This way of modeling the substrate have also been used in commercial substrate noise coupling tools [24].

Equations (2.2) and (2.3) have been used for modeling the substrate in many noise coupling publications, see for example [25], [26, Ch. 3], and [27, p. 39]. The idea of dividing the substrate into many small cells, and approximating the resistance and capacitance for each cell by the simple block expressions is quite natural. This has been done for example in [9] where the thermal behavior of the substrate



(a) The ith and jth substrate cells.

(b) The ith substrate node connected to neighboring substrate nodes.

Figure 2.1 Illustration of the finite difference method.

was studied, and in [28] where the electrical coupling through the substrate was studied.

The substrate is often treated as being purely resistive. This is a good approximation for low frequencies, but as the angular frequency ω of the noise becomes comparable to σ/ϵ the dielectric properties of the substrate cannot be neglected. The substrate must then be modeled as being both resistive and capacitive [29].

The finite difference method can be labeled as a microscopic approach, since the whole substrate is divided into many small cells. This is also the approach utilized in software based on finite element methods (FEM), such as Comsol Multiphysics [30] and widely used device simulators, such as MEDICI [31], Atlas [32], and ISE [33]. Since such microscopic simulations tend to be very time-consuming for large problems, they are mostly used at the device level, and not at the circuit level. For modeling substrate coupling between different circuits, these microscopic approaches are therefore not the preferred choice.

Another approach is the boundary element method (BEM). This model has been used in several published substrate noise coupling papers since the early 1990s, for example [34, 35], and [36]. The boundary element method gives the potential $V(\mathbf{r})$ at a sense-point $\mathbf{r}$ as a surface integral [37, Ch. 4],

$$V(\mathbf{r}) = \int_S J(\mathbf{r}')G(\mathbf{r},\mathbf{r}')dS, \tag{2.4}$$

where $J(\mathbf{r}')$ is the current density at the source-point $\mathbf{r}'$, and $G(\mathbf{r}, \mathbf{r}')$ is Green's function (which gives the potential at $\mathbf{r}$ due to a point charge at $\mathbf{r}'$). The problem is then solved if the current density across the surface and Green's function are known. Green's function can be calculated for certain substrate types [37, Ch. 4], but the current density has to be determined in some other way.

A common approach for solving (2.4) is to divide the surface S into many small elements [38, Ch. 6]. Note that it is only the different surface areas actually conducting current which have to be included, see Fig. 2.2. If the current density in each element is assumed to be constant, then equation (2.4) reduces to

$$z_{ij} = \frac{1}{A_j} \int_{S_j} G(\mathbf{x}_i, \mathbf{x}_j) dS_j, \tag{2.5}$$

where z_{ij} is the potential at element i due to a unit current injected into the substrate through element j, A_j is the area of element j, and $\mathbf{x}_i$ and $\mathbf{x}_j$ are two arbitrary points in elements i and j respectively.

Thus, the number of nodes in the problem is very much reduced compared to the microscopic approach. One drawback with the BEM is that the Green's function has to be calculated, which can be difficult for complicated substrate profiles. Furthermore, the accuracy of the solution also depends on how finely each contact is subdivided. Since the current density in a contact with constant potential diverges at the contact edges, a very fine mesh has to be used at the edges.

A third category of methods can be called macro-models. These methods describe how different circuit elements on the chip interact with each other through the substrate without having to solve equations describing the substrate in a microscopic way. Macro-models giving such explicit expressions have been published in the literature [38, Ch. 7], [39, 40], and [41]. These models have been derived from either numerical simulations or through fitting expressions to measured results.

One widespread macro-model, a refinement of the model in [42], was presented by Ozis et al. [41]. This model is expressed in z-para-

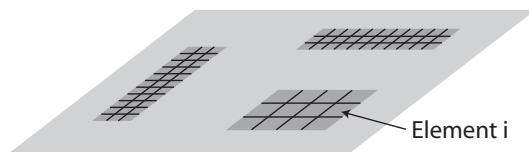


Figure 2.2 Three contacts on the substrate divided into small pieces.

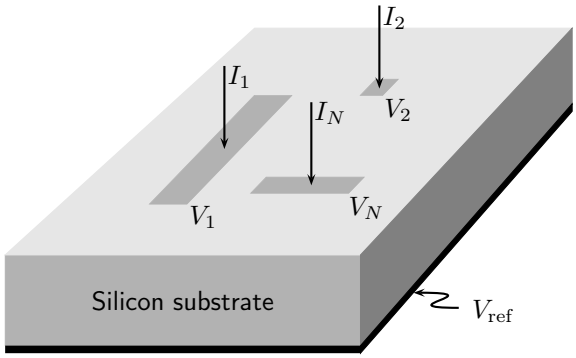


Figure 2.3 Schematic view of circuit components interacting with the substrate.

meter form, as

$$z_{ij} = \begin{cases} \dfrac{1}{k_1 A + k_2 P + k_3} & \text{when } i = j \\ \alpha_{ii} e^{-\beta d_{ij}} & \text{when } i \neq j. \end{cases} \tag{2.6}$$

In (2.6), d_{ij} is the edge-to-edge distance between contact i and contact j, A and P are the contact area and contact perimeter respectively. The model requires a number of fitting parameters, α, β, k_1, k_2, and k_3, but since $\alpha = z_{ii}$ for $d_{ij} = 0$, the number of fitting parameters is reduced to four. This model was derived for a heavily doped substrate with a grounded backplane. We discuss the model for the self-impedance (2.6) in Paper H.

The substrate noise coupling model which we present in the next section is in this context a macro-model. It models how the devices interact with each other, and the model is expressed using analytical functions.

2.2 Impedance Matrix Substrate Modeling

This and the next section summarize our substrate model as presented in Paper A (see [43] for further details). This section describes how the substrate can be treated as a multi-terminal device using a z--parameter formulation. Then, Section 2.3 shows how the substrate surface potential can be modeled, which in turn gives the details of the z-parameters of the multi-terminal substrate device.

For an IC with N devices interacting with the substrate (Fig. 2.3) the substrate is modeled as an N-port, where the port voltages and

currents are related by a linear relation as

$$\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{pmatrix} = \begin{pmatrix} z_{11} & z_{12} & \cdots & z_{1N} \\ z_{21} & z_{22} & \cdots & z_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ z_{N1} & z_{N2} & \cdots & z_{NN} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{pmatrix}. \tag{2.7}$$

The port voltages are written with respect to a reference node, which for thick substrates can be taken as the voltage deep in the substrate (henceforth also referred to as the substrate node). If the backside of the substrate is biased, this is taken as the reference node. A z-parameter description is chosen since the different matrix elements can be derived through calculating the potential at the surface of the substrate, as will be shown in the next section. If the substrate node is floating in Fig. 2.3, then the voltages can be written with respect to one of the surface contacts, for example contact N. This is further explained in [43].

The z-parameters are completely determined if the surface potential developed due to current injected into each contact can be calculated. The elements of the impedance matrix are defined as [44, p. B–4]

$$z_{ij} = \left.\frac{V_i - V_{\text{ref}}}{I_j}\right|_{I_k=0, \quad \forall k \neq j}. \tag{2.8}$$

Thus, to calculate z_{ij}, a current I_j is injected into terminal j, with all other terminals floating (except the reference node), and the floating potential V_i developed at contact i is calculated. Each diagonal element z_{ii} in (2.7) is the resistance between contact i and the substrate node. The off-diagonal element z_{ij} is the mutual resistance[1] between contacts i and j.

Fig. 2.4 shows a cross-section of an IC with two n-type MOSFETs, and three substrate contacts[2]. The resulting substrate device is thus seen to have five ports in this case. The interface between each circuit element and the corresponding substrate terminal is modeled as a flat contact[3]. We model these contacts as being equipotential and lying on the surface of the substrate. This is a necessary approximation for using the theoretical models discussed in the appendix.

[1] This is the terminology used by Sunde [45] and could perhaps also be called a transresistance.

[2] Substrate contacts are also called substrate taps. The corresponding contacts in a well are called well contacts or well taps.

[3] For the rest of the thesis, contacts and terminals are used interchangeably to mean the same thing.

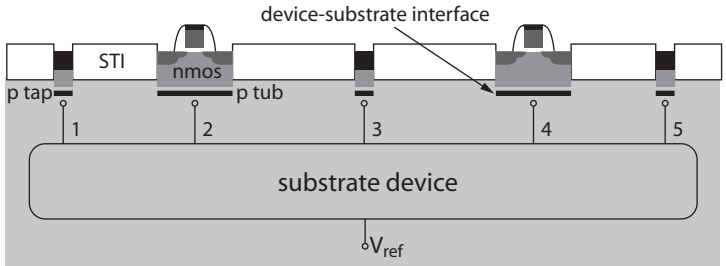


Figure 2.4 The substrate is modeled as a multi-terminal device, and the interface between the devices and the substrate is modeled as flat contacts, shown here by thick black lines.

All non-diagonal z-elements monotonically approach zero as the distances between the devices on the chip increases. This means that if all the distances between all devices on the chip can be considered as large, then only the diagonal elements in the impedance matrix are non-zero. In this case each diagonal z-element can be represented by a resistor connecting the surface contact to the substrate node. This node is for heavily doped substrates equal to the single node bulk node [8]. Thus, both the topology and the values of resistors in an equivalent network are in this case easily determined.

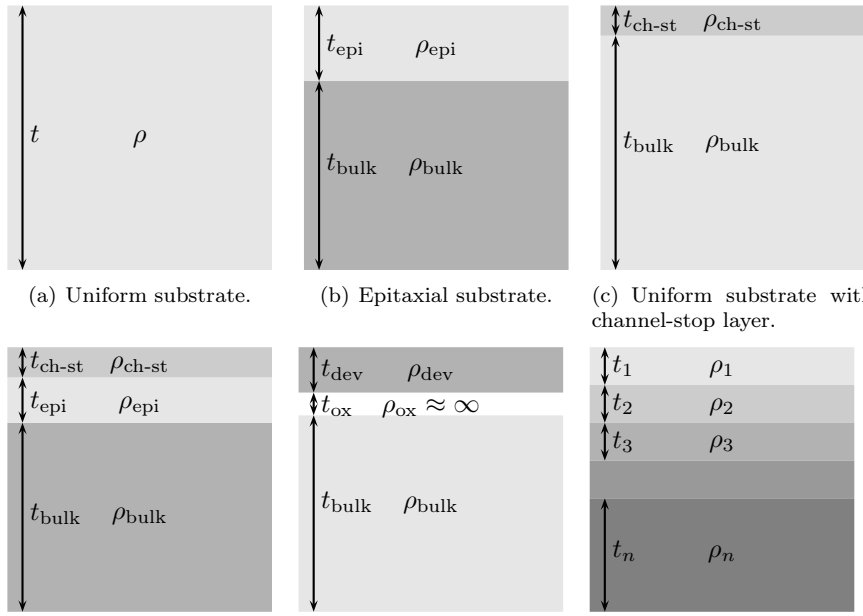
The impedance matrix depends on the substrate-doping profile and the geometry and locations of the contacts. The modeling of the matrix elements are discussed in the next section.

2.3 Surface Potential Modeling

The noise coupling problem is reduced to the problem of calculating the z_{ij}-elements of the impedance matrix. This is equivalent to the problem of calculating the surface potential due to current injected into each surface contact one at a time. Unfortunately, this problem is not trivial to solve for arbitrarily shaped contacts on non-uniformly doped substrates. Therefore, as a start, different substrate types are discussed.

The substrates used for integrated circuits are generally non-uniformly doped and the resistivity varies with depth into the substrate[4].

[4]The resistivity in the thin top layer where the devices are located of course varies in the lateral direction, but below this layer the resistivity only varies ver-



(a) Uniform substrate.

(b) Epitaxial substrate.

(c) Uniform substrate with channel-stop layer.

(d) Epitaxial substrate with channel-stop layer.

(e) SOI substrate.

(f) Multi-layer substrate.

Figure 2.5 Cross sectional views of different substrate types. Substrates (a)–(e) are naturally special cases of the substrate in (f)

In Fig. 2.5 the most common substrate doping profiles are shown. For modeling purposes the substrates are commonly assumed to consist of layers with different resistivity. The resistivity of each layer is typically between 0.001 Ωcm (for heavily doped layers) to 20 Ωcm (for lightly doped layers). The total thickness of the substrate is typically between 300 μm to 800 μm.

The two most commonly used substrates are the lightly-doped (or uniform) substrate, shown in Fig. 2.5(a), and the heavily-doped (or epitaxial) substrate, shown in Fig. 2.5(b). The uniform substrate, with a typical resistivity 10 Ωcm is often used with a thin ($\approx$ 1 μm thick low-resistivity ($\approx$ 1 Ωcm) channel-stop layer[5], see Fig. 2.5(c)). This substrate is common for radio frequency circuits. The reason is,

tically.

[5]The purpose of this layer is to raise the threshold voltage, so that parasitic transistor action is suppressed.

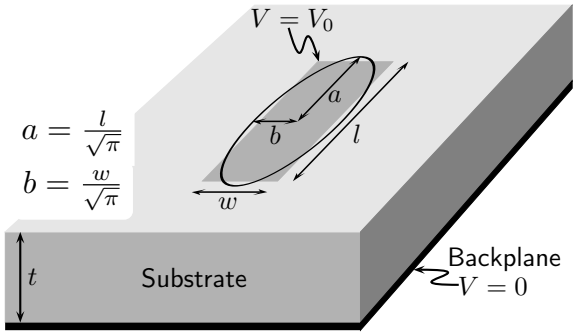


Figure 2.6 Elliptic approximation of the rectangular spreading resistance problem. The substrate is uniform with a resistivity ρ and thickness t.

among others, that the high-resistivity of the substrate provide better isolation of components.

The epitaxial substrate (typical values $\rho_{\text{epi}} = 10$ Ωcm, $t_{\text{epi}} = 10$ μm, $\rho_{\text{bulk}} = 1$ mΩcm) is commonly used in digital circuits. The reason being that the low resistivity of the bulk substrate decreases the voltage differences in the substrate, and therefore also the risk of latch-up [21, pp. 51–53].

Both the uniform and the epitaxial substrate types are used for mixed-signal ICs. The reason for choosing one or the other depends on whether the risk of latch-up in digital circuits or the risk of substrate noise, is deemed to be most critical.

The contacts interacting with the substrate can be of many different shapes. The most common, however, is the rectangular shape. Thus, a compact substrate model should at least be able to handle rectangular contacts on uniform, or epitaxial substrates. This is the topic of our modeling work presented in papers A-E and H. We will now summarize the main points in these papers.

The modeling challenges can be reduced to the problem of a rectangular contact on a uniform substrate over a ground plane, see Fig. 2.6. The first approximation is to replace the rectangular contact with an elliptical contact, with the same area and aspect-ratio. Then, for this case the impedance parameters read,

$$z_{ij} = \begin{cases} \dfrac{\rho}{2\pi\, a_i}\, \mathrm{F}\left[\arctan\left(\dfrac{k(t)\, t}{b_i}\right) \middle| 1 - \dfrac{b_i^2}{a_i^2}\right] & \text{when } i = j \\ z_{jj}\, \dfrac{2}{\pi} \arcsin\left(\dfrac{a_j}{d_{ij}}\right) e^{-f\left(\frac{t}{a_j}\right)\frac{d_{ij}-a_j}{t}} & \text{when } i \neq j, \end{cases} \tag{2.9}$$

where

$$k(t) = 1 + \frac{1}{1 + \frac{t}{b}}, \tag{2.10}$$

and

$$f\left(\frac{t}{a}\right) = \frac{\pi}{4}\left(1 + \frac{1}{1 + \frac{t}{4a}}\right). \tag{2.11}$$

The z_{ii}-part is derived from spreading resistance theory (details can be found in Paper H). In (2.9), ρ is the substrate resistivity, t is the substrate thickness, see Fig. 2.5(a), and d_{ij} is the center-to-center distance between contacts i and j. The rectangular contact, length l and width w, is approximated as an elliptic contact with semi-axes chosen as $a = l/\sqrt{\pi}$ and $b = w/\sqrt{\pi}$, respectively (without loss of generality $l \geq w$). $\mathrm{F}(\phi \,|\, m)$ is the incomplete elliptic integral of the first kind (defined in Paper H, see also [46, Ch. 17]).

The model for the self-impedance, z_{ii}, is discussed in detail in Paper H. There it is shown that the model accurately predicts the impedance of rectangular (and circular) contacts on both uniform and epitaxial substrates. This is not a trivial thing, since the model is expressed using only physical parameters, and does not require any extraction of parameters for fitting purposes.

The model for the mutual impedance in (2.9) has not been published. Therefore, this model will be discussed in more detail here. The model is composed of two functions. The exponential function is added since numerical simulations revealed that the surface potential falls exponentially for thin substrates. This is also in agreement with the model (2.6) presented by Ozis et al. [41]. For thick substrates, however, the potential should fall inversely with the distance, therefore the arcsin-function is added (see the appendix for details).

In Fig. 2.7 the normalized surface potential around a circular contact, calculated with (2.9), is shown for a few normalized substrate thicknesses[6]. For a normalized thickness of 100 the surface potential decreases as $\arcsin(a/d)$, which is characteristic for thick substrates (see Paper E). For normalized thicknesses less than 2 the surface potential is seen to decrease exponentially. Thus, (2.9) captures both the behavior of thick substrates and thin substrates in the same model.

[6]The z-parameters are obtained by dividing the substrate surface potential by the contact current.

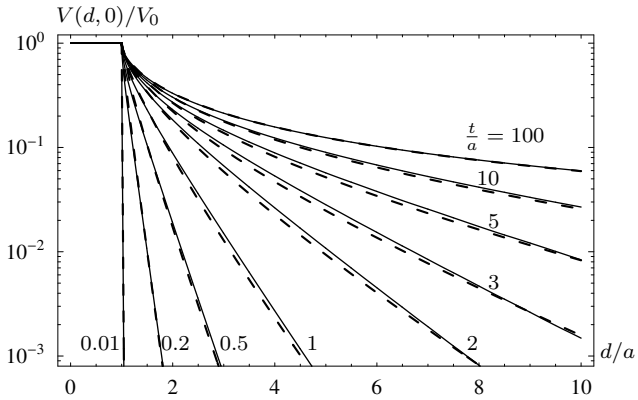


Figure 2.7 Modeled and simulated normalized surface potentials for several normalized substrate thicknesses, from $t/a = 0.01$ to $t/a = 100$. The circular contact radius is a and the backside of the uniform substrate is grounded. The dashed lines show the modeled results and the solid lines the finite element results.

This is very convenient, and is something that has not been done previously. For example, Lan et al. [47] presented two separate substrate models for uniform and epitaxial substrates.

If we compare our model, (2.9), with (2.6) we can note similarities. Both models are scalable in the width and length of the contact. Our model, however, is only expressed with physical parameters, and do not use fitting parameters. Our model also explicitly shows the dependence on substrate thickness and substrate resistivity.

The rate at which the potential falls is a function of the contact size, contrary to what is stated in [41]. It is only for two dimensional situations where the rate is independent on the contact size. Thus, the often stated rule-of-thumb that the impedance between two contacts is independent of the distance between them if the distance is four times the thickness of the epitaxial layer can be evaluated. For example, the distance needed to have the normalized surface potential decreased to one percent, can be seen to depend on the thickness of the substrate. Even for an infinitely thick substrate, the normalized surface potential will have dropped to one percent for the distance 64 times the contact radius.

As mentioned above, the impedance model (2.9) is applicable to uniform and epitaxial substrates (see Paper H). For more general situations, such as the multi-layer substrate in Fig. 2.5(f), the model

presented in Paper D can be used. This model treats circular contacts and is discussed in more detail in the appendix. The model is expressed in integral form and reads

$$z_{ij} = \begin{cases} \dfrac{\rho_1}{\pi a_j^2} \displaystyle\int_0^\infty A_1(u) \frac{\sin(a_j u)}{u^2} \, \mathrm{J}_1(a_j u) du & \text{when } i = j \\ \dfrac{\rho_1}{2\pi a_j} \displaystyle\int_0^\infty A_1(u) \frac{\sin(a_j u)}{u} \, \mathrm{J}_0(d_{ij} u) du & \text{when } i \neq j, \end{cases} \tag{2.12}$$

where the function $A_1(u)$ is defined in the appendix (Eqs. (A.36) and (A.37)). These integrals have to be solved numerically since analytical solutions do not exist. These equations were verified with numerical simulations in Paper D.

However, for the special case of a uniform semi-infinite substrate, (2.13) can solved analytically. The z_{ij}-elements are then given by

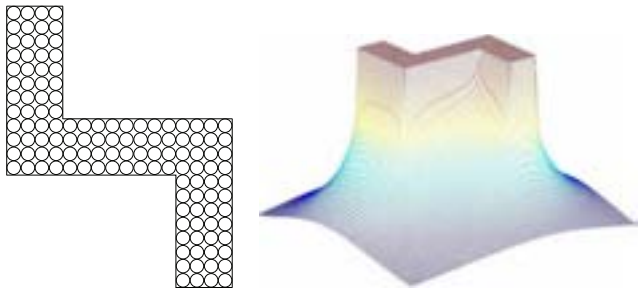
$$z_{ij} = \begin{cases} \dfrac{\rho}{4a_i} & \text{when } i = j \\ \dfrac{\rho}{2\pi a_j} \arcsin\left(\dfrac{a_j}{d_{ij}}\right) & \text{when } i \neq j, \end{cases} \tag{2.13}$$

where a_i is the radius of contact i, and d_{ij} is the distance between the centers of contacts i and j.

The impedance matrix resulting from the surface potential models will not be symmetric in general. For example, the z-matrix from (2.13) is not symmetric if the contacts are of different size. To see this, take two contacts labeled 1 and 2 as an example. Let the radius of contact 1 be a_1 and the radius of contact 2 be $a_2 \neq a_1$, then

$$\begin{aligned} z_{12} =& \frac{\rho}{2\pi a_2} \arcsin\left(\frac{a_2}{d_{12}}\right) \\ \neq& \frac{\rho}{2\pi a_1} \arcsin\left(\frac{a_1}{d_{12}}\right) = z_{21}. \end{aligned} \tag{2.14}$$

But as the distance $d_{12} \to \infty$, the matrix becomes symmetric as can be seen by Taylor series expansion of the arcsin-function. The non-symmetry of the impedance matrix contradicts the reciprocity theorem (see [48, pp. 233–236]), and is a consequence of the superposition approximation. The errors using the superposition model is, however, not that large when the substrate contacts are of comparable size, and not too close. This problem was studied in Paper C.



(a) Contact covered with many small circular discs.

(b) Surface potential resulting from superposition of all discs.

Figure 2.8 Illustration of how arbitrarily shaped contacts can be modeled.

For arbitrarily shaped contacts (2.12) cannot directly be used since it models *circular* contacts. But an arbitrarily shaped contact can be approximated by covering it with many small circular contacts, see Fig. 2.8. Then the current flowing through each small circular contact can be calculated by solving (2.7). Each small contact has the same potential in this case. Once the currents flowing through the small circular contacts are known the surface potential can be calculated. This was the method used for modeling the surface potential in Paper D (see also [43]). This approach is similar to the method used by Reitan and Higgins for calculating the capacitance of various conductors [49, 50], and to the method used for modeling the constriction resistance[7] between two electrodes in [51].

2.4 Resistance Modeling

The substrate impedance model presented in the previous sections can naturally also be used for modeling the resistance between two contacts. The resistance between two circular surface contacts, labeled i and j (with the backside of the substrate floating) can be modeled as

$$R_{ij}(d_{ij}) = z_{ii} + z_{jj} - z_{ij} - z_{ji}, \tag{2.15}$$

[7] A constriction resistance arise when two electrodes touch in a large area, but the actual current flowing between them only flows through a number of small patches.

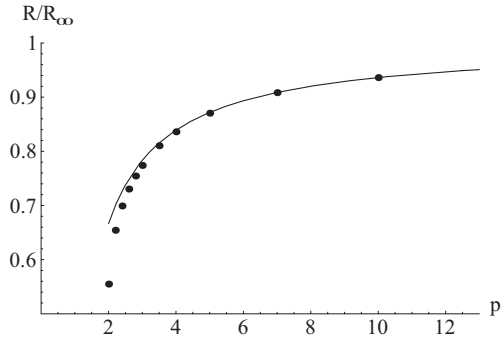


Figure 2.9 The normalized resistance between two coplanar circular contacts as a function of the normalized inter-contacts distance.

where d_{ij} is the distance between the contacts. Since $z_{ij} \to 0$ when $d_{ij} \to \infty$, the resistance saturates to the value $z_{ii} + z_{jj}$ which is denoted as $R_{ij\infty}$.

When the substrate is non-uniform the resistance between two circular contacts with equal radii a is from (2.15) and (2.12)

$$R(d) = \frac{2\rho}{\pi a} \int_0^\infty A_1(u) \frac{\sin(au)}{u} \left[\frac{\mathrm{J}_1(au)}{au} - \frac{\mathrm{J}_0(du)}{2} \right] du, \qquad (2.16)$$

where the function $A_1(u)$ captures the effects of the substrate not being uniform. This model is discussed in the appendix (see also [52]).

For a uniform substrate the resistance is, from (2.15) and (2.13), equal to

$$R(d_{ij}) = \frac{\rho}{2a} \left[1 - \frac{2}{\pi} \arcsin\left(\frac{a}{d_{ij}} \right) \right]. \qquad (2.17)$$

This is also the expression which (2.16) reduces to for uniform substrates (then $A_1(u) = 1$). The resistance (2.17) as a function of the normalized distance $p = d_{ij}/a$ is shown in Fig. 2.9, where the resistance is normalized to $R_\infty = \rho/(2a)$. The resistance (2.17) is an approximate model since it is based on superposition. This model was compared with the exact solution, presented by I. Kobayashi in 1939 [53], in Paper C. There it was shown that the error in using the approximate model is less than 1.25 percent for distances $d > 3a$. Thus, in this case superposition of potentials is accurate, and this is assumed to be so also for more general situations.

The resistance model for circular contacts on uniform substrates, (2.17), can be generalized so that the resistance between non-circular contacts on other substrates also can be modeled. To explain how,

Table 2.1 Measured parameters for the resistance between two coplanar contacts.

Contact 1	Contact 2	R_∞ (Ω)	d_0 (μm)	n ($-$)
1×1 μm^2	1×1 μm^2	4643	17.5	0.54
1×50 μm^2	1×50 μm^2	1193	58.3	1.33
1×50 μm^2	1×100 μm^2	1059	74	1.12

we make three observations of the resistance (2.17): the resistance as $d \to \infty$ is finite and equal to $R_\infty = \rho/(2a)$, when $d = 2a$ the resistance is $\frac{2}{3}R_\infty$, and finally, the slope at $d = 2a$ is equal to $R_\infty/(\sqrt{3}\pi a)$.

For modeling the resistance between two p+ substrate contacts on a non-uniform substrate, the edge-to-edge distance d_{ee} between the contacts is used, and the resistance should go to zero when $d_{ee} \to 0$. The three observations made above is required to hold with respect to d_{ee}. This is accomplished by

$$R(d_{ee}) = R_\infty \left[1 - \frac{2}{\pi} \arcsin \left(\frac{1}{1 + \left(\frac{d_{ee}}{d_0} \right)^n} \right) \right]. \tag{2.18}$$

In this expression the first two requirements are easily seen to hold. The slope of $R(d_{ee})$ at $d = d_0$ is

$$n \frac{R_\infty}{\sqrt{3}\pi d_0}. \tag{2.19}$$

Thus, the role of the parameter n is to adjust the slope of the resistance-curve.

The resistance model (2.18) was discussed in Paper A, together with measured results. It was shown that (2.18) could model the resistance between both square (1 μm $\times$ 1 μm) and rectangular (1 μm $\times$ 50 μm) contacts. The three parameters in (2.18) was extracted by fitting the expression to measured results (see Table 2.1 where the parameters for the resistance between a 1 μm $\times$ 50 μm) contact and a 1 μm $\times$ 100 μm contact is also included.

The empirical model (2.18) can model reasonably general doping profiles, not only multi-layer substrates. Figure 2.10 shows two examples. These doping profiles have been approximated as being multi--layered and the physical resistance between two circular contacts of radii $a = 0.5$ μm have been modeled using (2.16) and the equations giving $A_1(u)$ shown in the appendix. The resistances are shown by the dotted curves in the inset of Fig. 2.10. The empirical resistance

Table 2.2 The extracted resistance parameters.

	R_∞ (Ω)	d_0 (μm)	n ($-$)
Shallow profile	2766.15	14.2573	0.996561
Deep profile	12483.6	5.28552	1.16038

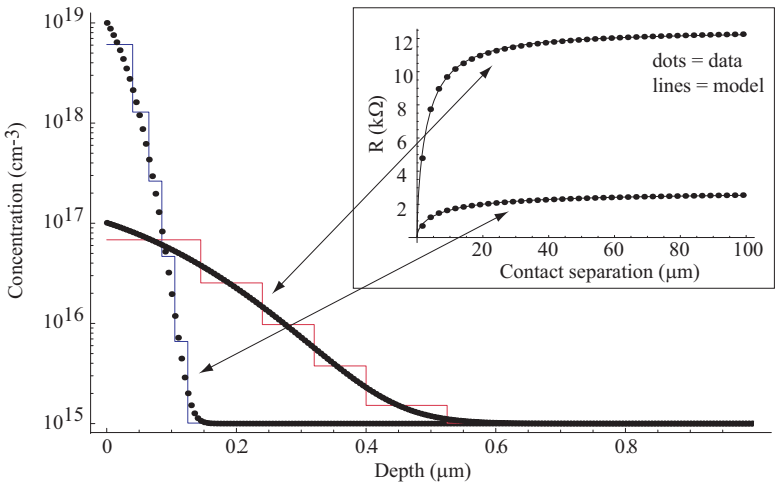


Figure 2.10 Two different doping profiles approximated by multi-layer profiles. The results using the model in the appendix for the resistance are shown by the dots in the inset. The empirical resistance model results are shown by solid lines.

model (2.18) has been fitted to the physical resistance model (2.16), and the extracted parameters are shown in Table 2.2.

The empirical resistance model (2.18) was used in Paper D (and [43]) for giving empirical z-parameter expressions for arbitrary substrates.

The resistance model (2.18) is very general. However, for small distances between irregular contacts, the distance could be hard to define properly. One solution, proposed by Lan et al. [47], is to define a geometric mean distance between the contacts. This concept has previously been used for inductance modeling, see [54, Ch. 3]. In general, however, the geometric mean distance is expressed in inte-

gral form. For rectangular contacts, for example, only approximate compact expressions are available [55, p. 42].[8]

Many papers have been published stating how the substrate noise falls with distance from the aggressor. These results, however, are often based on two-dimensional simulations, using for example Atlas [32] and MEDICI [31]. In [8] the noise was stated to fall linearly with distance from the aggressor, and in [56], the resistance between two contacts was claimed to increase at a rate somewhere between logarithmic and linearly, for uniform substrates.

We therefore set out to see how large the errors resulting from using two dimensional modeling is compared with the correct three dimensional modeling. This is the subject of Paper E, where the resistance dependence on geometry is investigated in detail. The results show that both the qualitative and the quantitative behavior of the resistances differ a great amount in two and three dimensions. This is also what we expected, and therefore substrate models based on two dimensional simulations should be analyzed carefully before utilization.

2.5 Substrate Network Modeling

This section discuss complications that appear when representing the substrate as a lumped resistor network. In the literature it is common practice to assume some reasonable substrate resistor network and then extract the resistance values from measurement or simulation data [39, 40, 41]. One must be very careful when trying to give the extracted resistances physical interpretation due to the complex interactions between *all* contacts which resistor networks do not inherently account for. We will use two examples to illustrate the difficulties.

We use the four-contact structure shown in Fig. 2.11 as the first example. The resistance between any pair of these contacts can be modeled using the resistance model (2.18). However, if more than two of the contacts are to be modeled at the same time, problems arise. The most general resistance network connecting the four contacts consists of six resistances, one resistance connected between each contact pair, see Fig. 2.11. In Paper A it was shown that all six resistances must be used to model the correct z-parameter behavior. But, two of the contacts were grounded in Paper A, and therefore the resistance

[8] The geometric mean distance between two circular contacts is equal to the distance between the centers of the contacts [54, p. 24].

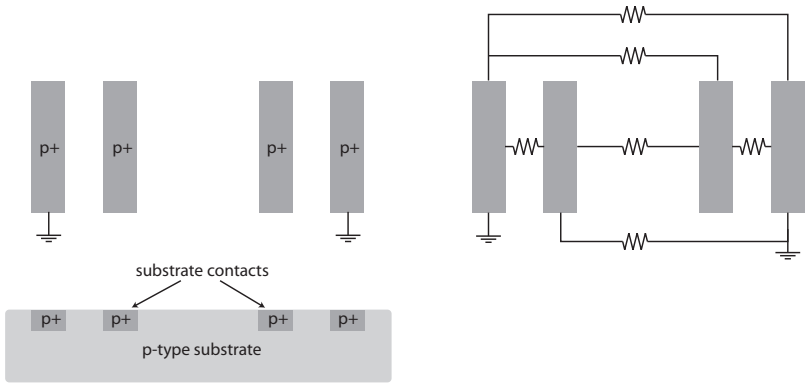


Figure 2.11 Top- and cross-sectional views of the four-contact example. The right-hand side pictures the resistor network.

between those contacts in the equivalent resistor network would not influence the circuit. Thus, for this example it is difficult to choose a *topology* of the network.

The second example is shown in Fig. 2.12. The network consists of three resistors, R_2 directly connects the two contacts and R_1 connects each contact to the equipotential backplane. If we let the backplane float, the total resistance R between the two contacts is

$$R(p) = \frac{2R_1(p)R_2(p)}{2R_1(p) + R_2(p)}, \tag{2.20}$$

where the resistance-dependence on the normalized distance $p = d/a$ is explicitly shown. The total resistance is from (2.17), and the resistance $R_1(p)$ is by superposition

$$R_1(p) = \frac{\rho}{4a}\left[1 + \frac{2}{\pi}\arcsin\left(\frac{1}{p}\right)\right]. \tag{2.21}$$

Solving for $R_2(p)$ gives

$$R_2(p) = \frac{\frac{\rho}{2a}\left[1 - \left(\frac{2}{\pi}\arcsin\left(\frac{1}{p}\right)\right)^2\right]}{\frac{4}{\pi}\arcsin\left(\frac{1}{p}\right)}. \tag{2.22}$$

It is seen that $R_2(p) \to \infty$ as $p \to \infty$. This means that $R(p) \to 2R_1(p)$ which gives the correct limiting total resistance. This example

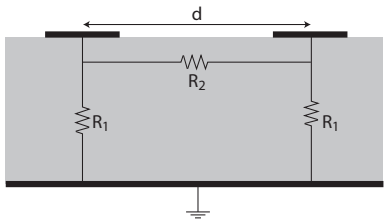


Figure 2.12 A uniform substrate modeled as a resistor network. The substrate is assumed to be very thick compared to the contact radius a, and the distance d between the contacts.

illustrates that the resistances in the network have to take into account the effect of nearby contacts. The resistances in the network are also non-physical in the sense that if we apply a voltage between say contact one and the ground-plane we measure R_1 to be $\rho/(4a)$, which is not the resistance we must use in our network. Thus, this example shows that it is difficult to model the *resistances* of the network.

2.6 Impedance Model for Digital Circuit Blocks

Recently, work have addressed substrate noise coupling at the floorplan stage of the design process to reduce the number of design iterations [57, 58, 59]. To estimate the interaction between digital and analog circuit blocks compact resistance models are commonly used. These models typically assume that noise is injected throughout the whole area of the circuit block, which rarely is the case. This section[9] presents a refined model for the interaction of circuit blocks with the substrate expressed using physical parameters such as the circuit block size, the size and number of small contacts, and the substrate resistivity.

The digital and the analog parts are divided into a number of circuit blocks. Then, in addition to constraints on silicon area and interconnect wire length, a constraint on how much substrate noise that is acceptable at sensitive circuit blocks is added. Each digital circuit block is assumed to inject noise independently of other circuit blocks, and each analog circuit block is assumed to be affected by the substrate noise independently of the other analog circuit blocks. As a measure of the amount of substrate noise, simplified compact models for the resistance, or impedance parameters, between circuits blocks have been used. This measure is then included in the cost function which is to be minimized in the floorplan algorithm.

[9]The work in this section was presented in [60].

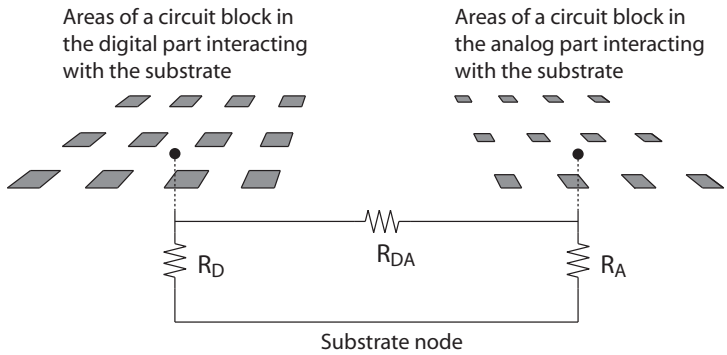


Figure 2.13 Schematic view of two regions coupled together on the substrate through their substrate contacts.

In Fig. 2.13 the substrate noise coupling scenario is schematically shown. The two regions represent a digital circuit block, on the left, and an analog circuit block, on the right, interacting with the substrate. The regions interacting with the substrate are shaded grey and represent substrate biasing p+ contacts in the two circuit blocks. This assumption is made since Badaroglu et al. [61] have shown that it is the power supplies in the digital circuits that dominate the substrate noise injection, and will increasingly dominate the noise injection as technology is scaled down.

The coupling between the circuit blocks in the two regions is commonly modeled as a Π-network as shown in Fig. 2.13 (see also for example [57]). If the lateral distance between the circuit blocks is great, the resistance, labeled R_{DA}, is very large, and the coupling between the circuit blocks is mainly conducted through the substrate node.

The substrate coupling from the j'th digital circuit block to the i'th analog victim circuit block, $\mathrm{SC_{ij}}$, is modeled by resistive division as [57]

$$\mathrm{SC_{ij}} = \frac{R_{\mathrm{Aj}}}{R_{\mathrm{Aj}} + R_{\mathrm{DiAj}}}, \tag{2.23}$$

where R_{Aj} is the resistance from the j'th analog circuit block to the substrate node, and R_{DiAj} is the resistance between the two circuit blocks i and j. The major distance dependent resistance is R_{DiAj}, for which Jeske et al. [57] used a model presented by Joardar [39]. This model was discussed in Paper A, and is a modified form of (2.17).

It is not shown in [57] how R_{Aj}, which is not as dependent on the inter-block distance, is modeled.

For epitaxial substrates, Cho et al. [59] used the compact substrate coupling model (2.6) [41, 42]. The coupling in z-parameter form is [59]

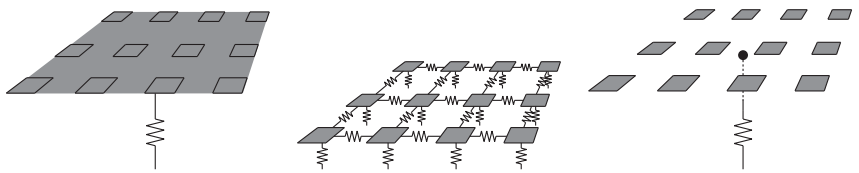
$$\mathrm{SC}_{\mathrm{ij}} = \frac{z_{\mathrm{DA}}}{z_{\mathrm{A}}}, \tag{2.24}$$

where $z_{\mathrm{DA}} I_{\mathrm{D}}$ ($z_{\mathrm{A}} I_{\mathrm{D}}$) is the potential developed at the analog (digital) circuit due to the current I_{D} injected into the substrate from the digital circuit.

Both the above models are compact and therefore simple to use. One drawback is that, when applied to model the interaction of the circuit block with the substrate, they assume that the whole area of the circuit block interacts with the substrate, see Fig. 2.14(a). This is obviously an approximation.

We assume that the substrate contacts in the two regions are evenly spread out in each domain, as shown in Fig. 2.13. The interaction with the substrate then appears to be a very complicated problem. This is why simplified models, such as that in Fig. 2.14(a), have been used [58, 59].

On the other hand, the more detailed model shown in Fig. 2.14(b) is not easy to use. The resistors in this network have to be extracted, for example by the substrate noise analysis tool in Cadence [62]. This results in a large resistor network for many contacts. It is therefore computer-intensive to simulate, see for example [63] where the digital circuit was reduced to a few *effective* inverters in order to be able to simulate the substrate coupling.



(a) Uniform injection of noise.

(b) Detailed resistor network model.

(c) Model proposed in this paper which combines the simplicity of the first model with the accuracy of the second detailed model.

Figure 2.14 Three different alternatives of modeling the interaction of a circuit block with the substrate.

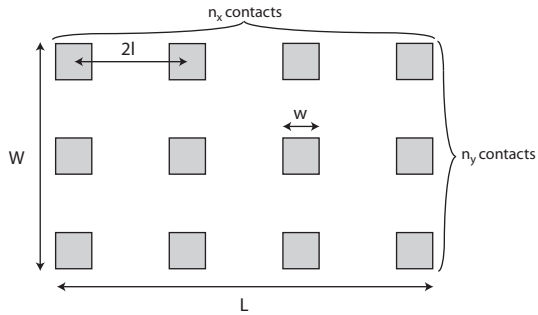


Figure 2.15 Schematic view of the distributed substrate contacts.

We propose to use a model presented by Ragnar Holm [64] for modeling the constriction resistance between two electrodes. This model is modified for our purposes in substrate noise coupling analysis. The derivation of the model is shown in the appendix.

The model reads

$$z_{ii} = \frac{\rho}{2\sqrt{\pi}\,nw} \arctan\left(\frac{\sqrt{4l^2 - w^2}}{w}\right) - \frac{\rho}{2\sqrt{\pi}} \frac{\sqrt{4l^2 - w^2}}{LW} + \frac{\rho}{2\sqrt{\pi}\,L} \mathrm{K}\left(1 - \frac{W^2}{L^2}\right). \tag{2.25}$$

This equation has been adjusted to the situation where the small contacts are square instead of circular, and the whole area where the contacts are spread out into is rectangular (instead of circular), see Fig. 2.15. In (2.25), ρ is the substrate resistivity, n is the total number of contacts ($n = n_x n_y$), w is the side-length of the square contacts, $2l$ is the inter-contact distance (center-to-center), L and W are the width and the length of the contact array, respectively. Finally, the function K is the complete elliptic integral of the first kind, see the appendix for a definition.

Equation (2.25) simplifies the modeling of digital noise injection considerably. It models how the substrate node is affected by the current injected into the substrate from a digital circuit block. But it can also be used for calculating the local effectiveness of arrays of substrate contacts in analog circuit blocks (see Section 3.2 and Paper F).

The total resistance as calculated with (2.25) is shown in Fig. 2.16. The large area which the contact array is placed into is 100×100 μm^2. The resistance of the contact array is shown as a function of the number of contacts on one side n_x (the total number of contacts

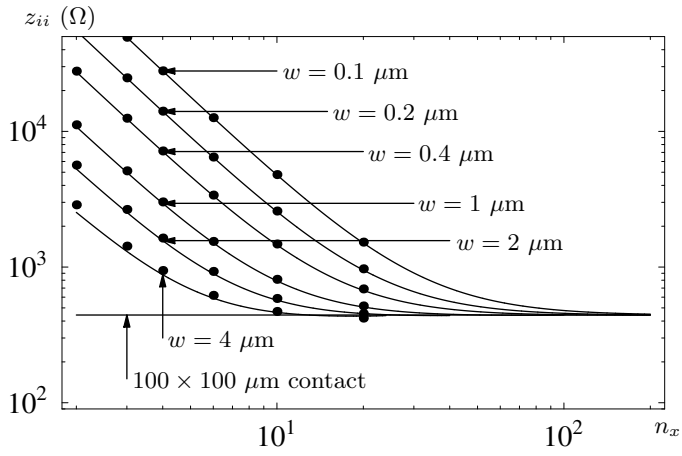


Figure 2.16 The total resistance for the array of substrate contacts calculated with (2.25) for several contact lengths. The array size is 100 μm × 100 μm and the substrate resistivity is 10 Ωcm. The results shown by filled circles are obtained with the surface potential model given in Paper D.

is $n_x \times n_x$), for several contact side lengths w. Thus the resistance is shown as a function of the contact density.

One interesting observation is that when the density of substrate contacts increases, the mutual interaction between the contacts increases. Therefore the total resistance saturates at a finite non-zero resistance. For example, quadrupling the number of substrate contacts from 10×10 to 20×20 for contacts with side length 0.4 μm, does not result in a fourth of the total resistance, but instead the total resistance is roughly reduced to one half.

This implies that the efficiency of digital circuits to inject noise into the substrate reduces for closely spaced injectors. Thus, from a substrate noise coupling perspective, the digital aggressors should be as closely packed as possible to decrease their power to inject noise into the substrate. On the other hand, on the analog circuit side, the ground biasing substrate contacts should be spread out as much as possible in order to decrease the grounding resistance (see Paper F).

In Fig. 2.17 the resistance of the contact array is shown for several contact arrays as a function of the inter-contact distance $2l$. As the inter-contact distance increases, the resistance of the contact array decreases since the current flows from each contact is deflected less from each other. Finally, the resistance saturates to the resistance from n parallel independent contacts. For the largest contact array, 50×50 contacts, the inter-contact distance has to be larger than a couple of hundred micrometers before the contacts act independently.

The resistance model for the digital circuit block can also be applied to model the ground array in, for example, the analog circuits.

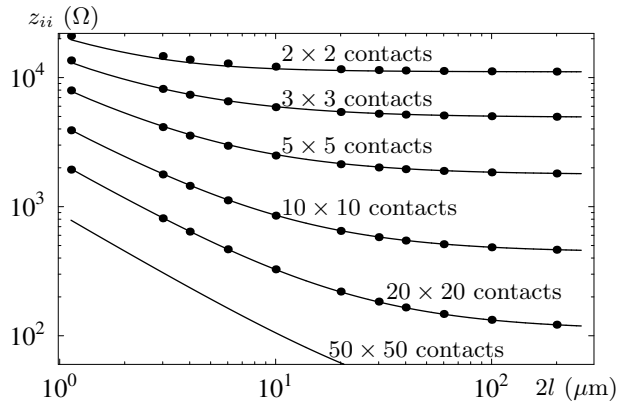


Figure 2.17 The total resistance for several contact arrays calculated with (2.25) as a function of the inter-contact distance. The results shown by filled circles are obtained with the surface potential model given in Paper D.

This is discussed in the next chapter. The resistance model, as formulated above, is applicable to uniform semi-infinite substrates. However, it should be possible to extend this model to finite thickness substrates. This would require replacing the third term in (2.25) by the expression appropriate for a finite thickness. We have not evaluated this idea, but this is something that could be suggested for further work.

3
Substrate Noise Reduction Methods

Several approaches have been presented for reducing substrate noise coupling. These techniques can be divided into three categories: minimizing the noise injected into the substrate, preventing the substrate from transmitting noise, and making the analog circuits less sensitive to substrate noise. The first section in this chapter provides an overview of different noise reduction methods proposed in the literature. The question how the substrate should be biased to reduce the susceptibility to substrate noise is investigated in more detail in Section 3.2. Section 3.3 discuss methods of using active circuits to decrease the noise transmission.

3.1 Overview of Noise Reduction Methods

Several well-known ways of reducing the substrate noise injected, transmitted, and received in mixed-signal circuits are mentioned in this section.

Since substrate noise in ICs to a large extent is due to parasitics between the chip and the package, it is effective to decrease these. For example, the inductance between the chip and the package, can be reduced by increasing the number of bond-wires, or using techniques such as flip-chip packaging.

In order to minimize the noise transmitted through the power supplies it is common to split the power supplies into analog and digital parts and even to use separate interconnects for biasing the substrate in the digital circuits (also called Kelvin grounding [61]).

When digital circuits switch, large amounts of charge has to charge or discharge various capacitances of the circuits. If this charge is not available, a voltage drop results, which also injects currents into the substrate through the biasing contacts. Therefore, capacitors are added close to the switching circuits on chip. These capacitors

are charged between the switching events, and supplies charge to the circuits when these switch. The voltage drops are therefore decreased [65].

A technique for making less noisy digital circuits was presented in [66]. Other logic families have also been investigated to see which injects the least noise into the substrate [67].

One of the most active circuits on the chip is the clock distribution network, since these contain a lot of inverters that switch with each clock period. These inverters create a large portion of the substrate noise on the chip. Badaroglu et al. [68] propose dividing the chip into several clock domains that do not switch at the same time. Thus, they decrease the peak switching noise, and the noise injected into the substrate. Another method is to drive the clock network with a smoother signal [69]. By using a clock signal with longer rise- and fall-times, both the peak noise and the high frequency components of the noise is decreased.

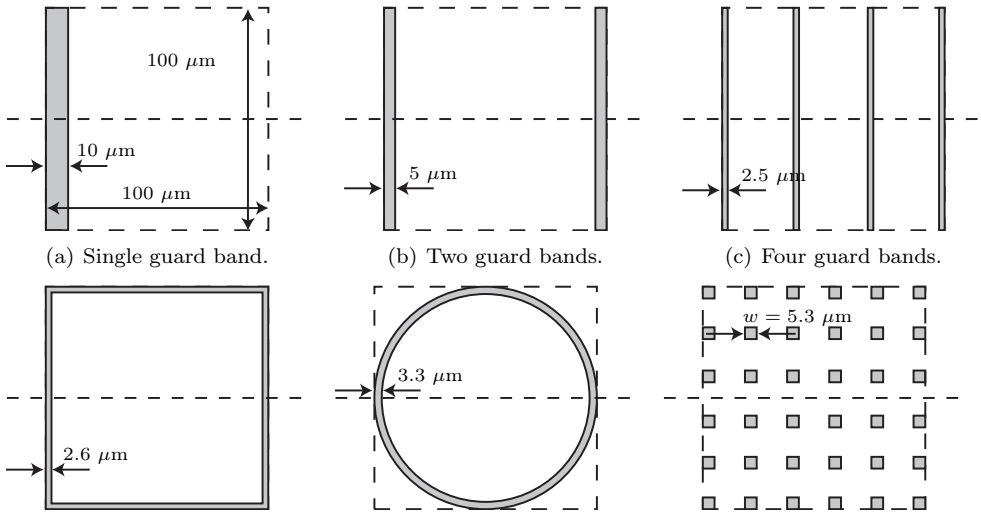
Instead of using conventional substrates, silicon-on-insulator (SOI) [70] or triple-well [71] substrates can be used for reducing the noise transmitted between circuit on the chip. But in these substrates the isolation is capacitive and is therefore gradually lost at higher frequencies [70]. The cost of these substrates is also higher than more common substrate types. Thus, for these reasons these substrates have not to date taken over the mixed-signal market [72]. Deep trench isolation are also used to decrease the coupling. In [73] deep N-well implantations was utilized for reducing the noise transmission, and this was found to be effective. Other methods have been proposed for modifying the substrate, such as Faraday cage isolation [74] and creating semi-insulating silicon by introducing dislocations [75].

Standard techniques for making the analog circuits less sensitive to substrate noise include: making these fully differential and thus less sensitive to common-signal noise, biasing the analog circuits and the digital circuits by separate power supply-lines, and surrounding the analog circuits with guard rings [65].

3.2 Substrate Grounding Methods

In this section different ways of grounding or biasing the substrate is presented (see Paper F for more details). Analytical expressions for the resistance of the grounding methods are also discussed.

The question how to isolate devices from each other quickly arose



(a) Single guard band. (b) Two guard bands. (c) Four guard bands.

(d) Rectangular guard ring. (e) Circular guard ring. (f) Distributed ground contacts.

Figure 3.1 Layout of different grounding structures. The grounded area and the square areas outlined with the dashed line, are equal in all cases.

after the IC was invented. Kurt Lehovec patented a method of using reverse biased pn-junctions, filed already in 1959 and issued in 1962 [76]. This method of isolation was discussed together with spatial separation of devices and using high resistivity silicon in 1963 [77]. Maxwell and Allison proposed a method of dielectric isolation of integrated devices in 1965 [78], an early variant of SOI. The method that eventually became the preferred choice was pn-junction isolation. However, as discussed in Chapter 1, this method is not always enough for mixed-signal circuits.

One strategy that is widely used for protecting analog circuits from substrate noise is to include guard bands or guard rings between the noisy circuits and the sensitive circuits [79]. These guards are substrate contacts connected to the ground reference. The idea is that these guard bands should "swallow" the noise, and therefore function as a wall protecting the sensitive circuits. The different ground options can be divided into distributed ground contacts, single or multiple guard bands, and guard rings (rectangular or circular), see Fig. 3.1.

Guard bands have been used in for example [63] and [80]. In [63] a

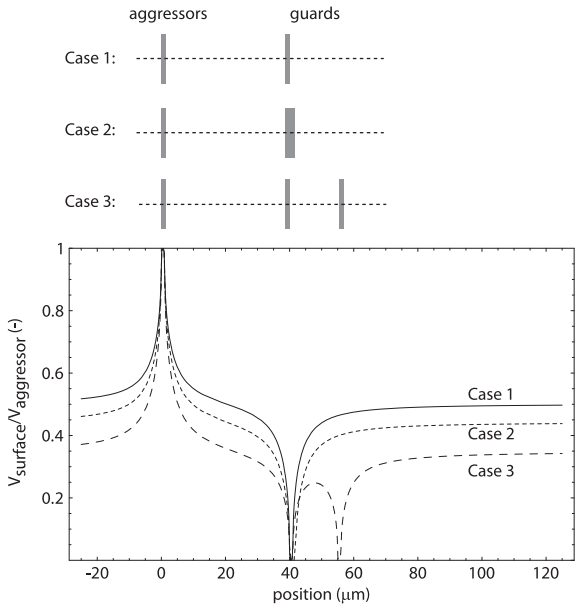


Figure 3.2 The normalized surface potential (along the dashed lines) for three different guard band structures. The guard band area in case 2 is equal to the combined area of the two guard bands in case 3.

very wide guard band was used and in [80] several guard bands were used. The efficiency of these, and other, isolation strategies is not known accurately. If a certain chip fulfills the noise restrictions it is often not known if the isolation strategy is an over-design or not.

In Paper F we investigated the efficiency of the different grounding options in Fig. 3.1. It was concluded that the best option is the distributed structure (see Fig. 5 in Paper F). The more distributed a ground structure is — the better (see Fig. 3.2 for an illustration).

Modeling of the different ground structures is also a concern. The single and multiple guard bands can be modeled by the equations discussed in Chapter 2. Rectangular guard rings can be modeled by superposition as illustrated in Paper E. The distributed ground structure can be modeled with the same model as discussed in Section 2.6.

The grounding resistance of a circular guard ring, an annulus, on a semi-infinite uniform substrate with resistivity ρ, can be modeled as

$$R_{\text{annulus}} = \begin{cases} \dfrac{R_1}{1 + 0.0143\frac{b}{a}\tan^3\left(1.28\frac{a}{b}\right)} & 1.1 < \frac{b}{a} < \infty \\ \dfrac{\rho \ln\left(\frac{16(a+b)}{b-a}\right)}{\pi^2(a+b)} & 1 < \frac{b}{a} < 1.1, \end{cases} \tag{3.1}$$

where

$$R_1 = \frac{\frac{\rho\pi}{8b}}{\arccos\left(\frac{a}{b}\right) + \sqrt{1-\left(\frac{a}{b}\right)^2}\,\operatorname{arctanh}\left(\frac{a}{b}\right)}. \tag{3.2}$$

This is an approximate expression derived from a model for the capacity of the ring presented by Smythe [81]. In these equations a and b are the inner and outer radius of the annulus, respectively. It should be mentioned that the resistance of the guard ring could be calculated by dividing it into small pieces and using superposition, as described for general contact shapes in Paper D and in [43]. This approach was used for calculating the capacitance of the annulus in [49].

The resistance of the circular ring as a function of the inner radius is shown in Fig. 3.3. The results given by (3.1), and the filled circles are numerical calculations performed with Comsol Multiphysics [30]. The agreement is seen to be excellent.

The surface potential around the guard ring can be modeled in the following way, see also Paper F. Assume that the current flowing through the guard ring can be approximated as flowing through the circle with radius $c = (a+b)/2$, the surface potential is given by [82, p. 208]

$$V_{\text{annulus}}(\varrho, 0) = \begin{cases} \dfrac{\rho I}{\pi^2}\dfrac{\mathrm{K}\left(\frac{\varrho^2}{c^2}\right)}{c} & \text{for } \varrho < c \\ \dfrac{\rho I}{\pi^2}\dfrac{\mathrm{K}\left(\frac{c^2}{\varrho^2}\right)}{\varrho} & \text{for } \varrho > c. \end{cases} \tag{3.3}$$

The expressions in [82] was given in integral form for a ring carrying a charge Q. Fortunately, the integrals have analytical solutions. We

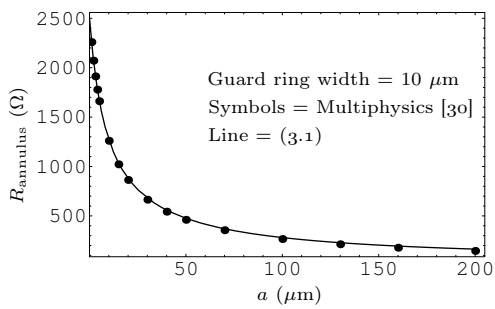


Figure 3.3 The resistance of a circular guard ring of fixed width as a function of the inner radius.

have also reformulated the problem as a current flow problem (note that Smythe uses electrostatic units). In (3.3), I is the total current flowing through the guard ring, and ϱ is the radial distance measured from the center of the guard ring. This model is compared with numerical results, obtained with Multiphysics, in Fig. 3.4 for several ring sizes. The agreement is seen to be very good, it is only very close to the guard rings where the model deviates appreciably from the numerical results.

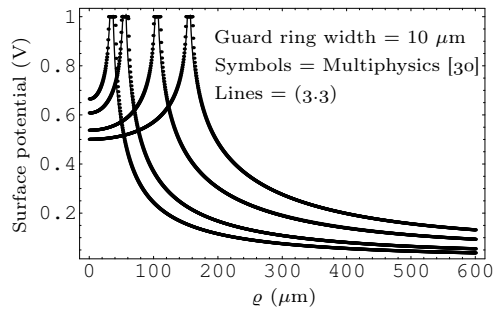


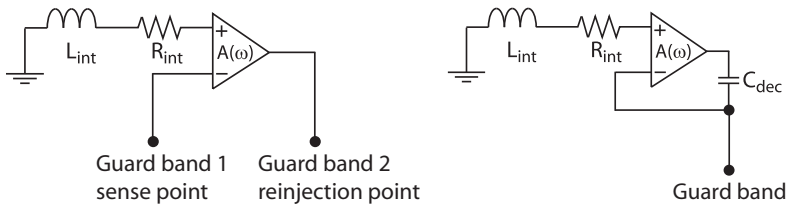
Figure 3.4 The radial surface potential of four guard rings biased at 1 V. The inner radii are 30, 50, 100, and 150 μm, respectively.

3.3 Active Suppression of Substrate Noise

This section discusses methods of using active circuits for reducing substrate noise. In Paper G we investigated one of these methods in detail, using an accurate model of the substrate.

Active circuits for substrate noise suppression was introduced by Maike-Fukuda et al. [83] in 1995. The idea, see Fig. 3.5(a), is to sense the noise by a substrate contact (guard band 1). This sensed noise will then be amplified and re-injected into the substrate through another substrate contact (guard band 2) in negative phase. Therefore, it is argued, the substrate noise will be canceled and will not reach the sensitive circuits. The substrate was in [83] modeled using a few lumped resistors. Active substrate noise cancelation was further investigated by Liu et al. [84] using a more finely meshed resistor network for the substrate.

In a recent paper [85] Tsukada et al. proposed using active circuits to decouple a guard band connection from the inevitable parasitic resistance and inductance of the grounding network (R_{int} and L_{int} in Fig. 3.5(b)). The idea is the following: since the current into the positive terminal of the operational amplifier ideally is zero, it will be



(a) Noise cancelation method [83]. (b) Noise decoupling method [85].

Figure 3.5 Two active noise reduction methods presented in the literature.

grounded. This will be transferred to a virtual ground at the negative terminal of the amplifier, since the voltage difference between the input terminals are ideally zero. In this way, the guard band connected to the substrate at ground potential. The noise current that flows into the guard band, continues through the decoupling capacitor without altering the guard band potential. Thus, the guard band will be a stable ground, contrary to the case when the guard band is connected directly to ground through R_{int} and L_{int}.

We investigated this method in Paper G using an accurate substrate model. Our results, however, show that there is no advantage using active decoupling compared with dc grounding.

The reason why the method in Fig. 3.5(b) is not efficient can be explained by the following example. Assume that the victim and the backside are floating and that both the aggressor circuit and the decoupling circuit are connected to the substrate node by a resistor R_{sub}, see Fig. 3.6. This simplification is accurate for situations where the aggressor and the guard band are far apart on the chip. Then the substrate voltage normalized to the aggressor voltage can be written as (see Paper G)

$$\frac{V_{\text{sub}}}{V_{\text{agg}}} = \frac{1 + j\omega R_{\text{sub}} C_{\text{dec}}(1+A)}{1 + (Z_{\text{agg}} + 2R_{\text{sub}})j\omega C_{\text{dec}}(1+A)}, \tag{3.4}$$

where Z_{agg} is the impedance through which the aggressor circuit injects noise into the substrate. When the substrate resistance R_{sub} is zero and $Z_{\text{agg}} = 1/(j\omega C_{\text{agg}})$, (3.4) reduces to the simpler expression shown in [85]. When the substrate resistance increases, (3.4) approaches the limit 1/2, exactly as in the dc grounding case. The situation is therefore simply a voltage division of the two substrate resistors. To be effective, the victim should have to be located close

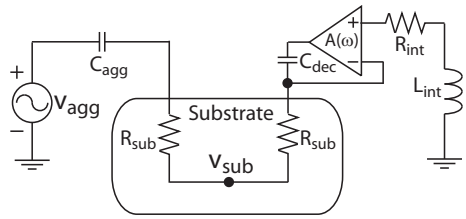


Figure 3.6 Substrate model for Tsukada's method applicable when the distance between the aggressor and the guard band is great.

to the guard band in this case, since the substrate node voltage is not efficiently reduced.

The situation can also be viewed in the following way. If the active decoupling method is to be efficient compared with dc grounding, the impedance seen from the substrate contact into the ground network has to small compared with the resistance from the substrate contact to the substrate node.

4
Summary

This chapter summarize the main conclusions obtained in the thesis and discusses the results. The chapter ends with pointing directions for further research in this area.

In this thesis we have presented substrate impedance models for noise coupling analysis. The model equations originate from spreading resistance theory. We have shown how to model rectangular contacts on uniform and epitaxial substrates with compact models. We have also shown how general contact shapes on multi-layer substrates can be modeled by superposition. These models are easy to implement and should be helpful for early design work of mixed-signal ICs.

The major contribution is the impedance model for uniform substrates. This model is scalable, and expressed using physical parameters. For epitaxial substrates, empirical models existed before this thesis. However, in this work we have shown that our compact substrate model can be applied to both uniform and epitaxial substrates.

We have discussed, and pointed out, difficulties with representing the substrate as a lumped resistor network. This provides the motivation for formulating the substrate noise coupling problem using an impedance matrix.

A compact model for the interaction of a digital circuit block consisting of many injectors was presented. This model is very efficient and can be useful at the floorplan stage of the design process.

The efficiency of several grounding methods have been investigated, and it was shown that the most effective option is to distribute the ground contacts as much as possible. Compact and scalable models for the main grounding techniques were presented.

A technique of using active circuits for providing a stable ground was investigated and compared with dc grounding using our substrate models. It was shown that the efficiency of the active decoupling was in most cases not appreciably better than dc grounding. It was also shown that this is highly dependent on the substrate resistivity.

Further work is needed to extend our substrate noise coupling model to include effects at high frequencies. The first step, to add capacitive effects, should not be too difficult. Preliminary work have been presented in [86].

Also, the model equations should be implemented in a circuit simulator to model the effect of substrate coupled noise in more complicated mixed-signal circuit examples.

The transistor in contemporary models communicate with the substrate through the bulk node. This bulk node should perhaps be replaced by a distributed model for certain situations where the substrate potential varies along the transistor.

It would also be of worth if the spreading resistance model for circular contacts could be extended to rectangular contacts. Then the spreading resistance of rectangular contacts on multi-layer substrates could be modeled by expressions in integral form. In my view, this would entail replacing the Bessel functions in the integral expression with Mathieu functions.

A
Appendix

This appendix contains detailed derivations of the model equations. In the first section, the potential around a charged circular contact on a uniform substrate is derived. In the second section, the extension of circular disc solution to multi-layered substrates is presented. Finally, the third section derives the resistance model for an array of identical contacts.

A.1 The Potential Around a Charged Circular Disc

The surface potential models and the resistance models used in this thesis are closely related to a specific problem: the potential $V(\mathbf{r})$ developed around a thin circular disc charged to the potential V_0 on a uniform substrate. The problem, shown in Fig. A.1, is to solve Laplace's equation which for the circular disc problem is most conveniently solved using cylindrical coordinates (ϱ, ϕ, z). Since the charged disc problem display circular symmetry (the potential on the disc is constant) the solution does not depend on the angle ϕ

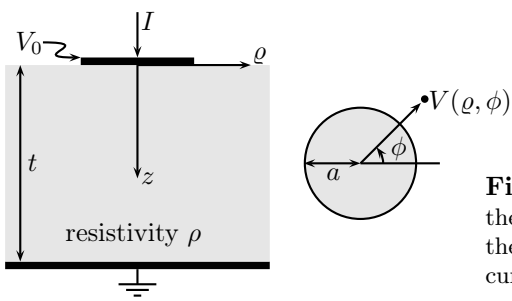


Figure A.1 Top and cross-sectional views of the circular disc problem. The disc is charged to the potential V_0 (or equivalently has the total current I flowing through it).

($V = V(\varrho, z)$). Laplace's equation then reads

$$\frac{\partial^2 V}{\partial \varrho^2} + \frac{1}{\varrho}\frac{\partial V}{\partial \varrho} + \frac{\partial^2 V}{\partial z^2} = 0. \tag{A.1}$$

This equation has to be solved in the region $0 \leq \varrho < \infty$, $0 \leq \phi < 2\pi$, $0 \leq z \leq t$ under the following boundary conditions

$$\lim_{\varrho \to \infty} V(\varrho, z) = 0 \tag{A.2}$$

$$\lim_{\varrho \to 0} V(\varrho, z) < \infty. \tag{A.3}$$

The last boundary condition requires the potential to be bounded as $\varrho \to 0$. By separation of variables (the potential is assumed to be of the form $V(\varrho, z) = R(\varrho)Z(z)$) the following two ordinary differential equations are obtained

$$\varrho^2 \frac{d^2 R}{d\varrho^2} + \varrho \frac{dR}{d\varrho} + u^2 \varrho^2 R = 0 \tag{A.4}$$

$$\frac{d^2 Z}{dz^2} - u^2 Z = 0, \tag{A.5}$$

where u^2 is a constant of separation. The first equation is a Bessel equation with the solutions

$$R(\varrho) = A\,\mathrm{J}_0(\varrho u) + B\,\mathrm{Y}_0(\varrho u), \tag{A.6}$$

where $\mathrm{J}_0(x)$ and $\mathrm{Y}_0(x)$ are zero-order Bessel function of the first and second kind, respectively. Since $V(0, z)$ is required to be finite, we must have $B \equiv 0$ since $\mathrm{Y}_0(\varrho u) \to -\infty$ when $\varrho \to 0$. Thus,

$$R(\varrho) = A(u)\,\mathrm{J}_0(\varrho u). \tag{A.7}$$

The solution of (A.5) is

$$Z(z) = C(u)e^{zu} + D(u)e^{-zu}. \tag{A.8}$$

Equations (A.7) and (A.8) give the following potential

$$V_u(\varrho, z) = \left[f(u)e^{-zu} + g(u)e^{zu}\right] \mathrm{J}_0(\varrho u), \tag{A.9}$$

where we have renamed $f(u) = A(u)C(u)$ and $g(u) = A(u)D(u)$. To proceed, the following boundary conditions are used:

$$V(\varrho, z) = V_0 \qquad \text{when } \varrho \leq a \text{ and } z = 0 \tag{A.10}$$

$$\frac{\partial V(\varrho, z)}{\partial z} = 0 \qquad \text{when } \varrho > a \text{ and } z = 0. \tag{A.11}$$

Equation (A.11) states that the current density flowing through the surface is identically zero except in the contact. To satisfy (A.10) and (A.11) a trial solution is

$$V(\varrho, z) = \int_0^\infty \left[f(u)e^{-zu} - g(u)e^{zu} \right] \mathrm{J}_0(\varrho u)du, \tag{A.12}$$

since the only restriction on u is that it should be a non-negative real number.

The unknown functions f and g, which also can be functions of a and t, even though this dependence is not shown explicitly, has to be determined through boundary conditions. Since, at $z = t$ the potential must be zero for all ϱ, the following equation has to be fulfilled

$$f(u)e^{-tu} + g(u)e^{tu} = 0, \tag{A.13}$$

which is equivalent to

$$g(u) = -f(u)e^{-2tu}. \tag{A.14}$$

The potential is then [87, p. 118]

$$V(\varrho, z) = \int_0^\infty f(u) \left[e^{-zu} - e^{(z-2t)u} \right] \mathrm{J}_0(\varrho u)du, \tag{A.15}$$

which can be written as [88, p. 247]

$$V(\varrho, z) = \int_0^\infty \frac{A(u)}{u} \frac{\sinh(t-z)u}{\cosh(tu)} \mathrm{J}_0(\varrho u)du, \tag{A.16}$$

if $f(u)$ is rewritten as

$$f(u) = \frac{A(u)}{u} \frac{1}{(1+e^{-2tu})}. \tag{A.17}$$

However, since the arguments in the elementary functions in (A.16) are dimensionless, the dimension of the integration variable u is inverse length. Thus, the whole integral expression in (A.16) is dimensionless, and we have to add a constant k with dimension volts in front of the integral. To determine this constant we simplify things by solving the problem for the case of a semi-infinite substrate. If, $t \to \infty$, (A.16) reduce to

$$V(\varrho, z) = \int_0^\infty \frac{A(u)}{u} e^{-zu} \mathrm{J}_0(\varrho u)du, \tag{A.18}$$

With this expression, the boundary conditions, (A.10) and (A.11), become

$$V_0 = \int_0^\infty \frac{A(u)}{u} \, \mathrm{J}_0(\varrho u) du \qquad \text{when } \varrho \leq a \text{ and } z = 0, \tag{A.19}$$

$$0 = \int_0^\infty A(u) \, \mathrm{J}_0(\varrho u) du \qquad \text{when } \varrho > a \text{ and } z = 0. \tag{A.20}$$

The function $A(u)$ which fulfils the boundary conditions is $\sin(au)$ [88, p. 64]. The constant k is determined by the condition that the current density $J_z(\varrho, 0)$ integrated over the contact equals the total current I. Thus,

$$\begin{aligned}
I &= \int_0^a \int_0^{2\pi} J_z|_{z=0} \varrho d\varrho d\phi \\
&= \int_0^a \int_0^{2\pi} \left(-\frac{1}{\rho} \left. \frac{\partial V}{\partial z} \right|_{z=0} \right) \varrho d\varrho d\phi \\
&= \int_0^a \int_0^{2\pi} \frac{1}{\rho} k \int_0^\infty \frac{\sin(au)}{u} \varrho u \, \mathrm{J}_0(\varrho u) du d\varrho d\phi \\
&= \int_0^\infty \frac{1}{\rho} 2\pi k \frac{\sin(au)}{u} u \int_0^a \varrho \, \mathrm{J}_0(\varrho u) d\varrho du \\
&= \int_0^\infty \frac{1}{\rho} 2\pi k \sin(au) \frac{a \, \mathrm{J}_1(au)}{u} du \\
&= \frac{2\pi a}{\rho} k \int_0^\infty \frac{\sin(au)}{u} \, \mathrm{J}_1(au) du \\
&= \frac{2\pi a}{\rho} k.
\end{aligned}$$

In the last step the fact that [46, p. 487],

$$\int_0^\infty \frac{\sin(au)}{u} \, \mathrm{J}_1(au) du = 1, \tag{A.21}$$

has been used. The constant k is therefore equal to $\rho I/(2\pi a)$, which has the dimension volt as required[1]. The final expression for the volt-

[1] This factor can also be written as $V_0 2/\pi$.

age distribution around a circular contact of radius a, on a semi-infinite substrate of uniform resistivity ρ is then

$$V(\varrho, z) = \frac{\rho I}{2\pi a} \int_0^\infty \frac{\sin(au)}{u} e^{-zu} \, \mathrm{J}_0(\varrho u) du. \tag{A.22}$$

At the surface ($z = 0$) (A.22) reduces to a special case of the discontinuous Weber-Schafheitlin integral [46, p. 487] with the solution

$$\int_0^\infty \frac{\sin(au)}{u} \, \mathrm{J}_0(\varrho u) du = \begin{cases} \dfrac{\pi}{2} & \text{when } 0 \le \varrho \le a \\ \arcsin\left(\dfrac{a}{\varrho}\right) & \text{when } \varrho \ge a. \end{cases} \tag{A.23}$$

At the surface, $z = 0$, (A.22) is therefore

$$V(\varrho, 0) = \begin{cases} \dfrac{\rho I}{4a} & \text{when } 0 \le \varrho \le a \\ \dfrac{\rho I}{2\pi a} \arcsin\left(\dfrac{a}{\varrho}\right) & \text{when } \varrho \ge a. \end{cases} \tag{A.24}$$

When $\varrho \gg a$, we can make the approximation $\arcsin(a/\varrho) \approx a/\varrho$, thus the surface potential simplifies to $\rho I/(2\pi\varrho)$. This is the surface potential from a point source, as derived below. Figure A.2(a) shows the surface potential expressed by (A.24).

The resistance between the disc and infinity is easily derived from (A.24) to be

$$R = \frac{\rho}{4a}, \tag{A.25}$$

which is a very fundamental relation in the theory of electric contacts [64, p. 16]. From (A.25) the limiting resistance between two far apart coplanar circular contacts is easily seen to be $\rho/(2a)$.

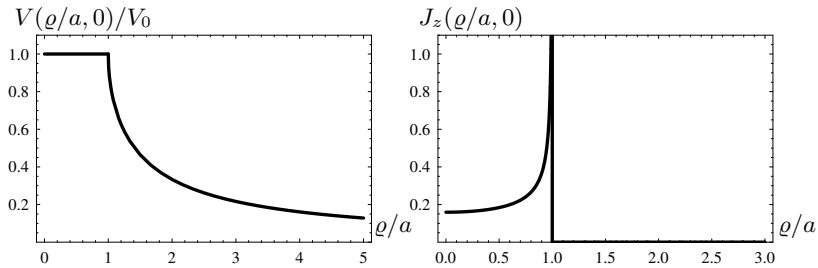
If the derivative with respect to z is taken in (A.22) the normal current density at the surface is [46, p. 487]

$$J_z(\varrho, 0) = \begin{cases} \dfrac{I}{2\pi a} \dfrac{1}{\sqrt{a^2 - \varrho^2}} & \text{when } \varrho \le a \\ 0 & \text{when } \varrho > a. \end{cases} \tag{A.26}$$

This current density is shown in Fig. A.2(b). Note that the current density diverges at the contact circumference.

In the limit $a \to 0$, (A.22) reduces to

$$V(\varrho, z) = \frac{\rho I}{2\pi} \int_0^\infty e^{-zu} \, \mathrm{J}_0(\varrho u) du, \tag{A.27}$$



(a) The radial surface potential of the disc.

(b) The normal current density along a radii at the surface.

Figure A.2 Surface potential and current density of the charged circular disc.

which can be solved analytically [89, p. 384]

$$\int_0^\infty e^{-zu}\,\mathrm{J}_0(\varrho u)du = \frac{1}{\sqrt{\varrho^2+z^2}} = \frac{1}{r}. \tag{A.28}$$

Thus, the potential around the disc reduces to the familiar expression for the potential from a point source when a approaches zero, that is ([64, p. 4], [90])

$$V(r) = \frac{\rho I}{2\pi r}. \tag{A.29}$$

We now return to the finite thickness case depicted in Fig. A.1. From (A.16) the potential at the substrate surface is

$$V(\varrho, 0) = \frac{\rho I}{2\pi a}\int_0^\infty \frac{A(u)}{u}\tanh(tu)\,\mathrm{J}_0(\varrho u)du. \tag{A.30}$$

Here the function $A(u)$ is not equal to $\sin(au)$, instead it has to be determined by solving an integral equation. This is a complicated problem, and there is no solution that can be expressed in elementary functions.

If the following series expansion of $\tanh x$ $(x > 0)$,

$$\tanh(x) = 1 + 2\sum_{n=1}^{\infty}(-1)^n e^{-2nx}, \tag{A.31}$$

is used (A.30) can be written as

$$V(\varrho,0)=\frac{\rho I}{2\pi a}\left\{\int_0^\infty \frac{A(u)}{u}\,\mathrm{J}_0(\varrho u)du+ \right.$$
$$\left. 2\sum_{n=1}^{\infty}(-1)^n\int_0^\infty \frac{A(u)}{u}e^{-2ntu}\,\mathrm{J}_0(\varrho u)du\right\}. \tag{A.32}$$

This expression can be interpreted as the surface potential due to an isolated disc in a semi-infinite substrate (the first term) plus the surface potential given by an infinite number of coaxial discs at $z = \pm 2t, \pm 4t, \ldots$ with alternating potentials of $-V_0$ and $+V_0$. Thus, the following approximation is given

$$V(\varrho,0)=\frac{I\rho}{2\pi}\left[\arcsin\left(\frac{a}{\varrho}\right)+2\sum_{n=1}^{\infty}(-1)^n\arcsin\left(\frac{a}{\sqrt{\varrho^2+s}}\right)\right], \tag{A.33}$$

where s is given as the positive solution to

$$\frac{\varrho^2}{a^2+s}+\frac{(2nt)^2}{s}=1. \tag{A.34}$$

The drawback of the series solution presented above is that for thin substrates, $t < a$, it requires many terms to be of reasonable accuracy.

A.2 Multi-Layer Substrate Potential Model

In this section the surface potential due to a current I injected into a *multi-layer* substrate through a circular contact of radius a is discussed. The problem is shown in Fig. A.3. An approximate solution to this problem was given by Sunde [45, p. 43] in the context of earth conduction effects. In 1969, Schumann and Gardner applied the same theory to spreading resistance modeling in semiconductors [91, 92]. The solution assumes that the current density in the circular contact is well approximated by the current density for the case of a semi-infinite uniform substrate, i.e. (A.26)[2]. This is of course an approxima-

[2]For certain substrate types, like thin uniform substrates on a perfectly conducting bottom layer, a better current density boundary condition was shown by

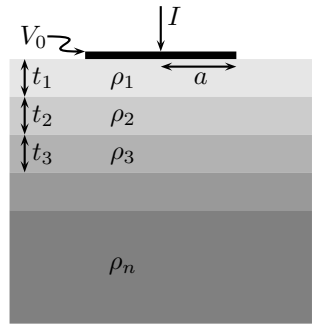


Figure A.3 A circular contact of radius a on a substrate consisting of n layers, each uniformly doped.

tion, which was well pointed out in [91], since an exact solution for the general problem does not exist[3].

The surface potential for a substrate consisting of n layers, can be expressed as [52]

$$V(\varrho,0)=\frac{I\rho_1}{2\pi a}\int_0^\infty A_1(u)\frac{\sin(au)}{u}\,\mathrm{J}_0(\varrho u)du, \tag{A.35}$$

where the function $A_1(u)$ is obtained through the recursive relations

$$A_i(u)=\frac{1-k_i e^{-2t_i u}}{1+k_i e^{-2t_i u}}, \tag{A.36}$$

and

$$k_i=\frac{\rho_i-\rho_{i+1}A_{i+1}}{\rho_i+\rho_{i+1}A_{i+1}}. \tag{A.37}$$

The nth layer is assumed to be infinitely thick, so $A_n=1$. In these equations t_i and ρ_i are the thickness and resistivity of each layer in the substrate, see Fig. A.3. These equations are derived from requiring that the potential and current density between adjacent layers are continuous.

The resistance between two coplanar circular contacts can now be modeled. In general, the potential for $\varrho<a$ using (A.35) will not be constant [93]. Because of this the average potential in the contact is

Leong *et al.* [93] to be a uniform current density. That is, the current density in the contact is assumed to be uniform and equal to $I/(\pi a^2)$.

[3]For certain special cases, such as a uniform layer on a bulk layer of zero resistivity, exact solutions has been presented [88].

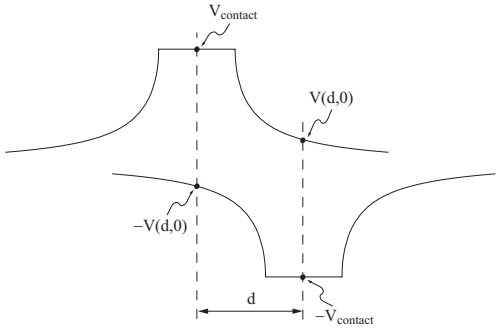


Figure A.4 Illustration of the superposition of two one-contact potentials.

taken as the contact potential

$$\begin{aligned} V_{contact} =& \frac{\int_0^a \int_0^{2\pi} V(\varrho,0)\varrho d\varrho d\phi}{\pi a^2} \\ =& \frac{2\pi}{\pi a^2}\frac{\rho_1 I}{2\pi a}\int_0^\infty A_1 \frac{\sin(au)}{u}\int_0^a \varrho\, \mathrm{J}_0(\varrho u) d\varrho du \\ =& \frac{\rho_1 I}{\pi a^3}\int_0^\infty A_1 \frac{\sin(au)}{u}\frac{a\,\mathrm{J}_1(au)}{u} du \\ =& \frac{\rho_1 I}{\pi a^2}\int_0^\infty A_1 \frac{\sin(au)}{u^2}\,\mathrm{J}_1(au) du. \end{aligned} \tag{A.38}$$

The potential difference between the two contacts, see Fig. A.4, can then be modeled as

$$\begin{aligned} \Delta V =& V_{\text{left disc}} - V_{\text{right disc}} \\ =& [V_{contact} - V(d,0)] - [-V_{contact} + V(d,0)] \\ =& \frac{2\rho_1 I}{\pi a}\int_0^\infty A_1 \frac{\sin(au)}{u}\left[\frac{\mathrm{J}_1(au)}{au} - \frac{\mathrm{J}_0(du)}{2}\right] du, \end{aligned} \tag{A.39}$$

which results in the following expression for the resistance between the two circular contacts [94]

$$R(d) = \frac{2\rho_1}{\pi a}\int_0^\infty A_1 \frac{\sin(au)}{u}\left[\frac{\mathrm{J}_1(au)}{au} - \frac{\mathrm{J}_0(du)}{2}\right] du. \tag{A.40}$$

For a uniform substrate $A_1 = 1$, and therefore the surface potential expression reduces to that in (A.22) for $z = 0$. If the substrate consist of two layers, then

$$A_1 = \frac{1 - k_1 e^{-2t_1 u}}{1 + k_1 e^{-2t_1 u}}, \tag{A.41}$$

and

$$k_1 = \frac{\rho_1 - \rho_2}{\rho_1 + \rho_2}. \tag{A.42}$$

Two degenerate cases are when the bottom layer is perfectly conducting ($\rho_2 \equiv 0$), resulting in

$$A_1 = \tanh(t_1 u), \tag{A.43}$$

and when the bottom layer is perfectly insulating ($\rho_2 = \infty$), giving

$$A_1 = \frac{1}{\tanh(t_1 u)}. \tag{A.44}$$

The A_1 in (A.44) inserted into (A.40) gives the model used in Paper E.

The resistance model (A.40) was introduced for spreading resistance modeling by Schumann and Gardner [92], and has been used in many papers in this area since then, see for example [95] and [96]. But for applications in modeling substrate effects in integrated circuits, the resistance model (A.40) does not seem to have been used.

A.3 The Resistance of a Contact Array

In this section we derive the resistance of the array of contacts discussed in Section 2.6. This derivation is important in order to understand the assumptions made and the limitations of the model. This derivation closely follows the one given by Holm [64, pp. 21–23], but is given for small square contacts in a large rectangular area, see Fig. 2.15.

A cross-sectional view of the contact array is shown schematically in Fig. A.5. If the whole area occupied by the contact array, shown by the lower large thick rectangle, would conduct current, the resistance would be (see Paper E)

$$R_3 = \frac{\rho}{2\sqrt{\pi}\, L} \mathrm{K}\left(1 - \frac{W^2}{L^2}\right), \tag{A.45}$$

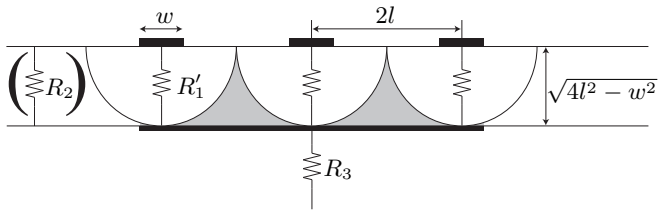


Figure A.5 Cross-sectional view of the contact array illustrating how the resistance model is derived.

where the function K is the complete elliptic integral of the first kind, defined as

$$\mathrm{K}(m) = \int_0^{\pi/2} \frac{d\theta}{\sqrt{1 - m\sin^2\theta}}. \tag{A.46}$$

However, the current is constricted to flow through the small contacts, each a square contact with side length w. The resistance R_1' from one of the small contacts to the semi-ellipsoid, is given by (see [64, p. 16])

$$R_1' = \frac{\rho}{2\sqrt{\pi}\,w} \arctan\left(\frac{\sqrt{4l^2 - w^2}}{w}\right), \tag{A.47}$$

where the height of the semi-ellipsoid is $\sqrt{4l^2 - w^2}$. Each of these resistances are assumed to be independent of each other. The total resistance is then simply $R_1 = R_1'/n$.

Now comes the key observation: The resistance due to the constricted current flow is equal to the resistances of all the small resistances in parallel *minus* the resistance of the region if the current was not constricted (the resistance R_2 of the rectangular block which is shaded grey in Fig. A.5). That is

$$R_1 - R_2 = \frac{\rho}{2\sqrt{\pi n}\,w} \arctan\left(\frac{\sqrt{4l^2 - w^2}}{w}\right) - \rho\, k \frac{\sqrt{4l^2 - w^2}}{WL}. \tag{A.48}$$

The numerical coefficient k is put into R_2, since in the limit $2l \to w$, we should have $R_1 - R_2 \to 0$ without becoming negative at any point. It can easily be shown that the coefficient is equal to $1/(2\sqrt{\pi})$.

The total resistance from the array of square contacts is then given by $R_1 - R_2 + R_3$, as shown in (2.25).

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Paper A

Substrate Resistance Modeling for Noise Coupling Analysis

Simon Kristiansson, Shiva P. Kagganti, Tony Ewert,
Fredrik Ingvarson, Jörgen Olsson, and Kjell O. Jeppson
Presented at the IEEE International Conference on Microelectronic Test Structures, Monterey, California, USA, March 17–20, 2003.

My contributions to this paper was the idea of using surface potentials to describe substrate noise coupling, derivations of the z-parameter expressions, performing measurements (together with Kagganti), and primary author of the paper. The circuit simulations were performed by Kagganti.

Paper B

Resistance Modelling in 1D, 2D, and 3D for Substrate Networks

Shiva P. Kagganti, Simon Kristiansson, Fredrik Ingvarson,
and Kjell O. Jeppson
Physica Scripta, vol. T114, pp. 217–222, 2004.

My contributions to this paper included theoretical analysis and discussions and preparing the paper for final publication. The device simulations were performed by Kagganti.

Paper C

A Comparison of the Exact and an Approximate Solution for the Resistance Between Two Coplanar Circular Discs

Simon Kristiansson, Shiva P. Kagganti, Fredrik Ingvarson,
and Kjell O. Jeppson
Solid-State Electronics, vol. 49, no. 2, pp. 275–277, 2005.

My contributions to this paper was initiating the study, carrying out the theoretical analysis, preparing the figures, and writing the paper.

Paper D

A Surface Potential Model for Predicting Substrate Noise Coupling in Integrated Circuits

Simon Kristiansson, Fredrik Ingvarson, Shiva P. Kagganti,
Nebojša Simić, Marinel Zgrda, and Kjell O. Jeppson
IEEE Journal of Solid-State Circuits, vol. 40, No. 9,
pp. 1797–1803, Sept. 2005.

Invited paper from the work presented at the Custom Integrated Circuits Conference [43]. My contributions was deriving the z-parameter expressions, developing the surface potential concept, and primary author of the paper. The measurements was performed by Kagganti. The figures in the paper was prepared by Ingvarson.

Paper E

Modeling of Rectangular Contacts for Noise Coupling Analysis in Homogeneous Substrates

Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson
Presented at the 23rd Norchip Conference, Oulu, Finland,
November 21–22, 2005.

My contributions to this paper was initiating the study, deriving the compact surface potential model and the resistance model, performing the finite element calculations, and writing the paper. Ingvarson wrote the Mathematica code used to calculate the BEM results used for comparison, and prepared figures 8 and 9.

Paper F

Properties and Modeling of Ground Structures for Reducing Substrate Noise Coupling in ICs

Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson
Presented at the IEEE International Symposium on Circuits and Systems, Island of Kos, Greece, May 21–24, 2006.

My contributions to this paper was initiating the study together with Ingvarson, performing the finite element simulations, deriving and modifying the equations used from Holm and Smythe, preparing the figures, and writing the paper.

Paper G

Evaluation of Using Active Circuitry for Substrate Noise Suppression

Rashid Farivar, Simon Kristiansson, Fredrik Ingvarson,
and Kjell O. Jeppson
Presented at the ACM Great Lakes Symposium on VLSI,
Stresa-Lago Maggiore, Italy, March 11–13, 2007.

My contributions to this paper included the theoretical analysis and discussion, preparing figures 1 and 2, and final writing of the paper.

Paper H

Compact Spreading Resistance Model for Rectangular Contacts on Uniform and Epitaxial Substrates

Simon Kristiansson, Fredrik Ingvarson, and Kjell O. Jeppson
IEEE Transactions on Electron Devices, vol. 54, no. 9,
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My contributions to this paper was initiating the investigation, deriving the spreading resistance model, performing the finite element calculations, preparing the figures, and writing the paper.

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