Transfer-free, lithography-free, and micrometer-precision patterning of CVD graphene on SiO<inf>2</inf>toward all-carbon electronics

Transfer-free, lithography-free, and micrometer-precision patterning of CVD graphene on SiO_2 toward all-carbon electronics

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A method of producing large area continuous graphene directly on SiO_2 by chemical vapor deposition is systematically developed. Cu thin film catalysts are sputtered onto the SiO_2 and pre-patterned. During graphene deposition, high temperature induces evaporation and balling of the Cu, and the graphene "lands onto" SiO_2. Due to the high heating and growth rate, continuous graphene is largely completed before the Cu evaporation and balling. 60 nm is identified as the optimal thickness of the Cu for a successful graphene growth and μm-large feature size in the graphene. An all-carbon device is demonstrated based on this technique.
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Since 2004,[1] graphene, a monolayer of carbon atoms in graphite, has become one of the most promising electronic materials. The unique feature of graphene is its integration of many special properties such as high optical transmittance, high electrical and thermal conductivity, mechanical flexibility and strength, into one material.[2,3] Methods for graphene synthesis include micromechanical exfoliation,[1] epitaxy,[4] liquid phase processes,[5] and chemical vapor deposition (CVD).[6–8] Among them, CVD has relatively low cost and rather high material quality and, most importantly, good compatibility with traditional semiconductor technologies. Therefore, it has become a mainstream production method for graphene thin films, where Ni and Cu are the dominant catalysts.[6–8] Nevertheless, most electronic applications require graphene to be situated on insulators, and hence a transfer process is needed. The transfer of an atomic layer, however, is irreproducible, time consuming, and hard to control, practically leading to inevitable contaminants, failure, and uncertainties, together with massive heavy metal emission.[9–11] Currently, the transfer is probably the largest obstacles in the graphene CVD technique toward real application. Another well-known issue in the graphene community is the contamination from photoresist. For most electronic applications, patterning of graphene is a must. Nevertheless, photoresist residues on graphene coming from the photolithography process, and sometimes from the transfer process as well, are extremely difficult to remove, resulting in graphene with severely degraded properties,[12] typically with a low mobility, a strong p-doping and the corresponding drift away of the Dirac point. For applications such as graphene sensors, it is vital to keep the Dirac point at its original position (gate voltage $V_g = 0$) for achieving the best sensitivity. But, due to the photoresist contamination, the graphene Dirac point can easily shift to gate voltages of several tens of volts or higher (with typically 300 nm SiO_2 gate dielectric). Indeed, to date, almost all of the good graphene electrical properties (i.e., high mobility and Dirac voltage ~0) are measured in devices fabricated by electron beam lithography, where the resist is more benign to graphene as compared with the photoresist. However, electron beam lithography is not the

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best choice for applications due to its time consuming and high cost nature. Therefore, it is urgent to develop a transfer-free and lithography-free technique for graphene patterning.

In recent years, metal-free noncatalytic growth of graphene directly on insulators is pursued.[13,14] However, without a catalyst, the material quality is modest and, furthermore, this technique cannot avoid lithography and thus the direct contact of graphene to photoresist. To develop a both transfer-free and lithography-free method, people turn to sacrificial metal assisted CVD. Here, the metal catalysts are either removed *ex situ* by post etching or *in situ* by vaporization, rendering a transfer-free technology. At the same time, as the metals can be lithographically patterned beforehand, and the shape of graphene follows that of the metals, the pattern can be transferred to graphene without the graphene undergoing any lithography, avoiding its direct contact with photoresist.

For those techniques that remove metals by post etching, typically a Ni film (could be patterned) is deposited onto an insulating substrate.[15–17] As the solubility of C in Ni is high, during the CVD, carbon will be absorbed into the Ni and segregate upon cooling down. The carbon that segregates downwards will form a graphene film at the Ni-insulator interface. After removing the Ni, the graphene is left on the insulator. The drawback is that the segregation is not uniform and difficult to control, leading to multilayer defects in the graphene. Su *et al.*[18] use Cu as the catalyst, which is known to have almost zero carbon solubility. This method guarantees a high monolayer rate. Nevertheless, due to the absence of the segregation mechanism, it has to rely on the penetration of the carbon precursor to the Cu-insulator interface via the gradual diffusion through the Cu grain boundaries. We have found that, at least under our condition, this diffusion is very difficult and we cannot reproduce the result in Ref. 18. In fact, for the two methods mentioned earlier, no matter using Cu or Ni, graphene is eventually grown at the metal-insulator interface. Based on the growth mechanism, it is known that the graphene contacts more tightly to the metal than the insulator. Therefore, after etching away the metals, the graphene is prone to breaking and becomes discontinuous. Indeed, this phenomenon has been observed in our experiments (see Fig. S1 of the supplementary material).

Consequently, we find the technique that removes metals by evaporation more promising. Ismach *et al.*[19] report that after growing graphene on Cu thin films on an insulator, the Cu can be *in situ* evaporated and the graphene "lands on" the insulator beneath. In this letter, we have systematically developed this method. Unlike Ref. 19 where the Cu film is deposited by evaporation, we use sputtering to produce the Cu. In sputtering, the size of metal particles (domains) in the film can be well controlled by the power, which is an advantage for the subsequent graphene deposition, as we will elaborate later. The Cu film thickness is ~60 nm, considerably thinner than the previously reported values (several hundred nm). Apart from saving Cu, the most obvious benefit is the dramatical reduction in the overall process time and the finer feature size during the patterning. Reference 19 reports that the Cu thickness has to be ≥450 nm to ensure its integrity before ramping to the graphene deposition temperature, so that the grown graphene can be continuous. In our experiment, by virtue of our extremely fast heating rate (~200 °C/min) and growth rate, even though Cu is as thin as 60 nm, a large area continuous graphene film can be guaranteed. Through the pre-patterning of the Cu catalyst by standard photolithography, we can easily obtain transfer-free patterned graphene with feature size of a few μm (thanks to the small thickness of the Cu film) without polymeric contamination. The growth mechanism is analyzed in detail, and the graphene room temperature properties are characterized via graphene field-effect transistors (FETs) fabricated therein. We also demonstrate that it is a facile technique toward future all-carbon electronics.

As shown in Fig. 1, Cu thin films are deposited by sputtering onto a heavily doped Si substrate with 300 nm SiO_2 layer. Our optimal sputtering power is 400 W, and the sputtering time is 130 s. The equipment for graphene growth is the Aixtron Black Magic nanocarbon CVD system, which is a vertical and cold-wall system allowing fast heating, cooling, and growth rates. The $Cu/SiO_2/Si$ samples are loaded to a local heater which is heated to 600 °C, undergoing a H_2 annealing (1000 SCCM) for 10 min, followed by the fast ramping to the growth temperature of 960 °C at ~200 °C/min. The growth atmosphere is a mixture of CH_4 (30 SCCM) and H_2 (20 SCCM) at 6 mbar chamber pressure. The deposition time is as short as 10 min. Immediately after the graphene growth, the machine is quench cooled down (>200 °C/min). Most of the Cu catalyst is vaporized during the

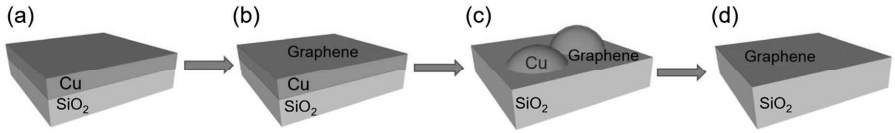

FIG. 1. Schematic illustration of our process of growing transfer-free graphene directly on the SiO_2 substrate via sputtered sacrificial Cu film. The Cu can also be pre-patterned by photolithography to avoid the direct patterning of graphene with photoresist. (a) Cu sputtering (typically 60 nm). (b) Graphene growth by CVD on Cu catalyst. (c) High temperature induced Cu evaporation. Some Cu will be aggregating and balling as well. (d) The remaining graphene is lying on the SiO_2 substrate.

graphene CVD, as shown in Fig. 1(c). The remaining Cu residual particles are gently removed by $FeCl_3$ solution. Figure 2(a) shows an optical image of the graphene sitting on SiO_2 after the process shown in Fig. 1. In the right part of the image, there is an intentionally made tweezer scratch to generate some contrast. Apparently, a macroscopically continuous and large area graphene film has been deposited successfully. For field-effect transistor fabrication, first, the source and drain electrodes are prepared either by lift-off photolithography of Pt/Ti (100 nm and 15 nm) or by photolithography and O_2 plasma etching of CVD graphite. In the latter case, the graphite is deposited using our previous recipe.[22] Then, the Cu thin films are prepared by lift-off photolithography and sputtering as described earlier. The shape of the graphene channel is thereby defined by pre-patterned Cu. The transistors are measured by a standard probe station at room temperature in an open ambient condition without any special treatment such as vacuum annealing or current annealing.

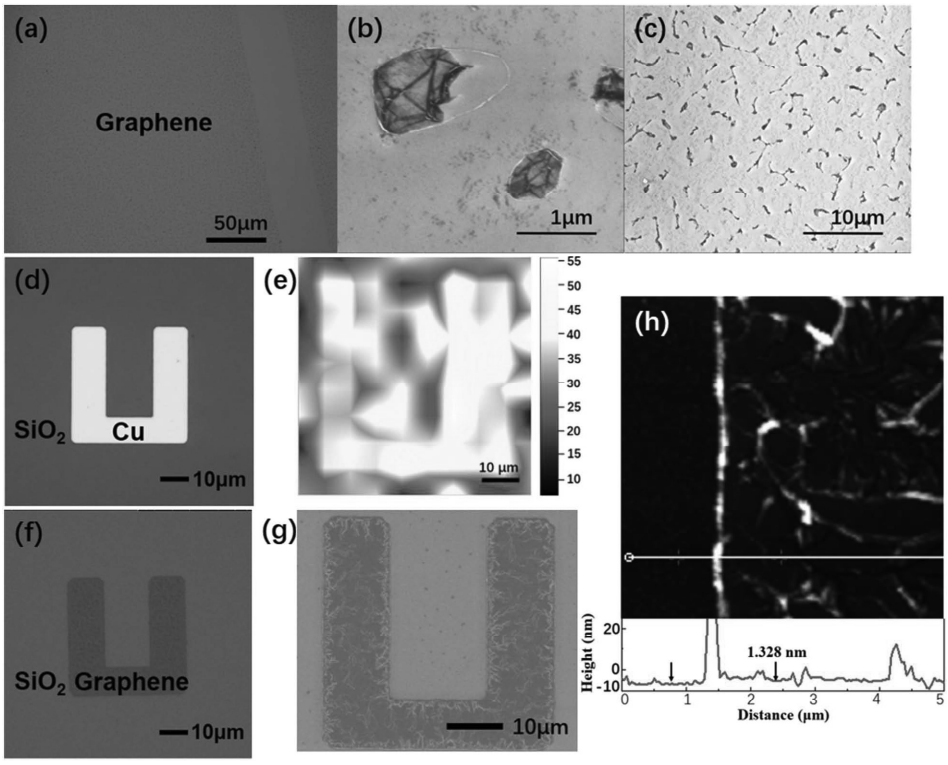

FIG. 2. (a) Optical and [(b) and (c)] SEM images of the as-grown graphene after etching away the residual Cu particles by $FeCl_3$. In (a), a scratch from the tweezer is seen, generating some optical contrast. The darker areas in (b) and (c) are graphene flakes originally grown on the Cu particles landed on the surface as a result of removing the Cu particles. (d) and (f) are optical images of the patterned sample after the depositions of (d) Cu and (f) graphene. (e) is the Raman mapping of the G peak of the patterned graphene. (g) is the SEM image of the patterned graphene. The dark dots around the graphene in (g) should be the graphene nucleus grown by the catalysis of copper vapor. (h) AFM image of the as-grown graphene over 5 μm × 5 μm area. The height profile is measured along the white line in (h). The height difference between the two points indicated by the arrows is 1.328 nm.

The growth mechanism can be explained as follows. By the end of the 10 min high temperature process at 960 °C, most of the sputtered Cu is evaporated (more rigorously, it should be called sublimation since the temperature is still slight lower than the Cu melting point). However, it is worth noting that in our machine, in contrast with traditional tube furnace type graphene CVD systems, the graphene growth speed is very fast. Full coverage of 1 in. Cu can be obtained within few minutes (see our previous publications).[10] Therefore, it is reasonable to postulate that when the Cu evaporation takes place, most of the graphene growth is already completed, as shown in Fig. 1(b). During the high temperature process, the Cu will aggregate (balling effect), as shown in Fig. 1(c). Due to the existence of the graphene "quilt," small amount of Cu particles will be kept on SiO_2. One could imagine that while the Cu film balling effect happens, the graphene that is already grown atop will have some tears, which facilitates the Cu evaporation. At the same time, the newly exposed Cu surface will be soon covered by the CVD grown graphene. Therefore, the Cu evaporation and graphene growth are two somewhat competing processes simultaneously occurring in the chamber. Figures 2(b) and 2(c) are the scanning electron microscopy (SEM) images of the graphene (Cu residues already etched). The atomic force microscopy (AFM) image is shown in Fig. 2(h). The thickness of the graphene measured along the white line is 1.328 nm and the average roughness of the substrate is Ra = 1.31 nm. For a perfect graphene lattice, the only known particles that can permeate it are protons.[20] However, in practice, during the processes described earlier in the chamber, the graphene is never perfect. Hence, the Cu residue particles, although covered by the graphene, can still be etched by $FeCl_3$. That is why we see no Cu particles in Figs. 2(b) and 2(c). X-ray photoemission spectroscopy (XPS) is a chemically sensitive technique that better enables the overall element content. Figure S2 (supplementary material) shows the XPS analysis for Fe, C, O, Cu and Si elements in the as-grown graphene. Silicon contamination was not found; however, we see the presence of Fe and Cu on the surface of the sample. The Fe element should come from the residual of etchant, and the copper element may come from the residual of the etchant or the copper contamination caused by the growth process. After the Cu residues are removed, the graphene on them will be quasi free-standing, resulting in the graphene flakes/particles seen in Figs. 2(b) and 2(c). We have observed that the shape of these graphene flakes roughly follows that of the Cu particles before chemical etching, which confirms our explanation. Ismach *et al.*[19] argue that when the Cu thickness is ≤450 nm, no continuous graphene can be achieved as the Cu is already massively evaporated or disintegrated. Nevertheless, we have shown that macroscopically continuous graphene can be attained even if the Cu is as thin as 60 nm. This can be explained by our very high graphene growth rate, as well as our quick heating up strategy, which allows the continuous graphene to be largely completed before the massive evaporation and balling take place.

In Ref. 18, a different mechanism is used to grow graphene directly on insulators. That is, the carbon precursor can penetrate the 300 nm Cu film and reach the Cu-insulator interface to form graphene via high temperature diffusion through the Cu grain boundaries. However, we have not managed to reproduce this result under our condition. We sputter 300 nm Cu on SiO_2 and tune the growth condition such that the Cu integrity is kept even after the graphene growth. After etching off Cu, we detect almost no graphene on SiO_2. Therefore, we believe the penetration growth is absent or plays a minor role in our experiments.

Figure 3(a) is a typical Raman spectrum of the as-grown graphene (λ = 532 nm). The G and 2D peaks confirm the graphitic structure. From the D peak height, it can be concluded that there are a number of defects in the graphene, which is a direct result of the tears and other structural defects during the Cu evaporation and balling. We notice that there is a peak next to the G peak in the Raman spectrum, which may be due to defects in graphene, leading to a strong D′ peak (1620 cm^{-1}). D′ peak is mainly caused by intravalley defect-induced resonant scattering, while D peak represents intervalley defect-induced resonant scattering.[21] The full width at half maximum of the 2D peak is typically ~50 cm^{-1}, suggesting that the film is most likely a monolayer with disorders.[21] Figures 3(b) and 3(c) are the Raman mapping data of the sample measured in a 24 μm × 24 μm area, where D/G and G/2D ratios are plotted. The graphene is seen to be relatively uniform.

As mentioned in the Introduction, we use sputtering because of its better controllability. Figures 4(a)–4(d) are the surface morphologies of the 60 nm Cu thin films sputtered at different

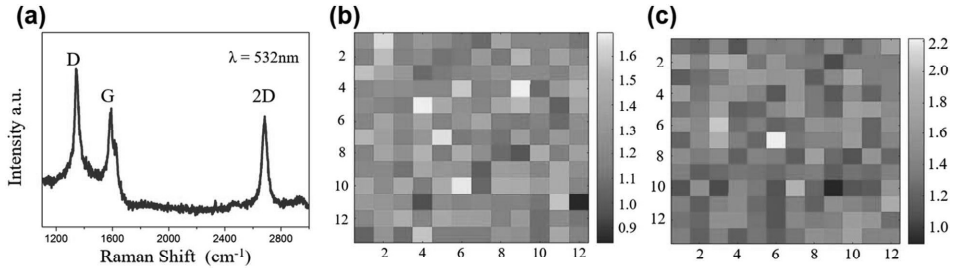

FIG. 3. (a) Typical Raman spectrum of the graphene grown by CVD with 60 nm sputtered sacrificed Cu film. (b) and (c) are Raman mapping of the D/G and G/2D ratios of the graphene over 24 μm × 24 μm area, respectively. The graphene is relatively uniform, but also has a number of defects as a result of the high temperature Cu evaporation and balling.

powers (50 W, 150 W, 300 W, and 400 W) after 10 min of graphene deposition. Clearly, with increasing power, the average size of the Cu particles produced by the high temperature balling effect increases as well. At smaller power, the particles are smaller but denser. From the work mechanism of magnetron sputtering, we learn that at higher power the argon ions have higher kinetic energies. Consequently, the size for the Cu particles ejected from the target is larger, resulting in the larger size of the Cu particles after the graphene CVD. The graphene defects mainly appear at the Cu aggregation area. Therefore, at smaller sputtering power, the graphene is more defective because the Cu particles are denser, although they are smaller. On the other hand, at larger power most graphene areas are reasonably good because the defects are concentrated and limited to fewer spots of Cu particles. The dependence of the graphene quality on the sputtering power is confirmed by Raman measurements [see Fig. 4(e)]. Meanwhile, we should point out that when the sputtering power is lower, not only the average size of Cu particles is reduced but also the Cu film will be easier to ball. As a result, the Cu film may ball even before the graphene growth, which will cause graphene to be discontinuous. We also find that the Cu film thickness needs to be optimized in order to achieve the best result (Fig. S4 of the supplementary material). If it is too thick, it takes more efforts to evaporate Cu. The lengthy evaporation induces more damages to the graphene.[19] On the other hand, if it is too thin, the Cu particles from the balling are small but also very dense, leading to more damaged areas in the graphene. Indeed, as depicted in Fig. 4(f), when Cu is 10 nm thin, the graphene is nonuniform with a large density of graphene flakes from the Cu particles. Note the scale bar in Fig. 4(f) is different from those in Figs. 4(a)–4(d). Figure 4(g) is the corresponding Raman signal, also implying its low quality (the 2D peak is almost missing). The Raman mapping of the graphene grown on the 10 nm Cu thin film is shown in Fig. S3 of the supplementary material. In the end, 60 nm is identified as the optimal condition in our experiments.

One of the major advantages of our technique is that Cu can be pre-patterned without contaminating the graphene by photoresist. Also, since our Cu is only 60 nm thin, a high precision in the patterning can be obtained. Figures 2(d) and 2(f) show the optical micrograph of the Cu pattern and the corresponding graphene pattern after the process, respectively. The two patterns are seen to be totally identical with micron precision. A control experiment has been carried out on the 300 nm Cu thin film, and we have not got as good precision, indicating that the Cu thickness is very crucial. Figure 2(e) is the Raman mapping data of the patterned graphene measured in a 75 μm × 75 μm area, where the G peak is plotted. We can see the G peak signal of the patterned graphene, and we have also observed the presence of the G peak signal around the patterned graphene. Figure 2(g) is the SEM image of the patterned graphene. We can see small, darker color dots around the patterned graphene in the picture, which are graphene nucleus. This phenomenon may be due to the catalysis of copper vapor, and the direct growth of graphene by copper vapor assist had been reported before.[23] Graphene FETs are fabricated using our direct growth technology. The Pt/Ti (we opt to use Pt/Ti due to its high melting point and stability during the graphene CVD) source and drain electrodes are prepared before the lithographical patterning of the 60 nm Cu catalyst, as shown in Fig. 5(a). We carry out these pre-patterning of Pt/Ti and Cu because we would like to isolate graphene from any photolithography process. After Pt/Ti and Cu are patterned, the graphene is grown using the above-mentioned method, and the graphene shape is defined by Cu. We note that Pt is also a good catalyst

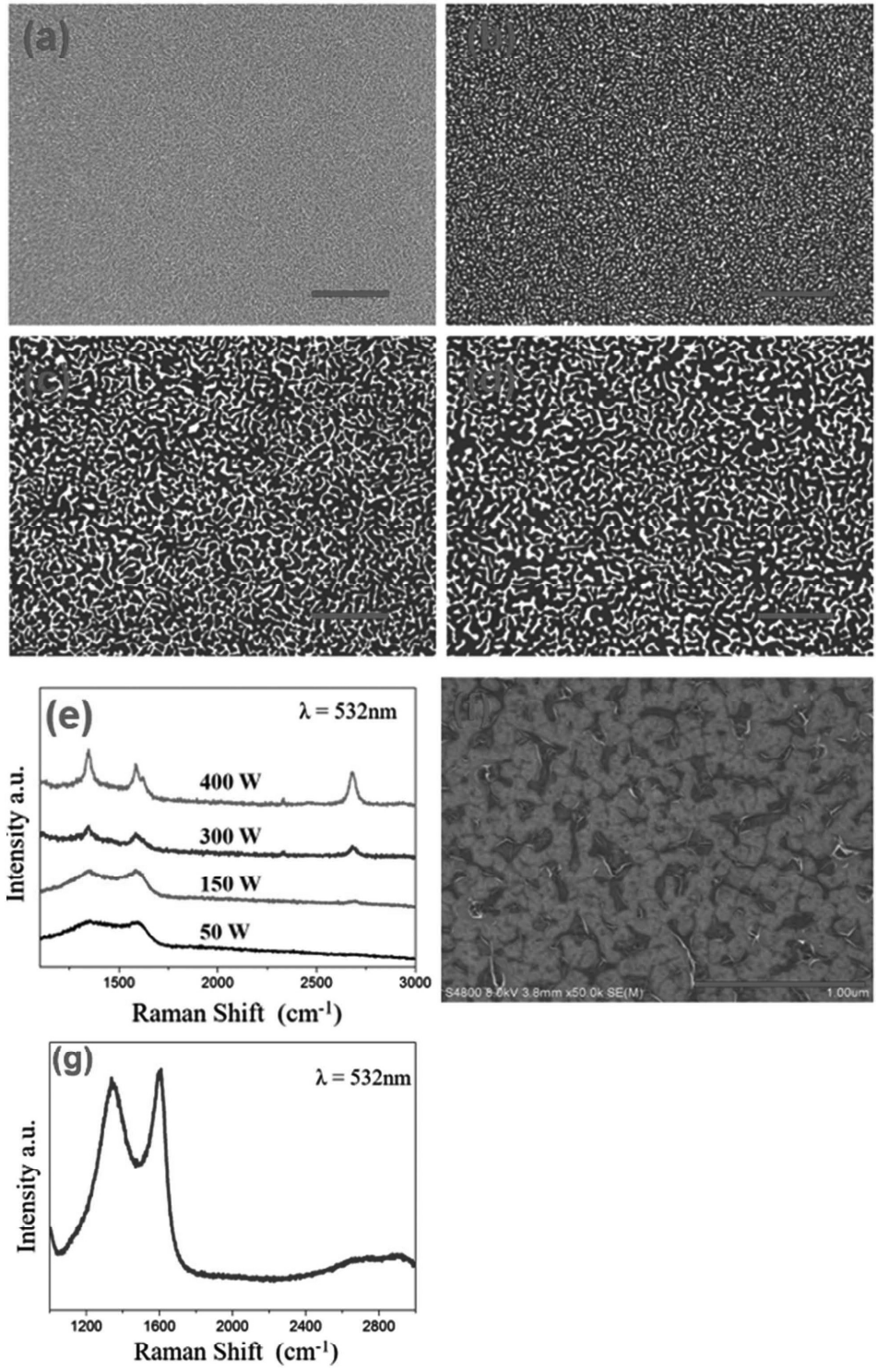

FIG. 4. Optical images of the Cu thin films sputtered at different powers after the graphene growth. The sputtering powers are (a) 50 W, (b) 150 W, (c) 300 W, and (d) 400 W, respectively, and the scale bar is 25 μm for (a)–(d). (e) Typical Raman spectrum of the graphene grown on the Cu thin films sputtered at different powers. (f) SEM micrograph of the graphene grown with 10 nm Cu after $FeCl_3$ etching. The graphene is nonuniform (color inconsistency) with a large density of graphene flakes. The scale bar is 1 μm. (g) Typical Raman spectrum of the graphene shown in (f).

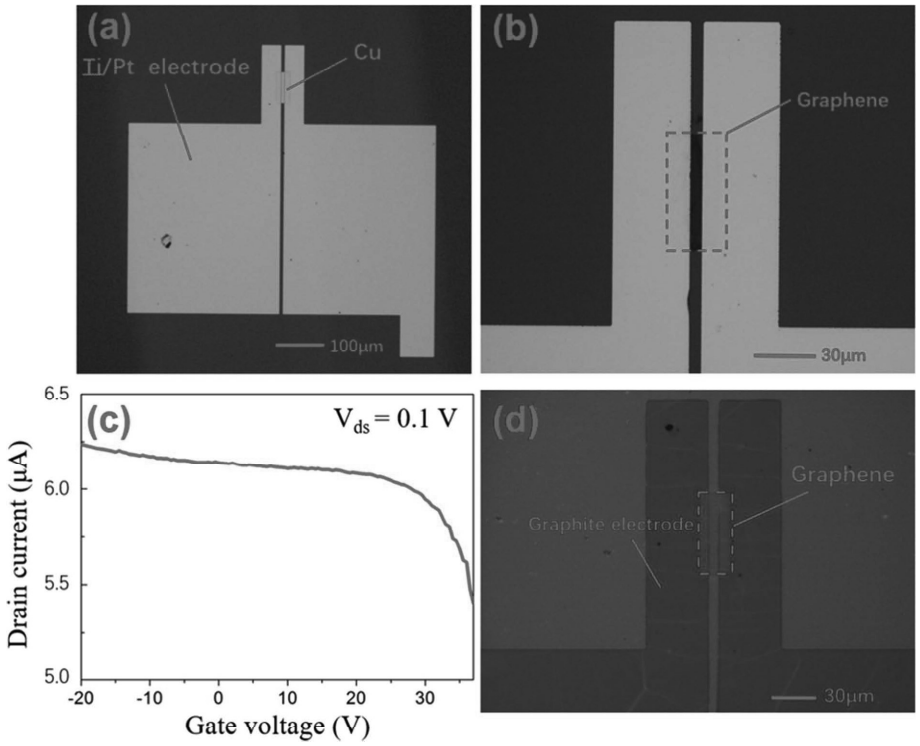

FIG. 5. (a) and (b) are optical images of the field-effect transistor made in the as-grown graphene. The aspect ratio of the graphene channel is 1:9, with the channel length being 7 μm. (a) and (b) are micrographs taken before and after the graphene growth, respectively. (c) Transfer properties of the graphene FET shown in (a) and (b). (d) Optical image of another graphene FET with CVD graphite source drain electrodes (all-carbon electronic device).

for the graphene CVD. Therefore, the graphene grown on Cu is well connected with the graphene on Pt, ensuring a good electrical contact between the source and drain electrodes and the graphene channel. This is confirmed by the electrical measurements. Figure 5(c) is the transfer property of the graphene FET shown in Figs. 5(a) and 5(b) measured at room temperature in open air without $FeCl_3$ etching and special treatment such as vacuum annealing. The graphene is unfortunately heavily p-doped. The reason for the p-doping is unclear at this stage but very likely due to the SiO_2 substrate induced charge transfer. We note that unlike the standard process of transferring graphene to SiO_2 at room temperature, here in the direct growth method the graphene-SiO_2 interaction is much more enhanced due to the high temperature process. This effect is suggested by previous report[18] as well as confirmed by our own studies.[14,22] The field-effect mobility of the graphene can be roughly estimated by $\mu = (L/WC_{ox}V_d)(\Delta I_d/\Delta V_g)$, where L and W are the channel length and width, C_{ox} is the gate capacitance, and V_d, I_d, and V_g the source-drain voltage, channel current, and gate voltage, respectively. The mobility is calculated to be not more than 27 $cm^2/(V\,s)$, which is much lower than expected. Apart from the influence from the Cu particle induced defects in the CVD graphene, the most dominant reason accounting for the low mobility is the charge scatterers from the SiO_2 substrate. If that mechanism can be confirmed by further studies, the severe doping and low mobility issue is not entirely intrinsic and could be improved by selecting other substrates (e.g., h-BN) that are more benign to graphene after high temperature process. Finally, in order to demonstrate the all-carbon electronics concept, we have also fabricated graphene FETs with graphite source drain electrodes, as shown in Fig. 5(d). The graphite electrodes are tens of nm thick and grown by CVD with our previously reported recipe,[22] which is patterned by O_2 plasma etching. The graphitic electrodes can survive extremely high temperature, have similar work function as the graphene, and are more economic and environment-friendly.

In conclusion, we have systematically developed a transfer-free, lithography-free process of forming large area continuous graphene directly on SiO_2/Si substrates. Sputtered Cu thin films are

used as the sacrificing catalysts during the graphene CVD. By virtue of our fast heating and deposition rates in the graphene CVD, the graphene growth is largely completed before the Cu evaporation and balling takes place. The sputtering power is altered and correlated to the final results. 60 nm is determined to be the optimal thickness of Cu. The Cu can be patterned beforehand and, therefore, the graphene is patterned without lithography and free from photoresist residues. Nevertheless, the Cu evaporation and balling does introduce a number of defects in the graphene and leave Cu residual particles therein, although it can be removed by $FeCl_3$. Due to the small thickness of Cu thin films, we have attained a precision of a few μm in the graphene patterning without transfer and lithography of the graphene. FETs with high melting point metal or graphite electrodes are fabricated in the graphene and severe p-doping and degradation of mobility are observed, which are attributed to the defects mentioned earlier, as well as the high temperature enhanced influence from the SiO_2/Si substrates. Further studies are required to understand and control the method in greater detail and explore its full potential.

See supplementary material for the optical images of the graphene directly grown on SiO_2 substrates by carbon diffusion through the Ni thin film, the XPS data of the sample, the Raman mapping of the graphene grown on 10 nm Cu, and the result of as-grown graphene on Cu thin films with different thicknesses.

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