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We report on the electrical properties of Al_2O_3 films grown on 4H-SiC by successive thermal oxidation of thin Al layers at low temperatures (200°C - 300°C). MOS capacitors made using these films contain lower density of interface traps, are more immune to electron injection and exhibit higher breakdown field (5MV/cm) than Al_2O_3 films grown by atomic layer deposition (ALD) or rapid thermal processing (RTP). Furthermore, the interface state density is significantly lower than in MOS capacitors with nitrided thermal silicon dioxide, grown in N_2O, serving as the gate dielectric. Deposition of an additional SiO_2 film on the top of the Al_2O_3 layer increases the breakdown voltage of the MOS capacitors while maintaining low density of interface traps. We examine the origin of negative charges frequently encountered in Al_2O_3 films grown on SiC and find that these charges consist of trapped electrons which can be released from the Al_2O_3 layer by depletion bias stress and ultraviolet light exposure. This electron trapping needs to be reduced if Al_2O_3 is to be used as a gate dielectric in SiC MOS technology. https://doi.org/10.1063/1.5021411

I. INTRODUCTION

4H-SiC metal-oxide semiconductor field-effect transistors (MOSFETs) are promising devices for power electronics. Such transistors are now commercially available for blocking voltages above 900 V.[1,2] These devices provide higher switching speeds and lower switching losses than Si MOSFETs. However, SiC MOSFETs cannot compete with Si technology for lower blocking voltages because of poor electron channel mobility which limits the device on-resistance. A key problem is the high density of so called near-interface traps (NITs) detected at the SiO_2/4H-SiC interface with energy levels near the SiC conduction band edge that limit the electron channel mobility.[3–6] Currently thermal oxides grown or annealed in NO or N_2O are the mainstream dielectrics but more reduction in NITs is needed.[7] Other large bandgap dielectrics such as AlN, Al_2O_3 and HfO_2 have also been investigated.[8–14] One of the alternatives is aluminum oxide (Al_2O_3) with bandgap of ~ 7.0 eV.[8,11,15] Recently, an amorphous Al_2O_3 has been used as a gate dielectric in graphene field effect transistors with some success.[16,17] Those Al_2O_3 films are grown by atomic layer deposition (ALD) at 300°C or thermal evaporation of metallic Al followed by low temperature oxidation to form Al_2O_3.[16,17] As grown Al_2O_3 deposited on 4H-SiC by ALD typically contains a large number of negative charges which are reduced after annealing in Ar at 1000°C but the Al_2O_3/SiC interface contains a high density of interface traps after such treatment.[9,10] More recently, studies on pre-deposition surface cleaning and post deposition annealing at different temperature in N_2O ambient are been performed on ALD

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grown Al_2O_3. A high density of negative charge is observed in such samples and after post deposition annealing at 1000°C, an interfacial SiO_x ($0 < x < 2$) layer grows containing a high density of interface traps.[18] There is a report on a very high peak field effect mobility of 300 cm^2/Vs in SiC MOSFETs using Al_2O_3 made by metal-organic chemical vapor deposition (MOCVD) with a thin SiO_2 interfacial layer to the SiC.[13] But, the mobility drops very rapidly with gate voltage and is less than 50 cm^2/Vs at moderate gate voltages. Recently, a MOSFET with ALD grown Al_2O_3, post-annealed in hydrogen ambient at 400°C, was reported with a field effect mobility of 57 cm^2/Vs. Even though these results are promising the Al_2O_3 layers were sensitive to electron injection resulting in large threshold voltage shifts of the MOSFETs.[19] In previous studies, a careful attention has not been paid to the origin of negative charges within the Al_2O_3 which normally are assumed to be a fixed oxide charge. In this work, we studied the interface quality of differently prepared Al_2O_3/4H-SiC interfaces, the breakdown properties of the Al_2O_3 dielectrics as well as the origin of negative charges within the Al_2O_3. Recently, we reported a very low density of NITs in Al_2O_3 layers formed on 4H-SiC by thermal oxidation of Al.[20] In this work, we investigate these layers in more detail and compare them with Al_2O_3 layers grown by ALD or RTP and with SiO_2/Al_2O_3 stack structure. We find that is it possible to grow Al_2O_3 films with negligible negative charge and very low density of interface states at the Al_2O_3/4H-SiC interface.

II. EXPERIMENTAL METHODS

The SiC samples used in this study consist of 10 μm thick n-type epitaxial layers, with a net doping concentration of ~ $1x10^{16}$ cm^{-3}, grown on 4 degrees off-axis (0001) 4H-SiC substrates. The Al_2O_3 layers are grown on the 4H-SiC substrates by different deposition methods. Prior to deposition all samples were rinsed in 2% HF for 1 min followed by rinse in deionized water and blown dry in nitrogen in order to remove the native oxide. In one of the deposition methods, a 1-2 nm thick Al metal layer is deposited by electron beam evaporation of Al in a vacuum chamber at a rate of 0.5 Å/s and then immediately the sample is baked on a hot plate in room environment at a temperature of 200°C for 5 minutes to form Al_2O_3 layer.[16,17,21] This process of deposition and subsequent oxidation is repeated twelve times to get target thickness of ~ 15 nm with an overall time span of about 4 hours. We refer to this method as hot plate Al_2O_3. A hot plate Al_2O_3 sample was grown at 300°C as well and we found no difference in the electrical properties of these samples. A stack of SiO_2/Al_2O_3 was made by growing a thick layer of 40 nm of SiO_2 on the top of the hot plate Al_2O_3 by plasma enhanced chemical vapor deposition (PECVD) at 300°C using source gases of oxygen and silane. An Al_2O_3 layer of 15 nm thickness was also grown by ALD at 300°C via thermal decomposition of $Al_2(CH_3)_6$ in water ambient. In addition, Al_2O_3 films were made by using rapid thermal processing (RTP). The RTP Al_2O_3 samples were prepared by evaporation of Al metal followed by rapid thermal oxidation in pure oxygen ambient. 6 nm of Al was deposited onto four separate SiC samples and subsequently oxidized at 500°C, 600°C, 700°C, and 1000°C for 30 min, 30 min, 15 min, and 5 min respectively. The Al deposition and oxidation cycle was repeated twice to achieve a target film thickness of 15 nm. Apart from the sample made at 1000°C, the resulting oxides were too leaky for CV characterization. The oxide thickness of all samples was estimated using X-ray reflectivity (XRR) and the crystallinity was investigated with X-ray diffraction (XRD) apart from the RTP grown samples. Our Al_2O_3 films in this study are amorphous with no crystallization observed by XRD. The chemical composition of the films has not been verified here experimentally but previous studies using similar growth methods reveal the formation of amorphous Al_2O_3.[22] Reference samples with 20 nm thick thermal SiO_2 grown in dry oxygen (at 1150°C for 90 min) as well as 37 nm thick thermal SiO_2 grown in N_2O (1240°C for 90 min) were also analyzed. The Al_2O_3 samples are summarized in Table I below.

Circular n-type MOS capacitors were made using Al as a gate metal. The backside contact was formed by thick Ni (100nm) metallization. The capacitance- and current-voltage measurements (CV and IV) are performed on circular MOS pads, with diameter of 300 μm and 100 μm, using Agilent E4980A LCR meter and Keithley 617 electrometer respectively. To estimate the interface quality of Al_2O_3/SiC interface, conventional CV measurements are performed at room temperature and at different frequencies ranging from 1 kHz to 1 MHz, while to examine the negative charges within the Al_2O_3, room temperature CV measurements are made using UV light illumination. IV measurements

TABLE I. Summary of Al_2O_3 MOS samples used in this study.

No.	MOS structures	Thickness of oxide	Method of oxide deposition
1	$Al/Al_2O_3/SiC$	~15 nm	Hot plate at 200°C
2	$Al/SiO_2/Al_2O_3/SiC$	~40 nm/15 nm	SiO_2 by PECVD at 300°C/Al_2O_3 by hot plate at 200°C
3	$Al/Al_2O_3/SiC$	~15 nm	ALD at 300°C
4	$Al/Al_2O_3/SiC$	~15 nm	RTP at 1000°C for 5 min

are used to examine the leakage current characteristics, the critical breakdown field and the tunneling barrier height of the dielectric Al_2O_3.

III. RESULTS AND DISCUSSION

Figure 1 shows CV spectra of aluminum oxide MOS capacitors measured at room temperature and at 1 kHz and 1 MHz frequencies. The gate bias is swept from depletion (negative bias) to accumulation (positive bias) and the capacitance signal for both frequencies is recorded simultaneously at each gate bias point. Figure 1(a) shows the CV curves for a hot plate Al_2O_3 sample. The dielectric constant deduced from the capacitance in accumulation (5 V) is about 6.5. A first estimate of the interface trap density is extracted from frequency dispersion of CV curves.[23] In this case, such dispersion is hardly visible indicating a rather low interface state density. Figure 1(b) shows the CV spectra of the SiO_2/hot plate Al_2O_3 dielectric stack. Small frequency dispersion is observed indicating some increase in the interface state density. Figure 1(c) shows the CV spectra for ALD grown Al_2O_3. Two noticeable features are observed in the low frequency (1 kHz) CV curve. A "hump" at ~ 0 V suggests the presence of specific rather deep interface traps that are not able to follow the 1 MHz test signal. Secondly the capacitance in accumulation is higher than the 1MHz curve and this is due to current leakage through the oxide which distorts the 1 kHz measurement. Figure 1(d) shows the CV

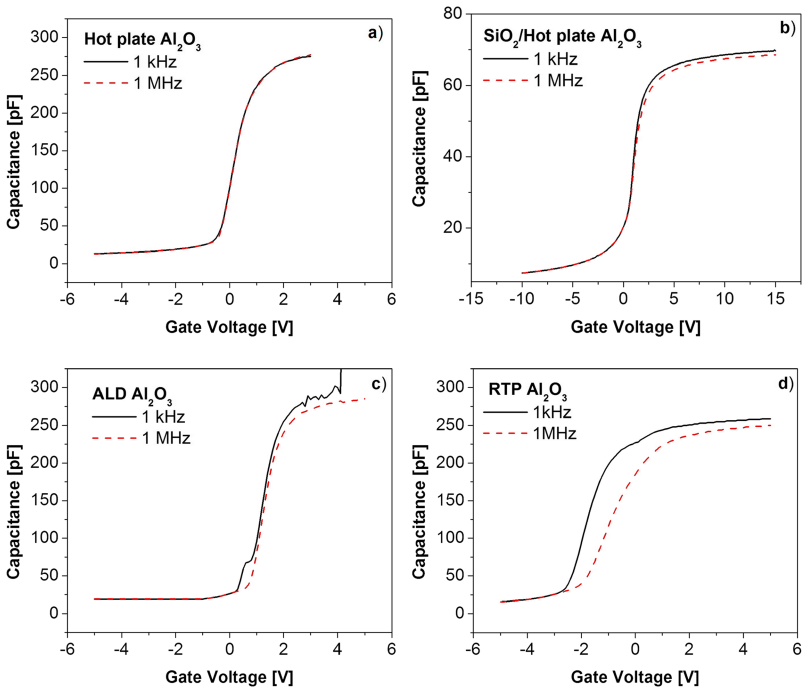

FIG. 1. CV curves at room temperature of: (a) a hot-plate Al_2O_3 MOS capacitor (b) a dielectric stack of SiO_2/hot plate Al_2O_3 (c) ALD grown Al_2O_3 and (d) RTP grown Al_2O_3.

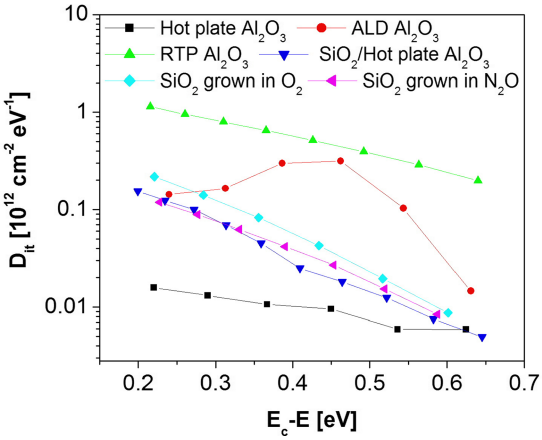

FIG. 2. Density of interface states (D_{it}) as a function of energy from the SiC conduction band edge, extracted from CV analysis at room temperatures for the sole and stack Al_2O_3 dielectric samples grown by different methods and samples with thermal SiO_2 grown in O_2 or N_2O ambient.

spectra for the RTP grown Al_2O_3. A very large frequency dispersion reveals high density of interface states.

Figure 2 compares the interface state density in the different Al_2O_3 samples extracted from frequency dispersion of room temperature CV data (between 1kHz and 1 MHz) together with data from reference samples with thermal SiO_2 made in dry oxygen or N_2O ambient. It is evident in figure 2 that the hot plate Al_2O_3 sample contains the lowest density of interface traps. The interface state density in the Al_2O_3 stack sample is comparable with nitrided reference SiO_2 sample but is lower than in reference SiO_2 grown in O_2. The ALD grown Al_2O_3 shows a peak in the interface state density at energies between 0.35-0.55 eV from the SiC conduction band edge. RTP grown Al_2O_3 has relatively high density of interface traps.

The MOS capacitors were investigated by IV as well at room temperature. Leakage current density vs electric field (J-E) curves for several different samples are shown in figure 3(a). The sole hot plate Al_2O_3 has breakdown field (~ 5 MV/cm) which is higher than the ALD and RTP grown Al_2O_3 films. This value of the breakdown field is about half the breakdown field achieved in the reference SiO_2/SiC MOS capacitor (light blue dash dot dot curve in figure 3(a). Reported breakdown field of Al_2O_3 on SiC varies in literature and the highest value, to our knowledge, is approximately 8 MV/cm in amorphous ALD grown films.[11] However, in that study the leakage current density prior to breakdown was of the order of 10^{-3} A/cm^2 which is few orders of magnitudes higher than in the hot-plate grown Al_2O_3. In case of the SiO_2/Al_2O_3 stack (dark blue dash dot curve in figure 3a), the effective breakdown field, $E_{eff} = \frac{V_G - V_{FB}}{t_{ox,total}}$ treating the dual dielectric as a single dielectric, is

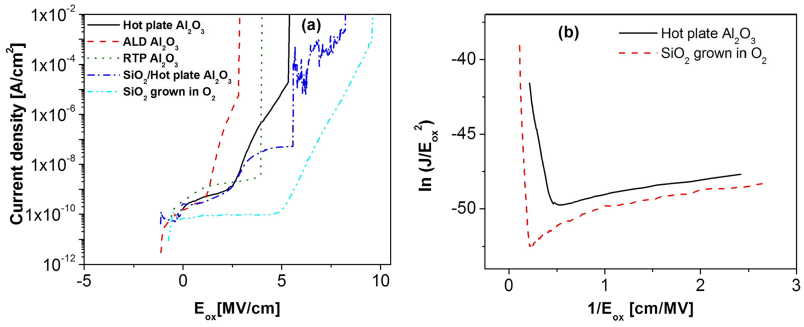

FIG. 3. (a) Comparison of leakage current density vs electric field across the oxide (J-E) of differently prepared Al_2O_3 along with a reference sample with thermal SiO_2 grown in O_2, (b) A Fowler-Nordheim plot for hot plate grown Al_2O_3 and for dry SiO_2.

~ 8 MV/cm. Here V_G, V_{FB} and $t_{ox,total}$ are the gate voltage, flatband voltage and the thickness of the dielectric stack respectively. A steep increase in the current is observed around 5 MV/cm but before that the leakage current value is relative low around 10^{-8} A/cm. The breakdown field across the Al_2O_3 dielectric can be determined by considering the difference of the dielectric constants in the stack using the expression:[24]

$$E_{Al2O3} = \frac{V_G - V_{FB}}{t_{Al2O3}} \times \frac{C_{ox,SiO2}}{C_{ox,SiO2} + C_{ox,Al2O3}} \tag{1}$$

Here t_{Al2O3} denotes the thickness of Al_2O_3. $C_{ox,SiO2}$ and $C_{ox,Al2O3}$ are the calculated capacitances of SiO_2 and Al_2O_3 respectively by taking into account the corresponding dielectric constant and thickness of the dielectric. This expression gives the breakdown field value of ~ 5.5 MV/cm across the Al_2O_3 dielectric in the stack. This indicates that the addition of SiO_2 layer on top of the hot plate Al_2O_3 has not much impact on the breakdown field of Al_2O_3 but the benefit of stack dielectric MOS capacitor is that it can operate at higher gate voltages.

Significant Fowler-Nordheim (F-N) tunneling is seen in the J-E profile of the sole hot plate Al_2O_3 and reference dry SiO_2 MOS sample. Therefore, the J-E response of these MOS sample was analyzed further using F-N tunneling mechanism to determine the tunneling barrier height. F-N tunneling current density across MOS devices at high field is described by:[25]

$$J = AE^2 \exp\left(\frac{-B}{E}\right) \tag{2}$$

Where, $A = \frac{q^3 m}{8\pi h m_{ox} \phi_b}$ and $B = \frac{8\pi\sqrt{2m_{0x}}\phi_b^{\frac{3}{2}}}{3hq}$. The parameters A and B depend on the tunneling barrier height ϕ_b and the effective mass of the tunneling electron m_{ox} in the oxide. A and B, can be derived from the experimental IV characteristics plotted as *ln (J/E^2) vs. 1/E*, a so-called F-N plot. The slope of the straight line at high electric fields gives B while A is determined from the intercept. Since B is the exponent in equation (2) for F-N tunneling current density, it is the prominent parameter in determining the current flow in the gate oxide.[25]

Figure 3(b) shows F-N plot for a hot plate grown Al_2O_3 and for a reference dry SiO_2. The value of parameter B is 38 MV/cm and 175 MV/cm for Al_2O_3 grown by hot plate and for reference dry SiO_2 respectively. The effective barrier height for the hot plate grown Al_2O_3/4H-SiC interface extracted from this analysis is 1.15 eV by taking effective electron mass in Al_2O_3 to be $0.2m_o$ where m_o is the free electron mass.[11] A SiO_2/4H-SiC barrier height of 2.50 eV is obtained by assuming m_{ox} in SiO_2 is $0.42m_o$.[26] This barrier height of the reference SiO_2/4H-SiC MOS sample is reasonably close to the previously reported values for dry SiO_2 determined by F-N tunneling mechanism.[26] The highest barrier height in literature for amorphous ALD grown Al_2O_3/4H-SiC, determined by F-N tunneling mechanism, is 1.58 eV as compared to 1.15 eV in our hot-plate.[11] This indicates that the hot plate Al_2O_3/4H-SiC interface has some defect states that limit the oxide breakdown field.

The Al_2O_3 samples are all found to be sensitive to electron injection except the RTP grown Al_2O_3. RTP grown Al_2O_3 may have a thin interface layer of SiO_2 that forms during the high temperature treatment as reported in literature.[9,10,18] The electron injection is observed by a shift of the CV curve after applying accumulation bias. Figure 4 shows such examples for hot plate and ALD grown Al_2O_3 samples. Repeated sweeps from depletion to accumulation result in a positive flatband voltage shift which saturates after several sweeps. This saturation has not been observed in the SiO_2/hot plate Al_2O_3 stack. The magnitude of the shift depends on the maximum accumulation voltage (in this case 5 V) and is larger in the ALD grown Al_2O_3. It is evident that electrons are trapped in the dielectric under accumulation bias and do not return to the SiC when the samples are biased in depletion. The electron charge trapped in the hot plate Al_2O_3 is approximately 3.4×10^{12} cm^{-2} and ~ 5.0×10^{12} cm^{-2} in the ALD Al_2O_3. This is significantly lower than previously reported in as grown ALD films where the densities are typically in the $1x10^{13}$ cm^{-2} range or higher.[9–11]

We examined the existence of electron capture and emission from traps within the aluminum oxide by using bias stress and UV illumination. The UV light was provided with a fluorescent lamp with mercury lines providing carrier generation across the 4H-SiC bandgap. Figure 5 shows the results of such an experiment for different Al_2O_3 samples at room temperature. The first reference CV (black solid curve) sweep is from depletion to accumulation on MOS pads after a stable flatband

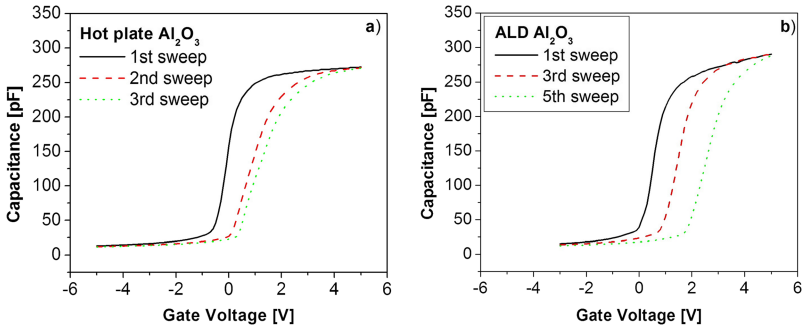

FIG. 4. (a) CV spectra of a hot plate Al_2O_3 sample upon repeated gate voltage sweeps from depletion to accumulation, (b) the same experiment for ALD grown Al_2O_3. The shifts of the CV curves are due to trapping of electrons within the Al_2O_3 under strong accumulation bias which saturates after several sweeps.

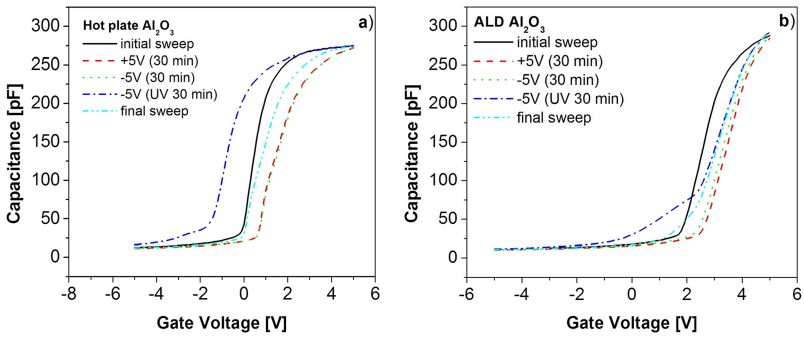

FIG. 5. CV characteristics (100 kHz) at 300 K of (a) hot plate- and (b) ALD- grown Al_2O_3 samples before and after applying positive or negative bias stress to them. The black solid curves denote the first reference curves made after obtaining stable flatband voltage at 300 K (see figure 4). The light blue dash dot dot curves are the final curves recorded at the end of the experiment. For details see main text.

voltage is reached (as in figure 4) The MOS capacitor is then kept in accumulation (+5 V) for 30 minutes and then the bias is swept from depletion (-5 V) to accumulation (+5V) and the CV (red dashed curve) is recorded. Electrons are injected into the oxide during the accumulation bias stress and electron trapping is detected as a positive flatband shift.

Next, a depletion bias of -5 V is applied for 30 min to examine if electrons are released from oxide traps under such conditions. The CV (green dotted curves) are recorded directly thereafter and are almost identical to the curves recorded after accumulation bias stress CV (red dashed curves) showing that there is insignificant release of electrons from oxide traps. Next, ultraviolet (UV) light is applied to the sample under depletion bias (-5 V) for 30 min. A negative flatband voltage shift of about 2 V is observed in the hot plate Al_2O_3 sample in the CV sweep following the UV light illumination (dark blue dash dot curve). It is evident that electrons trapped in the Al_2O_3 are released during the UV exposure. The number density of released electrons can be estimated by using the expression:

$$N_{it} = \frac{C_{ox}\,(V_{FB} - V_{FB(UV)})}{qA} \tag{3}$$

where V_{FB} and $V_{FB(UV)}$ are flat band voltages before applying accumulation bias stress and after UV light exposure to the MOS capacitors respectively. The number density of released trapped charge in hot plate Al_2O_3 sample is $\sim 4\text{x}10^{12}$ cm^{-2}. The flatband voltage after UV exposure is close to the theoretical value suggesting that most of the trapped electrons within the oxide are released during the UV treatment. These traps are filled again once the sample is biased in accumulation as seen in the final sweep (light blue dash dot dot curve).

The behavior in the other Al_2O_3 samples is similar regarding the effect of the UV light exposure. The same experiment for ALD Al_2O_3 is shown in figure 5b). As in the hot plate sample electrons are trapped within the oxide under accumulation bias and are not released again unless UV exposure under deep depletion is applied. The main difference here is that electrons are immediately re-trapped within the oxide during the first sweep after UV exposure (dark blue dash dot curve). A stretch-out of the CV curve suggests that electrons are recaptured within the oxide as the gate voltage leads the device to accumulation. In contrast, strong accumulation bias is needed to recapture electrons within the hot plate Al_2O_3 (see dark blue dash dot curve in Figure 5a).

The possible effect of the UV light is twofold. Firstly, it is possible that the UV photons are "absorbed" by the trapped electrons in the Al_2O_3 resulting in a release of the electrons to the SiC conduction band. Secondly, the UV exposure creates electron hole pairs and the depletion layer shrinks correspondingly. This means that the electric field across the oxide increases which can result in enhanced field assisted emission of electrons from traps within the Al_2O_3 to the SiC conduction band. We cannot distinguish between these two possibilities in this experiment but very similar behavior has been observed for thermal oxides on SiC containing sodium ions.[27]

This experiment demonstrates two things. First, the net negative charge observed in the Al_2O_3 layers is not a permanently fixed charge but rather electrons trapped within the oxide which can be released to the SiC using depletion bias and UV exposure. Such net negative oxide charge is reported in ALD grown Al_2O_3 in literature but the charge density is typically an order of magnitude higher than what is observed in this study.[9–11] The negative charge has been attributed to charged ions within the oxide and assumed to be fixed oxide charge but has not been investigated further as done here. Secondly, we have some initial trapping of electrons in the aluminum oxides during growth which is possible to enhance by accumulation bias.

The main results reported here are rather remarkable. Al_2O_3 grown by oxidation of Al on a hot plate has significantly better electrical properties than ALD or RTP grown films. However, electron injection and relatively low breakdown field (5MV/cm) are still parameters that need to be improved in order to use Al_2O_3 dielectrics in SiC MOS technology.

IV. CONCLUSIONS

We find the Al_2O_3 layer grown by repeated deposition and subsequent low temperature (200°C) oxidation of thin Al layers using a hot plate are more immune to electron injection and have a very low density of traps at the Al_2O_3/SiC interface compared to Al_2O_3 grown by ALD or RTP. Electron injection within the Al_2O_3 during positive bias stress and the release of injected electrons by UV light illumination show that our Al_2O_3 samples do not contain negative fixed charge as frequently mentioned in literature. Breakdown field of the hotplate Al_2O_3 is ~ 5 MV/cm which is higher than of Al_2O_3 samples grown by ALD or RTP but still only half the value obtained in thermal SiO_2 grown on 4H-SiC. It is possible to increase the breakdown voltage of the Al_2O_3 based MOS capacitors by depositing a SiO_2 layer on the top of hot plate Al_2O_3 and maintain low density of interface traps at the Al_2O_3/SiC interface.

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