Non-galvanic Interconnects for Millimeter-wave Systems

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Abstract

Fueled by the increasing demand for higher data rates, millimeter-wave (mmW) systems emerged as a candidate that can provide multi-gigabit per second (Gb/s) transmission. This demand is mainly driven by modern communication systems and several other wireless and sensing applications such as production quality inspection and imaging systems. The full realization of such systems has been always challenged by the lack of low-loss low-cost interconnects and high-level integration. This challenge is more critical in systems operating beyond 100 GHz where conventional packaging techniques would not be suitable from performance perspective.

D-band offers a wide spectrum ranging from 110 to 170 GHz and hence providing wide bandwidth that makes it suitable for high data rate systems. In this thesis, several interconnects that operate at D-band are presented. Different technologies were used to realize the interconnects. Two interconnects are realized in Embedded Wafer Level Ball Grid Array (eWLB) packaging technology. The technology has been widely used for low frequency applications. The proposed interconnects are based on slot antennas radiating to a standard air-filled waveguides. The interconnects achieve an average insertion loss of 3 dB and 3.4 dB across the frequency ranges 110-138 GHz and 116-151 GHz respectively. The proposed interconnects are generic and do not require any galvanic contacts. The utilized eWLB packaging technology is suitable for low-cost high-volume production and allows heterogeneous integration with other technologies as well.

A chip-to-waveguide transition based on unilateral finline structure is also demonstrated. The interconnect consists of a microstrip line implemented on a 75 um-thick substrate. The line then couples to a unilateral finline taper that is mounted in the E-plane of a standard D-band waveguide. The transition achieves a very low loss of only 0.7 dB and covers a very wide band ranging from 110 to 170 GHz.

A chip-to-waveguide transition in a commercial MMIC technology is also presented. The transition is based on Linearly Tapered Slot antenna (LTSA) structure. The antenna is implemented on a 50 um-thick Gallium Arsenide (GaAs) substrate. The transition exhibits an insertion loss of 1 dB across the frequency range 110-170 GHz.

This work presents low-cost high-performance mmW interconnects and addresses integration challenges facing systems operating beyond 100 GHz paving the way for high-volume commercialization of such systems in the future.

Keywords: D-band, interconnects, waveguide transition, taper, eWLB, mil-

limeter waves, THz, finline, slot antenna, LTSA, MMIC, GaAs, SiC, CMOS, InP, WR-6.5.

List of Publications

Appended Publications

This thesis is based on work contained in the following papers:

[A] A. Hassona, Z. Simon He, C. Mariotti, F. Dielacher, V. Vassilev, Y. Li, J. Oberhammer, H. Zirath, "A non-galvanic D-band MMIC-to-waveguide transition using eWLB packaging technology," *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Honolulu, HI, 2017, pp. 510-512.

[B] A. Hassona, V. Vassilev, Z. Simon He, C. Mariotti, F. Dielacher and H. Zirath, "Silicon Taper Based D-Band Chip to Waveguide Interconnect for Millimeter-Wave Systems," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 12, pp. 1092-1094, Dec. 2017.

[C] A. Hassona, Z. Simon He, O. Habibpour, V. Desmaris, V. Vassilev, S. Yang, V. Belitsky, H. Zirath, "A Low-loss D-band Chip-to-Waveguide Transition Using Unilateral Finline Structure," Accepted for publication in *2018 IEEE MTT-S International Microwave Symposium (IMS)*, Philadelphia, PA, 2018

[D] A. Hassona, Z. Simon He, V. Vassilev and H. Zirath, "D-band waveguide transition based on Linearly Tapered Slot Antenna," *2017 IMAPS Nordic Conference on Microelectronics Packaging (NordPac)*, Gothenburg, 2017, pp. 64-67.

Notations and Abbreviations

Notations

ε_r	Relative permittivity
δ	Loss tangent
ρ	Resistivity
σ	Conductivity
f	Frequency
ω	Angular frequency
C	Capacitance
T	Temperature
Ω	Ohm

Abbreviations

MMIC	Monolithic Microwave Integrated Circuit
eWLB	Embedded Wafer Level Ball Grid Array
WG	Waveguide
mmW	Millimeter-wave
BW	Bandwidth
SoC	System on Chip
RDL	Redistribution Layer
PCB	Printed Circuit Board
BGA	Ball Grid Array
DC	Direct Current
RF	Radio Frequency
THz	Terahertz
CPW	Coplanar Waveguide
SL	Slot Line
MS	Micro-strip
TFMSL	Thin-Film Micro-strip Line
HR	High Resistivity
Si	Silicon

SiC   Silicon Carbide
GaAs   Gallium Arsenide
WR   Rectangular Waveguide
LTSA   Linearly Tapered Slot Antenna
SIW   Substrate Integrated Waveguide
EM   Electromagnetic
PMC   Perfect Magnetic Conductor
AMC   Artificial Magnetic Conductor
PEC   Perfect Electric Conductor
BSV   Back-Side Via
Balun   Balanced to unbalanced

Contents

Chapter 1

Introduction

1.1   System Packaging Challenges at mmW

The increasing need for higher data rates makes mmW technologies an attractive solution for wireless systems [1]. This trend follows the evolution of modern communication systems requiring higher data rates [2] [3] . One of the main challenges that mmW systems are currently facing is the lack of convenient interconnects to interface with the outside world.

Conventional packaging techniques exhibit low performance at mmW frequencies. For instance, bondwires, which represent the most common interface for integrated circuits, show high inductive behavior above 100 GHz. The inductance of a bondwire is estimated to be roughly 1nH/mm [4] which means that even a short bondwire of 400 um length would yield an inductance of 0.4 nH and hence a reactance of 250 Ohms at 100 GHz. Such reactance is difficult to match to and any compensation techniques would show narrow band performance as presented in [5]. Moreover, bond pad size has to shrink as frequency gets higher to reduce its capacitive effects. The small size of bond pads at mmW makes the bonding process even more challenging and reduces the yield. Other approaches for packaging mmW systems have to be used.

Various techniques are presented in literature to realize such interconnects. One approach is to use silicon micro-machined interconnects [6]. The proposed interconnect can be used for chip-to-chip connectivity at mmW range, however, it would be challenging to implement the interconnect in a MMIC-to-waveguide fashion. Moreover, the interconnect shows a relatively high loss that might not be suitable for some applications.

Another technique is to couple the MMIC directly to the waveguide and hence achieve high coupling over wide frequency band [7]. The drawback of this technique is that it imposes limitations on MMIC size as it requires that MMIC dimensions do not exceed the critical limit that allows higher modes to propagate to the MMIC cavity. Moreover, most highly integrated circuits are relatively large in size and hence the MMIC size would exceed the subcritical dimension making the integration of MMIC-to-waveguide transitions on-chip impractical. To mitigate this problem, Deal et al. suggested using a non-rectangular MMIC [8]. That way, the MMIC portion on which the transition is implemented would be narrow enough not to allow cavity modes to propagate

while allowing the rest of the MMIC to have any arbitrary size. However, this solution requires complicated non-standard post-processing and is not cost-effective as it wastes chip area that can be utilized more efficiently.

Another way to overcome this, is to use a separate transition [9] [10]. Such transition can be narrow enough to prevent waveguide modes from leaking into the circuit cavity. The drawback of this solution is that it requires a bondwire connection between the transition and the MMIC. The use of bondwires is not suitable at mmW frequencies as discussed earlier and their inductive behavior would compromise the performance of the whole system.

One approach to realize mmW interconnects is to implement a microstrip to Substrate Integrated Waveguide (SIW) transition as suggested in [11]. However, such transition does not provide a direct connection to the outside world. An extra transition needs to be implemented to provide an interface with standard air-filled waveguides, which eventually would contribute to the overall loss of the system. Moreover, SIWs suffer from dielectric loss, which could be avoided if direct radiation to air is achieved efficiently.

1.2   Thesis Motivation and Contribution

This thesis addresses integration and packaging challenges facing mmW systems and provides several approaches to implement mmW interconnects. The proposed interconnects do not require galvanic contacts and can be implemented in the commercially-available MMIC and packaging technologies. The interconnects operate at D-band which is a suitable candidate for next generation high data rate mmW systems due to the wide bandwidth it provides.

Several technologies are investigated in this thesis to realize the interconnects. eWLB packaging technology is investigated and two D-band interconnects are demonstrated. The choice of eWLB technology is motivated by the need of a low-cost and high-volume process for mmW interconnects. eWLB packaging has been widely used for applications operating below 100 GHz [12] [13]. Recent development of a fully-integrated radar at 122 GHz using the technology was demonstrated in [14] but to the author's knowledge, no waveguide interconnects were developed using the technology at mmW frequencies.

eWLB technology relies on Ball Grid Arrays (BGA) to provide DC and low frequency connectivity. Several fully integrated mmW systems have been successfully demonstrated [15] [16] but eWLB technology was not used for packaging such systems. This is due to the relatively large size of BGA interconnectivity provided by eWLB manufacturers which is not suitable for mmW applications. Moreover, the discontinuities introduced by transitting from chip to eWLB through vias then from eWLB to PCB through BGA introduce many mismatches along the signal path which leads to undesired reflection and radiation losses that could be avoided if a non-galvanic approach was followed to realize such interface.

This work proposes implementing slot antennas directly radiating the signal to standard waveguides to provide mmW connectivity instead of using the conventional BGA. The proposed concept is verified by experimental results. The implemented interconnects achieve an average insertion loss of 3 dB and 3.4 dB across the frequency ranges 110-138 GHz and 116-151 GHz respectively. The

presented interconnects pave the road towards high volume commercialization of mmW systems using a mature packaging technology.

A chip-to-waveguide transition based on unilateral finline structure is also realized. Waveguide transitions based on finline structures were presented in literature at V-band and W-band [17] [18]. The proposed transition in this work is simple and compatible with most MMIC technologies. The transition exhibits very low loss of only 0.7 dB and a very wide bandwidth covering the whole D-band. The proposed solution does not require galvanic contacts and is compatible with most MMIC technologies. In addition, the transition can be implemented using only one metal layer.

This thesis also presents a chip-to-waveguide transition based on linearly tapered slot structure. The transition is implemented in a commercial MMIC technology. The proposed transition provides direct coupling to the waveguide from the chip without the need of any intermediate solutions. Moreover, it does not impose any limitations on chip size. The transition shows an average insertion loss of 1 dB across D-band.

The thesis is organized as follows. In Chapter 2, a literature review of previous work on eWLB packaging is presented. An overview of the eWLB technology used for this work is given. The interconnects implemented in this technology are presented and explained in detail. The measurement results are then shown and compared to simulations. Chapter 3 focuses on the chip-to-waveguide transition realized using unilateral finline structure. The structure is detailed and its theory of operation is discussed. Challenges for the implementation of the transition at D-band are explained and solutions are proposed. Experimental results are presented and compared to simulation results. In Chapter 4, a chip-to-waveguide transition based on LTSA is presented. The transition's design is discussed and simulation results are presented. Finally, Chapter 5 concludes and summarizes the presented work.

Chapter 2

D-band Interconnects in eWLB Packaging Technology

The increasing complexity of MMICs raises the challenge of packaging with tens or even hundreds of input and output (I/O) interfaces into a small area which can be mounted in a system. eWLB technology provides an attractive solution that packages the MMIC into a BGA mountable module with many I/O connections
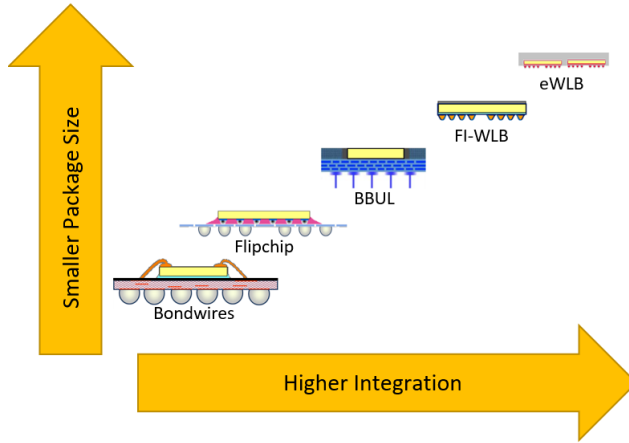
Figure 2.1: Evolution of packaging technology

As shown in figure 2.1, there are several solutions for IC packaging and interconnectivity. Wire bonding and flipchip are the conventional and most common techniques, however, achieving higher integration and lower losses at Microwaves and mmW is more feasible using wafer level packaging with BGAs [12] [19]. eWLB technology is a system integration platform introduced recently for wireless applications [20] [21] [22]. The small size of interconnections in eWLB technology results in reduced parasitics enabling good performance

up to mmW frequencies. Using eWLB technology does not only reduce the size of the package, but also achieves very high integration and I/O counts density. Moreover, passive components can be implemented outside the MMIC by exploiting the RDLs [12] [23]. The eWLB technology also enables the integration of several chips of different technologies in the same package.

eWLB I/Os can be classified based on frequency to DC/low-frequency I/O and mmW I/O. Low-frequency I/O has been proposed and studied in [24] [25] using standard eWLB connections, however, such conventional packaging technique using BGA is not suitable for mmW systems since the BGA would exhibit high reactance at such frequencies. A conventional eWLB transition shows an inductance of 0.46 nH/mm [26]. Such inductance would translate into high impedance for signals above 100 GHz making this technique not suitable at such frequencies. mmW frequency I/O connection up to 85 GHz has been proposed using antenna liked structure [13]. To the author's knowledge, mmW interconnection on eWLB technology above 100 GHz has not been proposed before. In this chapter, two D-band interconnects in eWLB technology are demonstrated and supported by experimental results.

2.1 Overview of eWLB Technology

The eWLB is based on an embedded device technology with fan-out redistribution. Figure 2.2 illustrates a cross-section of an eWLB package with fan-in and fan-out areas and RDLs. The fan-in area is limited by the chip size, while the fan-out area extends to the package edge. The fan-out area around the chip is the key feature of the eWLB technology, as it makes the eWLB package not limited by the chip size and allows high I/O density. In addition, the mold compound, which acts as a carrier, enables the realization of transmission lines and passives [12].
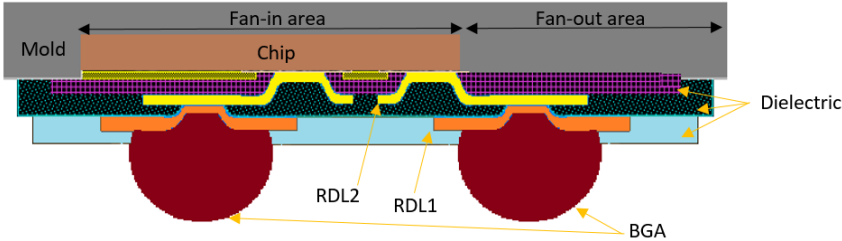
Figure 2.2: Cross-section of the eWLB package

The chip is placed in a face-down position on a carrier system and then encapsulated with the mold compound. The mold compound used also shows good electrical properties (tan $\delta = 0.004$) [27]. This enables the realization of low-loss transmission lines. Thin-film technology is then used to realize RDLs [27]. The thin-film technology offers the advantage of high precision and low cost. In addition, it enables flexible and customizable package design. The technology used for this work utilizes two thin-film RDLs separated by dielectrics layers as shown in figure 2.2. The standard metal build-up consists of Cu/Ni/Cu or Cu/Ni/Au stacked layers [27].

Two types of transmission lines can be implemented in eWLB technology which are thin-film microstrip lines (TFMSL) [28] [29] and coplanar structures such as slotline (SL) and coplanar waveguide (CPW) [30] [31] [32]. The advantage of TFMSL over CPW is the presence of ground metallization, which shields the line from the substrate effects. A coplanar topology, however, allows an easier connection of external components since signal and ground connections are on the same level. This is important at mmW frequencies where RF grounding must be close to the device. Furthermore, the characteristic impedance Z_0 in CPW lines is determined by the width of the central conductor together with the spacing to the ground plane which gives an additional degree of freedom in realizing Z_0. The main contribution of attenuation in coplanar waveguide comes from conductor and leakage losses. The latter, however, can be minimized by keeping the overall ground-ground spacing small relative to the substrate height and dielectric wavelength at the frequency range of interest. Further, the electrical characteristics of the coplanar circuits are less dependent on thickness variations of the substrate material compared to the conventional TFMSL configurations. Moreover, CPW requires only one metallization layer making it a feasible solution even in single-layer eWLB packages. In this work CPW lines are used as feeds for the antenna structures as will be discussed in detail in the following sections.

2.2 Slot Antenna Waveguide Transition

In this section, a generic approach for implementing MMIC-to-waveguide transitions based on eWLB process is presented with the support of experimental results.

2.2.1 Transition Design

The proposed packaging solution consists of an eWLB with an embedded MMIC, a printed circuit board (PCB) and an air-filled waveguide mounted on the PCB as shown in figure 2.3.

The eWLB technology used for this work provides two RDLs as discussed in the previous section. In general, RDL2 is used to provide connectivity to the MMIC and RDL1 is used along with BGAs to provide DC and low frequency connectivity from the MMIC to the PCB/outside world. In this work, instead of using conventional BGAs to provide connectivity for the D-band signal, RDL1 is used to realize an antenna that couples the signal to the waveguide avoiding galvanic connection.
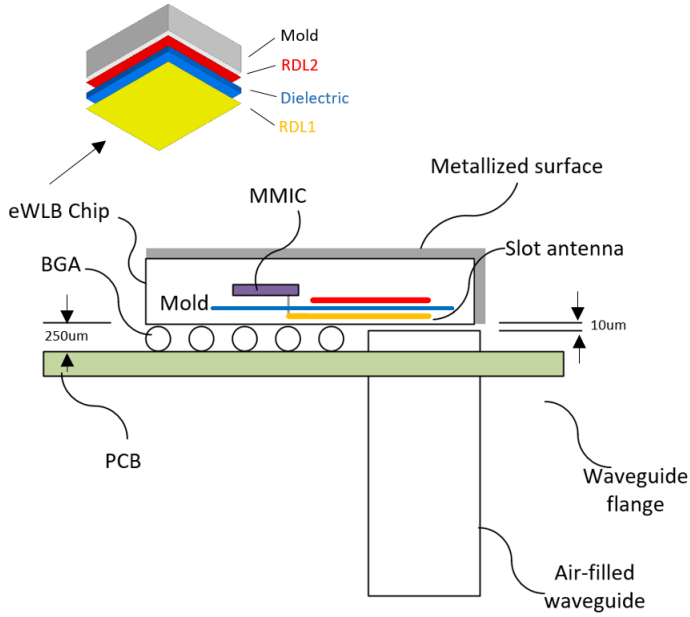
**Figure 2.3:** Simplified side-view of the proposed solution

Moreover, the dielectric constant of the eWLB substrate is 3.2 which is relatively low leading to low leakage into the substrate compared to silicon and other semiconductor substrates. In addition, the substrate height is 0.45 mm which is close to quarter wavelength at D-band and hence, metallizing the eWLB surface as shown in figure 2.3, makes it act as a backshort and hence achieve better radiation towards the direction of the waveguide. Simulations showed that the insertion loss of the transition improves by 0.5 dB if the eWLB surface is metallized. This metallization can be achieved either by applying reflective paint on eWLB surface or by simply placing the eWLB on a metallic surface.

2.2.2 Implementation of The Antenna

The fabricated eWLB chip is shown in figure 2.4. The antenna is implemented on RDL1 and is fed though CPW lines. In order to avoid shorting the signal line to the ground in case the waveguide wall made contact with the eWLB surface, the signal line was transited to RDL2 as shown in figure 2.4. Moreover, a 30-um deep channel was machined in the waveguide wall at the same position above the signal line as shown in figure 2.5 to avoid shorting it to the adjacent ground lines.
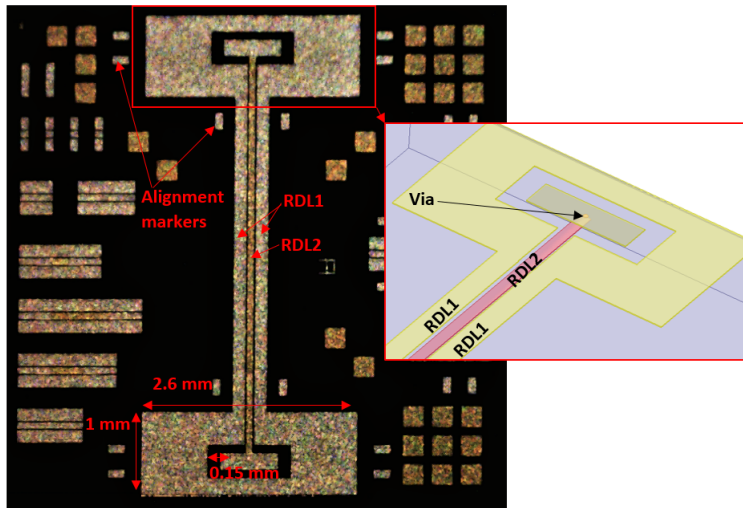
Figure 2.4: Photo of the fabricated eWLB
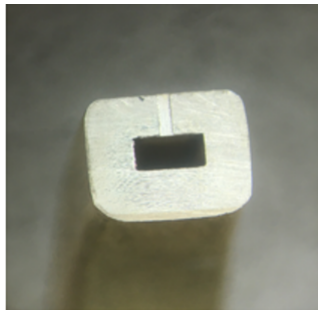
Figure 2.5: Waveguide photo showing the machined channel

The drawback of this implementation is that it increases the spacing between the signal line and the ground lines since they are not implemented on the same layer and that might in turn affect the characteristic impedance of the CPW line. In order to mitigate this, another implementation of the antenna was fabricated at which the signal line transits back to RDL1 after crossing the waveguide wall. The second implementation is shown in figure 2.6.
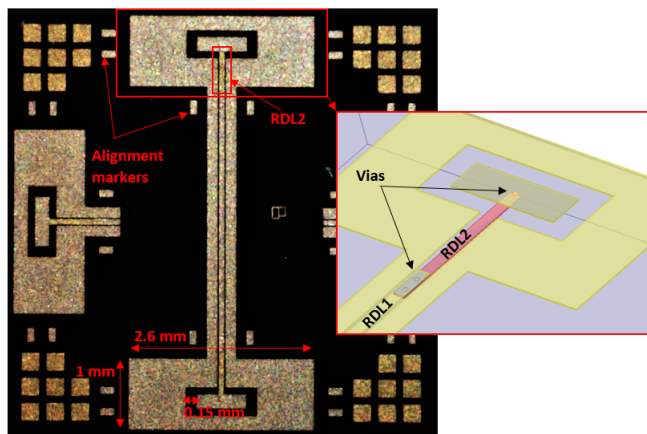
Figure 2.6: Photo of the second implementation of the eWLB

Both versions are implemented as a back-to-back solution allowing straightforward characterization and calibration. Alignment markers were used on RDL1 to accurately align the waveguide openings to the antenna to achieve maximum coupling as shown in figures 2.4 and 2.6. The antenna's slot width is 0.15 mm. The antenna occupies an area of $2.6 \times 1 \ mm^2$ and the whole eWLB occupies an area of $6 \times 6 \ mm^2$. CPW line test structures were also included to calibrate line losses and extract the transition loss accurately.

2.2.3   Experimental Results and Discussion

The focus of this work is the realization of the mmW transition and hence no DC or low frequency connectivity were realized nor tested and no PCB was employed in the tested structure. Detailed investigation of such connectivity in the same process is studied in literature in [27].

The eWLB chip was placed upside down and open-ended waveguide bends were mounted perpendicular to the eWLB surface as shown in figure 2.7. The whole setup was mounted on a probe station to allow accurate alignment of the waveguide openings and the antennas. The measurement setup consists of a Keysight PNA-X network analyzer and WR-6.5 VDI frequency extension modules to up/down-convert the signal frequency to D-band.
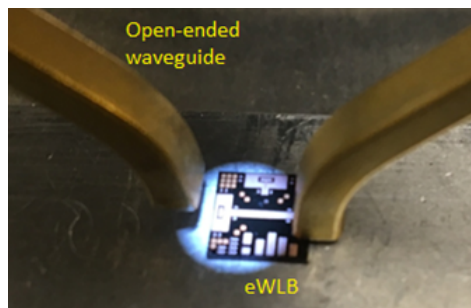
Figure 2.7: Photo of the measurement setup

Two-port calibration was performed to the inputs of the waveguide bends. The loss of the bends was then de-embedded using MATLAB to extract the transition loss. The two implementations discussed earlier were measured and the losses of the waveguides and the feed transmission lines were de-embedded. S-parameters of the single transition for both implementations are shown in figure 2.8. Implementation 1 refers to the design in which the signal line is implemented on RDL2 while implementation 2 refers to the design at which the signal line transit back to RDL1 after crossing the waveguide wall. Measurement results show no significant difference between the two implementations. That could be due to the relatively small thickness of the dielectric layer separating RDL1 and RDL2 that it did not have a significant impact on the characteristic impedance of the CPW line.
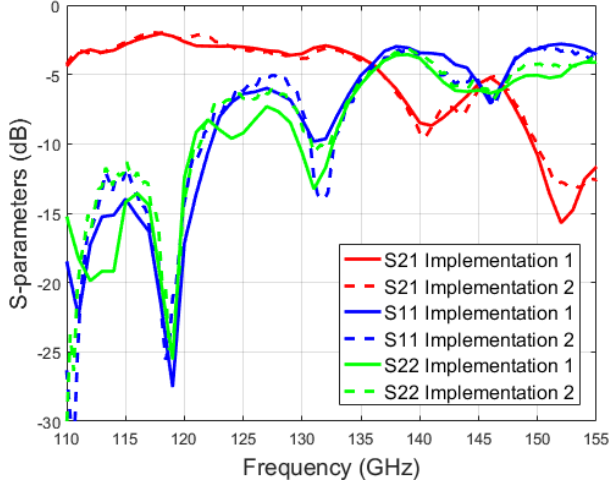
Figure 2.8: Measurement results of a single transition using the two different implementations
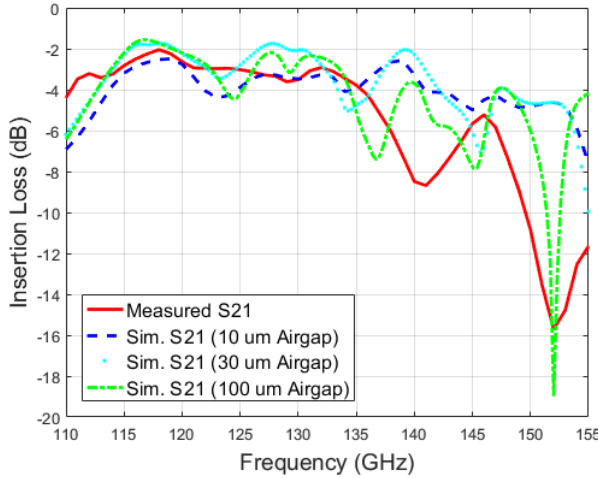
Figure 2.9: Insertion loss of the single transition
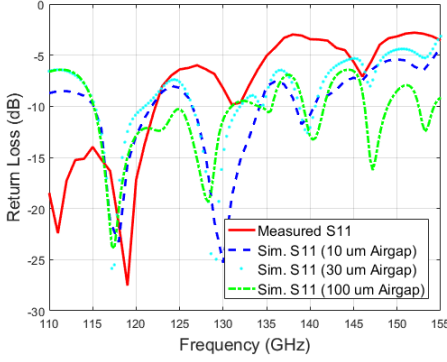
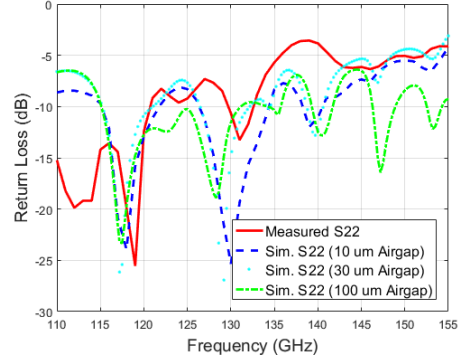**Figure 2.10:** Return loss of the transition at the input port

Figure 2.11: Return loss of the transition at the output port

Measurement results of the first implementation show an average insertion loss of 3 dB per transition and a maximum of 6 dB in the frequency range of 110 to 138 GHz as seen in figure 2.8. The transition has a 3-dB bandwidth of 22%.

Simulations were performed using HFSS 3D EM simulator and compared to measurements as shown in figure 2.9. It is noteworthy that the measured frequency response shows a shift towards lower frequencies compared to the simulated response. The sensitivity to the air gap between the waveguide and the eWLB was also simulated. As mentioned earlier, a galvanic contact is not needed and simulations showed that an air gap of up to 30 um can be tolerated with no degradation in performance and an air gap of 100 um causes slight degradation in bandwidth as shown in figure 2.9. The return losses at both the input and the output ports are shown in figures 2.10 and 2.11 respectively. Simulated return loss shows good agreement with measurements. The average achieved return loss across the frequency range 110-138 GHz is 10 dB and the minimum is 4 dB.

2.2.4 Future Improvements

The transition exhibits narrow-band performance and poor return loss at the higher part of the band. Implementing matching sections could lead to improvement in the transition's performance. Moreover, the air gap between the waveguide and the antenna causes the field to radiate outside the waveguide leading to radiation loss. This could be minimized by using artificial Perfect Magnetic Conductor (PMC) structures as will be discussed in detail in chapters 3 and 4.

2.3 Si Taper Based Interconnect

In this work a D-band slot antenna is implemented on the technology's RDL similar to the work presented in the previous section, however, the antenna here radiates to a high-resistivity (HR) silicon taper, which in turn radiates into an air-filled waveguide instead of radiating directly to the waveguide. The

proposed approach is also generic and the concept is supported and verified by experimental results.

2.3.1 Interconnect Realization
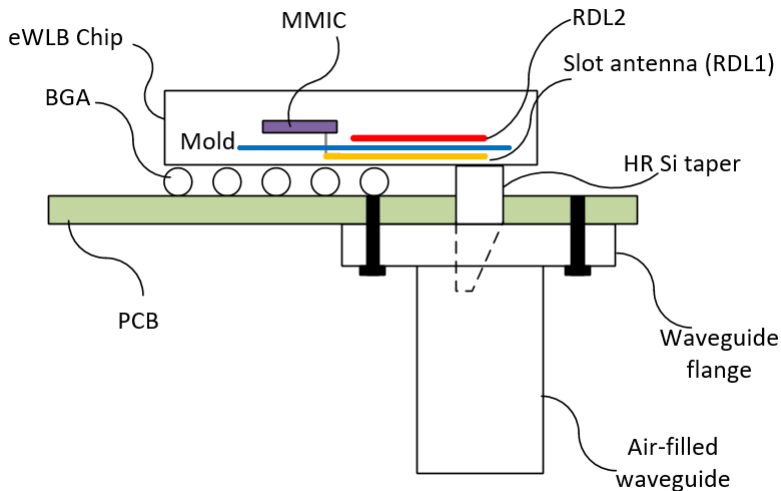
**Figure 2.12:** The proposed packaging system consisting of: The slot antenna implemented on an eWLB chip, MMIC, PCB, HR Si taper and an air-filled waveguide.

The proposed complete solution is shown in figure 2.12. The solution consists of an eWLB chip, MMIC, PCB, HR silicon taper and an air-filled WR-6.5 waveguide.

This work focuses on the mmW transition part of the system which is shown in detail in figure 2.13. The transition consists of a slot antenna fed by a CPW line. The antenna had to be implemented differently in this work since it radiates to a relatively small Si taper and hence the antenna design had to be more compact. This was achieved by using a rectangular slot instead of the ring slot that was employed in the work presented earlier. The compact implementation of the antenna allows using a small Si taper and hence avoid exciting higher modes.

The antenna is implemented on RDL1 and the signal line transits to RDL2 at the waveguide wall position as shown in figure 2.13 to avoid shorting it to the adjacent ground lines similar to the previous work. The slot dimensions are chosen to provide reasonable impedance matching to the silicon taper and minimize radiation leakage at the interface. The taper is machined using a micro-dicing saw and its dimensions are shown in figure 2.14. The taper is mounted normal to the slot and is then inserted into the air-filled waveguide. The use of the Si taper helps guide the field to the air-filled waveguide and reduces leakage to the substrate due to the high dielectric constant of Si. This helps achieve better results compared to direct radiation to the air-filled waveguide as presented earlier.
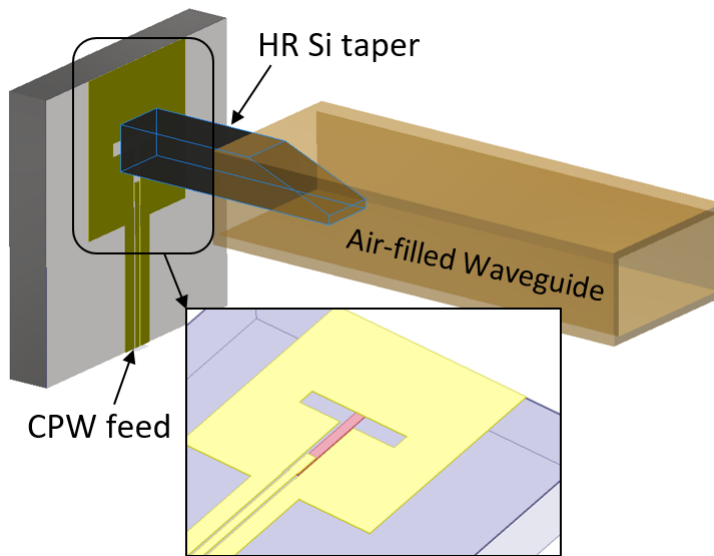
Figure 2.13: The implemented interconnect consisting of 3 parts: the slot antenna implemented on eWLB chip, HR Si taper and air-filled waveguide.
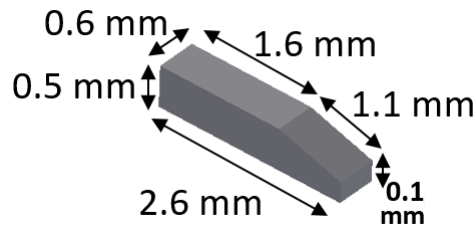

Figure 2.14: Dimensions of the machined HR Si taper

2.3.2   EM Simulations and Loss Analysis

HFSS 3D electromagnetic simulator was used to verify the performance of the structure as shown in figure 2.15. An air gap of 20 um between the antenna and the taper is included in simulations to model the non-galvanic contact effect. The S-parameters simulation showed an average insertion loss of 3.8 dB. Simulations show that the main contributors to the loss are the eWLB mold dielectric loss with an average contribution of 0.95 dB and the radiation at the interface between the antenna and the taper due to the air gap with a contribution of 0.71 dB to the total loss. Other sources of losses include the ohmic loss of the CPW feed lines and the dielectric loss of the taper and the adhesives used to assemble the interconnect. Table 2.1 summarizes the analysis of the interconnect loss and details contributions to the overall insertion loss. Simulation results are presented in the following section and compared to measurement results.
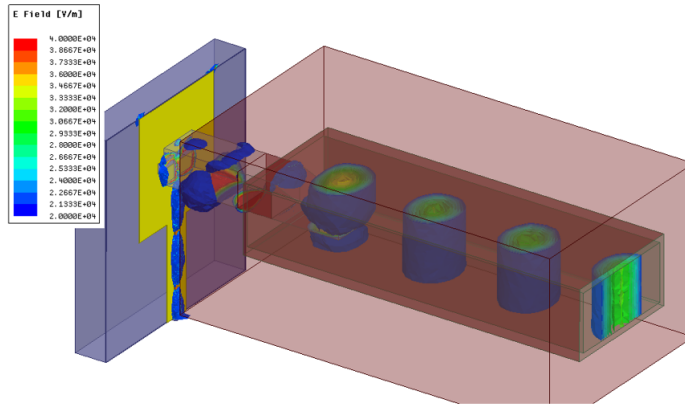
Figure 2.15: EM simulation of the complete solution.

Table 2.1: INTECONNECT LOSS ANALYSIS

Loss Source	Material	Material Parameters	Contribution to the Total Loss (dB)
eWLB mold dielectric loss	Plastic	ε_r=3.2 , δ=0.004	0.95
Radiation loss due to Antenna-to-Taper gap	-	20 um Air gap	0.71
Taper dielectric loss	HR Si	ε_r=11.7, ρ=4,000 Ω.cm	0.70
Transmission line loss	Copper	σ=5.9$\times 10^7$ S/m	0.65
Other materials losses	-	-	0.79
Total loss			3.8

2.3.3 Assembly Approaches

Two different approaches were followed to assemble the interconnect. In the first approach, a steel metal holder was machined and the taper slides through a hole in the holder that has the same dimensions of the taper as shown in figure 2.16. The taper is then glued to the holder using Glycol Phthalate Wax and the holder is attached to the air-filled waveguide using conductive epoxy. The holder dimensions and features are designed to provide accurate alignment of the taper to the air-filled waveguide.

Another approach was also attempted to assemble the interconnect using a dielectric foam based on polymethacrylimide known as "ROHACELL HF" instead of using a metal holder. The material posses a very low dielectric constant of 1.041 and a loss tangent of 0.0106. The material is semi-rigid and it accommodates the taper with reasonable mechanical stability. The assembled

solution using this approach is shown in figure 2.17.

(a)

(b)
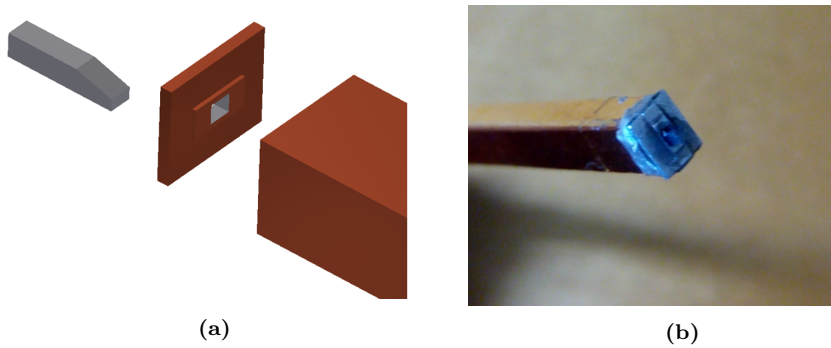
Figure 2.16: Assembly of the interconnect using metal holder (a) Illustrative view (b) Photo of the realized interconnect
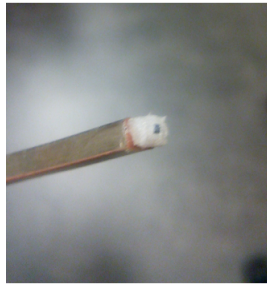
Figure 2.17: Photo of the assembled interconnect using ROHACELL HF dielectric

Both solutions were measured and the results are compared in figure 2.18. Results show that the assembly using the metal holder exhibit significantly better performance. The higher loss in the case of the dielectric foam could be due to the relatively high loss tangent of the material since both cases show similar return loss and hence the extra insertion loss in the foam's case is mostly due to the dielectric loss. Measurement results of the interconnect assembled using the metal holder is discussed in detail in the following section and results are compared to simulations.
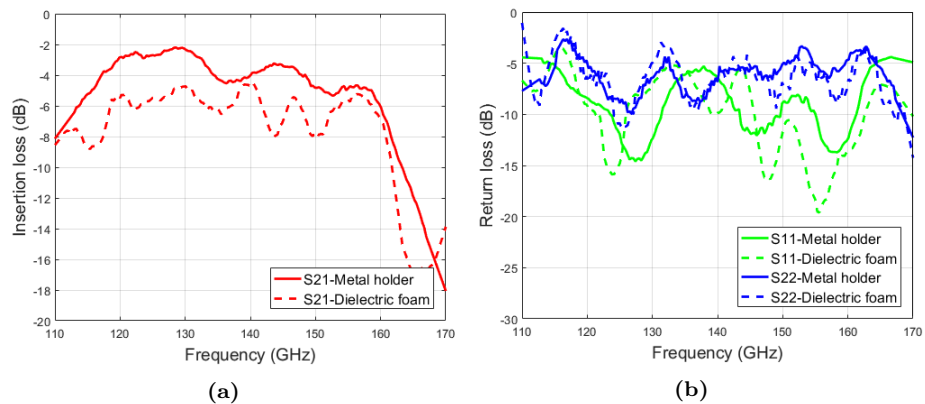
Figure 2.18: Measurement results of the two assembled solutions (a) Insertion loss (b) Return losses

2.3.4   Experimental Results and Discussion
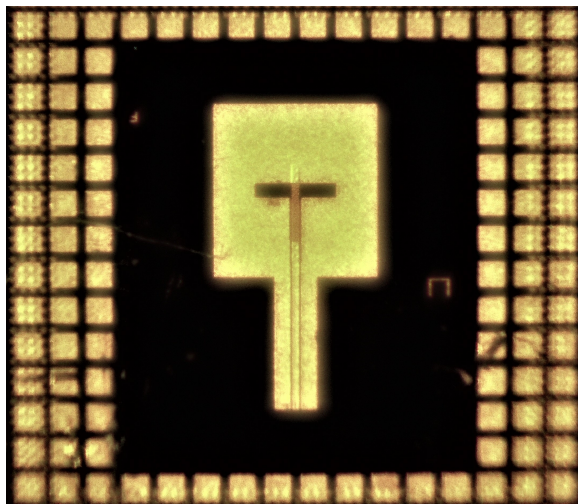
Figure 2.19: Photo of the implemented slot antenna

The fabricated slot antenna is shown in figure 2.19. The test setup consists of a Keysight PNA-X network analyzer and a pair of WR-6.5 VDI frequency extension modules to up/down-convert the signal to D-band as shown in figure 2.20. An open-ended waveguide bend is mounted perpendicular to the eWLB surface on one side of Cascade microtech's probe station allowing accurate positioning of the waveguide to the slot antenna. The taper along with the metal holder are attached to the open end of the waveguide bend. A D-band waveguide probe is mounted on the other side of the probe station to probe the CPW feed lines as mentioned earlier. Two-port calibration is performed to the outputs of the frequency extenders. The waveguide probe is then de-embedded by measuring the S-parameters of the probe on a calibration substrate including

Figure 2.20: Measurement setup for the interconnect with the waveguide bend on the left and waveguide probe on the right

open-circuit and matched loads to extract its insertion and return losses. The probe's s-parameters were then de-embedded using MATLAB. The waveguide bend is de-embedded by measuring a flanged waveguide of the same length and then de-embedding it in a similar fashion.

De-embedded measurement results of the interconnect show an average insertion loss of 3.4 dB over the frequency range of 116-151 GHz and a minimum of 2.1 dB as shown in figure 2.21. The results show good agreement with simulations. Sensitivity to taper misalignment and the air gap to the eWLB surface was also simulated and compared to measurements. Results show that an air gap of up to 40 um and a misalignment of 100 um in both lateral directions can be tolerated. The interconnect shows a 3-dB bandwidth of 26%. The return losses at the WR-6.5 side and CPW lines side are shown in figures 2.22 and 2.23 respectively.
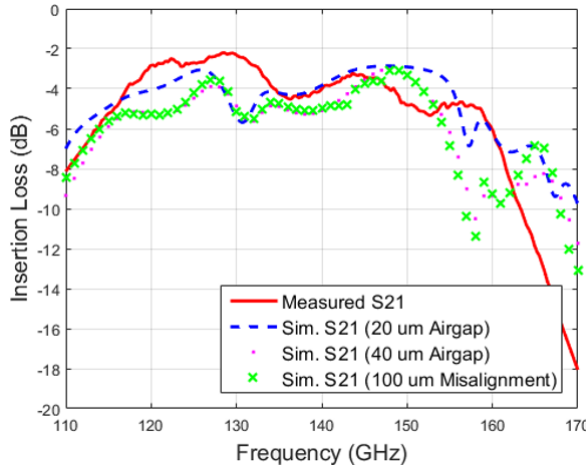
Figure 2.21: The insertion loss of the interconnect
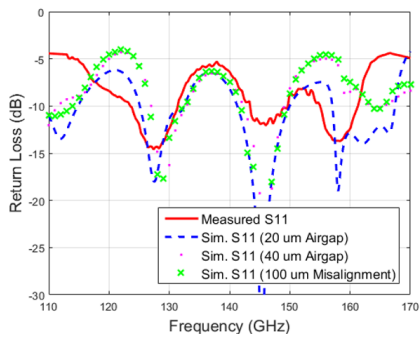
Figure 2.22: The return loss of the interconnect at the WR-6.5 reference plane
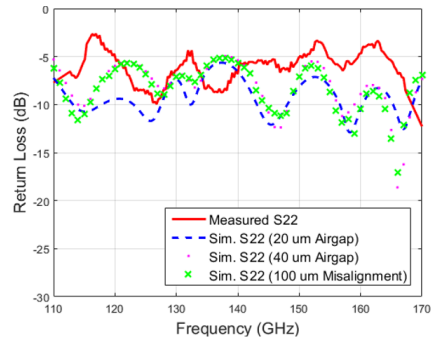
Figure 2.23: The return loss of the interconnect at the CPW reference plane

Chapter 3

Chip-to-Waveguide Transition Using Unilateral Finline Structure

3.1   Background

Finlines are quasi-planar structures that exhibit large bandwidth and high compatibility with planar circuit technologies. Finlines can be considered as shielded slot lines which are usually mounted in the E-plane of waveguides. The most common finline structures are unilateral, bilateral and antipodal as shown in figures 3.1a, 3.1b and 3.1c respectively

<div align="center">(a)   (b)   (c)</div>
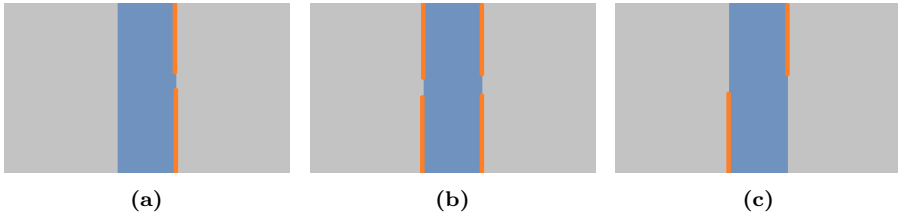
Figure 3.1: Cross section of common finline structures (a) unilateral finline (b) bilateral finline (c) antipodal finline

Unilateral finlines are the most convenient for fabrication. Bilateral finlines produce lower losses and antipodal finlines are used to realize transitions with impedance levels in the order of 10 Ohms. Waveguide transitions based on finline structures were presented at V-band and W-band and promising results were demonstrated in [17] [18]. The presented transitions showed low insertion loss of 2.3 and 1.6 dB at V-band and W-band respectively.

This chapter presents a D-band interconnect realized using unilateral finline structure due to its simplicity and wide-band performance. The interconnect consists of a microstrip line implemented on a SiC substrate. The line then couples to a unilateral finline taper that is mounted in the E-plane of a standard WR-6.5 D-band waveguide. The interconnect achieves low insertion loss and

covers very wide frequency range. The transition does not require any galvanic contacts nor any special processing and can be implemented in any of the commercially available semiconductor technologies. In addition, the transition does not impose any limits on chip size nor shape and is implemented using only one metal layer. In the following sections, the transition design is discussed in detail and then its performance is presented and compared to simulations.

3.2 Design of the Structure
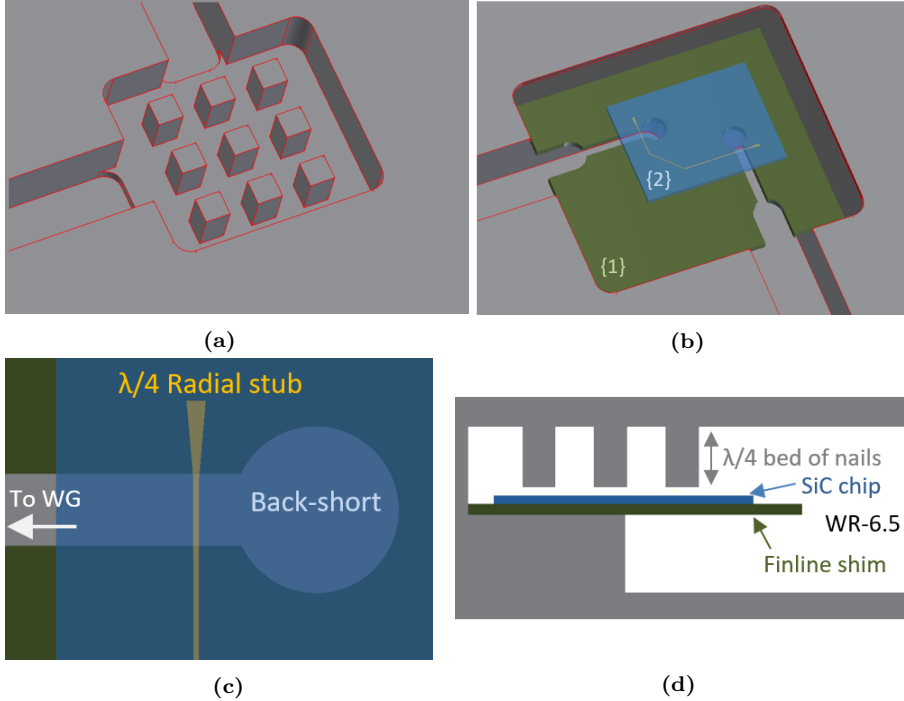
Figure 3.2: The proposed transition (a) Top part of split-block (b) Bottom part of split-block including {1} The finline metal shim and {2} The chip (c) Top view of the transition (d) Cross sectional side view of the whole solution

The proposed transition is shown in figure 3.2. It consists of a mechanical split-block with two D-band waveguide channels split in the E-plane. A unilateral finline is then implemented on a 0.15 mm-thick metal shim that is placed in the E-plane of the waveguide channel and is attached to the bottom part of the split block using conductive epoxy. The finline slot then couples the signal from the waveguide to a microstrip line implemented on a 75 um-thick SiC substrate (representing the MMIC test structure) which lies on top of the finline structure as shown in figure 3.2b. The finline ends with a cavity acting as a backshort and the microstrip line crosses the finline slot perpendicularly as shown in figures 3.2b and 3.2c.

The microstrip line ends with quarter-wave radial stubs at both sides and hence eliminating the need for vias to provide RF grounding. The microstrip line and the radial stub can be placed at any location on the chip and does

not require any special positioning (e.g. at the chip edge) as long as a crossing with the finline slot is made which provides more flexibility for MMIC design. Practically, the test chip presented here can be replaced with any MMIC fabricated on any high-resistivity substrate and the realization of the transition would require only the implementation of the radial stub from the MMIC perspective. The finline slot can either be machined in a separate metal shim similar to the presented work or it can be patterned on the back-metallization layer of the MMIC if the technology allows such feature.

3.3   Radiation Loss and Parallel Plate Cut-offs

One of the main sources of loss in such transitions is radiation losses. The radiation losses can be prevented in traditional packaging using metal cavities around the circuit, however, this technique is not suitable for highly integrated circuits that operate at high frequencies since the cavity size would be large to accommodate the chip and that would increases cavity resonances that can be excited which would eventually affect the performance of the circuit. Therefore, a special packaging technique should be used to prevent cavity modes and stop the undesired radiation.

One approach is to use a periodic structure located on top of the chip. The periodic structure should provide a high impedance boundary referred to as an Artificial Magnetic Conductor (AMC). The theory of operation of AMCs is that a Perfect Magnetic Conducting (PMC) surface located below the surface of a Perfect Electric Conductor (PEC) will create a cut-off of parallel plate modes when the spacing between the two plates is smaller than a quarter wavelength.

A detailed study of the behavior of different periodic structures is provided in [33]. A simple way to realize such structure is to use bed of nails [33] [34] as shown in figures 3.2a and 3.2d. The bed of nails structure is presented in literature for gap waveguide applications [35] [36]. MMIC transitions using the same concept were also demonstrated up to 100 GHz [37] [38]. The implemented bed of nails for this work has a quarter-wave height allowing it to act as a high impedance boundary at D-band and hence force the field to couple to the microstrip line and prevent loss due to radiation in undesired directions.
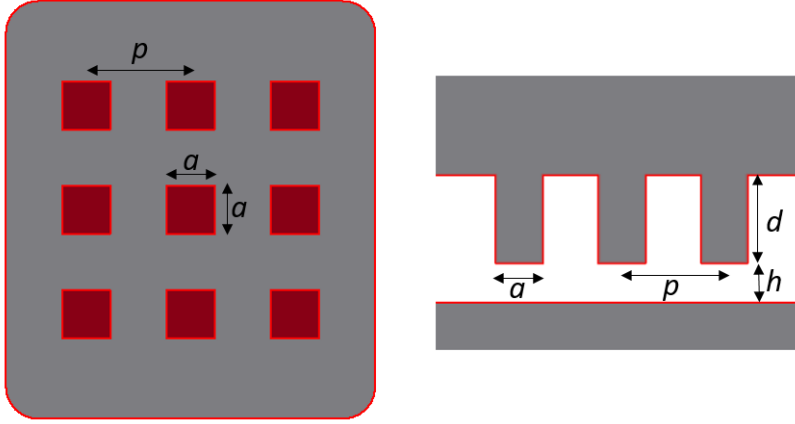
Figure 3.3: Bed of nails structure parameters

A thorough study of the cut-off bandwidth between parallel plates is presented in [33] showing how the main parameters of the structure affect the cut-off bandwidth. Those parameters include the length of the pins d, the distance to the other plate h, the period of the pins p and the dimensions of the pins a. Outcomes of the study presented in [33] were used along with 3D EM simulations to select the structure parameters that provide the largest possible bandwidth and lowest radiation loss at D-band. In the following section, the measurement results of the realized transition are presented and compared to simulations.

3.4 Measurement Results and Summary

Figure 3.4 shows photos of the machined mechanical split-block module with the bed of nails structure implemented in the top part of the module as shown in figure 3.4a and the unilateral finline structure with the bottom part of the module as shown in figure 3.4b. The module has standard WR-6.5 interfaces allowing it to be used and tested using standard systems as shown in figure 3.4c.

The fabricated SiC chip is shown in figure 3.5. The radial stub occupies an area of only $35 \times 145 \ um^2$ and the total test chip area is $1.8 \times 1.3 \ mm^2$. Both the chip and the module are implemented as back-to-back to allow straightforward characterization and testing of the transition.

(a)

(b)

(c)
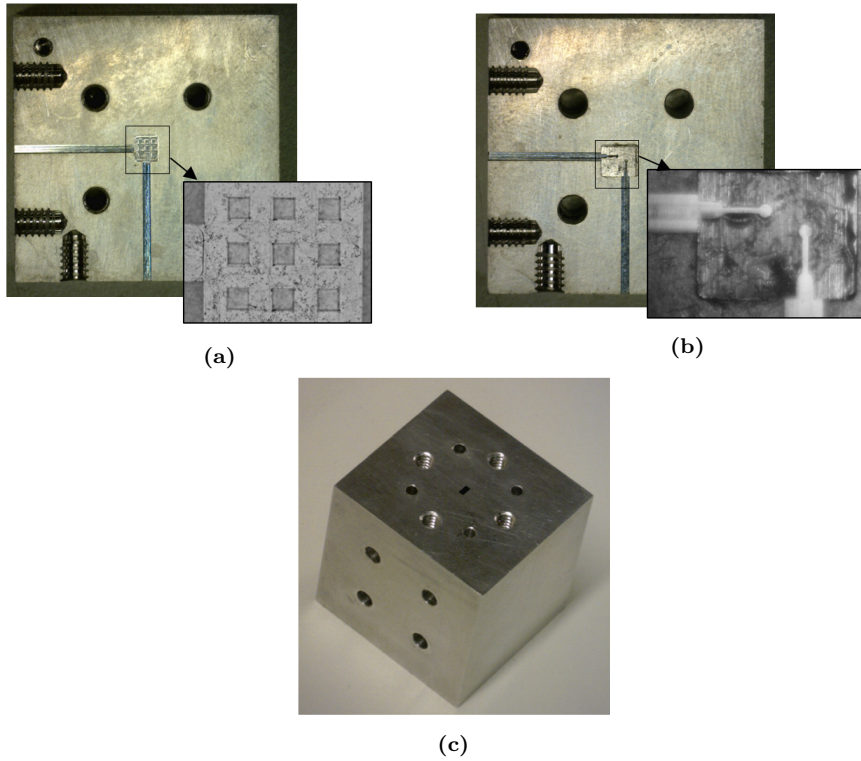
Figure 3.4: Photo of the fabricated mechanical split-block (a) Top part (b) Bottom part with the finline structure attached (c) Side view showing the standard WR-6.5 interface
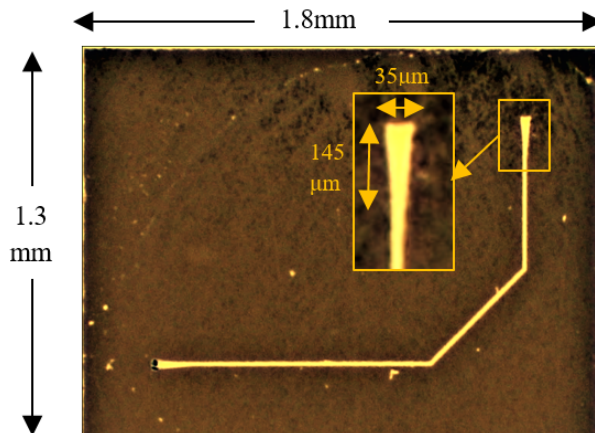
Figure 3.5: Photo of the fabricated SiC chip

The measurement setup is shown in figure 3.6. It consists of a network analyzer and two WR-6.5 frequency extension modules to up/down-convert the RF signal from the network analyzer to D-band. Two-port calibration was performed to the interfaces of the module.
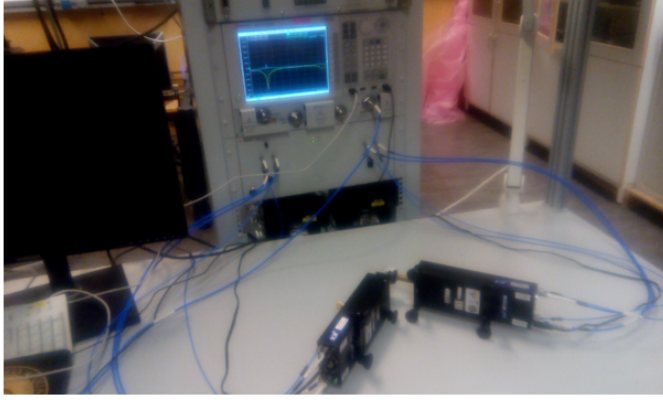
Figure 3.6: Measurement setup for the transition

Measurement results of the transition show a minimum insertion loss of only 0.7 dB per transition (i.e., 1.34 dB of loss for the back-to-back structure) and a maximum loss of 2 dB as shown in figure 3.7. The shown loss includes the ohmic loss of half of the microstrip line of 1.7 mm length and the loss of 12 mm-long split-block waveguide. The ohmic loss is estimated through simulations to contribute by 0.2 dB to the overall loss shown in figure 3.7. The transition exhibits a very wide band performance covering the entire D-band ranging from 110 to 170 GHz. The return losses of the transition at both sides are shown in figures 3.8 and 3.9. Results show an average return loss of 11 dB at both the input and output waveguide interfaces. The return loss could be further improved using smoother tapering profile for the finline slot and by using through substrate vias if the technology provides such feature.

Simulations were performed using HFSS 3D EM simulator and were compared to measurements. Simulations show good agreement with measurements. The transition's sensitivity to misalignment was also simulated. Results show that the transition can withstand a misalignment of 50 um with slight degradation in bandwidth at the higher edge of the band. Moreover, for a 75-um misalignment the transition can still maintain a maximum of 2 dB of loss up to 150 GHz. The presented transition does not require galvanic contacts nor any special processing and can be used in any MMIC technology. This work presented a simple integrated high-performance solution for packaging mmW systems.
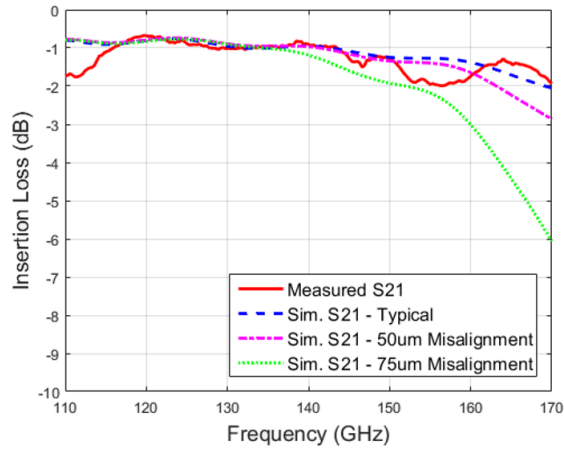
Figure 3.7: The insertion loss of a single transition
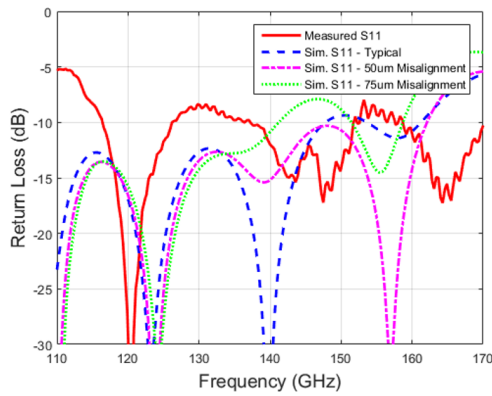
Figure 3.8: The return loss of the transition at the input WR-6.5 interface
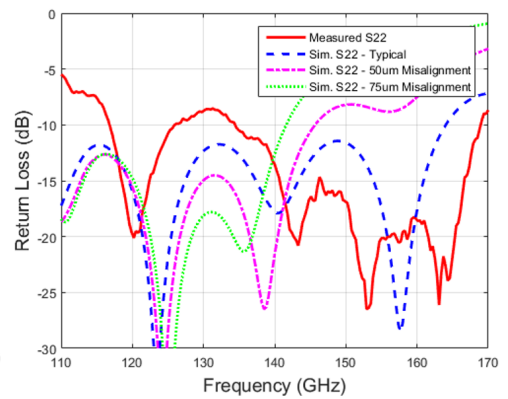
Figure 3.9: The return loss of the transition at the output WR-6.5 interface

Chapter 4

Linearly Tapered Slot Antenna Based Waveguide Transition

In this chapter, an on-chip MMIC-to-waveguide transition is realized based on LTSA structure. The antenna is implemented on a 50-um-thick GaAs substrate and placed in the E-plane of an air-filled D-band waveguide. The transition shows low insertion loss and covers the entire D-band. The proposed transition can be implemented directly on the MMIC and provides direct coupling to the waveguide without the need of any intermediate solutions. The transition also does not impose any limitations on MMIC size.

This chapter is organized as follows: Section 4.1 describes the details of the proposed transition. In section 4.2, two different techniques to minimize radiation loss are investigated and compared. Finally, in section 4.3, detailed 3D EM simulation results are presented and sensitivity to variations and alignment is discussed.

4.1   Design Methodology

The transition is based on LTSA structure [39] [40]. Figure 4.1 shows the proposed solution. The solution consists of an integrated antenna implemented on a 50-um-thick GaAs substrate. The structure is placed in the E-plane of an air-filled D-band waveguide.

In order to overcome the area limitation imposed by the waveguide dimensions, a 100-um slot is made through the waveguide's sidewalls as shown in figure 4.1. The slot is used to accommodate the MMIC portion on which the antenna is implemented, that way, the MMIC can have any arbitrary size independent of the waveguide dimensions. The drawback of this approach is that it allows waveguide modes to propagate through the circuit cavity. To mitigate this effect, a wall of Backside Vias (BSV) is implemented around the antenna to prevent field leakage within the substrate.
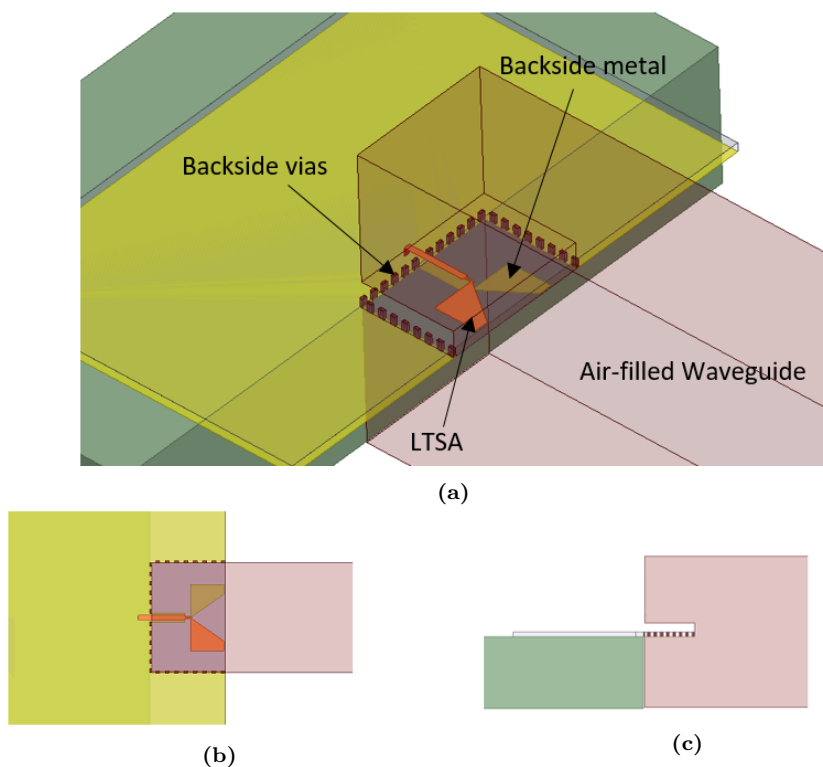
Figure 4.1: The proposed solution (a) 3D view (b) Top view (c) Side view
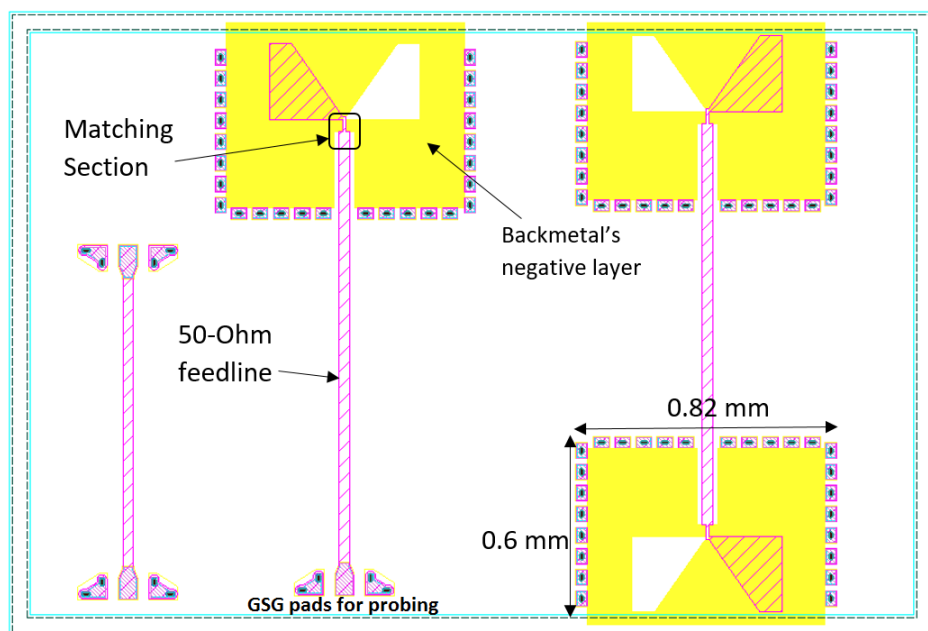
Figure 4.2: Chip layout

The antenna is implemented in a commercial GaAs process. The process provides two top metal layers and one back metal layer. The back metal has a dedicated mask and can be used to implement any structure. This feature allows the implementation of one of the sides of the antenna on one of the top layers and the other side on the back layer and hence achieve better E-field confinement within the substrate and better radiation to the waveguide as will be shown in simulation results in section 4.3.

The backside metal line feed for the antenna is connected to the ground plane outside the transition so that it provides a differential to single-ended microstrip transformation. This approach eliminates the need of a balun and hence reduces the overall loss of the transition. A matching section is introduced between the antenna and the 50-Ohm microstrip feeding line to compensate for the impedance discontinuity between them as shown in figure 4.2. The whole structure occupies an area of $0.82 \times 0.6 \ mm^2$. The antenna is implemented as both back-to-back and a single transition as shown in figure 4.2. Test structure for the microstrip line is included to be used for de-embedding line loss. It is noteworthy that the backside metal layer in this technology is defined as a negative layer which means that the layer is drawn where the metal should be removed as shown in figure 4.2.

4.2 Radiation Loss Mitigation

As discussed in the previous chapter, the presented transition similarly suffers from radiation losses. In this section, two techniques to mitigate radiation losses are investigated and compared in detail.
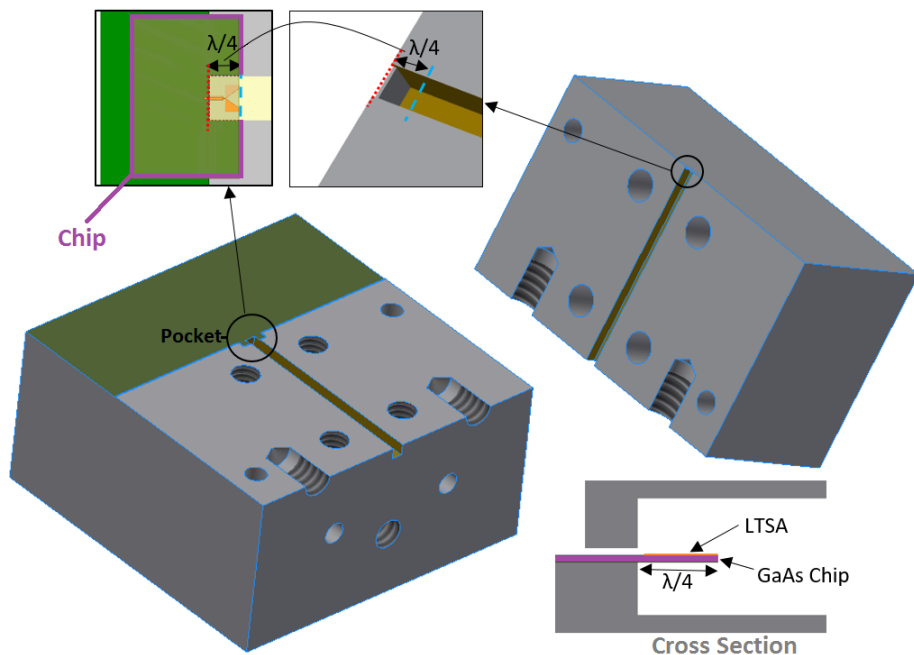

Figure 4.3: Split-block design of the mechanical structure

One technique to prevent radiation through the open end of the waveguide is to use a quarter-wave backshort implemented using a metal wall. Figure 4.3 shows the designed split-block structure used to test that technique. The structure consists of two parts: The bottom block accommodating the MMIC in a machined 50-um-deep pocket that extends 0.54 mm (Quarter wavelength) inside the waveguide channel and the top block including the other half of the waveguide channel and the backshort metal wall mentioned earlier to prevent radiation. A standard WR-6.5 flange is implemented on the sides of both blocks to interface with the outside world.

Another technique to stop back radiation is to use an artificial PMC realized by bed of nails similar to the work presented in chapter 3. The implemented bed of nails is shown in figure 4.4. Both techniques are simulated using HFSS and results are shown in figure 4.5. Results show that the bed of nails implementation has a lower in-band loss of 0.5 dB compared to 1 dB in the quarter-wave backshort case, however, the bed of nails structure exhibits lower bandwidth than the backshort case as shown in figure 4.5. The average return loss is 14 dB in the case of the bed of nails structure and 15 dB in the case of the quarter-wave backshort. Detailed simulation results of the quarter-wave backshort implementation are presented in the following section.

(a)   (b)
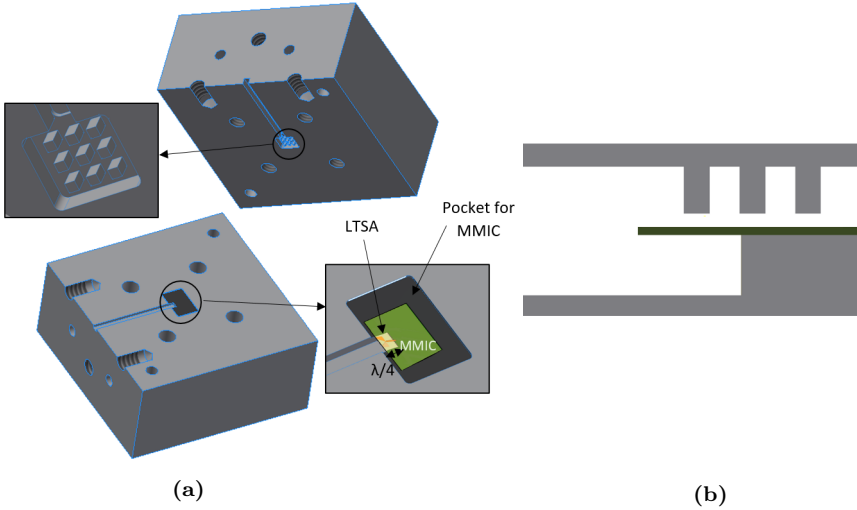
Figure 4.4: Bed of nails structure (a) 3D view (b) Side view
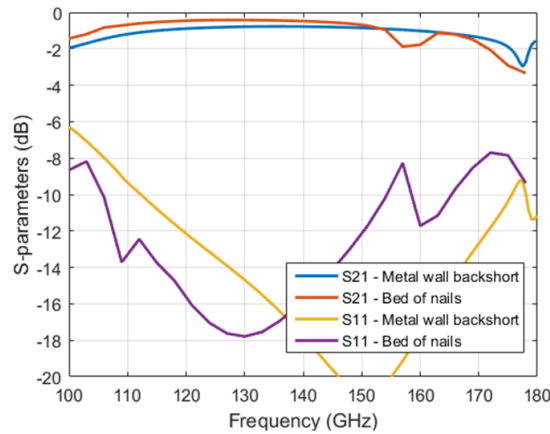
Figure 4.5: Comparison between the S-parameters of metal wall backshort and bed of nails implementations

4.3 Results and Conclusion

Simulations were performed using HFSS 3D electromagnetic simulator. E-field distribution simulation is shown in figure 4.6. The results show that the E-field is confined in the waveguide direction and no significant back radiation is present. This is due to the use of the BSVs and the backshort. The H-field distribution is also shown in figure 4.7.
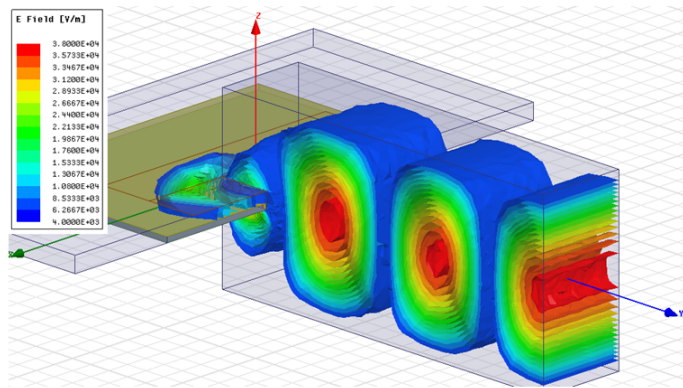
Figure 4.6: E-field magnitude distribution
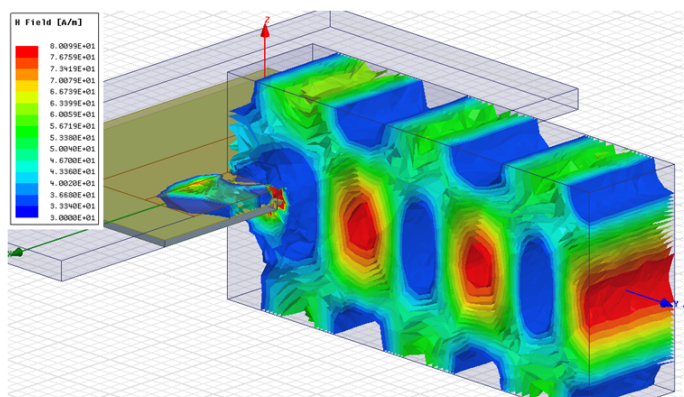
Figure 4.7: H-field magnitude distribution
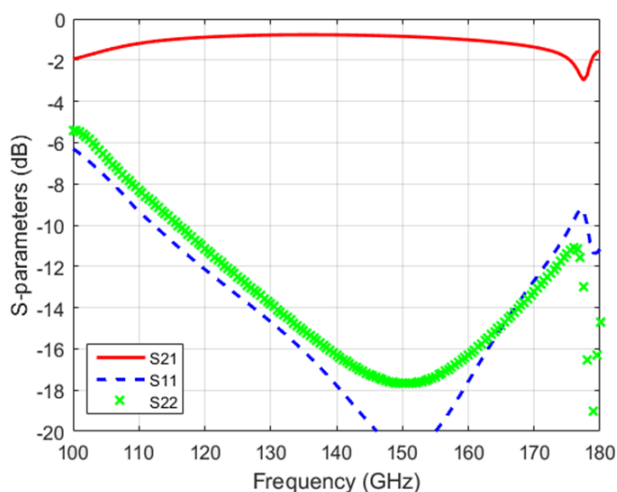
Figure 4.8: S-parameter simulation results

S-parameters of the complete transition are shown in figure 4.8. The whole transition exhibits a maximum insertion loss of only 1 dB covering the entire D-band ranging from 110 to 170 GHz. The minimum insertion loss within the same band is 0.85 dB. The 3-dB bandwidth is simulated to be from 93 to 197 GHz, however, at the higher edge of the band, higher order modes start to propagate and affect performance. Results also show an average return loss of 15 dB and a minimum of 9 dB.
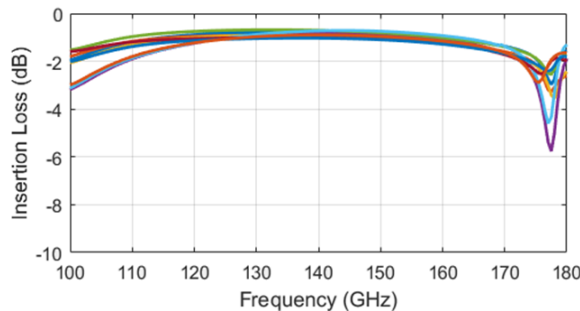
Figure 4.9: Transition's insertion loss when the MMIC position is shifted by -50 um to +50 um in both horizontal directions
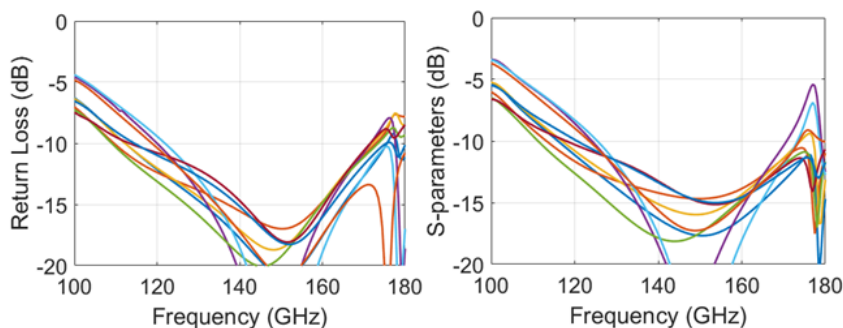
Figure 4.10: Transition's return loss when the MMIC position is shifted by -50 um to +50 um in both horizontal directions

In order to verify the transition's sensitivity to misalignment and positioning with respect to the waveguide opening, MMIC position was swept in both horizontal directions with an offset of up to +/- 50 um. Results shows that the transition is not sensitive to misalignment and performance shows only minor degradation at band edges as shown in figures 4.9 and 4.10.

A compact integrated MMIC-to-waveguide transition was presented in this chapter. The transition shows a maximum insertion loss of 1 dB and covers the frequency range 110 to 170 GHz. The proposed technique is generic and can be integrated with any circuitry. The transition provides low-loss wide-band connectivity for mmW systems and addresses integration challenges facing systems operating beyond 100 GHz.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis proposed several techniques for implementing mmW interconnects. eWLB packaging technology was investigated and two interconnects were demonstrated using this technology. The interconnect presented in section 2.2 was realized using a CPW-fed slot antenna radiating to a standard waveguide. Experimental results shows that the transition achieves an average insertion loss of 3 dB and a bandwidth of 22% at D-band. Another interconnect was proposed using the same technology in section 2.3. The presented interconnect consists of a slot antenna radiating to a HR Si taper inserted into an air-filled waveguide. Results show that the interconnect achieves an average insertion loss of 3.4 dB and a bandwidth of 26% at D-band. The presented interconnects represent a generic approach for packaging MMICs at mmW frequencies. Moreover, the presented work enables high-volume commercialization of mmW and THz systems as it is implemented in a low-cost commercial technology.

A low-loss D-band chip-to-waveguide transition has been demonstrated in chapter 3. The transition is realized using a unilateral finline coupling to a microstrip line that is implemented on a SiC substrate. The transition is suitable for on-chip integration with MMIC. Experimental results show that the transition achieves a low insertion loss of only 0.7 dB and covers a wide frequency range from 110 to 170 GHz. The transition presents a simple high-performance solution for packaging mmW systems supported by experimental results.

In chapter 4, a similar technique targeting direct implementation in MMIC technologies was proposed. A compact integrated waveguide transition based on LTSA was presented. The transition shows a maximum insertion loss of 1 dB and covers the whole D-band. The proposed technique can be integrated with any circuitry. The transition provides low-loss wide-band connectivity for mmW systems.

The work presented in this thesis addressed the integration challenges facing mmW systems and provided several solutions ranging from high-volume low-

cost interconnects with reasonable performance to low-loss high-performance solutions that provide higher integration. In addition, the presented interconnects do not require galvanic contacts and serve wide range of technologies and applications.

5.2   Future Work

The work done in the eWLB technology requires further expansion. Integrating the presented interconnects with MMICs and investigating the impact of the presented work and eWLB packaging in general on the overall performance of MMICs is of importance.

It would be interesting to integrate the work presented in chapters 3 and 4 with active circuitry at D-band and investigate the effects induced by such integration. The work presented in chapter 4 requires to be verified and supported by experimental results before that as well.

Acknowledgement

I would like to thank my family for the support they provided me through my entire life, without their love and encouragement; I would not have achieved what I achieved so far. I would like also to express my deep gratitude to Prof. Herbert Zirath, head of the Microwave Electronics Laboratory whose support, expertise and encouragement helped me finish this work. I would like also to thank my main supervisor Assoc. Prof. Vessen Vassilev for his guidance and continuous technical support and the long thorough discussions we had during the past 2 years of my study. My sincere thanks also goes to Asst. Prof. Zhongxia Simon He for all the valuable discussions that we had and for helping me get up to speed quickly and supporting my work continuously. I must also acknowledge Assoc. Prof. Vincent Desmaris for his help and the technical discussions we had.

I would like also to thank Dr. Sten Gunnarsson for his help and thorough technical feedbacks that helped me improve my work and keep everything on track.

Finally, I would like to thank all my colleagues for creating such a warm co-operative environment in the lab.

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