

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

VCSEL Cavity Engineering for High Speed  
Modulation and Silicon Photonics Integration

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Göteborg, Sweden 2018

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**Front cover illustration:** Optical micrograph of fully fabricated high-speed VCSELs on wafer.

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## Abstract

The GaAs-based vertical-cavity surface-emitting laser (VCSEL) is the standard light source in today's optical interconnects, due to its energy efficiency, low cost, and high speed already at low drive currents. The latest commercial VCSELs operate at data rates of up to 28 Gb/s, but it is expected that higher speeds will be required in the near future.

One important parameter for the speed is the damping of the relaxation oscillations. A higher damping is affordable at low data rates to reduce signal degradation due to overshoot and jitter, while lower damping is required to reach higher data rates. A VCSEL with the damping optimized for high data rates enabled error-free transmission at record-high data rates up to 57 Gb/s.

For future interconnect links it is of interest with tighter integration between the optics and the silicon-based electronics. Techniques to heterogeneously integrate GaAs-based VCSELs on silicon could potentially enable integrated multi-wavelength VCSEL arrays, thus increasing the data rate through wavelength division multiplexing. Heterogeneous integration of GaAs-based VCSELs would also benefit applications that need short-wavelength light sources, such as photonic integrated circuits for life sciences and bio photonics. Silicon-integrated short-wavelength hybrid-cavity VCSELs with up to 2.3 mW optical output power and 12 GHz modulation bandwidth, which enables data transmission at up to 25 Gb/s, are demonstrated by employing ultra-thin adhesive bonding. Further, a vertical-cavity silicon-integrated laser (VCSIL) with in-plane waveguide emission is demonstrated by employing an intra-cavity waveguide with a weak diffraction grating that couples light from the standing wave in the vertical cavity into an in-plane waveguide.

Keywords: Heterogeneous integration, high-speed modulation, large signal modulation, laser dynamics, on-chip laser source, optical interconnects, semiconductor lasers, silicon photonics, vertical-cavity silicon-integrated laser (VCSIL), vertical-cavity surface-emitting laser (VCSEL).



# List of Papers

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- [A] P. Westbergh, **E. P. Haglund**, E. Haglund, R. Safaisini, J. S. Gustavsson, and A. Larsson, “High-speed 850 nm VCSELs operating error free up to 57 Gbit/s,” *Electronics Letters*, vol. 49, no. 16, pp. 1021–1023, Aug. 2013. DOI: 10.1049/el.2013.2042.
- [B] **E. P. Haglund**, P. Westbergh, J. S. Gustavsson, and A. Larsson, “Impact of damping on high-speed large signal VCSEL dynamics,” *Journal of Lightwave Technology*, vol. 33, no. 4, pp. 795–801, Feb. 2015. DOI: 10.1109/JLT.2014.2364455.
- [C] **E. P. Haglund**, S. Kumari, P. Westbergh, J. S. Gustavsson, G. Roelkens, R. Baets, and A. Larsson, “Silicon-integrated short-wavelength hybrid-cavity VCSEL,” *Optics Express*, vol. 23, no. 26, pp. 33 634–33 640, Dec. 2015. DOI: 10.1364/OE.23.033634.
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*Other publications*

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Emanuel P. Haglund

*Göteborg*  
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# List of Abbreviations

<b>4-PAM</b>	4-level pulse amplitude modulation
<b>BCB</b>	benzocyclobutene
<b>BER</b>	bit error ratio
<b>BTJ</b>	buried tunnel junction
<b>CMOS</b>	complementary metal-oxide-semiconductor
<b>DBR</b>	distributed Bragg reflector
<b>DVS-BCB</b>	divinylsiloxane-bis-benzocyclobutene
<b>FEC</b>	forward error correction
<b>FIB</b>	focused ion beam
<b>GSG</b>	ground-signal-ground
<b>HCG</b>	high-contrast grating
<b>HPC</b>	high performance computer
<b>HVCL</b>	hybrid vertical-cavity laser
<b>ICP</b>	inductively coupled plasma
<b>MOCVD</b>	metal-organic chemical vapor deposition
<b>MPW</b>	multi-project wafer
<b>OMA</b>	optical modulation amplitude
<b>OOK</b>	on-off keying

<b>PCE</b>	power conversion efficiency
<b>PECVD</b>	plasma-enhanced chemical vapor deposition
<b>PIC</b>	photonic integrated circuit
<b>PL</b>	photoluminescence
<b>PRBS</b>	pseudo random bit sequence
<b>QW</b>	quantum well
<b>RIE</b>	reactive ion etching
<b>RIN</b>	relative intensity noise
<b>RT</b>	room temperature
<b>SCH</b>	separate confinement heterostructure
<b>SDM</b>	space-division multiplexing
<b>SEM</b>	scanning electron microscope
<b>SiP</b>	silicon photonics
<b>SOI</b>	silicon-on-insulator
<b>TJ</b>	total timing jitter
<b>VCSEL</b>	vertical-cavity surface-emitting laser
<b>VCSIL</b>	vertical-cavity silicon-integrated laser
<b>VNA</b>	vector network analyzer
<b>VOA</b>	variable optical attenuator
<b>WDM</b>	wavelength division multiplexing

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# Chapter 1

## Introduction

Today's lifestyle takes the connection to the Internet for granted. Connecting with friends and family through social networks, storing photographs, as well as streaming music and movies are just a few of the things we do online. Commonly this is referred to as cloud computing, as we use our smartphones, tablets, and computers etc. as terminals, while the actual processing and storage of the data is handled by huge data centers [1]. Since the computational capacity of a single computer is far from enough, these data centers consists of large amounts of interconnected servers, to provide simultaneous computing in the servers [2]. The parallelization technique has also been employed to build powerful high performance computers (HPCs). An example is the world's fastest (as of April 2018) supercomputer Sunway TaihuLight, that has over ten million cores [3].

Previously the interconnects have employed electrical copper cables, but the increasing amount of data transfer has forced the move to optical interconnects, due to the higher data rates, longer reach, and lower power consumption enabled by optical links [4]. The typical light source in such optical interconnects is the directly modulated GaAs-based vertical-cavity surface-emitting laser (VCSEL), due to its low-cost fabrication, circular beam profile matching the fiber core, energy-efficient operation, and high bandwidth at low drive currents [5]. Commercial VCSELs capable of data rates up to 28 Gb/s are currently available from several manufacturers [6]. However, data rates of 50 and even 100 Gb/s are expected in future standards, which will require even faster VCSELs.

To date, most of the optical interconnects ranges from a few meters up to a few hundred meters, but the majority of the links are below 30 m [7].

In the future it is expected that even shorter links, e.g. board-to-board and chip-to-chip interconnects, would benefit from the higher speed and efficiency of the optical interconnects [8]. However, this requires tighter integration between the electrical and the photonic integrated circuits (PICs) for feasible operation. Since the material of choice for electrical circuits, silicon, cannot be used to produce efficient light sources due to its indirect bandgap, several options are considered for both long and short haul communication, making use of hybrid, heterogenous and monolithic integration techniques, that are compatible with standard complementary metal-oxide-semiconductor (CMOS) fabrication. The most mature technique is the hybrid integration, where complete devices are integrated to the PIC [9], while heterogenous techniques relies on bonding of active layers that are processed directly on the target substrate [10]. Monolithic integration techniques would require increased quality of direct bandgap material grown directly on silicon to become an feasible option [11].

For long haul communication silicon photonics (SiP) PICs where long-wavelength lasers are needed, InP-based lasers integrated to the silicon-on-insulator (SOI) waveguide platform are preferred [11]. However, it should be noted that the competing and already commercially available InP-based PIC waveguide technology have been employed to manufacture transceiver PICs with impressive performance [12]. While for the shorter reaches, where the short-wavelength GaAs-based VCSEL technology is dominating the market due to cost and efficiency reasons, it becomes interesting to pursue the integration of VCSELs onto a silicon-based PIC platform. However, as SOI waveguides absorb short-wavelength light, it becomes necessary to use the complimentary platform based on silicon nitride (SiN) waveguides when considering GaAs-based light sources. Integration of GaAs-based VCSELs to such PICs would also benefit applications that require a short-wavelength light source, such as life sciences and bio photonics, where for example the presence of biological substances could be detected using microresonators [13].

## 1.1 State-of-the-Art of High-Speed VCSELs

Significant progress has been made the last years on increasing the bandwidth and data rates possible for directly modulated GaAs-based VCSELs. In 2007 researchers at NEC demonstrated 1090-nm VCSELs with 24 GHz bandwidth capable of transmitting data at rates up to 40 Gb/s [14]. A few years later in 2011 researchers at TU Berlin demonstrated 980-nm VCSELs operating up to 44 Gb/s [15]. In 2013, 850-nm VCSELs developed at Chalmers with 28 GHz

bandwidth [16] could support data rates up to 57 Gb/s at room temperature (RT, Paper A) and 40 Gb/s at 85°C [17]. By employing driver and receiver circuits with equalization from IBM these VCSELS could transmit data at rates up to 71 Gb/s at 28°C and 50 Gb/s at 90°C [18, 19]. In 2014, researchers at TU Berlin demonstrated 980-nm VCSELS operating up to 50 Gb/s at 25°C and 46 Gb/s at 85°C [20]. The latest generation of 850-nm VCSELS from Chalmers demonstrated bandwidths of up to 30 GHz and energy dissipation of less than 100 fJ/bit up to 50 Gb/s in 2015 [21]. Using a similar epitaxial structure as the 850-nm VCSELS developed at Chalmers in [16, 17] and Paper A, researchers at UIUC were in 2016 able to demonstrate 850-nm VCSELS with 29 GHz bandwidth at 25°C and 25 GHz at 85°C, which enabled data transmission at up to 57 Gb/s at 25°C and 50 Gb/s at 85°C [22]. Later that same year 980-nm VCSELS from TU Berlin were shown to operate at 50 Gb/s at ambient temperatures up to 75°C, while at 25°C they could operate at up to 52 Gb/s [23]. In 2017 1060-nm VCSELS, intended for interconnects with longer reach, developed at Chalmers with 22 GHz bandwidth at 25°C and 16 GHz at 85°C enabled the demonstration of data transmission at up to 50 Gb/s at 25°C and 40 Gb/s at 85°C [24]. These VCSELS also enabled 25 Gb/s transmission over 1 km 1060-nm optimized multimode fiber [25]. Researchers at TU Berlin demonstrated small-aperture 980-nm VCSELS with up to 31 GHz bandwidth at 25°C and 25 GHz at 85°C in 2017 [26]. However, these small-aperture VCSELS have not been showed to support data transmission yet.

## 1.2 State-of-the-Art of Si-Integrated VCSELS

Heterogeneous integration of InP-based VCSELS on silicon was first demonstrated using optical pumping below RT in 2013 by researchers at NAIST [27], while electrically pumped VCSELS with almost 1 mW output power and enabling data rates up to 5 Gb/s were demonstrated in 2015 by researchers at UC Berkeley [28]. Later in 2015, heterogeneously integrated GaAs-based VCSELS on silicon were demonstrated with output powers up to 1.6 mW at 25°C in Paper C. These VCSELS were shown to support data rates up to 20 Gb/s (Paper D). By adjusting the operating wavelength to better fit the gain characteristics of the active region in Paper E, the output power was increased to 2.3 mW at 25°C and 0.9 mW at 85°C, which enabled data transmission at up to 25 Gb/s at 25°C and 10 Gb/s at 85°C.

The ultimate goal of integrating VCSELS onto silicon is to achieve a light source for in-plane PIC waveguides. Prior to the recent demonstration of in-plane waveguide emission from a vertical-cavity laser in Paper E, there is,

to the best of the author's knowledge, only one demonstration of a silicon-integrated vertical-cavity laser with waveguide emission. This is an InP-based laser operated under pulsed optical pumping developed at DTU [29]. Later this laser was shown to have 27 GHz of bandwidth [30], although still under pulsed optical injection, which means that no parasitics or thermal effects are affecting the measured bandwidth.

### 1.3 Outline of Thesis

The thesis is organized as follows. The basic operation of VCSELs, and to some extent semiconductor lasers in general, is introduced in Chapter 2, while the dynamics of VCSELs are discussed in Chapter 3, which also covers the high-speed measurement techniques used for characterization. Light source integration on silicon photonics is presented in Chapter 4, while the integration of hybrid vertical-cavity lasers is discussed in Chapter 5. Chapter 6 describes the VCSEL and hybrid vertical-cavity laser fabrication processes, and finally a future outlook is given in Chapter 7.

## Chapter 2

# Vertical-Cavity Surface-Emitting Lasers

The vertical-cavity surface-emitting laser (VCSEL) is a semiconductor laser with its light output beam perpendicular to the surface. Today the VCSEL is a widely used laser source, but the early development had a slow start after the first experimental demonstration of a laser by Maiman in 1960 [31] and the first semiconductor laser in 1962 [32] by Hall *et. al.* Although Melngailis demonstrated a laser with its emission perpendicular to the substrate already in 1965 [33], the VCSEL is typically considered to have been invented by Iga in 1977 [34] and first demonstrated in 1979 by Soda and Iga *et. al.* [35]. Later Iga's group demonstrated the first room-temperature (RT) VCSEL in 1984 [36] as well as the first RT continuous-wave (CW) VCSEL in 1988 [37]. At Bell Labs, Jewel and Lee *et. al.* incorporated a GaAs-based quantum well in a cavity formed by monolithic reflectors [38] and demonstrated a low-threshold (1.3 mA) VCSEL under pulsed electrical injection at RT in 1989 [39] and finally also CW operation that same year [40]. The next year 1990, Coldren's group were able to achieve sub-milliampere threshold currents [41, 42].

In 1996, Honeywell (now Finisar) commercialized the first VCSELs, which had proton-implanted current apertures [43, 44]. This lateral current confinement technique was first demonstrated by Tai *et. al.* in 1989 [45]. Nowadays, the most commonly used scheme is an oxide aperture that confines both photons and electrons. Such an aperture is formed by selective lateral oxidation of high Al-content AlGaAs material. The native oxide was discovered by Holonyak's group in 1990 [46] and was first implemented as an oxide aperture

in VCSELs by Deppe's group in 1994 [47]. Choquette *et. al* demonstrated an all-semiconductor oxide-aperture VCSEL later that same year [48]. Nowadays, the applications of VCSELs ranges from optical communication, to high power light sources for e.g. illumination and surface treatments [49], and sensors for e.g computer mice [50], proximity sensors in smartphones [51], and the recent facial recognition system in Apples latest iPhone [52].

After this brief overview of the history of VCSELs, this chapter will introduce the basic operation of VCSELs, including its building blocks.

## 2.1 Semiconductor Lasers

Laser is an acronym for light amplification by stimulated emission of radiation. Amplification (or gain) is achieved by a quantum mechanical process that allows a photon to stimulate the deexcitation of an excited electron from a higher to a lower energy state if the photon energy corresponds to the energy difference between the two states. When the electron is deexcited a copy (same frequency, phase, and direction) of the stimulating photon is emitted. This process was predicted theoretically by Einstein in 1917 [53], after first theorizing the quantum nature of light and the photoelectric effect in 1905 [54], building on Planck's black-body radiation theory from 1901 [55]. A laser also needs optical feedback (even though it is not indicated in the acronym), which is typically achieved by inserting the gain medium in an optical resonator (or optical cavity) consisting of semitransparent mirrors. Lasing will occur if sufficient energy is supplied to the gain medium within the cavity.

To achieve lasing two criteria have to be met. The gain should be sufficient to compensate for all optical losses in the cavity (internal and mirror losses) and the phase of the field must repeat itself after one round-trip. The threshold material gain needed for lasing to start is given by

$$g_{\text{th}} = \frac{1}{\Gamma} [\alpha_i + \alpha_m] = \frac{1}{\Gamma} \left[ \alpha_i + \frac{1}{2L} \ln \left( \frac{1}{R_1 R_2} \right) \right], \quad (2.1)$$

where  $\Gamma = V_a/V_p$  is the optical confinement factor (i.e. the overlap between the active region and the optical field, where  $V_a$  is the volume of the active region and  $V_p$  is the lasing mode volume),  $\alpha_i$  and  $\alpha_m$  are the internal and mirror losses, respectively,  $L$  is the cavity length, and  $R_1$  and  $R_2$  are the mirror power reflectivities. In a semiconductor laser, the gain is provided by transitions across the bandgap, from conduction band states to valance band states. The bandgap energy of the semiconductor material will therefore determine the wavelength (or color) of the output light. The active region

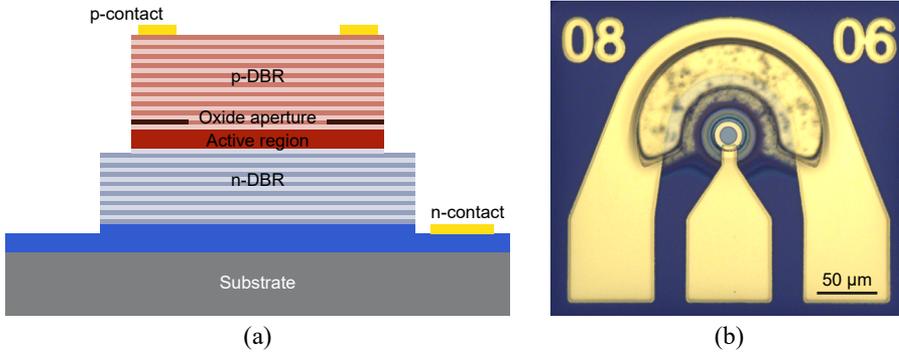


Fig. 2.1. (a) Schematic cross-section of a VCSEL, and (b) microscope top view of a VCSEL on wafer.

of a semiconductor laser is typically an intrinsic region sandwiched between  $p$ - and  $n$ -doped material that are designed to have higher bandgap than the intrinsic active material, which provides confinement of the carriers to the active region. By injecting carriers (electrons and holes), they accumulate in the active region. The injected current needed to reach the threshold gain in (2.1) is called the threshold current  $I_{th}$ .

The second criteria to achieve lasing is the phase condition, given by

$$\exp\left(-j\frac{2\pi}{\lambda_0/n_{eff}} \cdot 2L\right) = 1 \quad \Rightarrow \quad \lambda_0 = \frac{2Ln_{eff}}{m}, \quad (2.2)$$

where  $\lambda_0$  is the lasing wavelength (in vacuum),  $n_{eff}$  is the effective refractive index of the cavity, and  $m$  is an integer number.

The simplest possible semiconductor laser is the Fabry-Perot laser, which is an edge-emitting laser. The reflections at the cleaved facets, due to the high refractive index contrast between semiconductor material and air, give enough feedback to achieve lasing together with the high gain over a relatively long distance along the cavity.

## 2.2 Mirror Reflectivity

The VCSEL is a semiconductor laser where the optical cavity is oriented perpendicular to the semiconductor substrate surface, in contrast to edge-emitters. This means that light is emitted from the top or bottom surface,

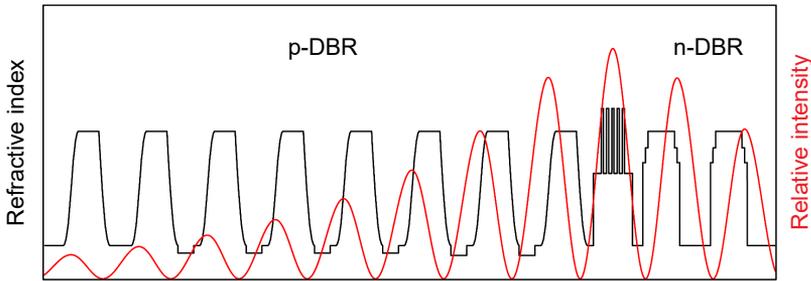


Fig. 2.2. Refractive index profile and simulated optical intensity along the optical axis of the VCSEL cavity in Paper A. Adopted from [57].

enabling simple wafer level testing of devices. However, since the cavity is vertical, the length over which the photons can interact with the gain medium is very short (tens of nanometers) resulting in small round-trip gain. This requires very high reflectivities ( $>99\%$ ) from the two mirrors defining the cavity to ensure that the optical losses in the cavity are sufficiently low [56]. A schematic cross-section and a microscope top view of a VCSEL can be seen in Fig. 2.1.

The reflectivity needed is typically achieved by using distributed Bragg reflectors (DBRs). A DBR consists of a number of pairs of alternating  $\lambda/4$ -thick layers, with different refractive index. Typically, DBRs for VCSELs are either epitaxially grown semiconductors or consist of dielectric materials. The number of pairs needed for  $>99\%$  reflectivity depends on the refractive index contrast between the layers. The materials available for epitaxial DBRs have relatively low refractive index contrast which requires  $\sim 20$ – $30$  DBR pairs for sufficient reflectivity [58], while dielectric materials have the possibility for much larger refractive index contrast and typically require less than 10 DBR pairs for sufficient reflectivity. The optical standing wave in a cavity formed by two semiconductor DBRs is shown in Fig. 2.2.

## 2.3 Gain

For sufficient gain the active region consists of multiple quantum wells (QWs) in a separate confinement heterostructure (SCH), where carriers are trapped leading to a high carrier density. The number of QWs employed in the active region is a tradeoff between a high aggregate material gain from many QWs and a high optical confinement by being able to pack the QWs around the

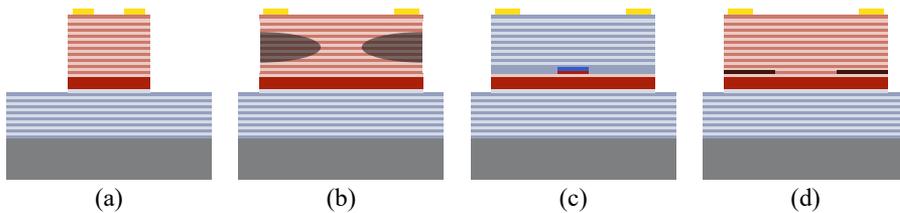


Fig. 2.3. Transverse confinement schemes: (a) etched air post, (b) ion implantation, (c) buried tunnel junction, and (d) oxide aperture.

antinode of the cavity standing-wave optical field [59]. At the same time, the number of QWs and their thickness affects the differential gain at the operating current density [60], as the differential gain depends on the carrier density. This makes it possible to optimize the number of QWs such that the maximum differential gain occurs at an achievable current density above threshold. Typically, around 3–5 QWs are used in state-of-the-art high-speed VCSELs.

Traditionally 850-nm VCSELs have employed GaAs QWs, but employing strained InGaAs QWs increases the differential gain, which is advantageous to reach higher speed [61].

## 2.4 Transverse Confinement

The photons are confined to the active region vertically by the two DBRs. Nevertheless, both carriers and photons need to be transversely confined to the center of the active region. Some examples of transverse confinement schemes are etched air post [39], ion implantation [62], buried tunnel junction (BTJ) [63], and oxide aperture [47], as illustrated in Fig. 2.3. The etched air post (Fig. 2.3a) is obviously the simplest solution where the optical field is confined by the large refractive index contrast between semiconductor and air, but scattering and carrier recombination at the semiconductor-air interface cause problems. Defining the aperture by implanting ions (Fig. 2.3b), usually protons, was as already noted successfully used for the first commercial VCSELs. The implanted regions become highly resistive, which confines the carriers to the center. However, the implantation does not change the refractive index significantly causing the optical field to be confined by gain guiding and thermal lensing (caused by the temperature rise in the active region under operation, which changes the refractive index slightly), which will cause the

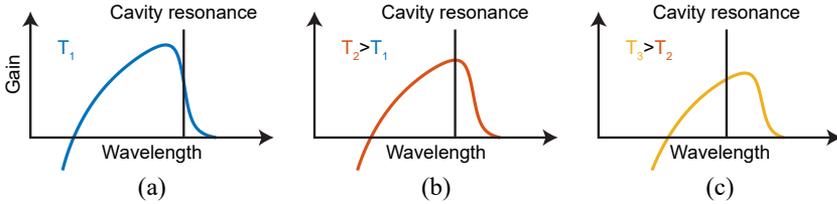


Fig. 2.4. Cavity resonance detuning with respect to the gain peak for increasing temperature.

modal behavior to depend on the injection current [64]. The BTJ (Fig. 2.3c) provides both optical and electrical confinement and has been successfully implemented for long-wavelength InP-based VCSELs, but it has proven more difficult to implement at shorter wavelengths [65], although InGaAs-based BTJ VCSELs at 1090 nm have been demonstrated [14]. Oxide-confined GaAs-based VCSELs (Fig. 2.3d) utilize selective oxidation of high Al-content AlGaAs layers to form the oxide apertures (in contrast to InP-based VCSELs that lack a high quality oxide), which provides both electrical and optical confinement since the resulting oxide is isolating and has lower refractive index than the non-oxidized material. Apart from the excellent high-speed properties presented in Section 1.1, oxide-aperture VCSELs have yielded power conversion efficiencies (PCEs) of more than 60% [66], and has been the confinement scheme of choice for this work.

## 2.5 Temperature Effects

Since the VCSEL cavity is short (on the order of the wavelength), the emission wavelength is set by the cavity resonance rather than the gain peak. The emission wavelength is therefore red shifting with temperature, which increases with current due to resistive Joule heating, due the temperature dependence of the refractive index of the semiconductor material. This causes the cavity resonance wavelength of GaAs-based VCSELs to increase with  $\sim 0.06\text{--}0.09\text{ nm}/^\circ\text{C}$ , while the gain peak is red shifted with  $\sim 0.32\text{--}0.33\text{ nm}/^\circ\text{C}$  due to bandgap shrinkage [67]. Obviously, the best situation arises when the cavity resonance is aligned with the gain peak, where the lowest threshold current is obtained, but the different red-shift rates will eventually position the gain peak too far away from the cavity resonance, increasing the threshold current too much for lasing to occur. To enable operation at elevated temperatures the cavity

resonance is often detuned with respect to the gain peak, i.e. the cavity resonance is red shifted with respect to the gain peak at room temperature, causing the resonance and gain to align at elevated temperature, see Fig. 2.4. This technique has been used to be able to operate well above 100°C [68].

To obtain a specific detuning it is important to know the gain peak wavelength of the QWs. Commonly, the gain peak is specified by the photoluminescence (PL) peak wavelength, as this can be easily measured during the calibration of the epitaxial growth. However, as the PL is a result of spontaneous emission, while the gain is a result of stimulated emission, the PL peak is different from the gain peak [69]. At 850 nm it can be estimated that the gain peak is red shifted with  $\sim 12$  nm from the measured PL peak of the QWs (Paper E). The red shift at other wavelengths scales accordingly [70].



# Chapter 3

## VCSEL Dynamics

The VCSEL is typically directly modulated with large signals. To improve the performance it is important to be able to predict the speed limiting factors. This chapter introduces the VCSEL small signal dynamics and briefly discusses some considerations for large signal operation. Further, the measurement techniques used to study both small and large signal dynamics are presented.

### 3.1 Small Signal Dynamics

It follows from the standard coupled rate equations that the intrinsic small-signal modulation response of a single mode laser is that of a damped second order system [71]. However, VCSELs are typically multimode, but due to the high overlap of the transverse modes they can still be treated as a single mode [72]. By also accounting for the parasitics by an additional pole, the transfer function is given by [71]

$$H(f) = \text{const.} \cdot \frac{f_r^2}{f_r^2 - f^2 + j\frac{f}{2\pi}\gamma} \cdot \frac{1}{1 + j\frac{f}{f_p}}, \quad (3.1)$$

where  $f_r$  is the resonance frequency,  $\gamma$  the damping factor, and  $f_p$  the parasitic cut-off frequency. The resonance frequency is given by

$$f_r = \frac{1}{2\pi} \sqrt{\frac{v_g \cdot (\partial g / \partial n) \cdot S}{\tau_p \cdot (1 + \epsilon S)}}, \quad (3.2)$$

where  $v_g$  is the group velocity,  $\partial g / \partial n$  the differential gain,  $S$  the photon density,  $\tau_p$  the photon lifetime, and  $\epsilon$  the gain compression factor. The increase of

the resonance frequency with the photon density is typically quantified by the  $D$ -factor defined as

$$D \equiv \frac{f_r}{\sqrt{I - I_{\text{th}}}}, \quad (3.3)$$

where  $I - I_{\text{th}}$  is the injected current above the threshold. The damping factor in (3.1) is given by

$$\gamma = K \cdot f_r^2 + \gamma_0, \quad (3.4)$$

where  $\gamma_0$  is the damping offset and the  $K$ -factor is given by

$$K = 4\pi^2 \left( \tau_p + \frac{\varepsilon}{v_g \cdot (\partial g / \partial n)} \right). \quad (3.5)$$

## 3.2 Bandwidth Limitations

The intrinsic bandwidth (without parasitics and thermal effects) is limited by the  $K$ -factor through

$$f_{3\text{dB,max}} = \frac{2\pi\sqrt{2}}{K} \quad (3.6)$$

and is typically exceeding 30 GHz [73]. In Fig. 3.1 the extracted intrinsic response of the VCSEL used in Paper A is shown to have a bandwidth exceeding 50 GHz (blue line). Due to thermal effects and parasitics, bandwidths at these levels are not reached in practice. Thermal effects will eventually limit the buildup of photon density, setting a limit on the maximum resonance frequency, consequently limiting the bandwidth to 33 GHz in Fig. 3.1 (orange line). The parasitics (resistance and capacitance) will reduce the actual modulation current through the active region at frequencies above the cut-off frequency, resulting in an effective bandwidth of  $\sim 24$  GHz (yellow line).

This means that it is important to design VCSELs with low heat generation, good heat conductivity, low resistance, and low capacitance to overcome the thermal effects and the parasitics. Better heat conductivity can be obtained by employing binary alloys in the DBR [74]. The DBR resistance can be reduced by graded interfaces and modulation doping or by bypassing the DBR using intra-cavity contacts [66]. The parasitic capacitance across the oxide layer can be reduced by including additional oxide layers, which will effectively increase the oxide thickness and reduce the capacitance [75–77].

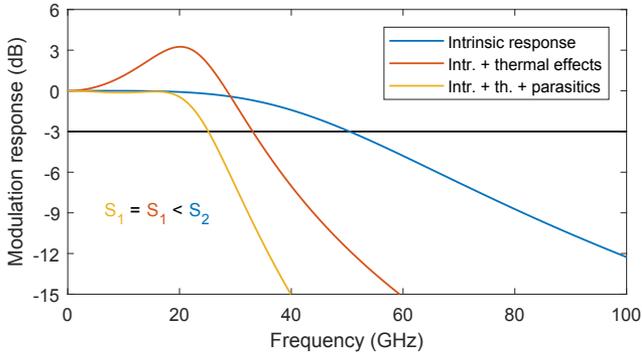


Fig. 3.1. Intrinsic and extrinsic modulation response extracted from the VCSEL used in Paper A with  $K$ - and  $D$ -factors of  $0.17 \text{ ns}$  and  $9.0 \text{ GHz}/\text{mA}^{1/2}$ , respectively, along with a parasitic pole,  $f_p \approx 17 \text{ GHz}$ . The three curves are obtained at different bias conditions (photon densities,  $S_1$  and  $S_2$ ).

### 3.3 Large Signal Dynamics

Since the  $K$ -factor depends on the photon lifetime,  $\tau_p$ , it is possible to tune the  $K$ -factor by adjusting the photon lifetime. It is possible to reduce the photon lifetime by a shallow surface etch of the top DBR layer, since the photon lifetime is set by the reflectivities of the DBRs. This will give a slightly out of phase reflection at the semiconductor-air interface, effectively lowering the DBR reflectivity and consequently also the photon lifetime and  $K$ -factor [78].

In Paper B, this effect was utilized to investigate the impact of damping (through the  $K$ -factor) on high-speed large signal VCSEL dynamics. It was found that the optimum damping depends on the data rate. Lower data rates can afford higher damping, whereas to achieve higher data rates it is crucial with lower damping to reach the bandwidth and output power needed in the link. However, too low damping will cause excessive overshoot and ringing, which is detrimental for the signal quality.

### 3.4 Modulation Formats

Traditionally, VCSEL-based links have employed simple two-level modulation formats to transfer data streams, where the ones and zeros are represented by setting the VCSEL in either its on- or off-state. This binary modulation format

is called on-off keying (OOK). However, to meet the increasing bandwidth demands, future standards like Ethernet 50GBASE-SR and 200GBASE-SR4 [79], Fibre Channel 64GFC-SW and 256GFC-SW4 [80], and InfiniBand HDR (50G, 200G, and 600G) [81] will employ 4-level pulse amplitude modulation (4-PAM) (where every symbol carries two information bits) with forward error correction (FEC) codes. Both Ethernet and InfiniBand standards will include a Reed Solomon (544,514) FEC code [82] and have specified pre-FEC bit error ratio (BER) limits at  $2.4 \cdot 10^{-4}$  and  $1.09 \cdot 10^{-4}$ , respectively, to achieve a post-FEC BER better than  $10^{-15}$  [79, 80]. These standards will operate at lane rates around 50 Gb/s, which seems feasible as the VCSELs in [16, 17] and Paper A recently were shown to operate error-free up to 68 Gb/s using OOK and up to 110 Gb/s using 4-PAM over 100 m wideband multimode fiber with the use of transmitter equalization [83].

The transition from OOK to 4-PAM does double the spectral efficiency, but it comes at a price, as a 4.8 dB sensitivity penalty is introduced for 4-PAM compared to OOK at the same symbol rate [84], while a 3.3 dB sensitivity penalty is introduced at the same data rate [85]. This means that an increased optical modulation amplitude (OMA) is needed to achieve similar link budgets as with OOK. Further, the introduction of more levels tightens the tolerances on relative intensity noise (RIN), which arises from spontaneous emission being coupled into the lasing mode [69], and total timing jitter (TJ), that decreases the timing margin between symbols where the data can be retrieved [86].

The VCSEL photon lifetime has an impact on 4-PAM performance, as the photon lifetime affects both the modulation response, RIN, and OMA. A recent study (similar to Paper B, but on 4-PAM instead of OOK) showed that longer photon lifetimes are favorable for 4-PAM signaling as the longer photon lifetime provides sufficient damping of the modulation response and suppresses RIN, even though sacrificing the OMA [87]. These results are consistent with the future VCSEL designs for 4-PAM operation that is considered by the VCSEL industry [88].

## 3.5 High-Speed Measurements

In order to characterize the VCSELs high-speed properties both small and large signal measurements have to be performed. The small signal modulation response provides data that allows for fitting of the theoretical transfer function in Section 3.1, while the large signal experiments are closer to the real application of data transmission.

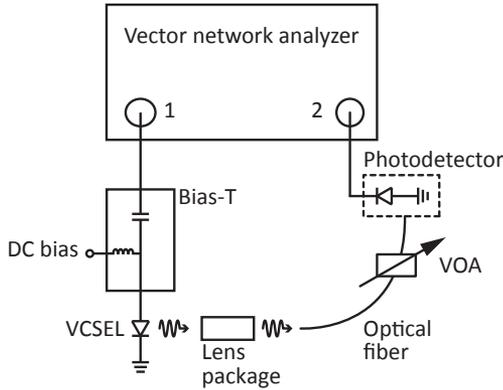


Fig. 3.2. Measurement setup for the small signal modulation response.

### 3.5.1 Small Signal Modulation Response

The small signal modulation response ( $S_{21}$ ) is measured using a vector network analyzer (VNA) connected to the VCSEL through a bias-T to allow DC biasing. By employing VCSEL bondpads that are matching the ground-signal-ground (GSG) probe pitch, the VCSEL can be probed directly on wafer. The output light from the VCSEL is coupled into a short multimode fiber using either an anti-reflection coated lens package or a butt-coupled bare fiber tip. The fiber is connected through a variable optical attenuator (VOA) to a high-speed photodetector connected to the VNA. The VOA is included to avoid saturating the detector. The measured data is then corrected for the response of the probe and detector before the transfer function (3.1) is fitted to the response. From the fit the  $K$ - and  $D$ -factors can be extracted. A schematic of the measurement setup can be seen in Fig. 3.2.

### 3.5.2 Large Signal Data Transmission

To perform large signal data transmission experiments an OOK signal consisting of pseudo random bit sequences (PRBSs) from a pattern generator is amplified and fed to the VCSEL through a bias-T and a GSG probe. The light is coupled into a multimode fiber connected to a photoreceiver through a VOA. The electrical signal from the photoreceiver is connected to an oscilloscope to record eye diagrams (an overlay of the signal waveform) or an error analyzer synchronized with the pattern generator to count the number of errors in the

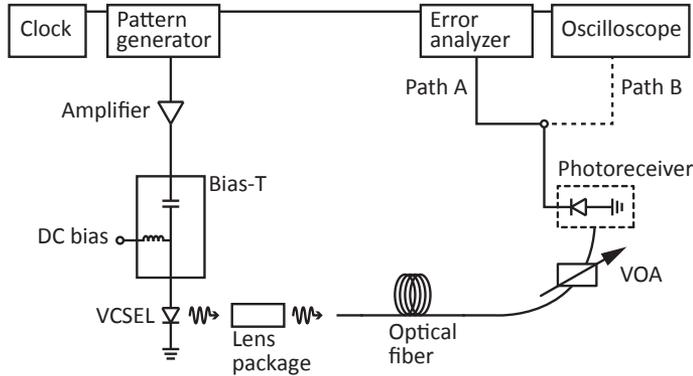


Fig. 3.3. Large signal data transmission setup. Path A is used to measure BERs, while path B is used to record eye diagrams.

received signal. A schematic of the setup is shown in Fig. 3.3. By relating the number of errors to the total number of bits the bit error ratio (BER) can be calculated. For very low BERs, the time needed to accumulate errors is very long. For reasonable measurements times it is therefore necessary to use statistical methods. It is required that  $N_{\text{bits}}$  is detected without any error to ensure a BER below  $p$  with a statistical confidence  $c$ , where  $N_{\text{bits}}$  is given by [89]

$$N_{\text{bits}} = -\frac{\ln(1-c)}{p}. \quad (3.7)$$

Typically a statistical confidence of 95% is required, which for a BER below  $10^{-12}$  (often defined as error-free) require  $3 \cdot 10^{12}$  error-free bits, which corresponds to measurement times of 5 and 1 min at 10 and 50 Gb/s, respectively. However, in this work  $6 \cdot 10^{12}$  error-free bits were required, corresponding to a BER below  $5 \cdot 10^{-13}$  with 95% confidence or alternatively a BER below  $10^{-12}$  with 99.75% confidence.

## Chapter 4

# Silicon Photonics Integration

Silicon photonics (SiP) has attracted significant attention since the mid-1980s [90, 91]. The vision from the start has been to realize photonic integrated circuits (PICs, or “superchips”, as they were called) including both optical and electrical circuits on silicon [92–94]. The main reason to pursue SiP PICs is the potential to integrate many functions in a PIC that can be produced in high volumes at low cost in CMOS fabs. Today SiP PIC platforms for both long and short wavelengths are becoming mature [95, 96], and most basic building blocks, i.e. low-loss waveguides, on- and off-chip couplers, modulators, and detectors, etc. are already available [97]. The applications of the SiP PIC platforms of the different flavors ranges from coherent optical communication [98] to sensing [99] and spectroscopy [100]. Luxtera has already commercialized a SiP transceiver [101], while several foundries and consortiums like IMEC [102] and AIM Photonics [103] offer multi-project wafer (MPW) runs, making it possible to share the development cost among several users. Nevertheless, the Holy Grail of SiP PICs, efficient on-chip light generation, is still an open question [104]. A possible route is heterogeneous integration of direct bandgap III-V material that can provide the optical gain needed. The rest of this chapter will introduce heterogenous integration and applications that would benefit from a short-wavelength on-chip light source.

## 4.1 Heterogeneous Integration

Integration of lasers onto a SiP PIC can be made in different ways [105, 106]. The laser can be processed on its native substrate and transferred to the PIC using flip-chip techniques [107–113] or the III-V material can be grown directly on the Si substrate [114, 115]. However, flip-chip techniques require stringent alignment of the individual lasers, while direct growth of high quality III-V material has proven difficult. An alternative technique is bonding of epitaxial III-V films onto the PIC, which can be processed after bonding exploiting lithographic alignment techniques. This is referred to as heterogeneous integration.

The bonding can be either direct (using Van der Waals forces) or adhesive [116]. Adhesive bonding has the advantage of being more resistant against surface roughness and contamination. This work (Paper C–F) has been focused on heterogeneous integration of short-wavelength VCSELs (or VCSEL-like lasers), where the epitaxial layers have been transferred to a reflector on a Si substrate using ultra-thin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding [117]. The most mature SiP platform is based on silicon-on-insulator (SOI) optical waveguides [118]. However, SOI waveguides absorb short-wavelength light, which makes the silicon nitride (SiN) waveguide [119] platform, with similar properties and CMOS-compatibility [120], an attractive choice for integrated GaAs-based lasers.

## 4.2 Applications of Si-Integrated GaAs-Based Lasers

As the distance where it is beneficial to transit from traditional electrical interconnects to optical interconnects is decreasing with increasing lane rates, a low-cost and low-power optical transmitter becomes increasingly attractive for the shortest distances, like intra-chip, chip-to-chip and board-to-board links [116]. A possible candidate as light source for such optical links is the integrated GaAs-based laser, which has the potential for high-speed communication and energy-efficient operation [21]. If such a light source was integrated on a PIC, it could be possible with tighter integration of several transmitters either using space division multiplexing [121] or wavelength division multiplexing (WDM) [122].

Another application is bio sensing through spectroscopy, where the light from the integrated laser is probing a microresonator that has been chemically functionalized to react to the presence of a specific biological molecule. By using

a functionalized material that changes its refractive index, and consequently also the microresonator resonance wavelength, it becomes possible to track when specific biological molecules binds to the PIC surface by sweeping the wavelength of an on-chip laser across the resonance [99]. One specific reason to use an integrated GaAs-based light source for such a sensor is the therapeutic window that ranges from 750 to 930 nm, where the photo-damage of cells is minimal and the water absorption negligible [100].



## Chapter 5

# Hybrid Vertical-Cavity Lasers

As discussed in the previous chapter it would be beneficial for several applications in different fields with an on-chip GaAs-based light source for SiP PICs. This chapter introduces the concept of vertical-cavity lasers integrated onto a SiN PIC platform, which has been developed in collaboration between Chalmers and Ghent University. The concept is based on a GaAs-based “half-VCSEL” epitaxial structure, containing a DBR and an active region, that is transferred to a reflector on silicon, resulting in a hybrid vertical-cavity laser (HVCL) with surface-emission (i.e. a hybrid-cavity VCSEL), see Fig. 5.1(a). The hybrid cavity means that the optical field extends over both the GaAs-based and Si-integrated parts, which provides an opportunity to tap off some optical power into in-plane waveguides on the SiN SiP PIC. By suppressing the surface emission (by increased top mirror reflectivity), while coupling some light into in-plane PIC waveguides it is possible to form a HVCL with in-plane emission. The in-plane coupling of the HVCL can be achieved by placing a weak diffraction grating inside the cavity [123] above the dielectric DBR on the Si substrate that is used as the back reflector, see Fig. 5.1(b). Due to its resemblance with a VCSEL, we call this HVCL a vertical-cavity silicon-integrated laser (VCSIL). An alternative option is to use a SiN high-contrast grating (HCG) as both reflector and coupler (Fig. 5.1c) [29], which also could be used to set the resonance wavelength of individual HVCLs by the grating parameters [124, 125] to enable fabrication of fully integrated multi-wavelength laser arrays for short-wavelength WDM optical interconnects [126].

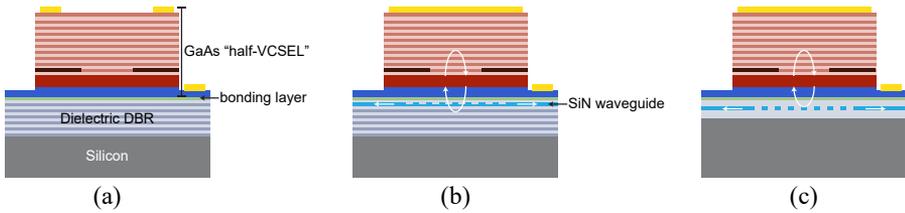


Fig. 5.1. Hybrid vertical-cavity lasers with surface emission (a), in-plane waveguide emission using a weak diffraction grating (b), and using a HCG (c).

## 5.1 Silicon-Integrated Hybrid-Cavity VCSEL

The silicon-integrated hybrid-cavity VCSEL is designed to investigate the impact of having a hybrid vertical cavity, while the purpose of perusing such a device is to take the first step towards a VCSIL with in-plane emission. This device allows development of the integration technique and investigation of the thermal impacts of employing a dielectric bottom DBR. The bottom DBR consists of 20 pairs of  $\text{Ta}_2\text{O}_5$  and  $\text{SiO}_2$  on a silicon substrate. Onto this DBR, the epitaxially grown GaAs-based device structure is adhesively bonded using DVS-BCB. The epitaxial device structure is a “half-VCSEL” with a 23-pair  $p$ -type  $\text{Al}_{0.90}\text{Ga}_{0.10}\text{As}/\text{Al}_{0.12}\text{Ga}_{0.88}\text{As}$  top DBR, a  $p$ - $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$  layer for oxide aperture formation that laterally confines photons and carriers, an active region with five 4 nm thick  $\text{In}_{0.10}\text{Ga}_{0.90}\text{As}$  QWs, and an  $n$ - $\text{Al}_{0.12}\text{Ga}_{0.88}\text{As}$  intra-cavity contact layer. An optical micrograph of a fully fabricated silicon-integrated hybrid-cavity VCSEL is shown in Fig. 5.2(a).

In Paper C and D, the detuning between the gain peak and the cavity resonance wavelength was too small (see Section 2.5 on detuning and its effect on temperature performance). This resulted in early thermal rollover and sub-optimal performance at elevated temperatures. To investigate this issue and improve the performance of the hybrid-cavity VCSELs, the impact of adjusting the bonding interface thickness was studied in Paper E. The bonding interface thickness consists of the combination of the  $\sim 40$  nm thick DVS-BCB bonding layer and a thin  $\text{SiO}_2$  film deposited on the dielectric DBR prior to bonding. By adjusting the  $\text{SiO}_2$  film thickness the VCSEL cavity resonance can be tuned. The results showed that the bonding interface can be chosen to optimize the performance, for e.g. maximum performance (optical output power or modulation speed) at a given temperature, or temperature-stable performance. The bonding interface thickness tuning allows operation at ambient temperatures up to  $100^\circ\text{C}$ , large signal data transmission at up to

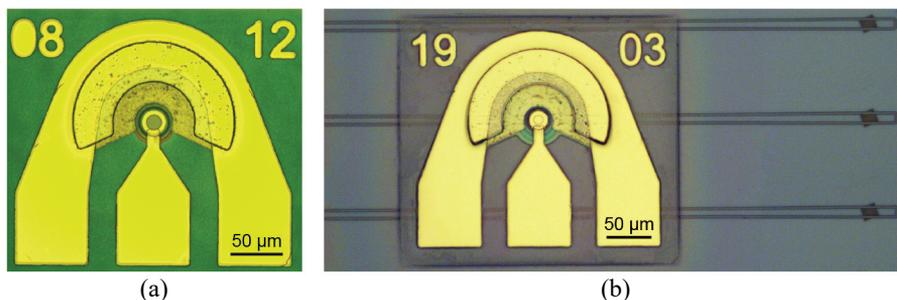


Fig. 5.2. Optical micrographs of (a) a silicon-integrated hybrid-cavity VCSEL and (b) a VCSIL with in-plane waveguide (to the right are grating couplers to enable measurements of the on-chip optical power).

85°C, and higher output powers and modulation speeds at room temperature compared to what was achieved in Paper C and D.

## 5.2 Vertical-Cavity Silicon-Integrated Laser

To take the final step towards a VCSIL with in-plane emission, a SiN/SiO<sub>2</sub> waveguide structure is included between the dielectric DBR on Si and the bonding interface layer. This waveguide structure has a weak diffraction grating below the oxide aperture to enable coupling of light from the optical standing wave in the vertical cavity into the in-plane SiN waveguide. The design of the grating period and duty cycle in combination with the vertical placement of the waveguide inside the cavity is critical as it should provide both sufficient feedback to the cavity and sufficient out-coupling to the waveguide [127]. Here, SiO<sub>2</sub> cladding layers of 610 nm and 780 nm are deposited below and above the 300 nm thick SiN waveguide layer to allow correct waveguide coupling and cavity feedback from the weak grating. As this thickness is added within the cavity, it obviously decreases the optical confinement to the active region compared to the surface-emitting cavity design in Paper C–E. Nevertheless, aiming for a resonance wavelength with optimum performance at room temperature (Paper E) and using the same epitaxial material as the silicon-integrated hybrid-cavity VCSELs enabled the demonstration of VCSILs with in-plane emission (Paper F). As the weak diffraction grating introduces mode and polarization dependent losses, the resulting output light in the waveguide is single polarization and close to single mode. An optical micrograph of a fully fabricated VCSIL with in-plane waveguide is shown in Fig. 5.2(b).

To the best of the author's knowledge, this is the first demonstration of an electrically injected (and continuous-wave) HVCL heterogeneously integrated to an in-plane silicon-based waveguide regardless of gain material.

### 5.3 Thermal Effects

Silicon has inherently good thermal conductivity, but the dielectrics used to form a reflector on top of the silicon have worse thermal conductivity and will act as an insulation that prevents the heat generated in the HVCL active region to escape down to the substrate. The hybrid-cavity VCSELs and VCSILs in Paper C–F therefore have  $\sim 4$  times worse thermal impedance than ordinary oxide-confined VCSELs [128], which will affect both static and dynamic performance negatively. To improve the performance the heat must be allowed to spread, for example using integrated metallic heat spreaders [129] or thermal shunts [130].

## Chapter 6

# VCSEL and VCSIL Fabrication

The complex VCSEL and VCSIL epitaxial structures used in this work were grown by metal-organic chemical vapor deposition (MOCVD) on undoped 3" GaAs substrates at IQE Europe Ltd. In MOCVD, organic molecules are used to transport III-metals (Al, Ga, In) to the heated substrate, where they react with arsine ( $\text{AsH}_3$ ) to form a III-As epitaxial film [131]. After the epitaxial growth VCSELs and VCSILs were fabricated using a range of standard processing steps, including photolithography, thin film deposition, etching, and wet oxidation. This chapter introduces these processing steps and describes the full fabrication process for high-speed VCSELs, silicon-integrated hybrid-cavity VCSELs, and VCSILs with waveguide emission.

### 6.1 Photolithography

Photolithography is the standard method to transfer a pattern on a mask onto a semiconductor wafer in the semiconductor industry. Even though several more advanced techniques with sub-micron resolution exist, such as nanoimprint and electron beam lithography, standard UV photolithography has been the main lithography technique of choice in this work since the resolution of approximately  $1\ \mu\text{m}$  [131] is sufficient for most processing steps. However, control of transverse modes and the polarization state using surface structures would require the higher resolution of nanoimprint and electron beam lithography.

Photolithography relies on the optical sensitivity of a photoresist, which is spin coated on the wafer at a few thousand rounds per minute to form a thin film of a few micrometers. The photoresist is then selectively exposed with ultraviolet light through a chromium photomask. During the following development, the exposed or non-exposed photoresist will be removed depending on whether the photoresist has positive or negative tone. The pattern is now transferred to the wafer and can be used to protect parts of the wafer surface during subsequent etching or deposition steps.

In the VCSIL fabrication process, the waveguide and weak diffraction grating are defined using electron beam lithography (at Ghent University, Belgium). To achieve a device with in-plane waveguide emission, high alignment accuracy is needed between the oxide aperture and the weak diffraction grating on the waveguide. In a high volume production, that could easily have been achieved using a stepper, which is a non-contact projection UV photolithography technique. In our low volume research process line, direct laser writing is used instead, which has an alignment accuracy of 200 nm and a resolution of 0.7  $\mu\text{m}$ , similar to what can be achieved in a stepper. The direct laser writer has an array of pixels that can be individually controlled to either block or transmit light from a UV laser. By sweeping the light from the pixel array over the sample in several segments, a full pattern can be written in the photoresist, which is then developed in the same manner as in standard photolithography.

## 6.2 Thin Film Deposition

There are several different techniques to deposit thin films. In this work the dielectric material silicon nitride (SiN) has been deposited using sputtering and plasma-enhanced chemical vapor deposition (PECVD), while metals have been deposited using sputtering and electron beam evaporation.

Sputtering is a technique where inert ions in a plasma are accelerated towards a target of the material to deposit. The accelerated ions will knock out target atoms that will diffuse toward the wafer where they form a thin film [132]. In the SiN case, reactive  $\text{N}_2$ -gas is injected to form a dielectric thin film with the sputtered silicon atoms, whereas metals are deposited without the presence of any reactive gas.

Since the PECVD is plasma enhanced, the gases injected to the chamber can be made chemically reactive by the plasma even at relatively low temperatures, which is important to avoid damage to the GaAs epitaxial structure or any contacts [131]. In this work SiN was deposited by injecting  $\text{SiH}_4$  and  $\text{N}_2$  into

an Ar plasma, where they react to form a SiN thin film on the wafer surface. During both sputtering and PECVD the resulting stoichiometry will depend on the deposition conditions and is therefore typically denoted  $\text{Si}_x\text{N}_y$ .

Another way of depositing metal is by electron beam evaporation, where metal is heated by an incident electron beam. When the metal is heated beyond its melting point, it will evaporate. The atoms in the vapor will travel through the vacuum chamber and form a metal film on the substrate surface [132].

## 6.3 Etching

Removal of AlGaAs material can be achieved with both wet and dry etching techniques. Wet etching is as the name suggests based on liquid solutions that are able to chemically dissolve material, often with good selectivity. However, wet etching is hard to accurately control and will not result in vertical sidewalls, as perfect anisotropic etching is difficult to achieve. Dry etching, which makes use of chemicals in gaseous form in a plasma, on the other hand has the possibility to combine a chemical etch with a physical, since the chemical reactions can be combined with ion bombardment [131]. The combination of chemical and physical etching makes it possible to adjust the process parameters to achieve an anisotropic etch.

The main dry etching technique used in this work has been inductively coupled plasma (ICP) reactive ion etching (RIE). The ICP is used to create a high-density plasma of the reactive gases used. Ions from the plasma are accelerated toward the substrate where they will chemically react with the surface removing material from the horizontal surface resulting in a directional etch. The gas used to etch the AlGaAs epitaxial structure is a mixture of  $\text{SiCl}_4$  and Ar. ICP RIE was also used to etch  $\text{Si}_x\text{N}_y$  with  $\text{NF}_3$ , and benzocyclobutene (BCB) using a mixture of  $\text{CF}_4$  and  $\text{O}_2$ . The etch depth can be accurately monitored by an *in situ* laser interferometer endpoint detection system in the ICP RIE system.

To obtain precise shallow etch depths of the top DBR layer to tune the photon lifetime Ar ion milling was used. Ar ion milling is a purely physical process where inert Ar ions are generated and accelerated towards the wafer surface where the ions sputter material from the surface [131]. Since the etch is not chemical, the etch rate is predictable and the etch depth can be controlled by the etch time.

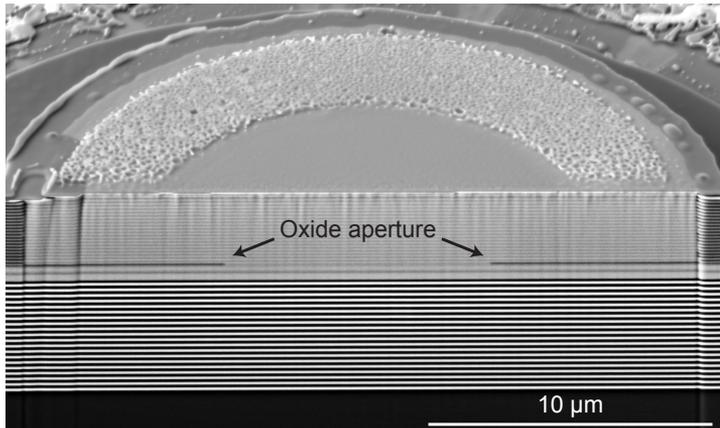


Fig. 6.1. SEM micrograph of an oxide aperture (indicated) in a FIB VCSEL cross-section.

## 6.4 Wet Oxidation

Selective wet oxidation of high aluminum-content AlGaAs is used to form the VCSEL oxide aperture. The wet oxidation is performed after the mesa etch by exposing the high aluminum-content AlGaAs layers to water vapor at elevated temperature [133]. The wet oxidation rate depends on the aluminum content, making it possible to include secondary oxide layers that oxidizes slower than the primary oxide layers. In this work an N<sub>2</sub>-bubbler is used to transport water vapor from a water beaker held at 95°C to the oxidation furnace held at 420°C, achieving a typical oxidation rate of  $\sim 0.3 \mu\text{m}/\text{min}$  for Al<sub>0.98</sub>Ga<sub>0.02</sub>As. The oxidation front is observed *in situ* using IR illumination and a microscope with a CCD camera. Since the oxidation rate is very sensitive to the temperature even the small temperature gradient across the sample is enough for the oxide aperture diameter to become non-uniform [133]. To improve the uniformity the sample can be rotated 180° after half the oxidation time. A scanning electron microscope (SEM) micrograph of an oxide aperture in a focused ion beam (FIB) VCSEL cross-section is shown in Fig. 6.1.

## 6.5 High-Speed VCSEL Fabrication Process

Before processing, the 3" wafer is cleaved into  $8 \times 10$  mm chips. After cleaning the chips, Ti/Pt/Au *p*-contacts are deposited along with alignment marks

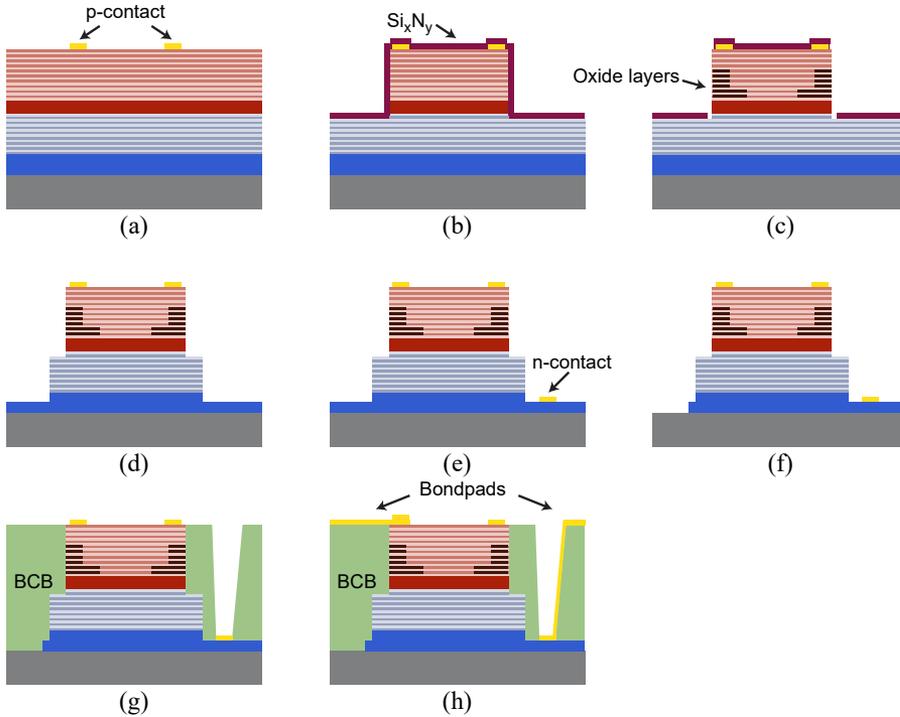


Fig. 6.2. The process steps for high-speed VCSEL fabrication includes: (a) *p*-contact deposition, (b) mesa etching followed by deposition of  $\text{Si}_x\text{N}_y$ , (c) oxide aperture formation after opening of the  $\text{Si}_x\text{N}_y$  on the mesa side walls, (d) second mesa etching, (e) *n*-contact deposition, (f) *n*-contact layer removal beneath the *p*-bondpad, (g) planarization with BCB, and (h) deposition of bondpads.

using electron beam evaporation. A hard mask, defined in sputtered  $\text{Si}_x\text{N}_y$ , for circular mesas with diameters of 22, 24, 26, 28  $\mu\text{m}$  is etched using ICP-RIE with  $\text{NF}_3$  chemistry, followed by etching the mesas using ICP-RIE with  $\text{SiCl}_4$  chemistry. The *in situ* laser interferometer endpoint detection system of the ICP-RIE system is used to stop accurately at the desired etch depth and expose the oxide layers without exposing the AlAs layers in the bottom DBR. The chip and mesa surface is protected by a PECVD deposited  $\text{Si}_x\text{N}_y$  layer, which is removed at the mesa sidewalls before oxidation. Oxide apertures are formed by wet oxidation at  $420^\circ\text{C}$ . A second mesa is etched down to the contact layer below the bottom DBR, again using ICP-RIE with  $\text{SiCl}_4$  chemistry. The protective  $\text{Si}_x\text{N}_y$  layer is removed using ICP-RIE with  $\text{NF}_3$  chemistry, followed by electron beam evaporation of Ni/Ge/Au *n*-contacts, annealed in an inert  $\text{N}_2$  atmosphere at  $430^\circ\text{C}$  for 30 s. The contact layer is removed outside the mesas and the *n*-contacts to reduce the bondpad capacitance. A thick BCB layer is spin-coated to planarize the surface and allows for deposition of Ti/Au bondpads in a GSG configuration by sputtering. Finally, the top DBR layer was thinned by Ar ion milling to set the photon lifetime. The fabrication process for high-speed VCSELs is illustrated in Fig. 6.2.

## 6.6 Silicon-Integrated Hybrid-Cavity VCSEL Fabrication Process

The silicon-integrated hybrid-cavity VCSELs have a similar fabrication process as the high-speed VCSELs (Section 6.5) after the bonding of the GaAs-based “half-VCSEL” structure to the dielectric DBR on Si using DVS-BCB and removal of the GaAs substrate. However, to allow residual gas trapped in the bonding layer to escape during subsequent high temperature process steps the individual VCSELs were isolated by trenches etched through the epitaxial III-V structure before the mesas. Further, to reach the thin intra-cavity contact layer just below the active region, the mesa etch is stopped within the contact layer, where the *n*-contacts are deposited and annealed after oxidation and removal of the protective  $\text{Si}_x\text{N}_y$  layer. The fabrication process for silicon-integrated hybrid-cavity VCSELs is illustrated in Fig. 6.3.

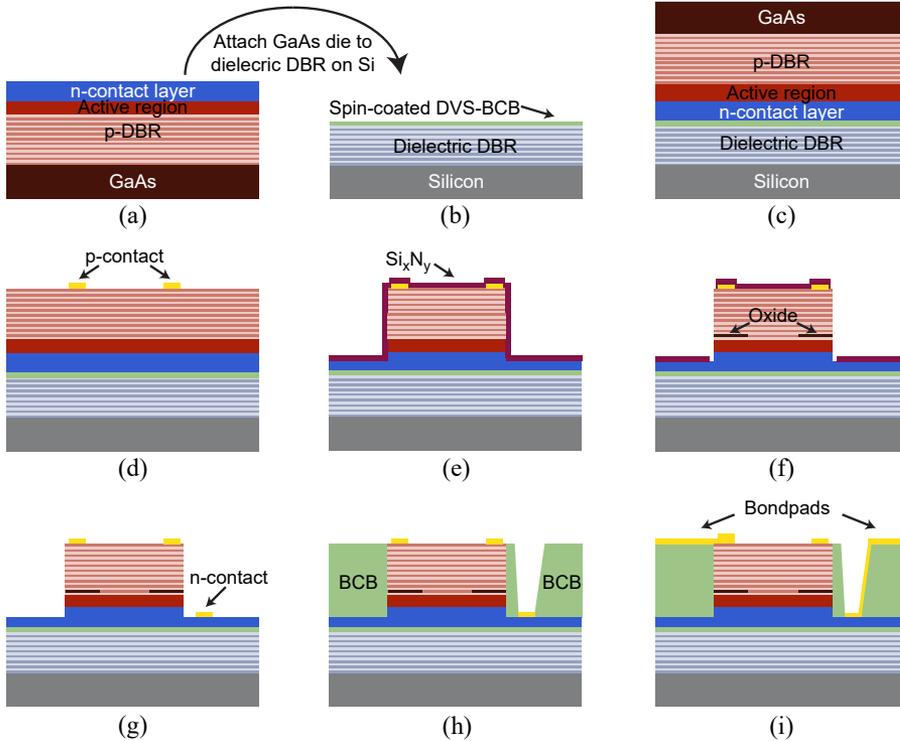


Fig. 6.3. The process steps for silicon-integrated hybrid-cavity VCSEL fabrication includes: (a-c) bonding of the GaAs-based “half-VCSEL” structure to the dielectric DBR on Si spin-coated with DVS-BCB followed by removal of the GaAs substrate, (d) *p*-contact deposition, (e) mesa etching followed by deposition of  $\text{Si}_x\text{N}_y$ , (f) oxide aperture formation after opening of  $\text{Si}_x\text{N}_y$  on mesa side walls, (g) *n*-contact deposition, (h) planarization with BCB, and (i) deposition of bondpads.

## 6.7 Vertical-Cavity Silicon-Integrated Laser Fabrication Process

The vertical-cavity silicon-integrated laser (VCSIL) fabrication process is similar to the silicon-integrated hybrid-cavity VCSEL fabrication process (Section 6.6). Before bonding the “half-VCSEL” structure to the dielectric DBR on Si and the removal of the GaAs substrate, SiN/SiO<sub>2</sub> waveguide structures with weak diffraction gratings for in-plane coupling from the vertical cavities are deposited and patterned (using electron beam lithography) on top of the dielectric DBR. The oxide apertures and consequently the mesas need to be accurately aligned to the weak diffraction gratings, which is achieved by patterning the *p*-contact rings and mesas using direct laser writing. The direct laser writing could be exchanged with a stepper in a high volume production line. The remaining AlGaAs material outside the device structure was removed to isolate the devices before the subsequent high temperature process steps and to avoid power leakage from the waveguides into the higher refractive index AlGaAs material. Finally, top surface emission is suppressed by deposition of a top Au reflector using electron beam evaporation. The VCSIL fabrication process is illustrated in Fig. 6.4.

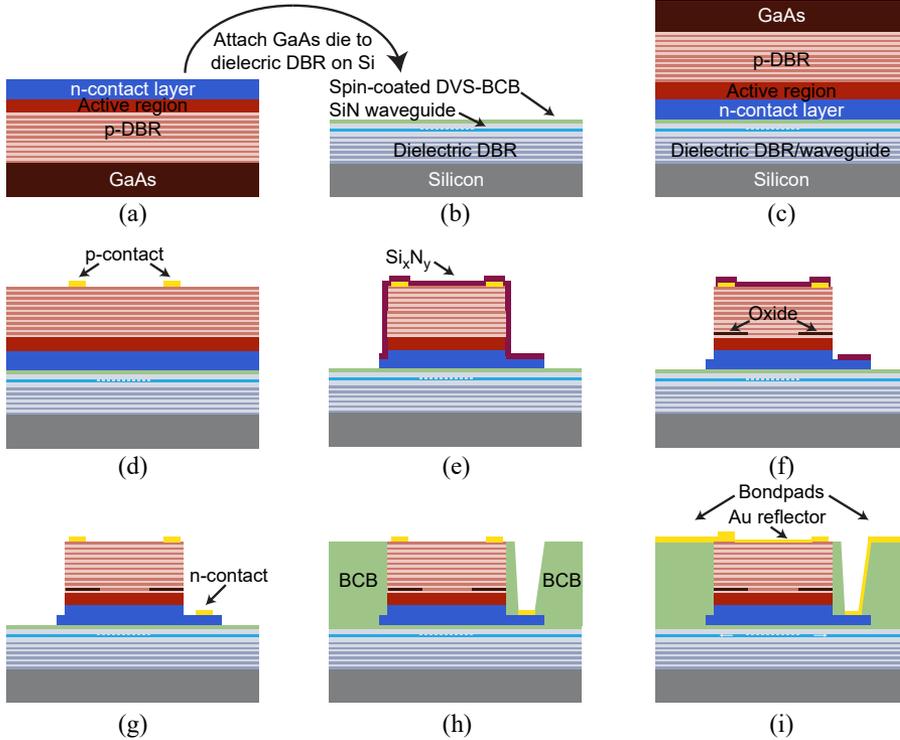


Fig. 6.4. The process steps for VCSIL fabrication includes: (a-c) bonding of the GaAs-based “half-VCSEL” structure to the dielectric DBR and waveguide structure on Si spin-coated with DVS-BCB followed by removal of the GaAs substrate, (d) *p*-contact deposition, (e) mesa etching followed by deposition of  $\text{Si}_x\text{N}_y$  and device isolation, (f) oxide aperture formation after opening of  $\text{Si}_x\text{N}_y$  on mesa side walls, (g) *n*-contact deposition, (h) planarization with BCB, and (i) deposition of bondpads followed by deposition of top Au reflector.



# Chapter 7

## Future Outlook

As indicated in Chapter 3, the high-speed VCSEL performance is limited by the device resistance and capacitance along with heat generation and thermal impedance. Employing intra-cavity contacts is a viable route that bypasses the DBR resistance, which already has led to record-high PCE [66]. By also moving to longer wavelengths (for example 980 nm or 1060 nm) by adding more indium in the QWs the differential gain is increased, which is beneficial for high-speed operation. Further, at wavelengths above 940 nm it is possible to use binary GaAs in the DBRs, which could benefit the thermal impedance and the electrical resistance.

Even though some improvements of high-speed VCSEL performance could be expected through reduced resistance, capacitance, and thermal impedance, it is probable that it will not be enough to meet the future bandwidth demands. The future standards already consider higher order modulation formats like 4-PAM together with FEC codes. It also becomes increasingly important to co-optimize the driver and receiver electronics (possibly also including equalization) with the VCSEL to achieve best performance without increasing the power consumption.

However, there have also been efforts to circumvent the current speed-limiting factors through the photon-photon resonance, reaching 37 GHz bandwidth [134], and by utilizing polarization dynamics by optical spin-injection, reaching 80 GHz [135]. Another way of improving the capacity that already is used in long-haul optical communication is multiplexing. The most obvious way is by using a multi-wavelength transmitter, for example with wavelength-set HCG-VCSELs [125], or employing space-division multiplexing (SDM) using bundled fiber ribbons [136] or multicore fibers [137] together with matching

VCSEL arrays [121], but one could also envision mode multiplexing, for example by generating light with different orbital angular momentum [138] that excites different mode groups in the multimode optical fiber.

The silicon-integrated hybrid-cavity VCSELs needs to be further developed with better thermal properties and lower capacitance to be able to catch up with state-of-the-art high-speed VCSELs. This can possibly be achieved by integrated metallic heat spreaders and additional oxide layers, as discussed in Sections 5.3 and 3.2.

Advances have been made in exchanging the adhesive wafer bonding technique with transfer printing. By doing so, complete lasers are processed on their native substrate, where they to some extent can be tested before being transferred to the target substrate using a stamp [139, 140]. This technique has good alignment capabilities and allows better usage of the epitaxial material, as area magnification techniques makes it possible to use a smaller III-V source substrate for several larger SiP chips [141].

The ultimate goal of pursuing a silicon-integrated VCSEL-like laser is to realize an efficient integrated light source on SiP PICs with in-plane waveguide emission. Paper F was the first demonstration of such a device with electrical injection and the only other demonstration to date used optical pumping and resulted in low output power [29]. In order for this concept to be a viable option, the output power level need to be increased, while the thermal properties need improvement. These issues originates to a large extent from the high thermal impedance bottom reflector.

Finally, the realization of integrated multi-wavelength arrays of VCSILs would enable the realization of PIC-based WDM transmitters for optical interconnects and multi-wavelength sources for bio photonics and life sciences. This could be obtained by including a HCG as both reflector and coupler, or moving to transfer printing that would allow the introduction of a wavelength-setting layer that is defined on the PIC before device printing.

# Chapter 8

## Summary of Papers

### Paper A

“High-speed 850 nm VCSELs operating error free up to 57 Gbit/s,”  
*Electronics Letters*, vol. 49, no. 16, pp. 1021–1023, Aug. 2013. DOI:  
10.1049/el.2013.2042.

This paper presents error-free data transmission at RT without equalization up to 57 Gb/s over 1 m OM4 multimode fiber. At longer fiber lengths, 55 Gb/s and 43 Gb/s over 50 and 100 m, respectively, were demonstrated. The results were obtained using a VCSEL with the damping optimized for high data rates. The VCSEL has a bandwidth of  $\sim 24$  GHz, and  $K$ - and  $D$ -factors of  $\sim 0.17$  ns and  $\sim 9$  GHz/mA<sup>1/2</sup>, respectively. The data rates over the two shorter fiber lengths are still (5 years later) record-high for binary links without equalization. The result over 100 m fiber was record-high until UIUC demonstrated transmission at 46 Gb/s over this length at RT earlier this year [142].

**My contribution:** I performed all measurements, analyzed the results, and co-authored the paper.

## Paper B

**“Impact of damping on high-speed large signal VCSEL dynamics,”** *Journal of Lightwave Technology*, vol. 33, no. 4, pp. 795–801, Feb. 2015. DOI: 10.1109/JLT.2014.2364455.

In this paper, the results from a study of how damping affects the large signal VCSEL dynamics are presented. Through measurements of turn-on delays, eye diagrams, and BERs, it is concluded that the optimum damping depends on the data rate. At low data rates it is affordable with more damping, whereas at higher data rates the higher bandwidth and slope efficiency of a less damped VCSEL are needed.

**My contribution:** I fabricated the VCSELs together with P. Westbergh. I performed all measurements, analyzed the results, and wrote the paper. I also presented the results at the IEEE International Semiconductor Laser Conference 2014 (Palma de Mallorca, Spain).

## Paper C

**“Silicon-integrated short-wavelength hybrid-cavity VCSEL,”** *Optics Express*, vol. 23, no. 26, pp. 33 634–33 640, Dec. 2015. DOI: 10.1364/OE.23.033634.

This paper presents the design, fabrication, and static performance of a short-wavelength hybrid-cavity VCSEL heterogeneously integrated on silicon. DVS-BCB adhesive bonding is used to attach a GaAs-based “half-VCSEL” to a dielectric DBR on silicon to form a hybrid vertical cavity, where the standing-wave optical field extends over both the GaAs- and silicon-based parts. A 9- $\mu\text{m}$  oxide-aperture diameter hybrid-cavity VCSEL produces 1.6 mW of output power at 845 nm.

**My contribution:** I established the GaAs-processing part of the silicon-integrated hybrid-cavity VCSELs at Chalmers and fabricated the VCSELs after S. Kumari, Ghent University, performed the bonding and substrate removal. I performed the measurements, analyzed the results, co-authored the paper, and was the corresponding author. I also presented the results at SPIE Photonics West 2016 (San Francisco, CA, USA).

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## Paper D

**“20-Gb/s modulation of silicon-integrated short-wavelength hybrid-cavity VCSELs,”** *IEEE Photonics Technology Letters*, vol. 28, no. 8, pp. 856–859, Apr. 2016. DOI: 10.1109/LPT.2016.2514699.

This letter presents the dynamics of the silicon-integrated hybrid-cavity VCSELs in Paper C, with optimized damping (Paper B) for large signal data transmission. A 5- $\mu\text{m}$  oxide-aperture diameter hybrid-cavity VCSEL with a small signal bandwidth of 11 GHz is capable of error-free data transmission up to 20 Gb/s. The hybrid-cavity VCSEL has  $K$ - and  $D$ -factors of 0.2 ns and 7 GHz/mA<sup>1/2</sup>, respectively. An analysis of the small signal modulation response reveals that the bandwidth (and consequentially the possible data rate) is limited by both thermal effects and parasitics.

**My contribution:** I fabricated the silicon-integrated hybrid-cavity VCSELs after S. Kumari at Ghent University performed the bonding and substrate removal. I performed the measurements and analyzed the results, wrote the paper, and presented the results at SPIE Photonics West 2016 (San Francisco, CA, USA).

## Paper E

**“Silicon-integrated hybrid-cavity 850-nm VCSELs by adhesive bonding: Impact of bonding interface thickness on laser performance,”** *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 23, no. 6, Paper 1700109, Nov.–Dec. 2017. DOI: 10.1109/JSTQE.2016.2633823.

In this paper a study of the performance of silicon-integrated hybrid-cavity VCSELs with different bonding interface thicknesses between the GaAs-based “half-VCSEL” and the bottom dielectric reflector on silicon is presented. By adjusting this thickness, it is possible to optimize the laser performance at a specific ambient temperature or for temperature-stable performance. This enabled output powers up to 2.3 mW at 25°C and 0.9 mW at 85°C for 10- $\mu\text{m}$  oxide-aperture diameter devices, and data transmission at up to 25 Gb/s at 25°C and 10 Gb/s at 85°C for a 5- $\mu\text{m}$  oxide-aperture diameter device. Finally, measurements show that the bonding interface thickness does not affect the thermal impedance.

**My contribution:** I fabricated the silicon-integrated hybrid-cavity VCSELs after S. Kumari at Ghent University performed the bonding and substrate removal. I performed the measurements, analyzed the results, wrote the paper, and presented the results at the IEEE International Semiconductor Laser Conference 2016 (Kobe, Japan).

## Paper F

**“Vertical-cavity silicon-integrated laser with in-plane waveguide emission at 850 nm,”** *Laser & Photonics Reviews*, vol. 12, no. 2, Paper 1700206, Feb. 2018. DOI: 10.1002/lpor.201700206.

This paper presents the results from the demonstration of the first vertical-cavity silicon-integrated laser (VCSIL) with in-plane waveguide emission using electrical injection. This is achieved by placing a weak diffraction grating on the intra-cavity SiN/SiO<sub>2</sub> waveguide layer. By placing this grating inside the cavity, light can be tapped off from the vertical cavity into the in-plane SiN waveguide. A 5- $\mu\text{m}$  oxide-aperture VCSIL with 1.1 mA threshold current produces an on-chip single-sided optical output power up to 73  $\mu\text{W}$ . As the weak grating also suppresses higher order modes, a side-mode suppression ratio as high as 29 dB is obtained.

**My contribution:** I established the GaAs-processing part of the vertical-cavity silicon-integrated lasers (VCSILs) at Chalmers and fabricated the VCSILs after S. Kumari at Ghent University fabricated the waveguides and weak diffraction gratings and performed bonding and substrate removal. I performed the measurements, analyzed the results, and co-authored the paper.

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