Millimeter-wave Transceiver ICs for Ultrahigh Data Rate Communications
Using Advanced III-V and Silicon Technologies

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Sona Carpenter
To my family
for their enduring love and support.
Abstract

Today’s main driving parameter for radio transceiver research is the ability to provide high capacity while maintaining low cost, small form factor, and low power consumption. Direct conversion architectures (due to the feasibility of monolithic integration) at millimeter-wave (due to wideband availability) have attracted large interest in recent years because of their potential to meet these demands. The communication system operating at frequencies above 100 GHz enabling 10-100 Gbit/s wireless communication in various applications ranging from personal area networks for portable electronic devices, 4G and 5G mobile communication infrastructure, high data rate backhaul, real-time transmission of high-definition videos, short range chip to chip communication (wireless in a box), long-range high-speed communication (using phased arrays), and >40 Gbit/s transmission over dielectric waveguide is of interest in this thesis. However, it is a challenge to design and implement millimeter-wave transceivers that can utilize such wideband effectively for the high data transmission.

This thesis addresses the design challenges and implementation at the individual circuit building blocks of the RF front-end as well as system level considerations for the realization of a fully integrated monolithic microwave integrated (MMICs) transmitter (TX) and receiver (RX) circuits at 110-170 GHz (D-band) in III-V 250 nm indium phosphide double heterojunction bipolar transistor (InP DHBT) and commercial 130 nm SiGe BiCMOS technologies.

The research described in this thesis is focused on the design and characterization of a direct conversion in-phase/quadrature-phase (I/Q) modulator and demodulator, frequency multiplier circuits and integration of fully integrated transceiver chipsets demonstrating the highest RF and IF bandwidths at this frequency to date. The TX/RX chipset consists of an X3 LO frequency multiplier integrated with an I/Q modulator/demodulator and a low-noise amplifier (LNA)/power amplifier (PA). This integration allows us to design the oscillator at one third of the fundamental D-band LO frequency. The chosen design simplifies the packaging of the TX/RX chips and hence reduces the cost and power consumption. A 110–170 GHz RF amplifier is used to improve the noise figure of the RX chip and to increase the gain and transmitted power for the TX chip.

The chipset is multifunctional and can be used in both homodyne and heterodyne architectures supporting high data rate transmission using wide modulation bandwidth and spectral-efficient modulation formats. For QPSK and 64 QAM modulation schemes, the measured data-rates using this chipset are 48 Gbit/s in homodyne mode and 18 Gbit/s in heterodyne mode, respectively. At the time of writing this thesis, this is the highest data-rate reported in the literature for fully integrated wireless systems in the D-band.

The main interest of the work is in real time wireless data traffic transmission on designed TX/RX chipsets. Therefore, the TX/RX front-end circuitry is mounted in compact split-block waveguide modules in a collaborative teamwork. The D-band TX/RX front-end modules were integrated into radio units demonstrating successfully a real time error-free wireless data transmission with 5.3 Gbit/s using 64 QAM modulation over a 1 GHz channel with spectrum efficiency of 5 bit/s/Hz. The work from this thesis demonstrates the world’s first fully functional spectrum efficient link at frequencies greater than 100 GHz.

Keywords: 110-170 GHz, D-band, InP DHBT, SiGe BiCMOS, MMIC, single chip, Gilbert-cell mixer, I/Q modulator, demodulator, transmitter, receiver, direct conversion, frequency multiplier, high data rate, high-order modulation, millimeter-wave communication, QPSK, QAM, 5G, point-to-point radio.
List of Publications

Appended Publications

This thesis is based on work contained in the following papers:


Other Publications

The following papers have been published but is not included in the thesis. The content partially overlaps with the appended papers or is out of the scope of this thesis.


Thesis

As part of the author’s doctoral studies, some of the work presented in this thesis has previously been published in [O]. Figures, tables and text from [O] may therefore be fully or partly reproduced in this thesis.

Notations and Abbreviations

Notations

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>$c$</td>
<td>Speed of light in vacuum</td>
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<tr>
<td>$f$</td>
<td>Frequency</td>
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<tr>
<td>$g_m$</td>
<td>Transconductance</td>
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<tr>
<td>$\omega$</td>
<td>Angular frequency</td>
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<tr>
<td>$A$</td>
<td>Amplitude error</td>
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<tr>
<td>$\theta$</td>
<td>Phase error</td>
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<tr>
<td>$V_{RF}$</td>
<td>RF voltage</td>
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<tr>
<td>$F$</td>
<td>Noise factor</td>
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<tr>
<td>$I_c$</td>
<td>Collector current</td>
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<tr>
<td>$k$</td>
<td>Boltzmann constant</td>
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<tr>
<td>$T$</td>
<td>Temperature</td>
</tr>
<tr>
<td>$V_t$</td>
<td>Threshold voltage</td>
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<tr>
<td>$BV_{CEO}$</td>
<td>Collector-emitter breakdown voltage</td>
</tr>
<tr>
<td>$BW$</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>$C$</td>
<td>Capacity</td>
</tr>
<tr>
<td>$P_{TX}$</td>
<td>Transmitter output power</td>
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<tr>
<td>$P_{RX}$</td>
<td>Received power</td>
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<tr>
<td>$E_b$</td>
<td>Bit energy</td>
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<tr>
<td>$N_o$</td>
<td>Noise spectral density</td>
</tr>
<tr>
<td>$R_b$</td>
<td>Bit rate</td>
</tr>
<tr>
<td>$I_c$</td>
<td>Collector current</td>
</tr>
<tr>
<td>$C_{je}$</td>
<td>Emitter base junction capacitance</td>
</tr>
<tr>
<td>$C_{cb}$</td>
<td>Collector base junction capacitance</td>
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Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>AWG</td>
<td>Arbitrary Waveform Generator</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>AWGN</td>
<td>Additive White Gaussian Noise</td>
</tr>
<tr>
<td>BCB</td>
<td>BenzoCycloButene</td>
</tr>
<tr>
<td>BPF</td>
<td>Band Pass Filter</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EVM</td>
<td>Error Vector Magnitude</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
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<tr>
<td>EDGE</td>
<td>Enhanced Data rates for GSM Evolution</td>
</tr>
<tr>
<td>f&lt;sub&gt;MAX&lt;/sub&gt;</td>
<td>Maximum Frequency of Oscillation</td>
</tr>
<tr>
<td>f&lt;sub&gt;T&lt;/sub&gt;</td>
<td>Transition Frequency</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide</td>
</tr>
<tr>
<td>HBT</td>
<td>Heterojunction Bipolar Transistor</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>HetNet</td>
<td>Heterogeneous Network</td>
</tr>
<tr>
<td>IIP3</td>
<td>Input referred 3rd order Intercept Point</td>
</tr>
<tr>
<td>IRF</td>
<td>Image Reject Filter</td>
</tr>
<tr>
<td>IRM</td>
<td>Image Reject Mixer</td>
</tr>
<tr>
<td>IRR</td>
<td>Image Rejection Ratio</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>LSB</td>
<td>Lower Side Band</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LTE</td>
<td>Long Term Evolution</td>
</tr>
<tr>
<td>LTI</td>
<td>Linear Time Invariant</td>
</tr>
<tr>
<td>MIMO</td>
<td>Multiple Input Multiple Output</td>
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<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
</tr>
<tr>
<td>MIC</td>
<td>Microwave Integrated Circuit</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>QPSK</td>
<td>Quadrature Phase Shift Keying</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RFIC</td>
<td>Radio Frequency Integrated Circuit</td>
</tr>
<tr>
<td>RX</td>
<td>Receiver</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>TX</td>
<td>Transmitter</td>
</tr>
<tr>
<td>USB</td>
<td>Upper Side Band</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector Network Analyzer</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>WiFi</td>
<td>Trade name for IEEE 802.11 Wireless Technologies</td>
</tr>
<tr>
<td>WPAN</td>
<td>Wireless Personal Area Network</td>
</tr>
<tr>
<td>WiMAX</td>
<td>Worldwide Interoperability for Microwave</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless Local Area Network</td>
</tr>
<tr>
<td>2DEG</td>
<td>2-Dimensional Electron Gas</td>
</tr>
<tr>
<td>3G/4G/5G</td>
<td>Third/Fourth/Fifth Generation Mobile Communications Technology</td>
</tr>
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Chapter 1

Introduction

From 2-way pagers to cellular telephony and now to the wireless internet access on handheld devices, the world is becoming a complex connected network of nodes or devices. The wireless communication systems have gone a long way from transmitting the clicks of Morse code over short distances to demanding 3D movies, webpages, and now images from Jupiter. This rapid increase in the number of wireless devices, such as tablets, laptops, and smartphones, together with rapidly growing demand for broadband services, such as telemedicine, online gaming and future 3D teleconferences, has led to research in new and novel systems for transmitting multi-gigabit data rates and enabling good coverage as well as low cost network implementation. Fig. 1.1 (a) and (b) show the forecast demand for faster and faster data transmission speeds over time and the quest for high-throughput wireless links that can meet current needs as well as enabling new applications and future growth [1-3].

Figure 1.1: (a) Data rate trends in wired, wireless and cellular over the years. Data rate increases by a factor of 10 every 5 years (Courtesy ISSCC [1]). (b) The three main uses for future cellular network (Courtesy Ericsson AB [3]).
1.1 Emerging technologies for ultra-broadband communication

1.1.1 Evolving mobile network

Mobile data traffic is experiencing exponential growth, driven by smart devices and high bandwidth applications. With the upgrading of mobile network radio base stations (RBS) from 2G (second generation) to 3G (third generation) and LTE (Long Term Evolution), the capacity requirement of the backhaul links has increased vastly. According to the Cisco Visual Networking Index (VNI) Global Mobile Data Traffic Forecast, global mobile data traffic will increase sevenfold between 2016 and 2021 [4-5]. This necessitates a strong communication backbone to enable higher capacity and quality of service (QoS) to each node in the mobile networks especially in dense urban areas. Currently, microwave and fiber are the main solutions for connecting base stations to the central switched network (backhaul network). The advantages of fast deployment and ease of relocation make the microwave solution more attractive than fiber, but it has limited capacity compared with the fiber solution.

A variety of techniques are now being explored to meet the demand [6-9], such as the introduction of smaller (pico/femto) cell base stations in densely populated areas, e.g. public transport hubs, shopping malls etc., where macrocell can offload its data traffic resulting in higher data rates for the end-user.

1.1.2 HetNet- cost and energy efficient backhaul option

Fig. 1.2 illustrates a mobile network in an urban scenario, which is called Heterogeneous Network (HetNet). Here one or more smaller base stations called small cells are embedded in a conventional cellular network to enhance the capacity [10]. Base station A has direct access to a fiber backhaul, which is used to support the mobile data traffic in that area. When there is a need for increased capacity, base station B must be set up to share the traffic load. Base stations A and B are macrocell base stations that can cover a large area, but the performance of these macrocells would reduce dramatically for indoor user equipment. Microcell base stations can be added to serve indoor user equipment such as offices and bus stations and can be a good complement to the macrocells. These small cell base stations cover a smaller area but deliver high per-user capacity and consume less power than traditional base stations [11]. This also enables frequency reuse resulting in efficient utilization of the available spectrum.

HetNet enables an ultra-dense radio access network for next generation mobile communication. A microwave based backhaul capability is the key of deployment of these small cells. Since many small cells are required to provide the coverage of a single macrocell, this wireless backhaul solution necessitates a small form factor and must be cost effective.
1.1.3 Massive multiple-input multiple-output (MIMO) systems

Another method for increasing the communication speed is to use multiple antenna systems. Multiple-input multiple-output (MIMO) is a method for multiplying the capacity of a radio link using multiple transmit and receive antennas [12]. MIMO technology is already in use in current and emerging wireless standards like LTE and LTE-Advanced (LTE-A) using a maximum of 8 antennas. This number will increase to large antenna arrays of hundreds or thousands of antennas in massive MIMO [13-14].

For such MIMO applications, a massive number of transceivers are required which must be low-cost, compact and should operate within the power budget.

1.1.4 Wireless systems for chip-to-chip communication

Today’s electronic devices have multiple chips on a printed circuit board (PCB). This requires exchange of large amount of data between processor chips or between a processor chip and a memory chip or between modules on a motherboard or board-to-board communications. This number of chips increases as devices require more functions and applications resulting in more complicated interconnections among chip. This interconnection becomes more and more troublesome due to the growth of data rates beyond tens of Gbit/s.

To complement a wired link and obtain more flexibility, the wireless chip-to-chip communication [15-16] needs fiber-comparable capacity requiring high operational bandwidth and compact systems.
1.2 Millimeter-wave spectrum

Based on Shannon’s theorem, the maximum data-rate of a communication channel (channel capacity (C)) is related to the frequency bandwidth of the channel (BW) and the signal-to-noise ratio (SNR) as shown in Eq. 1.1 [17]. One way to increase the communication data rate is to use more bandwidth. Therefore, the interest in systems operating at millimeter-wave (mm-wave) is continuously increasing due to the availability of large bandwidth for high-speed applications.

\[ C = BW \log_2(1 + SNR) \]  

(1.1)

Figure 1.3: Frequency allocation of radio spectrum [18-19]. The marked band are allocated by FCC for fixed and mobile communication.

Figure 1.4: An antenna gain of 36 dBi has 3.7 m diameter at 2.5 GHz and the corresponding diameter at 145 GHz is 6 cm (Courtesy Prof. Herbert Zirath).
The mm-wave is the electromagnetic spectrum between 30 GHz to 300 GHz, which corresponds to wavelengths from 10 mm to 1 mm. The frequencies below 100 GHz have been relatively well explored and are already in use for various existing applications [18]. This makes it difficult to accommodate the wide bandwidth requirements of emerging applications.

The mm-wave radios typically operate over distances of several kilometers using highly directional beams that also help to prevent interferences. This characteristic, along with large available bandwidth makes mm-wave technology an ideal solution for high-speed point-to-point wireless communications. Fig. 1.3 shows the effect of rain on wave propagation at different frequencies. High attenuation lines are observed at 60 GHz, 120 GHz, 183 GHz and a minimum attenuation occurs between these frequencies. Both high and low attenuation bands are interesting for high-speed communications. In this thesis, receiver and transmitter circuits operating in the 110-170 GHz and 140-220 GHz frequency ranges will be described.

### Short range communication

The high absorption peaks in Fig. 1.3, can be used to limit the coverage of a wireless network for increased security and minimum regulatory control. The attenuation over distance prevents the signal from being detected far beyond the intended recipient. Furthermore, the use of directional antennas decreases the spreading effect by limiting the angle of arrival of the signal. Such type of high-speed short links can be used for a number of applications such as wireless gigabit Ethernet, large file transfer, wireless gaming, high definition multimedia interface (HDMI) cable replacement/uncompressed high definition (HD) video streaming, mobile distributed computing, wireless docking stations. Wireless local area network operating at 60 GHz for short-range data and video streaming is the example of such application [20].

### Medium range point-to-point communication

On the other hand, low attenuation between the absorption lines are suitable for the multi-gigabit data transmission over ranges of a few km [21]. An E band (71-76 GHz, 81-86 GHz) point-to-point data link for mobile backhaul networks is an example of this type of application [22]. Moreover, antenna size and spacing in multiple antenna systems are also reduced at higher frequency, making the system more compact and affordable and a comparison is shown in Fig. 1.4.

### Other applications

The range resolution of imaging systems is inversely proportional to the pulse duration. Therefore, high available bandwidth at mm-wave can be used to increase the quality of the obtained images. The systems operating beyond 100 GHz have gained increased interest in emerging applications such as detection of concealed explosives [23], high precision industrial radar sensors [24] [25], inter-satellite communication, high resolution active and passive imaging applications in the field of diagnostics, security, vision systems, medical and airborne applications [26]-[30]. Millimeter wave radars can be used to measure the distance or speed of aircraft, ships, automotive vehicles, and many other objects.
1.3 Millimeter wave communication – opportunities and challenges

Millimeter wave technologies

The millimeter-wave integrated circuits have been possible due to rapid advancement in transistor and integrated circuit technologies over the last decade [31] [32]. Therefore, it becomes possible to fully integrate radio and radar transceivers with their passive devices and antennas on a single chip. Each semiconductor technology has particular strengths and weaknesses with respect to various applications [33]. III-V MMIC technology are best suited for the noise performance and signal generation at millimeter-waves [34]-[38]. SiGe BiCMOS technologies are preferred in commercial applications because of lower cost, higher reliability and combination with digital CMOS control circuits such as high-speed communication, automotive radars, sensing and imaging [39]-[42].

System implementation challenges at mm-wave

Traditionally, mm-wave systems have been assembled via a number of bulky and expensive sub-blocks including low-noise amplification, frequency conversion, and local oscillator (LO) signal generation. These sub blocks are waveguide modules with embedded MMICs from different technologies. The chips can be mounted on a common carrier through wire bond or flip-chip etc. [43]-[45]. This type of package contains chip level interconnects, transmission lines and even some passive circuitry, controlled impedance lines, and grounding structures, all in a protective casing. Then, the sub-blocks are assembled into one unit in order to form a system. This type of system has a large number of interconnections between chips which increases parasitic, reflections, insertion losses and degrades the mm-wave performance of circuits. Another drawback is increased weight, high assembling and testing cost as well as higher power consumption, which scales with the number of MMICs.

1.4 Thesis motivation

Need for a single chip mm-wave front-end solution

One of the most effective ways to reduce cost and achieve compactness is to decrease the number of MMICs by increasing the level of integration. Thus, there has been tremendous effort by both industry and academia to integrate the complete transmitter and receiver on a single chip. This enables ease of manufacturing, as well as reduction in cost and weight. This also presents new challenge for structural innovation at the system level for the applications as mentioned in previous section.
Therefore, in this thesis, it has been an important motivation to look for different front-end building blocks, which can be integrated into multifunctional MMIC to form flexible system for many applications.

**State-of-the-art in data transmission**

Despite intense research in mm-wave wireless communications, the most published experiments in data transmission use simple modulation schemes such as amplitude shift keying (ASK) [46], on-off keying (OOK) [47], or binary phase-shift keying (BPSK) [48]. The modulation format is simple and reliable, but the end result is low spectrum efficiency (1 bit/s/Hz). The spectral efficiency can be increased by using more complicated modulation techniques, such as multilevel phase shift keying (PSK) or multilevel quadrature amplitude modulation (QAM). A quadrature PSK (QPSK) of 20 Gbit/s at 120 GHz in a laboratory environment with 1 bit/s/Hz of spectrum efficiency is demonstrated in [49]. A 16-QAM 10 Gbit/s at 140 GHz with 2.86 bit/s/Hz spectral efficiency was demonstrated in [50]. In multi-channel transmission, the aggregate data rate of 100 Gbit/s using 16 QAM and 8 QAM modulation is demonstrated in [51]. A 256 QAM with 14 Mbit/s is demonstrated by [52] at 220 GHz. Fig. 1.5 compares published data transmission results with the results in this thesis.

**1.5 Thesis contribution**

This thesis consists of eight publications on the design and characterization of building blocks and their integration to make front-end transceiver chipsets for high-speed communication in both III-V (0.25 µm InP DHBT) and silicon (130 SiGe BiCMOS) technologies operating at D-band. Design emphasis is made on simple, yet robust direct conversion architecture that can be integrated on a single chip. The designed chipsets can be used to work in both heterodyne mode and homodyne mode. The chipsets have been verified experimentally.
System measurements are also described where bit error rate (BER), EVM and eye diagrams are measured when the presented TX and RX MMICs are used for a modulated signal transmission and reception. Fig. 1.6 summarizes and presents the data transmission results performed on the modulator, TX/RX chipset and TX/RX modules using various complex modulation formats. The thesis contains the design, implementation and characterization of the following circuits:

1. A direct conversion quadrature modulator and demodulator circuits with a novel topology for D-band communications using InP DHBT and SiGe BiCMOS technologies are presented. The passive structures for the circuits are designed and properly EM simulated which becomes increasingly important for the design success. The circuit covers the entire D-band, which is the widest bandwidth reported up to date.

2. A fully integrated broadband direct conversion in-phase/quadrature-phase (I/Q) TX and RX chipset is integrated and implemented in InP DHBT technology. The chipset consists of a X3 LO frequency multiplier integrated with an I/Q modulator or I/Q demodulator, and a low-noise amplifier (LNA) or power amplifier (PA).

3. A data transmission experiment using transceiver chipsets was demonstrated with QPSK and multiple-order QAM modulation. The InP DHBT chipset was tested both in homodyne and heterodyne architectures. A data rate of 48 Gbit/s with QPSK modulation was achieved. These tests indicate that the presented MMICs are especially well suited for transmission and reception of wireless signals at data rates which exceed the present state-of-the-art in the D-band by a factor of two. Real-time wireless data transmission on packaged TX/RX chipset in modules is also demonstrated and compared with state-of-the-art published results.

4. The SiGe BiCMOS quadrature up and downconverting mixers at D-band are designed fabricated and measured together with data transmission results. The demodulator circuit is integrated with low noise amplifier, and microstrip to waveguide transition at RF port as well as D-band amplifier and X6 multiplier at LO port into a multifunctional RX chip.
1.6 Thesis outline

The thesis is organized as follows: Chapter 1 addresses the need for increasing capacity in current and future communication networks and proposes several capacity enhancing next generation solutions. This gives the motivation of looking for high-data-rate, low cost and compact single chip front-end solutions at mm-wave. The remainder of the thesis is organized in four main parts, corresponding to four main questions and the answers thereto.

- What is the path loss incurred by millimeter-wave systems, and what factors affect the link budget analysis? Which radio architecture is most suitable to realize the compact and cost effective mm-wave systems?
- What is the choice of component technology available to MMIC designers? Benefits of heterostructure for realizing high-speed device.
- Which circuits should be used to implement the target architecture?
- What are the experimental setups and the results obtained for testing and characterizing an mm-wave transceiver circuits?

In Chapter 2, the theoretical background of thesis is described, including the concept of point-to-point link budget analysis and the principles of operation of front-end transceiver architectures with insights into the design issues at mm-wave frequencies. This choice affects the circuit design presented in the subsequent chapters. Chapter 3 outlines the choice of high frequency technologies available to MMIC designers, starting with the properties and attributes of the different semiconductor substrate materials, followed by the high-speed heterojunction devices. Chapter 4 provides a detailed description of design, characterization and measurement of front-end circuit building blocks operating in D-band and designed in InP DHBT. The chapter starts with a brief description of: the multilayer back-end InP DHBT technology, the principle of operation of mixer topology; the design of on-chip passive structures, modulator/demodulator circuits and balanced frequency multipliers. Chapter 5 describes the integration and implementation of the RF transceiver front-end circuits (LNA, modulator, LO frequency multiplier, power amplifier, demodulator) to form a multifunctional transmitter and receiver chips demonstrating state-of-the-art results. Chapter 6 demonstrates the data transmission tests on TX/RX chipset of which the design is presented in Chapter 4 and 5. Real-time wireless data transmission on TX/RX modules is also demonstrated and compared with state-of-the-art published results. Chapter 7 presents the design and implementation of a quadrature upconverting and downconverting mixer circuits using commercial 130 nm SiGe BiCMOS process. The demodulator circuit is further integrated with low noise amplifier, and microstrip to waveguide transition at RF port as well as D-band amplifier and X6 multiplier at LO port in order to build a multifunctional RX chip. Chapter 8 summarizes the main conclusions of the thesis together with potential future research opportunities. Finally, appended papers [A-H] are summarized in Chapter 9. The related articles, [A]-[H], are included at the end of the thesis.
Chapter 2

Point-to-Point Communication System Consideration

This chapter describes the theoretical background of the thesis with basic concepts and requirements of point-to-point communication systems. It starts with link budget analysis and choice of modulation techniques followed by the review of front-end system architectures and their performance limitations in monolithic integration. The system level specifications and the performance targets of the circuits that make up those systems are the focus of this thesis. Transceivers working in the 110-170 GHz frequency range that implement the concepts of this chapter will be described in Chapters 4, 5, 6 and 7.

2.1 Point to point communication

The objective of an RF transceiver is to transmit and receive information. The transmitter (TX) processes the data signal and applies the result to the antenna. Similarly, the receiver (RX) senses the signal picked up by the antenna and processes it to reconstruct the original data information. A key factor for a communications link in any wireless design is the calculation of the maximum reliable distance between transmitter and receiver.

2.1.1 Link budget

As illustrated in Fig. 2.1, a basic radio communication system consists of a transmitter and receiver with their antennas separated by a distance (d). The transmitter emits the modulated signal to the air via an antenna. In the receiver, the signal power at the antenna output is defined as the received power ($P_{RX}$), which is given by Eq. (2.1) and Eq. (2.2) [53-55].
Received power (dBm) = Transmitted power (dBm) + Gains (dB) – Losses (dB) \hspace{1cm} (2.1)

\[ P_{RX} = P_{TX} \times G_{ATX} \times L_{Channel} \times G_{ARX} \] \hspace{1cm} (2.2)

Where \( P_{TX} \) is the transmitter output power, \( G_{ATX} \) is the transmitter antenna gain, \( G_{ARX} \) is the receiver antenna gain and \( L_{Channel} \) the channel loss. Antenna gain is given by \( G_{ATX} = E_A \times D \). Here, \( E_A \) is the antenna efficiency and \( D \) is the directivity. At millimeter-wave, the channel loss \( (L_{channel}) \) mainly includes the path loss \( (L_{path}) \) and atmospheric loss \( (L_{atm}) \), neglecting other interferences.

\[ L_{channel} = L_{path} \times L_{atm} \] \hspace{1cm} (2.3)

The path loss is given by the Friis equation, which is given by Eq. (2.4) where \( d \) is the distance and \( \lambda \) is the wavelength of the radiated signal.

\[ L_{path} = \left( \frac{4 \pi d}{\lambda} \right)^2 \] \hspace{1cm} (2.4)

\[ L_{path} \; (dB) = 20 \log_{10} \left( \frac{4 \pi d}{\lambda} \right) \] \hspace{1cm} (2.5)

The atmospheric loss is given by Eq. (2.6) \cite{56}, where \( \alpha (f) \) is the measured values of the atmospheric attenuation.

\[ L_{atm} = 10^{-\frac{1}{10} \alpha (f) \times d} \] \hspace{1cm} (2.6)

\[ L_{atm} \; (dB) = -\alpha (f) \times d \] \hspace{1cm} (2.7)

Figure 2.2: Atmospheric attenuation in dry air versus frequency \cite{59}.
Chapter 2. Point-to-Point Communication System Consideration

The path loss and atmospheric loss increase with distance and frequency. A plot of the atmospheric attenuation in the mm-wave frequency range is given in Fig. 2.2 [57] [58]. The noise power at the RX input is simply assumed by Eq. (2.8), where $k$ is the Boltzmann constant, $T$ is the temperature, and $BW$ is the bandwidth.

$$N_{in} = k \times T \times BW$$

(2.8)

The input SNR ($SNR_{in}$) is then given by

$$SNR_{in} = \frac{P_{TX} \times G_{ATX} \times L_{channel} \times G_{ARX}}{k \times T \times BW}$$

(2.9)

Accordingly, the SNR at the receiver output ($SNR_{out}$) is related to the $SNR_{in}$ by the noise factor ($F$) of the receiver and is given by

$$SNR_{out} = \frac{SNR_{in}}{F} = \frac{P_{TX} \times G_{ATX} \times L_{channel} \times G_{ARX}}{k \times T \times BW \times F}$$

(2.10)

Typically, communication systems specify the required SNR ($SNR_{req}$) for the system performance because the bit error rate ($BER$) is determined by the $SNR_{out}$. In such real systems, the $SNR_{out}$ should be higher than the $SNR_{req}$, introducing the link margin ($LM$).

$$SNR_{out} = SNR_{req} \times LM$$

(2.11)

Therefore, the link margin is given by

$$LM = \frac{P_{TX} \times G_{ATX} \times L_{channel} \times G_{ARX}}{SNR_{req} \times k \times T \times BW \times F}$$

(2.12)

As expressed in Eq. (2.12), the quality of a wireless link depends on several factors related to the transmitter, the receiver, and the medium through which the signal propagates. Each black box in Fig. 2.1 contains many functions and a more preliminary view of wireless transceivers is shown in Fig. 2.3.

![Figure 2.3: Generic RF transceiver block diagram.](image-url)
From the link analysis in Eq. (2.12), we can readily make two observations. The first is that the TX must drive the antenna with a high power level so that the transmitted signal is strong enough to reach far distances. Transmitter output power is especially important when combined with the fact that output power drops with increasing frequency due to limitations in the active devices employed in the circuits. The second is that the RX should be able to sense a small signal and should first amplify the signal with low noise.

The noise factor (noise figure in dB) of the receiver determines the threshold for the minimum signal that can be reliably detected by the receiver. Therefore, the noise figure and power gain of the first stage play a dominant role in the receiver and can be calculated by the Friis formula [60]. Hence, the link budget should be carefully planned and designed for a reliable communication system.

2.1.2 Modulation techniques

The wireless communication transceiver design has constraints of limited allocated spectrum mandating the use of bandwidth-efficient modulation. The choice of modulation scheme is affected by spectrum efficiency and minimum required SNR for acceptable bit error probability.

\[
\text{Spectrum efficiency (}\eta\text{)} = \frac{\text{data bits transferred per second (}R_b\text{)}}{\text{carrier bandwidth in Hertz (}BW\text{)}},
\]

The unit of spectrum efficiency (\(\eta\)) is bit/s/Hz and theoretical value for different commonly used modulation schemes are listed in Table 2.1. It can be seen that a modulation scheme with higher spectrum efficiency can support a higher data rate but is more vulnerable to noise and interference which increase bit error rate (BER). Bit error probability gives a numerical description of the performance degradation in an additive white Gaussian noise (AWGN) environment. The bit error probabilities of various modulation schemes are listed in Table 2.1 [61]. The function Q is called the complementary error function or co-error function and is given in [55].

<table>
<thead>
<tr>
<th>Modulation Scheme</th>
<th>Data Rate (BW=1 GHz)</th>
<th>Spectrum Efficiency ((\eta))</th>
<th>Bit Error Probabilities</th>
</tr>
</thead>
<tbody>
<tr>
<td>OOK</td>
<td>0.5 Gbit/s</td>
<td>0.5 bit/s/Hz</td>
<td>(Q\left(\frac{E_b}{N_0}\right))</td>
</tr>
<tr>
<td>BPSK</td>
<td>0.5 Gbit/s</td>
<td>0.5 bit/s/Hz</td>
<td>(Q\left(\frac{2E_b}{N_0}\right))</td>
</tr>
<tr>
<td>D-BPSK</td>
<td>0.5 Gbit/s</td>
<td>0.5 bit/s/Hz</td>
<td>(0.5 e^{-\frac{E_b}{N_0}})</td>
</tr>
<tr>
<td>QPSK</td>
<td>1 Gbit/s</td>
<td>1 bit/s/Hz</td>
<td>(Q\left(\frac{2E_b}{N_0}\right))</td>
</tr>
<tr>
<td>D-QPSK</td>
<td>1 Gbit/s</td>
<td>1 bit/s/Hz</td>
<td>(0.5 e^{-\frac{E_b}{N_0}})</td>
</tr>
<tr>
<td>8-PSK</td>
<td>1.5 Gbit/s</td>
<td>1.5 bit/s/Hz</td>
<td>(\frac{2}{3} Q\left(\frac{6E_b}{N_0} \sin \frac{\pi}{8} B\right))</td>
</tr>
<tr>
<td>16-QAM</td>
<td>2 Gbit/s</td>
<td>2 bit/s/Hz</td>
<td>(0.375 Q\left(\frac{2E_b}{5N_0}\right))</td>
</tr>
</tbody>
</table>
Assuming the bandwidth is BW, $E_b$ is the signal energy received per bit and $N_0$ is the spectral density of AWGN. The SNR can be written as:

$$SNR = \frac{Signal \ power}{Noise \ power} = \frac{E_b \cdot R_b}{N_0 \cdot BW}$$

$$= SNR \ per \ bit \ \left(\frac{E_b}{N_0}\right) \ast \ Spectrum \ efficiency \ \left(\frac{R_b}{BW}\right)$$

Fig. 2.4 (a) presents the theoretical BER curves versus required CNR for some commonly used modulations. The carrier to noise ratio (CNR or C/N) is SNR of a modulated signal.

### 2.1.3 Error vector magnitude (EVM)

Error vector magnitude (EVM) provides insight into the quality of the modulated signal/symbol and is a measure used to quantify the performance of the wireless communication system. With an ideal modem, the received constellation points are located at the ideal coordinates. Error vector magnitude for a symbol is described in Fig. 2.4 (b).

![Figure 2.4: BER versus CNR for the selected modulations. For a given BER, a greater CNR is needed for the higher QAM levels (b) EVM in constellation plot [54-55].](image)

Figure 2.5: Effect of I/Q mismatch on QPSK signal constellation (a) gain error, (b) phase error [62].
The imperfections in the implementation such as I/Q mismatch (gain, phase, DC offset), carrier leakage, low image rejection ratio, phase noise, nonlinearity cause the actual constellation points to deviate from the ideal locations. As an example of deteriorations to increased BER (increases EVM), two impairments on a QPSK signal are illustrated in Fig. 2.5 [62].

### 2.2 Receiver architecture

This and the next section provide an overview of various transmitter and receiver architectures. The heterodyne architecture is discussed which is not very suitable to high levels of integration, followed by an overview of a number of other front-end architectures which are more useful to single-chip implementations. A review of their design issues and trade-offs is given which helps to determine their potential for emerging applications. Complexity, cost, power dissipation, and the number of external components have been the primary criteria in selecting transceiver architectures.

![Image of Receiver Architecture](image)

Figure 2.6: Block diagram of a simple heterodyne downconversion. Rejection of image versus suppression of interferers for (a) high IF and (b) low IF [62].
2.2.1 Heterodyne receiver

The block diagram of a heterodyne receiver is shown in Fig. 2.6. The RF signal is first filtered by a band pass filter (BPF), which removes the unwanted out-of-band signals. A low noise amplifier (LNA) is used to amplify the input signal with minimum noise. The desired signal located at the frequency $\omega_{RF}$ is frequency translated to the intermediate frequency $\omega_{IF}$ by an LO signal $\omega_{LO}$ in the mixer. However, the signal centered at the image frequency $\omega_{IF} + 2\omega_{IF}$ denoted $\omega_{IM}$ is also frequency translated to $\omega_{IF}$. The image signal can be much stronger than the desired signal. Therefore, the image signal must be sufficiently attenuated by using an image reject filter before the frequency translation [62]. Another band pass filter (channel-select filter) centered at the wanted IF frequency is used at the mixer output. The input signal band is translated from RF to IF to relax the Q requirement of the channel-select filter, because filtering a narrow channel centered at high frequencies and accompanied by large interferers demands prohibitively high quality (Q) filters.

Problem of Image

The choice of the $\omega_{IF}$ is critical for this architecture. The choice of $\omega_{IF}$ depends on the characteristics of practical filter implementations and results in trade-off between sensitivity and selectivity as follows:

- A high $\omega_{IF}$ results in maximum image signal attenuation from the image reject filter, but increases the design challenges in the IF filtering and amplification circuits as shown in Fig. 2.6 (a).
- A lower $\omega_{IF}$ is preferred for increased quality of channel selection and results in relaxed $\omega_{IF}$ filtering and amplification requirements but has poor image rejection as shown in Fig. 2.6 (b).

2.2.2 Superheterodyne receiver

The issue of trade-off between sensitivity and selectivity in the simple heterodyne architecture is solved by extending the concept of heterodyning to the multiple downconversions. Each frequency conversion is followed by filtering and amplification. This architecture is called superheterodyne or dual-IF architecture and is illustrated in Fig. 2.7.
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This technique relaxes the Q required by each filter but the second downconversion also entails the problem of image. Such multiple mixing complicates the receiver design due to the increased number of nonlinear components and is very vulnerable to spurious signals [62].

Implementation complexity

The excellent performance in heterodyne architecture is achieved by using the best technologies to implement the various components. For example, the RF/IF filters are typically implemented using ceramic filter technology, the image reject filter using surface acoustic wave (SAW) technology; and depending on the nature of the circuit the remaining components are implemented in gallium arsenide, indium phosphide, silicon bipolar, and silicon CMOS. However, such a large number of components and interconnects may lead to unwanted internal coupling of the signal particularly marked at higher frequencies. In addition, it increases the power consumption and temperature of the chip and results in unwanted effects. Finally, the larger chip area is not favorable when price and large scale integration are of concern.

2.2.3 Image-reject receiver

The trade-offs governing the use of image-reject filters in heterodyne architectures have motivated the use of image-reject topologies such as the Hartley [63-64] topology as shown in Fig. 2.8.

![Hartley image reject radio receiver architecture](image)

Figure 2.8: Hartley image reject radio receiver architecture [63].

![Image rejection versus amplitude and phase imbalance](image)

Figure 2.9: Image rejection versus amplitude and phase imbalance [65].
The image reject mixer can be used as the first mixing stage in the superheterodyne receiver of Fig. 2.7. In image reject topology, a local oscillator signal is required that generates in-phase (I) and quadrature (Q) signals which are 90 degree out of phase with respect to each other. Another 90 degree phase shifter is required at the mixer output. This type of mixer topology relies on different phase shifts to present a lower conversion gain to the signal at the image frequency as compared to the desired signal and therefore IF can be chosen to be low enough for channel filtering. This architecture is also called a low-IF receiver [66]. This architecture increases complexity in the active circuitry but is favorable from an integration point of view.

Practical Considerations

In practice, the degree of image rejection achieved by an image reject receiver is sensitive to the amplitude mismatch and phase error between the I and the Q paths as well as by the quadrature phase mismatch in the two local oscillators [65]. This trade-off between image rejection and amplitude/phase imbalance is given by Fig. 2.9, where $A$ is amplitude and $\theta$ is phase errors. Integrated circuit implementations typically achieve 25-40 dB of image rejection. If additional image rejection is required, a high intermediate frequency can be used making the image signal far away from the center frequency of the RF filter. This provides an additional attenuation of the image signal. Image rejection topologies have become popular with the advent of monolithic integration. This facilitates better component matching due to their close proximity on the die.

2.2.4 Homodyne receiver

In a homodyne receiver, the modulated RF carrier is directly downconverted to baseband through a single mixing process [63] [67]. This architecture is also known as zero-IF or direct conversion architecture. Fig. 2.10 (a) shows the block diagram of the homodyne architecture where the image problem disappears since the information signal acts as its own image eliminating the need for an image reject filter (IRF). The channel select filter can be replaced by a low-pass filter (LPF) which can be easily integrated in the monolithic integration.

Figure 2.10: (a) Simple homodyne receiver (b) homodyne receiver with quadrature downconversion [78].
Therefore, this architecture eliminates all intermediate frequency components and their associated design challenges. This leads to low cost, smaller size and less power consumption. In a direct conversion receiver, if the signal is phase modulated signal, a quadrature (or I/Q) downconversion mixer is needed to recover the phase information, as illustrated in Figure 2.10 (b).

**Challenges and solutions**

The biggest concern in a direct conversion receiver is the low frequency noise referred to as flicker noise generated by the electronic components, especially the baseband amplifier. Since the information signal is converted to DC, the flicker noise of amplifiers and mixers can severely degrade the signal-to-noise ratio of the signal or DC offsets can saturate the baseband circuits, such as amplifiers and filters.

Also, any part of the LO signal which leaks to the input of the receiver, mixes with itself and becomes a DC component. This DC signal is in the same band as the information signal and can effectively reduce the signal-to-noise ratio. Generally, any even-order nonlinearity of the mixers and RF amplifiers is a potential problem with direct conversion receivers [62]. Even-order intermodulations generate baseband components which again come on top of the information signal and degrade its quality.

The DC offset problem can be solved by shaping the information signal to contain less information at lower frequencies where the noise is higher and which then can be filtered using a high-pass filter. This technique is particularly suited to wideband channels where a few kilohertz of the channel can be wasted with no significant drop in the data rate. On the other hand, a high-pass filtering is not feasible if prohibitively large capacitors or resistors are required and especially if very low corner frequencies are required [62].

### 2.3 Transmitter architecture

The transmitter mainly performs the reverse functions of the receiver. An RF transmitter performs modulation, up-conversion, and power amplification. The transmitter architectures are found less than receiver architectures due to relaxed specification of noise, interference rejection, and band selectivity in transmitters as compared to receivers.

![Figure 2.11: Heterodyne transmitter.](image-url)
2.3.1 Heterodyne transmitter

Fig. 2.11 shows the heterodyne architecture of a transmitter. The baseband I and Q channels undergo quadrature modulation at a lower frequency \( \omega_1 \) (called the intermediate frequency) and is upconverted by a second mixer to \( \omega_1 + \omega_2 \). The first BPF suppresses the harmonics of the IF signal, while the second removes the unwanted sideband centred around \( \omega_2 - \omega_1 \). This architecture also solves the problem of LO pulling in transmitters because the PA output spectrum is well away from the frequency of the VCOs [68-70]. The difficulty in two-step transmitters is that the bandpass filter following the second upconversion must reject the unwanted sideband by a large factor, typically 50 to 60 dB. This requires a high Q second filter centred at a higher frequency. This is typically achieved by a passive and relatively expensive off-chip device.

2.3.2 Homodyne transmitter

If the transmitted carrier frequency is equal to the local oscillator frequency, the architecture is called direct conversion architecture. A direct quadrature modulator is required to modulate both amplitude and phase of the carrier as shown Fig. 2.12. Two orthogonal carriers are generated from the local oscillator signal and are modulated by the in-phase and quadrature components of the baseband signal [63]. The modulated carriers are then added together and amplified before transmission. The quadrature modulator input does not need to be tuned and the modulation bandwidth is instead determined by the operating bandwidth of the baseband circuitry. This architecture does not require IF and RF filters making it feasible for integration in a single chip. This architecture is used to design the modulator in Chapters 4 and 7.

This architecture also eliminates the drawback of heterodyne architecture of Sec. 2.3.1 where a direct conversion transmitter can be used as a single sideband upconverter at the second stage in a heterodyne transmitter of Fig. 2.11. The upper and lower sidebands can be separated by an additional 90 degree hybrid at the input without any need for additional filtering. The intermediate frequency can be set as low as possible for channel selection.

The quality of sideband suppression depends on the phase balance of the two carrier signals. This is in fact how the quadrature modulator and transmitter will be characterized in Chapters 4, 5 and 7. To maintain the waveform quality of the modulated signal, phase and amplitude mismatch of both I/Q input and the quadrature LO signals need to be minimized.

![Figure 2.12: Homodyne transmitter.](image-url)
If \( A \) is the amplitude and \( \theta \) is the phase mismatch in the circuit then sideband suppression can be calculated by Eq. (2.13).

\[
\text{Sideband supression (dB)} = 10\log\left[\frac{1+A^2+2A\cos\theta}{1+A^2-2A\cos\theta}\right]
\]  (2.13)

Depending on the modulation format and system requirements additional correction may be applied to remove the phase and amplitude errors. Numerous analog and digital methods for I/Q mismatch correction are available [68-70].

**Design challenges and solutions**

Direct conversion architecture suffers from significant drawback of carrier leakage through the mixer [74]. LO leakage is the presence of the LO signal at the transmitter output. This unwanted signal is located within the band of the transmitted signal and cannot therefore be avoided by means of filtering. LO leakage is caused by signal coupling from the local oscillator to the output or DC content of the input signal. The associated LO phase noise degrades the performance of the transmitted signal [71].

Digital signal processing can be used to remove the DC component of the baseband signals but it is nevertheless very important that the mixers which are used in the modulator design exhibit a very high level of isolation between the LO and RF ports. This requirement can be fulfilled by using double-balanced mixer topologies in direct conversion architecture.

**2.4 Transceiver performance metrics**

The main design specifications for a receiver are the frequency of operation, dynamic range, gain, power consumption, and, image rejection (in image reject architecture). Typical parameters to characterize the transmitter performance are the output power, transmit Power Spectral Density (PSD) mask (or Adjacent Channel Power Ratio ACPR), the error vector magnitude (EVM).

**Unwanted Emissions and output power**

The signal radiated by the transmitter antenna must comply with strict rules imposed by both the wireless standard and radio regulations in each country. Federal Communications Commission (FCC) for instance is the regulatory agency in USA. This limits the maximum power that can be transmitted in a specific frequency band. This power is defined by a modulation mask to ensure negligible radiation in adjacent channels. In addition, relative adjacent channel power for the modulated signal is also specified by the wireless standards.
Sensitivity and Dynamic Range

The dynamic range is specified in terms of sensitivity and linearity. The noise floor and gain compression set a minimum and maximum realistic power range called dynamic range [62-63]. The figure of merit for linearity is the total harmonic distortion (THD). The non-linearity leads to a large number of harmonics at the output for a single tone at the input. THD is defined as the ratio of the sum of the powers of all the harmonics present at the output of the circuit, to the power of the fundamental tone at the output.

Noise

Noise in electronic circuits is caused by random processes such as thermal vibrations in active and passive electronic components at ambient temperatures above absolute zero or the flow of electronic charges through potential barriers. The thermal, shot, and flicker noise are the most important types of noise sources encountered in semiconductor devices and integrated circuits.

Phase noise

The noise arising from the short term phase fluctuations in a signal is defined as a phase noise. These fluctuations appear as a noise spectrum spreading out either side of the signal and is shown in Fig. 2.13 [63]. In the case of the transmitter, local oscillator noise is amplified by the subsequent amplifier stages and is transmitted together with the wanted signal by the antenna degrading the quality of the transmitted signal. In the receiver, the noise components in the LO mix with other signals that are offset from the LO resulting in degradation of the SNR at the output signal [71].
Chapter 2. Point-to-Point Communication System Consideration
Chapter 3

High Frequency Semiconductor Devices

Monolithic circuits are based on complex semiconductor structures and a good understanding of the internal operation of devices is essential for the design and analysis of the circuits using them. This chapter outlines the choice of component technology available to MMIC designers, starting with the properties and attributes of the different semiconductor substrate materials, followed by the description of high-speed heterojunction devices. Heterojunction technologies are used for the designs presented in Chapters 4, 5, 6 and 7 of this thesis.

3.1 Semiconductor substrate material

A Monolithic Microwave Integrated Circuit (MMIC) is a microwave circuit in which the active and passive components are fabricated on the same semiconductor substrate [72]. The performance characteristics of the transistors and of the final MMIC is dependent on the choice of semiconductor for the substrate material [73]. The resistivity of the semiconductor substrate in its semi-insulating state is responsible for the loss and Q-factor of the passive components created on its surface [74]. High resistivity wafers are required for higher inductor quality factors and to minimize cross talk between transistors.

The most commonly used substrate materials are Silicon (Si), Gallium Arsenide (GaAs), and Indium Phosphide (InP) [75] [76]. The Silicon Carbide (SiC) and Gallium Nitride (GaN) [77] substrate materials are wide band-gap semiconductors. They have higher breakdown voltages and can operate at higher junction temperatures. Therefore, they are able to generate higher output powers than the other semiconductor materials.

3.2 High frequency active devices

The high-frequency active devices used in MMICs can be divided into field effect transistors (FET) and bipolar transistors [78]. Transistors are three terminal devices, where a signal on one input can control the current flowing between two other terminals. In digital mode the transistor switches between off and on states, and in an analog mode, a small change in the input signal at the gate or base terminal is amplified between the other two terminals.
Field-effect transistors consists of metal oxide semiconductor field effect transistor (MOSFET), metal semiconductor field effect transistor (MESFET) and the high electron mobility transistor (HEMT). Commercial HEMTs are realized in several III-V material systems such as GaAs/InGaAs, InP/InGaAs, and AlGaN/GaN. The high-frequency bipolar transistors include the most widely used SiGe HBT, GaAs HBT, and InP HBT. HBT stands for heterojunction bipolar transistor. All state-of-the-art high frequency transistors include some heterojunctions and compound materials [79-86].

3.2.1 High frequency figures of merit

The transistor bandwidth is defined in terms of two RF figures-of-merit, the current gain cutoff frequency ($f_t$) and the maximum frequency of oscillation ($f_{MAX}$). The current gain cutoff frequency is the frequency at which the small signal current gain ($h_{21}$) of the transistor becomes unity (0 dB). The maximum frequency of oscillation is the frequency at which the unilateral power gain ($U$) of the transistor becomes unity [87-88]. For a bipolar transistor, the current gain cutoff frequency is given by Eq. (3.1) where $\tau_c$ and $\tau_b$ are the collector and base transit times, respectively, $C_{je}$ is the emitter-base junction capacitance, $C_{cb}$ is the total collector base junction capacitance, and $R_{ex}$ and $R_c$ are the extrinsic emitter and collector resistances, respectively.

$$\frac{1}{2\pi f_T} = \tau_c + \tau_b + \frac{kT}{qI_c} (C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb}$$

(3.1)

The maximum frequency of oscillation depends on the $f_t$ of the transistor and the base-collector junction parasitic given by Eq. (3.2), where $R_b C_{cb}$ is the product of the base resistance and the collector-base junction capacitance.

$$f_{MAX} = \sqrt{\frac{f_T}{\ln R_b C_{cb}}}$$

(3.2)

Both $h_{21}$ and $U$ are frequency dependent and roll off with a slope of −20 dB/dec at high frequencies. These quantities are useful in comparing different types or generations of transistors as well as in predicting the performance of circuits incorporating the devices.

3.3 Heterojunction devices

A heterojunction device is the device in which the junction of two semiconductor materials is formed having different band gaps. Heterojunction significantly enhances the device performance by modifying the bandgap of certain layers in the structure.
3.3.1 High electron mobility transistor (HEMT)

In a FET device, the current flows through a channel between source and drain. The number of carriers in the channel is modulated by the gate voltage. The current can be increased by increasing the doping concentration in the channel. On the other hand it decreases the electron mobility. This trade-off between high mobility and high carrier concentration cannot be avoided. The tradeoff can, however, be avoided by using a heterojunction structure obtaining high electron concentrations in a lightly doped material which also ensures high mobility \[74\]. The high electron mobility transistor (HEMT) utilizes a vertical architecture incorporating layers of different materials. This forms a device channel in which the electrons are physically separated from their parent donors resulting in increased electron mobility. The current flows from the source to the drain under the gate contact via the high mobility channel (also called two-dimensional electron gas). Another consequence is the reduction in electrons collision which improves the noise figure of the HEMT compared with that of ordinary FETs \[79\][85]. Therefore, HEMT devices have improved high frequency noise and gain characteristics compared with conventional GaAs MESFETs.

The cross-section of an AlGaAs/GaAs HEMT and its conduction band profile is shown in Fig. 3.1 (a) and 3.1 (b), respectively. In a AlGaAs/GaAs HEMT, the lattice constants of AlGaAs and GaAs are almost identical simplifying the complexities of the growth of high quality single-crystal AlGaAs/GaAs heterostructures \[86\].
3.3.2 InP heterojunction bipolar transistor (InP HBT)

The Heterojunction Bipolar Transistor (HBT) was developed to overcome the limitations of conventional bipolar transistors. In a classical homojunction bipolar transistor, thinner base regions and higher doping levels are required to reach higher operating frequencies. This results in significant leakage effects due to higher electric fields across narrow depletion regions. The reduction in base width increases the base resistance, which slows the device response time. The base resistance can be reduced by increasing the base doping concentration, which decreases the current gain [89]. It is, therefore, difficult to optimize the base thickness and doping concentration for high-speed, high gain and low base resistance in homojunction bipolar transistors. The introduction of heterojunctions improves the transit time, current gain and base resistance simultaneously.
A typical structure of HBT is shown in Fig 3.2 (a) [63]. It has buried n-type collector layer under a p-type base. The emitter layer is a highly n-type doped top layer having a different band gap from the base layer. A wider bandgap material is used for the n-type emitter and a smaller bandgap semiconductor for the p-type base resulting in band diagram as in Fig. 3.2 (b). This emitter-base heterojunction completely changes the ratio between electron and hole currents. In a forward bias condition, holes must overcome a much larger potential barrier than electrons resulting in less hole current injected into the emitter. On the other hand, the electron current injected into the base increases which results in a high current gain even if the doping concentration in the base is high [74].

The most common III-V material combinations are AlGaAs/GaAs, InGaP/GaAs, InP/InGaAs, InAlAs/InGaAs/InP, InP/InGaAs/InP, and InP/InGaAsSb/InP [90].

### 3.3.3 SiGe heterojunction bipolar transistor (SiGe HBT)

The SiGe HBT is different from standard silicon bipolar transistors because the base is constructed from a different semiconductor material (grading Ge in silicon base) [63]. The SiGe has a bandgap that is lower than silicon. Increasing the germanium concentration in the base reduces the bandgap further. The Ge concentration in the base is shown in Fig 3.3 (a) which results in the band diagram of Figure 3.3 (b). The graded base structure introduces an additional built-in electric field which speeds up the movement of electrons across the base. This reduces the transit time of electrons moving from the base into the collector and enables the SiGe HBT to operate at higher frequencies than silicon bipolar. The germanium concentration grading in the base increases the current gain. This allows to increase the doping in the the base, and therefore reduces the base resistance without significantly degrading current gain. The lower base resistance is desired to increase $f_{MAX}$ and to decrease the noise figure ($NF_{MIN}$). In addition, Ge grading in base also increases the Early voltage which is desirable in analog applications where a large intrinsic voltage gain is required.

Figure 3.3 (a) Doping strategy for SiGe HBT (b) energy band diagram of graded-base SiGe HBT [63] [79][74].
3.4 Summary

Compared to InP HEMTs, double-heterojunction bipolar transistors (DHBTs) with a wide bandgap InP collector will have a higher breakdown voltage at a given current gain cutoff frequency $f_T$ [90]. Highly scaled indium phosphide (InP) heterojunction bipolar transistor (HBT) technologies have been demonstrated with maximum frequencies of oscillation ($f_{\text{MAX}}$) of $>1$ THz and circuit operation has been extended into the lower end of the terahertz (THz) frequency band [91] including 200 mW power amplifiers operating at $>200$ GHz [92]. The biggest challenge for compound semiconductors is the production cost and yield compared with those of Si-based technologies.

SiGe HBT based technology is also gaining increasing relevance for emerging millimeter-wave markets. It allows the integration of multiple application specific functionalities on a single silicon chip (RF ASIC) with excellent yield and uniformity and the possibility of integrating the digital circuits to take into account RF impairments [93-94]. The challenge in designing mm-wave circuits using these high performance bipolar devices on Si is the lossy Si substrate and the need for signal isolation. This makes the integration of multi-channels receivers and transmitters more challenging in terms of ensuring signal integrity across the substrate and routing signal. While SiGe devices have shown capability in the mm-wave range, they are unlikely to replace III-V devices in applications where either ultra-low noise or high-output power is required.
Chapter 4

Design of InP DHBT Integrated Active and Passive Circuits

This chapter elaborates the design and implementation of quadrature up and downconverting mixer circuits as well as balanced frequency multipliers with respect to their major performance parameters along with the design of on-chip passive structures in the D-band frequency range. The circuits are implemented as MMICs in InP DHBT technology. Some of the critical design and layout issues are discussed and the comparison is made with state-of-the-art reported work in recent literature.

4.1 250 nm InP DHBT MMIC technology

The presented circuits are designed and fabricated using an InP Double Heterojunction Bipolar Transistor (DHBT) technology with an emitter width of 0.25 μm. This technology uses two heterojunctions in the device by using a p-type InGaAs base and an n-type InP collector/emitter. It allows a base with higher doping and thereby a thinner base resulting in

![Figure 4.1: Cross-section of the 250 nm InP DHBT process. (Courtesy Teledyne Scientific Company, USA)](image-url)
higher cut-off frequency [95-96]. InP based HBT transistors have superior material properties and a wide bandgap InP collector leading to terahertz frequency operation with high voltage handling capacity [34]. Terahertz Monolithically Integrated Circuits (TMIC’s) low-noise and driver amplifiers [35], high-speed power-DACs [36], voltage controlled oscillators [37-38], static [97] and dynamic frequency dividers [98-99] and frequency converters [100-101] have been designed and fabricated using this technology.

Fig. 4.1 shows a representative cross-section of the back-end of the 250 nm InP DHBT MMIC process, which is developed by Teledyne Technologies, Inc., Thousand Oaks, California, USA [95-96] [102]. This process includes thin-film resistors (TFR), MIM capacitors, and 4-levels of interconnect metal (M1-M4). A 1 µm thick benzocyclobutene (BCB) spin-on-dielectric (εr ~2.7) is used as the interlayer dielectric between each metal layer. Electroplated Au-based interconnects are used for the metallization layers, where M1-M3 have a thickness of 1 µm and M4 has a thickness of 3 µm. Fabricated transistors exhibit a typical DC current gain (β) of around 25 and can operate with an emitter current density of up to 12 mA/μm² with a maximum collector emitter voltage of 2 V. The collector emitter breakdown voltage (BVCEO) is greater than 4 V at lower current densities. The fT and fMAX of this process are 350 GHz and 650 GHz, respectively. The multi-layer back-end process introduces new possibilities of complicated layouts in a relatively smaller physical area as well as the challenges in the circuit design.

4.2 Gilbert-cell active mixer

Fig. 4.2 (a) and Fig. 4.2 (b) show the single balanced mixer and the Gilbert-cell mixer, respectively. Both the topologies have two parts: input stage (lower transistors) and switch stage (upper transistors). The input stage is called the transconductance stage that converts the RF voltage signal to a current signal. The switch stage is driven by the local oscillator. It switches the current through the lower (RF) transistor(s) back and forth between the two different resistive IF loads.

![Figure 4.2: (a) Single balanced mixer topology (b) Classic Gilbert-cell mixer topology.](image-url)
Ideally, the emitters of the LO transistors are virtual ground for the LO. This generates no LO voltage on the collectors of the RF transistors and LO signal switches the LO switching transistors on and off without affecting the RF transistors. HBT works better (i.e. faster) as current switches in the LO stage due to their exponential (I_C versus V_{BE}) relationship as compared to the square (I_D versus V_{GS}) relationship of the FET device. Therefore, HBT based Gilbert mixers typically operate at higher frequencies compared to FET based Gilbert mixers. In the conventional Gilbert mixer, the sources of the RF transistors are connected to a current source to cancel even order currents generated in the RF transistor pair.

A drawback of the single balanced mixer compared to the Gilbert-cell mixer is the lack of inherent port isolation. The biggest concern in direct conversion receivers is the LO signal which leaks to the input of the receiver. It mixes with itself and becomes a DC component. This DC signal is in the same band as the information signal and can effectively reduce the dynamic range. Similarly, in a direct conversion transmitter, any carrier leakage through the mixer is fed together with the wanted RF signal to the input of the power amplifier where it gets amplified and transmitted through the antenna. This often results in a residual LO signal of the same magnitude as the wanted RF signal. This creates interference and possibly breaking spectrum regulations for the overall system. Therefore, it is important to minimize the LO-to-RF leakage, i.e. to enhance the LO-to-RF isolation by using double balanced topology. In bipolar transistor technologies, the Gilbert-cell mixer is popular for its excellent properties, such as relatively high conversion gain, broad operating bandwidth, and good port-to-port isolation [103-104].

In Fig. 4.2 (a), suppose an differential RF signal \( V_{RF}(t) \) as in Eq. (4.1) is applied to the transconductance stage which converts it to current \( I_{RF}(t) \) given by Eq. (4.2). The \( g_m \) in the bipolar technology is given by Eq. (4.3), where \( I_C \) is the collector current and \( V_t \) (25 mV at 25 °C) is the thermal voltage. \( V_t \) is given by equation Eq. (4.4), where \( k \) is the Boltzmann constant, \( T \) is the temperature and \( q \) is the charge.

\[
V_{RF}(t) = V_R \ast \cos(\omega_{RF}t) \tag{4.1}
\]
\[
I_{RF}(t) = g_m \ast V_{RF}(t) \tag{4.2}
\]
\[
g_m = \frac{I_C}{V_t} \tag{4.3}
\]
\[
V_t = \frac{kT}{q} \tag{4.4}
\]

The transistors Q3, Q6 and Q4, Q5 turn on and off alternately. In the positive half period of the LO signal, Q3, Q6 are turned on and Q4, Q5 are turned off. In the negative half period, Q4, Q5 are turned on and Q3, Q6 are turned off. To fulfill this requirement, the LO signal must be kept at a suitable magnitude to ensure accurate switching. The LO switching function \( T(t) \) is shown in Fig. 4.3 where

\[
T_1(t) = \frac{1}{2} + \frac{2}{\pi} [\sin \omega_{LO} t + \frac{1}{3} \sin 3\omega_{LO} t + \cdots] \tag{4.5}
\]
\[
T_2(t) = -\frac{1}{2} + \frac{2}{\pi} [\sin \omega_{LO} t + \frac{1}{3} \sin 3\omega_{LO} t + \cdots] \tag{4.6}
\]
Chapter 4. Design of InP DHBT Integrated Active and Passive Circuits

The RF current is multiplied by the LO switching function $T(t)$ and produces an output IF current which then passes through $R_L$ and gives differential output signal $V_{IF}(t)$ as Eq. (4.7).

$$V_{IF}(t) = 2g_m R_L T(t) V_{RF}(t)$$  \hspace{1cm} (4.7)

If $T(t)$ is a square wave with 50 percentage duty cycle, the symmetry causes the even-order LO harmonics to drop out of the LO spectrum [105]. The RF signal gets multiplied by a single frequency cosine at $\omega_{LO}$ and produces output spectral lines at $\omega_{LO} \pm \omega_{RF}$ which are the desired upconverted or downconverted frequencies and is shown in Fig. 4.4. From Fig. 4.4, there will be harmonics of the LO present at $3\omega_{LO}, 5\omega_{LO}$, etc., that will also mix with RF signal to produce outputs called spurious or undesired signals. All mixing terms with even harmonics of the LO including the DC term are cancelled due to the balanced topology (odd symmetry in $T(t)$). This reduces the number of spurious signals at the output compared with unbalanced mixer topology, making the selection of the LO and IF frequencies less restrictive. Any signal which couples to the output from the LO or RF ports of the balanced mixer appears as a common mode signal on the IF port.
In order to make sure that this common mode does not affect the mixer performance, it should be rejected with for instance an amplifier stage with high common mode rejection ratio (CMRR) or a passive centre-taped transformer. Therefore, to take full advantage of this design, an IF balun, either active (a differential amplifier) or passive (a transformer or hybrid), is required.

### 4.3 On-chip millimeter-wave passive component design

The quadrature balanced mixers presented in Sec 4.4 and Sec. 4.5 require generation and distribution of differential 90 degree phase-shifted millimeter-wave signals. In order to minimize the sensitivity to noise and undesired couplings, single-ended signals are converted to differential as soon as they are interfaced to the chip. RF and LO baluns are designed to a interface differential circuit to single-ended signals. The same balun design is used on both local oscillator (LO) and RF ports since these signals are at the same frequency for direct-conversion transmitter and receiver architectures.

Balanced signal lines utilize the broadside coupling on M4 and M3 while M1 is still present as a DC return path and also to provide a well-defined ground reference for common-mode

![Figure 4.5](image-url): 3D layout and simulated amplitude imbalance and phase difference between output ports of (a) RF and LO marchand balun (b) differential LO coupler [A].
signals. Proper implementation of these passive structures and their modeling accuracy is very important for design success at millimeter-wave. Fig. 4.5 (a) shows 3-D layout and simulated amplitude imbalance and phase difference between output ports of RF/ LO Marchand balun.

Fig. 4.5 (b) shows the generation of four quadrant phases of the LO signal that can either be performed by cascading a single ended 90 degree hybrid with two 180 degree hybrids, or differential 90 degree hybrid. Quadrature differential LO signals are generated with an on-chip differential coupler. The isolated port is terminated in a 100 ohm TFR resistor and M1 is included under the whole structure as a common mode reference. The 3-D view and simulated performance of the coupler in terms of amplitude and phase imbalance are shown in Fig. 4.5 (b). It is seen that the coupler has a 1.4 dB amplitude and a 7 degrees phase imbalance between the two output ports in the D-band. The reflection coefficients on the input and output ports are simulated to be lower than -18 dB. The phase and amplitude imbalance errors can increase the bit error rate of a communication system, and depending on the system requirements, additional analog and digital methods may be applied for this systematic correction [18]–[25].

Unlike conventional transmission line based matching techniques, custom spiral inductors are implemented and used together with MIM capacitor of the process to perform impedance matching in this design. While MIM capacitor models are available in a process design kit, spiral inductors had to be custom designed and modeled to be used in matching networks and inductive loads. Fig. 4.6 shows the geometry of a two-turn on-chip inductor and its extracted equivalent model. \( L_1, R_1 \) and \( L_2, R_2 \) are the effective inductance and resistance of each turn in the M3 and M4 layers, respectively, and \( C_c \) models the capacitive coupling between the turns. \( C_{sub}, L_{sub} \) and \( R_{sub} \) represent the lumped capacitance, inductance, and resistance between metal segments and the M1 ground plane, respectively. For a 40-pH inductor used in this design, the simulated quality factor is as high as 50 at 200 GHz and the self-resonance frequency is 348 GHz.

Figure 4.6: 3-D layout and lumped-element model of a multilayer on-chip inductor [A].
4.4 Design and implementation of D-band direct conversion I/Q demodulator

Fig. 4.7 shows block diagrams of two possible configurations of a quadrature demodulator. While both topologies are similar in principle, the presented circuits have the 90 degree phase shift on the LO signal because the quadrature phasing on a RF signal path increases the noise figure of the receive path due to loss caused by the passive network [62]-[63].

4.4.1 Circuit design and implementation challenges

The schematic of the designed broadband direct quadrature downconverting mixer is shown in Fig. 4.8. The circuit consists of two double balanced Gilbert mixer cells and the LO phase generator. The L-C network on the bases of Q₁-Q₄ transistors maximizes the base-emitter voltage swing for effective switching. The RF port of the mixer is impedance matched to 50 ohm to interface to a low-noise amplifier or directly to the antenna. The inductance of the routing transmission lines is sufficient and does not need any spiral inductor at the RF port. This is advantageous in order to reduce the input loss and therefore the noise of the mixer. Resistive IF loads are used to avoid the need for large on-chip inductors and to minimize the risk of instability. All transistors have emitter lengths in the transconductance stage and switching pairs are scaled to optimize the mixer performance. For fast switching performance, Q₁-Q₈ transistors are chosen to be 2 µm and Q₉-Q₁₂ transistors are accordingly scaled to 4 µm length for better linearity and current handling. The IF ports are isolated from the next stage by emitter followers which are also biased with current sources and are designed to match to 50 ohm over a broad bandwidth. The operating condition is set by the reference current which is mirrored to the two mixer cells as shown in Fig. 4.8.

![Figure 4.7: Two variation of demodulator topology depending on 90 degree hybrid location where each mixer is a double balanced Gilbert-cell mixer [A].](image-url)
The base bias to the RF differential pair and LO quad is applied through the resistors and inductors respectively. A collector voltage of 2.7 V is applied to the two mixing cells and emitter follower, where the mixing cells draw 8.5 mA and the emitter follower requires 17 mA of collector current. It will be shown later that this collector current also results in good noise performance. The voltages applied to the bases of the switching and transconductance transistors are 2 V and 1.4 V, respectively.

The mixer circuits are designed with differential topology to maximize the isolation between the LO and RF ports. The choice of differential topology for a quadrature architecture complicates the distribution of multiple phases of the LO signal on the chip. By taking advantage of the multilayer stack, this approach significantly reduces the consumed chip area. The chip photograph of the direct carrier quadrature downconverter is shown in Fig. 4.9. As annotated in the figure, the mixer cells including the transconductance stages and the switching quads are densely laid out in the center in order to minimize any unwanted parasitic effects. The LO distribution and phasing as well as the matching networks are all symmetrically planned around the mixing cells to maintain the amplitude and phase balance of the modulator as much as possible. As mentioned earlier, RF and LO baluns are placed close to the GSG pads and may

Figure 4.8: Simplified schematic diagram of direct conversion quadrature downconverting mixer circuit [A].
be removed in future integrations. The chip area is mostly determined by the pads but the active chip area including the two baluns is 560 μm x 440 μm. Other interconnects, though only very short, are modeled as transmission lines and their effects are included in the simulation. These components are EM-simulated in HFSS and imported into the circuit design environment for co-simulation.
4.4.2 CW and NF measurement

CW measurement

Mixer measurement involves particular challenges since three signals at different frequencies and different levels are involved and their power should be measured either as absolute quantities or in relation to each other. This requires measurement techniques other than

![Diagram of CW measurement setup](image)

Figure 4.10: CW measurement setup of downconverter (a) illustration of setup, (b) photo of setup in the laboratory.
those used for linear devices such as filters and amplifiers. Setting up and calibrating frequency offset measurements are typically harder and require more equipment.

Fig. 4.10 shows the continuous wave (CW) measurement setup. GSG probes with WR6.5 waveguide interface were used on LO and RF ports and a dual differential GSSGSSG for the balanced IF ports. The LO signal is provided from an Agilent 8257D synthesizer together with a X4 frequency multiplier unit by VDI. A WR6.5 isolator is added after the second X2 unit to make sure that its performance remains the same when connected to the mixer chip. The output signal power of this combination is measured with an Erickson power meter and is between -3 dBm and 1 dBm including the 2 dB loss of the LO probe. An HP 83650A synthesizer together with a X4 frequency multiplier unit from VDI is used as a CW RF signal source. A variable attenuator is inserted after the multiplier in order to control the input power and to minimize possible VSWR at the input port.

Figure 4.11: Quadrature demodulator measured (a) image rejection and conversion gain versus LO frequency for IF at 1 GHz (b) output power at 1 GHz versus input power at 167 GHz [A].

Figure 4.12: Quadrature demodulator measured (a) output power at 1 GHz versus RF frequency (b) SSB noise figure, image rejection ratio and conversion gain versus collector current [A].
The quadrature demodulator is characterized as an image-reject downconverting mixer and performance parameters like image rejection ratio, conversion gain, noise figure and RF bandwidth are measured. The four outputs from the downconverting mixer are connected to three external hybrids through the GSSGSSG probe. Insertion loss and phase imbalance of the external three hybrid combination was measured with a Rohde Schwarz four-port network analyzer and shows a maximum of 0.6 dB amplitude and 5 degrees of phase imbalance between the 4 ports at 1 GHz. Matched cables and components are chosen in order not to introduce additional amplitude and phase error to the output signal. In order to avoid complication in data analysis these errors are not removed from the measurement results presented below.

The conversion gain of the mixer is measured with an input RF signal power of -20 dBm to ensure linear operation of the mixer. The frequency of the input signal is varied across the entire D-band from 110 GHz to 170 GHz and the output IF signal power is measured on the spectrum analyzer. In every RF signal setting, the LO frequency is switched to both above and below the RF frequency in order to measure the conversion gain in both the lower and upper sidebands. The ratio of the two output powers is then regarded as the image rejection ratio. The frequency of the IF output signal is fixed at 1 GHz. As can be seen, the mixer chip has 35 GHz of 3-dB RF bandwidth from 125 GHz to 160 GHz and maximum conversion gain as high as 14 dB. It is also seen that the mixer exhibits up to 35 dB of image rejection ratio (IRR) and is always better than 27 dB across the whole D-Band. This good image rejection is due to a good balance of the balun, the coupler and the symmetry of the two mixing cells. The decreases in image rejection at higher frequency can be due to lower available LO power. Measured results are also compared with simulations in Fig. 4.11 (a) and it can be seen that they are in good agreement given the high frequency of operation and complexity of the circuit.

Linearity of the circuit is measured by sweeping input RF signal power at several fixed frequencies. Fig. 4.11 (b) shows the output power at 1 GHz versus input power at 167 GHz. The maximum output power of the circuit versus RF frequency is shown in Fig. 4.12 (a) and is as high as 4 dBm from 130 to 155 GHz. Measurements are repeated at different collector current to find the best operating point. Fig. 4.12 (b) shows the measured conversion gain and image rejection ratio as a function of collector current. It can be seen that there is an optimum collector current for the maximum gain and image rejection.

**NF measurement**

Fig. 4.13 shows the setup used to measure the noise figure of the mixer chip. An Agilent N8975A Noise Figure Analyzer (NFA) is used to measure the noise figure and transducer gain of the mixer. The NFA is configured in downconverter mode and is also connected to the Agilent 8257D signal source to sweep the LO frequency. The IF port of NFA is calibrated at 1 GHz using an ISSN-06-32D noise source. A WR6.5 noise source from Elva 1 is also used in this measurement. The noise source is specified to have an average ENR (Excess Noise Ratio) of 12 dB with 2 dB variation over the D-band. The insertion loss of the measurement setup between the noise source and the DUT greatly affects the accuracy of the noise figure measurement.

The loss in waveguide sections is measured versus frequency and together with the 2 dB loss of the D-band RF probe (specified by the manufacturer) is loaded into the NFA. The two signal sources, the spectrum analyzer, the noise figure analyzer as well as some of the bias
supplies controlled by a computer. This enabled a complete set of measurements to be taken across different frequency combinations and bias currents. Since LO and RF signals are generated by frequency multiplication, their power levels can only be varied with manual attenuators.

Measured SSB noise figure and conversion gain of the downconverter versus LO frequency are shown in Fig. 4.14. The results include noise contribution of IF components as well. However, since the mixer provides conversion gain, the noise figure is dominated by the noise figure of the mixer.

Figure 4.13: Quadrature demodulator noise figure measurement setup (a) illustration (b) photo in the laboratory.
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As shown in Fig. 4.14, the measured conversion gain from the CW measurement setup and from the noise measurement setup are in agreement with each other, which verifies accurate calibration of the setup.

Performance comparison with state-of-the-art

Table 4.1

The downconverting mixer with published papers in similar frequency range

<table>
<thead>
<tr>
<th>Ref</th>
<th>Freq. (GHz)</th>
<th>Noise figure (dB)</th>
<th>Conv. gain (dB)</th>
<th>Input P dB (dBm)</th>
<th>Power cons. (mW)</th>
<th>LO power (dBm)</th>
<th>Technology</th>
<th>Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>106</td>
<td>122</td>
<td>12 (SSB)</td>
<td>23 (max.)</td>
<td>-</td>
<td>150</td>
<td>3</td>
<td>0.25µm SiGe C-HBT</td>
<td>Subharmonic-Mixer</td>
</tr>
<tr>
<td>107</td>
<td>127</td>
<td>22</td>
<td>4</td>
<td>-</td>
<td>89.1</td>
<td>9</td>
<td>0.13µm SiGe BiCMOS</td>
<td>Subharmonic-Mixer</td>
</tr>
<tr>
<td>107</td>
<td>122</td>
<td>11</td>
<td>31 (diff.)</td>
<td>-44</td>
<td>370</td>
<td>-</td>
<td>0.13µm SiGe BiCMOS</td>
<td>LNA+SHM+VCO</td>
</tr>
<tr>
<td>108</td>
<td>122</td>
<td>11.5</td>
<td>13</td>
<td>-20</td>
<td>900</td>
<td>-</td>
<td>0.13µm SiGe HBT</td>
<td>PA+LNA+Mixer +Prescaler</td>
</tr>
<tr>
<td>108</td>
<td>123</td>
<td>5</td>
<td>3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.13µm SiGe HBT</td>
<td>LNA + Quadrature Mixer</td>
</tr>
<tr>
<td>109</td>
<td>140</td>
<td>12.3</td>
<td>30 (diff.)</td>
<td>-</td>
<td>1500</td>
<td>-</td>
<td>0.13µm SiGe BiCMOS</td>
<td>Transceiver</td>
</tr>
<tr>
<td>110</td>
<td>144</td>
<td>12.5</td>
<td>48</td>
<td>-</td>
<td>214</td>
<td>-</td>
<td>65nm CMOS</td>
<td>5 stage LNA + Mixer + tripler</td>
</tr>
<tr>
<td>111</td>
<td>158-165</td>
<td>11-14</td>
<td>20-25 (diff.)</td>
<td>-</td>
<td>1400</td>
<td>-</td>
<td>SiGe BiCMOS</td>
<td>3 stage LNA+I/Q DBM</td>
</tr>
<tr>
<td>112</td>
<td>150-162</td>
<td>8.5</td>
<td>24</td>
<td>-35</td>
<td>490</td>
<td>-</td>
<td>0.25µm SiGe HBT</td>
<td>LNA+I/Q Mixer + Prescaler</td>
</tr>
<tr>
<td>113</td>
<td>150-165</td>
<td>9.5 (min.)</td>
<td>27 (max.)</td>
<td>-</td>
<td>160</td>
<td>-8</td>
<td>SiGe HBT</td>
<td>LNA + DBM</td>
</tr>
<tr>
<td>Paper [A]</td>
<td>110-170</td>
<td>11 (max)</td>
<td>14.5 (max)</td>
<td>-2</td>
<td>67</td>
<td>0</td>
<td>0.25µm InP DHBT</td>
<td>I/Q Mixer</td>
</tr>
</tbody>
</table>

Figure 4.14: Measured SSB noise figure and conversion gain versus LO frequency [A].
A performance of the downconverter is compared with other published results in Table 4.1. Published results have different complexity levels and not all reports have in-phase and quadrature (I/Q) performance. Image rejection is, therefore, not included in this table. It is seen that the presented demodulator circuit exhibits as high as 14 dB of SSB conversion gain and as low as 11.5 dB SSB noise figure with more than 25 dB IRR and 4 dBm saturated output IF power. The circuit covers the entire D-band, which is the widest bandwidth reported up to date. The IF bandwidth has been limited by the measurement setup, will be evident from the data transmission measurement results presented in Chapter 6.

4.5 Design and implementation of D-band direct conversion I/Q modulator

4.5.1 Circuit design and layout challenges

The schematic diagram and fabricated chip photo of quadrature direct carrier upconverting mixer is shown in Fig. 4.15 and Fig. 4.16, respectively. In the modulator circuit, the low frequency signal is applied to the lower transistors, converted to current signals and switched by the LO signal. The baseband ports are DC coupled to the bases of the transconductance

![Simplified schematic diagram of quadrature upconverter](image)

Figure 4.15: Simplified schematic diagram of quadrature upconverter [B].
stages as blocking capacitors for such frequencies may occupy very large chip area. For impedance matching, 50 ohm resistors are placed in parallel to the base which are also used for bias. Circuit design is discussed in detail in [B]. Collector and base voltages of switches are applied to virtual RF grounds of the load and LO matching network respectively. The mixer is biased at Vcc of 3.3 V and draws 21 mA of collector current. The LO and IF base voltages are 3 V and 2 V, respectively.

4.5.2 Measurement results

The modulator is characterized as a single-sideband (SSB) upconverting mixer and parameters such as the conversion gain, carrier suppression and output power compression were measured. Details of the measurement setup are shown in Fig. 4.17. A CW signal with four well balanced phases is applied to the differential I and Q ports so that one of the sidebands can be suppressed. These signals are generated from an HP 83620B synthesizer together with three external hybrids.

On the RF side, a Rohde and Schwarz spectrum analyzer is used with an external D-Band harmonic mixer. In order to assure linear operation of the harmonic mixer, an attenuator is inserted right after the probe as shown in Fig. 4.17. The conversion loss of the combination of the attenuator and the harmonic mixer is calibrated by comparing the measurement of a CW signal (from the VDI source) to an Erickson power meter. For the third order intercept point measurement, the two tones are generated by two separate signal sources which share the same reference frequency and the outputs are added with a resistive combiner as shown in Fig. 4.17. The two frequencies are separated by 50 MHz.

The measured conversion gain and sideband suppression of the mixer for lower sideband operation are shown in Fig. 4.18 (a). The IF frequency is set to 1 GHz and signal power at each
Figure 4.17: Illustration of the CW and OIP3 measurement setup used to characterize the quadrature modulator [A] [B].

Figure 4.18: Quadrature modulator measured (a) conversion gain and image rejection over the LO frequency (dash lines are simulated results) (b) Measured LO to RF isolation versus LO frequency [B].

Figure 4.19: Quadrature modulator measured (a) output power at 155 GHz versus input power at 1 GHz (b) maximum output power versus LO frequency (c) OIP3 versus LO frequency [B].
of the IF ports is -18 dBm. The LO signal power entering the chip is also shown for reference. As can be seen the mixer exhibits up to 6 dB conversion gain which decreases for higher frequencies as the LO power drops.

This behavior can be reproduced in the simulation and therefore the frequency behaviour of the chip is expected to be flat and better than 6 dB over the 115 GHz to 155 GHz. Sideband suppression is better than 15 to 22 dB. The ripples in the plots at the upper edge of the frequency band are anticipated to be due to poor calibration of the harmonic mixer and possible impedance mismatches. Fig. 4.18 (b) shows the LO to RF isolation of the mixer. This is the power of the output signal at LO frequency compared with the power applied to the LO port. It can be seen that the isolation is better than 20 dB for most of the frequency band and can be as high as 27 dB at some frequencies.

Fig. 4.19 (a) shows the output power at 155 GHz when the input power at 1 GHz is varied. As can be seen, the mixer can provide more than -5 dBm output power at its 1dB compression point. Fig. 4.19 (b) shows the maximum output power over LO frequency from 115 GHz to 155 GHz. The output power is on average -2 dBm but can be as high as 3 dBm at 120 GHz where more LO power is available to the mixers. Fig. 4.19 (c) shows the third order intercept point of the modulator over the LO frequency. In this measurement, the total input power to the chip is -15 dBm (-18 dBm in each I and Q inputs). It can be seen that mixer has an OIP3 higher than 0 dBm in most of the frequencies in D band.

Performance comparison with state of the art

From Table 4.2, it is seen that the modulator circuit has a measured conversion gain of 6 dB with 27 dB suppression of the LO signal relative to the desired signal. This circuit also covers the widest bandwidth among the published results. The outstanding performance of this circuit makes it an excellent candidate for integration into a complete transmitter for high-speed communication in the D-band. This circuit was integrated into a transmitter chip and is described in Chapter 5.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Freq. (GHz)</th>
<th>Conv. Gain (dB)</th>
<th>LO-RF/IRR(dB)</th>
<th>Psat (dBm)</th>
<th>Power cons. (mW)</th>
<th>Topology</th>
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<td>10.1</td>
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</table>
4.6 Design and implementation of balanced frequency doubler at 110-170 GHz

This section describes the design of integrated frequency sources which are the key components for millimeter-wave applications in telecommunications, imaging and remote sensing. The requirements for a local oscillator source in such applications are related to output power, tuning range, noise performance and DC power consumption. At lower frequency, the oscillator source normally has a wide tuning range and a lower phase noise. The oscillator is often cascaded with frequency multipliers to generate desired output at higher frequencies. Active frequency multipliers are chosen for this design due to relatively high conversion efficiency and low input power requirement compared with passive multipliers. A balanced approach is used in the design, which has improved bandwidth, higher conversion gain and higher fundamental rejection compared with unbalanced topology. However, unbalanced topology has the advantages of low DC power consumption and compactness but it suffers from narrow bandwidth and fundamental signal need to be rejected.

Circuit design

Fig. 4.20 (a) shows the simplified schematic of the designed frequency doubler. The doubler was designed using two common-emitter HBTs in a balanced push-push configuration to obtain a strong second harmonic output with odd harmonic suppression. The circuit has a signal dividing scheme at the input using a balun which provides two differential phase signals, one for each transistor. A Marchand balun is designed at a center frequency of 70 GHz. The EM simulated amplitude and phase imbalances between 60 - 80 GHz are better than 0.9 dB and 2.1 degrees, respectively. The resulting differential phase outputs from two transistors are combined together cancelling the fundamental output while constructively adding the output at the second harmonic. At the output of the doubler, a post amplifier can be added to achieve a...
higher gain and higher output power. The matching between the balun and the transistor is done using a DC-blocking MIM capacitor and a series microstrip line. The size of the transistor is determined by a trade-off consideration between the second-harmonic output power and DC power consumption. The device size of both the transistors are identical and are chosen to be 4 µm to achieve the generation of the second harmonic signal with a maximum gain. The circuit is biased at 1.2 V and 16 mA leading to a maximum DC power consumption of 19.2 mW. Fig. 4.20 (b) shows a micro photograph of the fabricated circuit. The chip dimension is 0.45 × 0.4 mm².

Performance verification

On-wafer probe measurements were performed to characterize the frequency doubler MMIC using GSG-probes for the RF in and out ports. Details of the measurement setup for the doubler are shown in Fig 4.21 (a). A Keysight PNA-X N5247A network analyzer with a VDI WR6.5 (110-170 GHz) frequency extension module at the output port is used for measuring the desired second harmonic output in the D-band. The input signal from 56 to 67 GHz is provided by the network analyzer and a W band source from the OML is used to provide an input signal from 75 to 83 GHz. The fundamental frequency suppression from 75 to 83 GHz was measured by an external W-band harmonic mixer (R&S SAM110) together with a spectrum analyzer. An attenuator is inserted before the external harmonic mixer in order to assure its linear operation. The conversion loss of the attenuator and harmonic mixer combination is calibrated by comparing the output of a VDI source with the spectrum analyzer and Erickson power meter.

Fig. 4.21 (b) shows the output power versus input frequency at an input power of 6 dBm for the fundamental, second and third harmonics of the input signal. It can provide up to 4.2 dBm of output power at second harmonic and has a 3-dB output bandwidth of 38 GHz from 120 to 158 GHz corresponding to 27.3 % relative bandwidth. The measurement of fundamental and third harmonic components in the complete frequency band was limited by the setup.

Figure 4.21: Frequency doubler (a) illustration of the measurement setup (b) measured (solid) and simulated (dashed) output power of the frequency doubler at fundamental, 2nd and 3rd harmonic signals versus the input frequency [C].
The second harmonic output power at 130 GHz versus input power at 65 GHz is varied and a saturated output power of 4.2 dBm is obtained at an input power of 6 dBm. The power efficiency $\eta = 100 \times \frac{P_{\text{out}}}{P_{\text{in}}+P_{\text{dc}}}$ of the doubler is calculated to be 11.9 % at 130 GHz and 5 dBm input power where $P_{\text{out}}$ and $P_{\text{in}}$ denote the output power and input power of second harmonic and input signal, respectively, $P_{\text{DC}}$ denotes DC power consumption.

### 4.7 Design and implementation of a balanced frequency tripler at 140 -220 GHz

**Circuit design**

The topology of the presented balanced frequency tripler is showed in Fig. 4.22. The output power of the transistor with fundamental, and higher order harmonic items under different base bias is varied. For effective third harmonic generation and minimization of the second harmonic, the base of the transistor is biased where third harmonic components is dominant relative to other harmonics. The presented circuit employs two broadside-coupled Marchand baluns at the input and output ports. The input balun is designed at the central frequency of the input frequency band and has a simulated 0.5 dB amplitude and 1.5 degree phase imbalance between 50-65 GHz. The output balun is centered at three times the input frequency. It has 1 dB amplitude and 2.8 degree phase imbalance between 150-195 GHz. Due to the balanced configuration the second harmonic signals from each path cancel each other whilst fundamental and third harmonic signals add in phase. However, due to the large frequency separation, the fundamental signal at the output combining circuit is filtered using a coupled line band-pass

![Figure 4.22: Simplified circuit schematic of the frequency tripler circuit [C].](image)
filter. A one stage buffer amplifier is used in order to amplify this signal. Metal-Insulator-Metal (MIM) capacitors are used for DC blocking.

**Measurement results**

A photograph of the fabricated circuit is shown in Fig. 4.23. The device size of the multiplier stage is identical and chosen to be 4 µm while the device for the amplifier stage is 5 µm. The measurement setup is similar to the setup used for doubler measurement and is described in [C]. At 6 dBm input power, it consumes a DC power of 26 mW. Fig. 4.24 (a) shows the saturated output power of the fundamental, second and third harmonics versus input frequencies. All in-band harmonics are found below 20 dB with respect to the desired third harmonic. It showed a 3.8 dBm maximum output power at the third harmonic between 168 to 189 GHz and has a 3-dB output bandwidth of 27 GHz from 162 to 189 GHz (15.3 % relative bandwidth).

![Die micrograph of G-band frequency tripler MMIC (chip surface is 0.9 x 0.4 mm^2) [C].](image)

**Figure 4.23**: Die micrograph of G-band frequency tripler MMIC (chip surface is 0.9 x 0.4 mm^2) [C].

![Frequency tripler chip measured (solid line) and simulated (dash line) (a) output power of fundamental, 2nd and 3rd harmonic signals in function of the input frequency at input power 7 dBm (b) third harmonic output power at 168 GHz versus input power at 56 GHz [C].](image)

**Figure 4.24**: Frequency tripler chip measured (solid line) and simulated (dash line) (a) output power of fundamental, 2nd and 3rd harmonic signals in function of the input frequency at input power 7 dBm (b) third harmonic output power at 168 GHz versus input power at 56 GHz [C].
4.8 Summary

The design, characterization and implementation of a quadrature up and downconverting mixers (I/Q modulator/demodulator) is presented for D-band applications utilizing an InP DHBT-MMIC technology. Circuits exhibit a wideband RF and IF bandwidth which is needed for high data rate communication. The quadrature modulator and demodulator were further integrated in Chapter 5 into TX/RX chipset. Balanced frequency multipliers for output frequencies in the D and G bands are also described. Table 4.3 summarizes and compares the results of doubler and tripler frequency multipliers with the published papers of different technologies and topologies. These results highlight the significant potential of presented balanced active frequency multipliers for millimeter-wave frequency synthesis chains.

<table>
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<th>Conv. Gain (dB)</th>
<th>Rejection (dBc)</th>
<th>Relative BW (%)</th>
<th>DC power (mW)</th>
<th>Power efficiency (%)</th>
<th>Area (mm²)</th>
<th>Technology (fT/fMAX GHz)</th>
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<td>-</td>
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<td>14.4</td>
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<td>30</td>
<td>12.6</td>
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<td>250 nm InP DHBT (350/600)</td>
<td>[121]</td>
</tr>
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<td>-2</td>
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<td>0.9x0.4</td>
<td>250 nm InP DHBT (350/600)</td>
<td>Paper [C]</td>
</tr>
</tbody>
</table>

4.8 Summary

The third harmonic output power at 168 GHz versus input power at 56 GHz is shown in Fig. 4.24 (b). The tripler is able to deliver 3.8 dBm output power with input power of 7 dBm. The tripler’s power efficiency is calculated to be 7.7% at 168 GHz (third harmonic) and 7 dBm input power.

Table 4.3
Comparison of active frequency multiplier circuits
Chapter 5

110-170 GHz Fully Integrated InP DHBT Transceiver Chipset

After describing design methodologies and examples of mm-wave building blocks (modulator, demodulator, frequency multipliers) in chapter 4, this chapter focuses on the integration of circuits into multifunctional TX/RX chipset. The design, characterization and implementation of an integrated chipset comprising an in-phase/quadrature phase (I/Q) transmitter (TX) chip and a receiver (RX) chip is presented for D-band applications in InP DHBT MMIC technology.

5.1 Implementation of direct conversion I/Q transmitter

The architecture of the fabricated transmitter is illustrated in Fig. 5.1. It consists of two quadrature mixers, an X3 multiplier for the LO, and a three-stage PA. The chip photo and circuit schematic are shown in Fig. 5.2 and Fig. 5.3, respectively. The quadrature mixer/modulator is presented in [A] and described in full detail in Chapter 4. An external 36-56 GHz signal is used as the LO, and its frequency is tripled by an on-chip frequency multiplier to cover the entire D-band. The multiplier is presented in [121] and consists of two stages. The first stage operates in class B to provide the first and second harmonics of the signal to the second stage. The second stage is biased in class C and mixes the two harmonics to generate the third harmonic of the input signal. A bandpass Chebyshev filter is used at the output to remove all unwanted harmonics from the signal and to provide the modulator with a clean sinusoidal at three times the input frequency.

Figure 5.1: Block diagram of (a) quadrature direct conversion transmitter (b) implemented I/Q transmitter chip.
This integration allows us to design the oscillator at one third of the fundamental D-band LO frequency. The RF amplifier is a three-stage common emitter design and buffers the modulator output from the external load. It provides 20 dB gain and saturated output power of 9 dBm. The amplifier design is of “lossy match” type, utilizing resistively loaded stubs at the input and output of each amplifier stage, to achieve a very wide bandwidth coverage.

The output from the chip is a single-ended modulated signal, and inputs to the chip are a single-ended LO and differential I and Q signals which are DC coupled. The single-ended LO and RF signals are converted to differential by on-chip Marchand baluns. The DC bias feed lines are properly RF decoupled to avoid unwanted feedback and combined to reduce the number of DC pads. The optimum operating condition is set by providing proper base currents to the amplifier and frequency multiplier, while the current of the modulator is set by the current mirror.

One key challenge in fully integrated mixed signal IC is the isolation between circuit blocks through sufficient spacing between different sensitive components. To mitigate these unwanted coupling effects and to reject common mode noise, techniques such as differential topology, separate supply. After the circuit is fabricated, its characterization and measurement processes are not straightforward. Whereas complete solutions for testing exist in the lower mm-wave frequency range (up to 67 GHz), they are not always available above 100 GHz. The I/Q transmitter chip is characterized as a single sideband (SSB) frequency transmitter. The setup used to measure the transmitter was similar to that used to characterize the modulator in Sec 4.5 of Chapter 4.

Figure 5.2: Chip photo of the 110-170 GHz TX MMIC. The chip measures 1.3 x 0.9 mm² [D].
Three-stage D band Amplifier

First stage of amplifier

I/Q Modulator

X3 Frequency Multiplier chain

Figure 5.3: Simplified circuit schematic of the 110-170 GHz TX MMIC [D].
Figure 5.4: TX measured and simulated conversion gain of (a) upper and lower sidebands versus LO frequency at fixed 1 GHz input signal. The applied LO frequency to chip is one third of it (b) upper and lower sidebands versus IF frequency at fixed 48 GHz LO [D].

Figure 5.5: TX measured and simulated (a) conversion gain versus input LO power at LO frequency of 47 GHz and Input IF at 1 GHz (b) LO power at RF port versus LO frequency for input at 1 GHz (c) output power and conversion gain at 153 GHz versus input power at 1 GHz (d) output power of the transmitter versus RF output frequency at an input frequency of 1 GHz [D].
Performance verification

The TX is characterized in single side band mode, and parameters like the conversion gain at upper and lower sidebands, LO power requirement, LO to RF isolation, output power compression and saturated output power are measured. An input IF signal of 1 GHz with -28 dBm is applied to the IF port. The LO input signal with 4 dBm power is varied from 36 to 56 GHz. The LO leakage and spectral components at two sidebands were measured at the RF port.

The simulated and measured conversion gain for the upper and lower sideband gains versus LO frequency are shown in Fig. 5.4 (a). A conversion gain of 23 dB is achieved from 120 to 155 GHz. The unwanted sideband is suppressed by 18–25 dB. As mentioned in the previous subsection, the sideband suppression is related to amplitude and phase mismatch [65]. The IF bandwidth is measured by varying the input signal frequency from 1 to 18 GHz at a fixed LO of 48 GHz. The measured conversion gain variation is shown in Figure 5.4 (b). The transmitter provides relatively flat gain up to 18 GHz at LSB where the gain drops by 4 dB. This is believed to be dominant due to the upper frequency limitation of the external hybrids and not the chip itself. To study the conversion gain dependency on LO power, a 1 GHz, -28 dBm CW signal is applied at the IF with LO power at 47 GHz swept from 0 to 7 dBm. The results are plotted in Fig. 5.5 (a), showing a maximum gain of 26 dB at an LO power of 4 dBm or higher. The measured LO power at RF port is shown in Fig. 5.5 (b) for swept LO frequency and fixed IF of 1 GHz. Figure 5.5 (c) shows the output power and conversion gain at 153 GHz versus input power at 1 GHz. It can be seen from Figure 5.5 (d), that the maximum output power is 9 dBm from 125 to 138 GHz and drops to 5.5 dBm at 153 GHz. The TX chip consumes 165 mW of DC power.

5.2 Implementation of direct conversion I/Q receiver

The block diagram and fabricated chip photo of the I/Q RX are shown in Fig. 5.6 and Fig. 5.7, respectively. As can be seen, many of the circuit blocks and footprints are reused from the transmitter chip. The demodulator is presented in detail in [A] and described in Chapter 4. The LO multiplier is identical to the transmitter, and the RF amplifier is also based on the same
design as described above with DC bias optimized for minimizing the noise figure. The simplified circuit schematic is shown in Fig. 5.8. The outputs from the chip are DC-coupled differential I and Q signals and the inputs are single-ended LO and RF signals which are converted to differential before the demodulator. The chip size is 1.3 x 0.9 mm$^2$.

**Performance verification**

In the direct conversion RX mode, the four baseband signals are applied as differential I and Q baseband signals. In image reject frequency converter mode, however, they represent four phases of the IF signal. Additional 90 degree and 180 degree hybrids are used to connect these ports to the spectrum analyzer for testing the RX. The measurement setup is similar to the one used to characterize the demodulator circuit in Sec. 4.6 of Chapter 4.
Figure 5.8: Simplified schematic of the 110-170 GHz RX MMIC.
Chapter 5. 110-170 GHz Fully Integrated InP DHBT Transceiver Chipset

Figure 5.9: RX measured and simulated conversion gain of (a) upper and lower sidebands versus LO frequency at fixed 1 GHz output. The applied LO frequency to chip is one third of it (b) upper and lower sidebands versus IF frequency at 49 GHz LO [D].

Figure 5.10: RX (a) output power and conversion gain at 1 GHz versus input power at 140 GHz (b) saturated output power at 1 GHz IF over RF frequency (c) simulated noise figure and conversion gain versus IF frequency at 45 GHz LO [D].

The SSB conversion gain of the receiver chip is measured at an input RF signal power of -30 dBm and the frequency is varied from 100 to 170 GHz. The LO signal is swept together with the RF signal frequency to maintain a fixed IF of 1 GHz. The input LO power is 4 dBm. At each RF frequency, the LO frequency is switched above and below the RF in order to measure conversion gain in both lower and upper sidebands.

The measured and simulated results are shown in Fig. 5.9 (a). As can be seen, the measured conversion gain varies from 20 to 25 dB between 115–155 GHz. The 5 dB RF bandwidth extends over 40 GHz. The ratio of the two output powers is defined as the image rejection ratio (IRR) and is 24 dB for most of the RF frequencies. Similar to sideband suppression, the imbalance in the RX can be calculated leading to 0.7 dB of amplitude imbalance or 5 degrees of phase imbalance or a combination. These imbalance errors can increase the bit error rate of
a communication system and depending on the system requirements, additional analog and digital methods may be applied for this systematic correction [68-70].

The measured and simulated conversion gain versus IF frequency is shown in Fig. 5.9 (b) for a fixed LO frequency of 49 GHz. The measured 5 dB IF bandwidth of the RX is 18 GHz, which is again believed to be limited by the external hybrid network. Fig. 5.10 (a) shows the measured output power and conversion gain at 1 GHz versus input power at 140 GHz. The receiver can provide up to 4 dBm output power at 1 dB compression point. The maximum output power at 1 GHz versus RF frequency is shown in Fig. 5.10 (b) and is as high as 4 dBm from 120 to 155 GHz. The sensitivity of the receiver is an important parameter affecting the maximum data rate for different modulation schemes. The simulated noise figure and gain of the complete receiver chip over RF frequency is shown in Fig. 5.10 (c). It has 0.5 dB of noise figure variation from 9.1 to 9.6 dB between 115–170 GHz. The total DC power dissipation of the RX chip is 192 mW.

5.3 Performance comparison with state of the art

A TX/RX chipset for high data rate D-band wireless links is demonstrated utilizing a 250 nm InP DHBT technology. The chipset can be used in both homodyne and heterodyne architecture. The presented chipset has the largest RF bandwidth and IF bandwidth and consume low DC and LO power among published millimeter-wave TX/RX circuits operating in D-band and F-band (90-140 GHz). Table 5.1 and Table 5.2 show the comparison of presented circuits to millimeter-wave TX/RX circuits. The chipset can be used for the point-to-point wireless communication for 4G and 5G mobile communication infrastructure, high data rate backhaul, low-latency wireless HDTV transmission and >40 Gbit/s transmission over a dielectric waveguide. The measured RX conversion gain is 26 dB, with a simulated noise figure of 9 dB. The measured TX conversion gain is 20 dB and saturated output power is 9 dBm.

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<th>Technology (fT/fMAX GHz)</th>
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<th>LO-RF Isolation (dB)</th>
<th>RF Bandwidth (GHz)</th>
<th>Output power (dBm)</th>
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<td>Input P1dB (dBm)</td>
<td>LO Power (dBm)</td>
<td>DC Power (mW)</td>
<td>Ref.</td>
</tr>
<tr>
<td>------------</td>
<td>--------------------------</td>
<td>-------------</td>
<td>----------------</td>
<td>------------------</td>
<td>-----------------</td>
<td>---------------</td>
<td>----------------</td>
<td>------</td>
</tr>
<tr>
<td>110-170</td>
<td>250 nm InP (350/650)</td>
<td>LNA + I/Q demodulator + X3</td>
<td>25</td>
<td>9.5</td>
<td>-23</td>
<td>4</td>
<td>192</td>
<td>Paper</td>
</tr>
</tbody>
</table>

Table 5.2
Performance comparison of receivers
Chapter 6

High-speed Data Transmission Experiments on TX/RX Chipset and Module

This chapter validates the functionality and effectiveness of the TX/RX chipset (presented in Chapter 5) in a data transmission link in both direct-modulation (zero-IF architecture) as well as in heterodyne architecture of front-end systems. This TX/RX chipset is packaged in modules and the packaged TX/RX chips were integrated into two radio units to demonstrate real-time wireless data transmission.

6.1 Direct data transmission verification on TX/RX chipset

In direct or homodyne data transmission, the transmitter modulates/upconverts and the receiver demodulates/downconverts the received signal. This transmission was performed through a dielectric waveguide medium as well as wirelessly through antennas.

6.1.1 Waveguide based measurement (wired)

The experimental setup is shown in Fig. 6.1. The transmitter and receiver MMICs are probed on wafer on two probe stations. A two meter D-band dielectric waveguide is used to feed the RF signal from the transmitter to the receiver. The transmitter and receiver share the common LO source through a power splitter. The available LO power for each MMIC is then less than 1 dBm. A dual-channel pulse pattern generator (PPG, Anritsu MP1800) is used to generate two independent pseudo-random binary sequence (PRBS), which are synchronized at the same data rates. The I and Q input ports of the direct modulation transmitter are driven differentially by these two data streams, and the phase of the RF signal is modulated by these data to form a QPSK modulated output. The output from the transmitter chip which is connected to a two meter long dielectric waveguide (15 dB loss) is measured using an external D-band passive mixer (Radiometer Physics SAM-170, conversion loss 26 dB). A spectrum analyzer is used to measure the spectrum of the modulated signal. The measured spectrum of a 12 Gbit/s QPSK signal centered at 142 GHz is also shown in Fig. 6.1. The peak-to-peak voltage of the data stream is adjusted while monitoring the output power of the spectrum. At the receiver side, the I- and Q- output ports are connected to a LeCroy 10Zi real-time oscilloscope which is used to measure the eye-diagram of the output signal of the receiver. A bit error detector measures the BER. The eye diagram is measured at different data rates and shown in Fig 6.1.
Chapter 6. High-speed Data Transmission Experiments on TX/RX Chipset and Module

Figure 6.1: Illustration of experimental setup for direct QPSK data transmission over D-band. Transmitter output spectrum of a 12 Gbit/s QPSK modulated signal at 142 GHz and measured eye diagram at 36, 40, and 44 Gbit/s data rate are also shown [E].

Figure 6.2: Photo of the experimental setup in the laboratory of Fig. 6.1.
6.1.2 Antenna based measurement (wireless)

The experimental setup for the direct wireless data transmission is illustrated in Fig. 6.3. The output RF signal from the TX chip is connected to the antenna through a 1 meter long dielectric waveguide. The transmitted wireless signal is received by another similar antenna, which is connected to the receiver through another 1 meter dielectric waveguide. The wireless distance is 1.8 meter. The gain of each antenna is 40 dBi with beam width of 3 degree. No external IF amplifier is needed and consequently is not used in the measurement. The photo of the experiment setup are shown in Fig. 6.4. Measured eye diagrams for 15, 20, 22 and 24 Gbit/s QPSK signals on the I channel at the RX output is shown in Fig. 6.5. The transmission performance is compared with state-of-the-art in Table 6.1.
Figure 6.5: The measured eye diagram obtained at the RX output for wireless (a) 30 Gbit/s QPSK (15 Gbit/s per channel) with BER 4.4x10^{-6} (b) 40 Gbit/s QPSK (20 Gbit/s per channel) with BER 2.1x10^{-5} (c) 44 Gbit/s QPSK (22 Gbit/s per channel) with BER of 4.8x10^{-4} (d) 48 Gbit/s QPSK (24 Gbit/s per channel) with BER <2.3x10^{-3} [D].

Table 6.1
Performance comparison of transmitters

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Frequency (GHz)</th>
<th>Data rate</th>
<th>Modulation</th>
<th>Integration</th>
<th>Psat. (dBm)</th>
<th>DC power (mW)</th>
<th>Gain (dB)</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[125]</td>
<td>120</td>
<td>9 Gbit/s</td>
<td>ASK</td>
<td>Oscillator+ASK Modulator</td>
<td>-19.2</td>
<td>80.9</td>
<td>-</td>
<td>65nmCMOS</td>
</tr>
<tr>
<td>[126]</td>
<td>120</td>
<td>10 Gbit/s</td>
<td>ASK</td>
<td>Frequency doubler + ASK Modulator+ Power amplifier</td>
<td>0</td>
<td>500</td>
<td>-</td>
<td>0.1µm InP-HEMT</td>
</tr>
<tr>
<td>[109]</td>
<td>140</td>
<td>4 Gbit/s</td>
<td>ASK</td>
<td>Amplitude Modulator+ LO Amplifier+VCO</td>
<td>-8</td>
<td>-</td>
<td>-</td>
<td>SiGe BiCMOS</td>
</tr>
<tr>
<td>[127]</td>
<td>142</td>
<td>14 Gbit/s</td>
<td>OOK</td>
<td>Oscillator+Mixer+PA</td>
<td>8.7</td>
<td>66</td>
<td>7dB (diff.)</td>
<td>0.13µm BiCMOS</td>
</tr>
<tr>
<td>Paper [D]</td>
<td>110-170</td>
<td>48Gbit/s QPSK</td>
<td>I/QModulator+PA+LO tripler</td>
<td>5</td>
<td>165</td>
<td>25</td>
<td>0.25µm InP DHBT</td>
<td></td>
</tr>
<tr>
<td>Paper [G]</td>
<td>120-150</td>
<td>12 Gbit/s QPSK</td>
<td>Modulator</td>
<td>-4.5</td>
<td>52</td>
<td>9.5 dB</td>
<td>0.13µm SiGe BiCMOS</td>
<td></td>
</tr>
</tbody>
</table>
6.2 Data transmission on TX/RX chipset in heterodyne architecture

Data transmission experiments in a heterodyne architecture are demonstrated using I/Q TX and I/Q RX as a SSB TX and IF RX, respectively. The illustration of the experiment set is shown in Fig. 6.6. The TX and RX MMICs are probed “on-wafer” using two probe stations, and a 1 meter D-band dielectric waveguide is used to feed the RF signal from TX to RX. The TX and RX share a common 53 GHz LO source through a power splitter. An Arbitrary Waveform Generator (Tektronix AWG70002A) is used to generate high order QAM signals centered at 5 GHz IF. The generated signal is fed to the SSB TX which upconverts the IF input signal to RF centered at 164 GHz. A variable attenuator is used in between the TX and RX to control the RF signal going into the RX preventing the RX from saturating. The RX downconverts the incoming RF signal to IF before sampling by a real-time oscilloscope.

![Diagram of measurement setup](image)

Figure 6.6: Illustration of the measurement setup used to transmit QAM modulated data over the D-band using TX/RX chipset in heterodyne configuration. The block diagram of MATLAB implemented digital QAM demodulator based on data from a real-time oscilloscope is also shown [D].
6. High-speed Data Transmission Experiments on TX/RX Chipset and Module

(Tektronix MSO72504DX) with a fixed 100 GSample/s sampling rate. A digital RX is also implemented utilizing MATLAB code and is described in Paper [D].

The power spectral density, total EVM from TX to RX and spectral efficiency for the received 16, 32, and 64 QAM IF signal are shown in Table 6.2.

### Table 6.2
Measured constellation, IF bandwidth, EVM And spectral efficiency in data transmission experiment

<table>
<thead>
<tr>
<th>Modulation</th>
<th>16-QAM</th>
<th>32-QAM</th>
<th>64-QAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constellation</td>
<td><img src="image" alt="Constellation 16-QAM" /></td>
<td><img src="image" alt="Constellation 32-QAM" /></td>
<td><img src="image" alt="Constellation 64-QAM" /></td>
</tr>
<tr>
<td>Received IF Magnitude Spectrum</td>
<td><img src="image" alt="Magnitude Spectrum 16-QAM" /></td>
<td><img src="image" alt="Magnitude Spectrum 32-QAM" /></td>
<td><img src="image" alt="Magnitude Spectrum 64-QAM" /></td>
</tr>
<tr>
<td>Symbol /Data rate</td>
<td>(4 Gsymbols/s) / (16 Gbit/s)</td>
<td>(4 Gsymbols/s) / (20 Gbit/s)</td>
<td>(3 Gsymbols/s) / (18 Gbit/s)</td>
</tr>
<tr>
<td>EVM (rms %)</td>
<td>10.8281</td>
<td>10.5947</td>
<td>6.8467</td>
</tr>
<tr>
<td>Data rate/IF BW = Spectral efficiency</td>
<td>16 Gbit/s/6 GHz = 2.7 bit/s/Hz</td>
<td>20 Gbit/s/6.5 GHz = 3.1 bit/s/Hz</td>
<td>18 Gbit/s/5 GHz = 3.6 bit/s/Hz</td>
</tr>
</tbody>
</table>

6.3 Spectrum efficient real-time data transmission on TX/RX module

The front-end TX/RX chips presented in Chapter 5 are packaged in waveguide modules and were integrated in two radio units. This work was performed in a team from Chalmers and Ericsson AB. A real time wireless data transmission was demonstrated using spectrum efficient multilevel QAM modulation schemes.
6.3.1 TX/RX module design and performance

The TX/RX Module design and performance, as described in detail in Paper [F], is based on the split-block technique, where the RF waveguide is split in the middle of the broad wall as shown in Fig. 6.7. A carrier board is used to provide interface to the IF, LO and RF ports of the MMIC and also features an integrated waveguide to microstrip transition. The board consists of a 1 mm copper plate covered with a 50 um Rogers Ultralam 3908 bonding film and a 50 um Rogers Ultralam 3850HT dielectric. The back to back waveguide transitions were fabricated and measured. The loss of one transition is 0.9 dB and 1.7 dB for frequencies of 120 GHz and

![Image](image_url)

Figure 6.7: TX or RX module (a) with the carrier board and LO, IF and RF ports (b) module has dimensions of 56/38/20 mm [F].
In this chipset, the bottom metal layer [M1] was used as a ground layer which is present at the upper surface of the wafer. Therefore, the ground of the MMIC is not connected to the waveguide block when the circuit is attached to a waveguide block requiring an additional bond-wire to provide a connection between the MMIC ground and the waveguide block. In addition, larger bond pads were used to improve the yield after bonding the circuits and provide sufficient area to place a pair of bond wires, reducing the inductance of the bond wire interface.

140 GHz. This loss does not include effects related to the bond wire between the transition and the MMIC.

In this chipset, the bottom metal layer [M1] was used as a ground layer which is present at the upper surface of the wafer. Therefore, the ground of the MMIC is not connected to the waveguide block when the circuit is attached to a waveguide block requiring an additional bond-wire to provide a connection between the MMIC ground and the waveguide block.

In the second version of chipset fabrication, the modified chipset contains thru-substrate vias connecting an additional metal layer on the bottom of the MMIC to the top ground layer providing a direct connection between the grounds when the MMIC is attached to the waveguide block. In addition, larger bond pads were used to improve the yield after bonding the circuits and provide sufficient area to place a pair of bond wires, reducing the inductance of the bond wire interface.

Figure 6.8: TX and RX module measured (a) USB gain versus RF frequency (b) receiver NF and LSB/USB Gain for LO frequencies: 117.6, 126, 132 and 141 GHz where each sideband is given for IF=1 GHz to 6 GHz [F].

Figure 6.9: USB and LSB gain versus RF frequency [F].
Chapter 6. High-speed Data Transmission Experiments on TX/RX Chipset and Module

6.3.2 Real-time wireless data transmission

The TX module shows a gain of 12 dB at 143 GHz with an output power of -2.3 dBm at 1 dB gain compression. The RX module has a gain of 15 dB with a noise figure (NF) of 13 dB at 143 GHz. The minimum NF of 10 dB is measured at 132 GHz. The performance of TX/RX modules is shown in Fig. 6.8 and Fig. 6.9 and described in more detail in Paper [F].

6.3.2 Real-time wireless data transmission

The TX/RX modules were integrated into transmitter and receiver radio-units consisting of TX/RX modules, PLL synthesizer, a real-time modem (BW= 1 GHz), 40 dBi antennas, and an IF board to convert baseband to IF and vice versa. The setup is illustrated in Fig. 6.10. The symbol rate of the modem was limited to 888 Mbaud/s. The PLL synthesizer provides LO of 11.625 GHz for the TX module, which is multiplied to 46.5 GHz and applied to the LO port of the TX module, with IF centered at 3.5 GHz and the transmitted upper sideband RF centered at 143 GHz. The LO for the RX is synthesized at 11.75 GHz, it is multiplied to 47 GHz in a series of two commercial doublers and then applied to the RX module. The RX module downconverts it to IF centered at 2 GHz. In the experiment one transmitter and one receiver radio-units were separated by 10 m and several modulation formats and symbol rates were tested. The data rate achieved is 5.3 Gbit/s using 64 QAM, with BER of $3.3 \times 10^{-8}$ and SNR of 24 dB over a 1 GHz channel. The installed outdoor radio unit for hop length of 200 m is shown in Fig. 6.11 along with a photo of the experiment setup in the laboratory.
6.4 Summary

Data rates up to 44 Gbit/s with QPSK modulation over a dielectric waveguide and up to 48 Gbit/s with multi-level QAM/QPSK modulations over air were transmitted and measured. An 18 Gbit/s 64 quadrature amplitude modulation (QAM) signal was transmitted in heterodyne mode with measured TX-to-RX an error vector magnitude (EVM) of less than 6.8% and a spectrum efficiency of 3.6 bit/s/Hz. This is the first implementation and demonstration of a RX/TX chipset for D-band applications, utilizing an InP DHBT-MMIC technology. Real-time wireless communication-links beyond 100 GHz have been demonstrated at [49], [50] and [128]. The highest order of modulation among them is 16 QAM realized with a front-end based on a combination of InP HEMT and Schottky diode technologies [50]. Our results present the first real-time transmission of data at 143 GHz at a distance of 10 m using a fully integrated chipset incorporated in split-block waveguide modules. At the time of writing this thesis, a 64 QAM over a 1 GHz channel resulting in a data rate of 5.3 Gbit/s with a spectrum efficiency of 5bit/s/Hz has been achieved. This is expected to support higher modulation over longer distances (>200 m) with presented TX/RX module performance. The outdoor experiment in different weather conditions was in progress and initial measurements demonstrated error free transmission over a 200 m hop length.
Chapter 7

SiGe BiCMOS Front-end Circuits Design and Implementation

This chapter presents the design and characterization of direct conversion I/Q modulator and demodulator MMICs implemented in a commercial SiGe BiCMOS process operating at D-band frequency range. It also describes the technology used and integration of a demodulator circuit into a RX chip. These circuits achieve state-of-the-art performance in SiGe BiCMOS technology.

7.1 130 nm SiGe BiCMOS Technology

The presented I/Q modulator and demodulator circuits are designed in a 130 nm SiGe BiCMOS process from Infineon Technologies (B11HFC) [129]. This process combines the strengths of two different transistor technologies, namely the bipolar transistor and the CMOS transistor. This unique combination opens up the opportunity for Si-based RF system-on-chip solutions [130]. The process features high-speed npn HBTs with maximum \(f_{T}/f_{MAX}\) of 250 GHz/400 GHz and \(BV_{CEO} = 1.5 \text{ V}\).

Figure 7.1: Cross-section of the 130 nm SiGe BiCMOS B11HFC process (Courtesy Infineon Technologies).
Figure 7.2: Direct conversion quadrature modulator circuit (a) block diagram (b) schematic diagram together with on-chip RF/LO Marchand baluns and differential quadrature LO phase shifter [G].
The cross section of the process back-end is shown in Fig. 7.1. It includes npn transistors, metal-oxide-semiconductor (MOS) transistors, metal film resistors, MIM capacitors, junction capacitors, pin diodes, and 6-levels of interconnect (M1-M6). Cu-based interconnects are used for the metallization layers, with four thin lower layers (M1-M4) and two thick upper layers (M5-M6).

### 7.2 D-band direct conversion I/Q modulator

#### Circuit design

The block diagram of the I/Q modulator circuit is shown in Fig. 7.2 (a). The circuit consists of two Gilbert-cell mixers, an on-chip integrated differential quadrature LO coupler, and an RF Marchand balun. RF/LO Marchand baluns are designed using upper thick M6 and M5 metal layers. Fig. 7.2 (b) shows the schematic of the presented circuit. The input baseband signals are converted to current signals by the differential transconductance stage (T9-T10, T11-T12) and are fed to the differential pair (T1-T4, T5-T8) which is also called switching quads.

![Differential Coupled-Line LO Coupler](image)

**Figure 7.3:** Chip photograph of the quadrature modulator circuit [G].
Chapter 7. SiGe BiCMOS Front-end Circuits Design and Implementation

The up-converted RF differential output currents are added and are connected to a balun for differential to single-ended output conversion. Current mirrors were included to control the currents in the mixer. For optimal performance, the switching quad transistors are chosen 2 µm long and the transconductance transistors are accordingly 4 µm long. The larger device allows for higher current swings and therefore increased linearity.

The baseband input ports are DC coupled. Decoupling capacitors ($C_d$) are incorporated to avoid potential instability of the circuit. The chip photograph is shown in Fig. 7.3. The techniques used in making the circuit layout are those used for the modulator circuit in Chapter 4 and presented in detail in Paper [G]. This technology puts extra challenges in layout design because whole structure needs to comply with DRC density requirements to satisfy the layout density and uniformity criteria. This is performed by dummy filling/cheesing of different layers in layout and their effects needs to be carefully taken into account in critical circuit areas. The mixer collector is biased at $+2.8$ V and takes 16 mA current. The LO and IF bias voltages are $+2$ V ($V_{LO}$) and $+1.7$ V ($V_{IF}$).

Figure 7.4: The CW measurement setup of the I/Q modulator (a) photo in the laboratory (b) illustration.
Measurement setup and circuit characterization

Details of the measurement setup are shown in Fig. 7.4. A Keysight PNA-X N5247A network analyzer with a VDI WR6.5 frequency extension module at the RF port is used in the measurement. The I/Q modulator is on-wafer characterized as a single sideband up-converting mixer. A CW signal with balanced four phases is applied to the differential I and Q ports. The input signal power to both the I and Q ports are -27 dBm. The LO signal is provided from an Agilent 8257D synthesizer together with a VDI6.5 X4 multiplier chain. The LO power (measured with an Erikson power meter) after considering the probe loss is between 4 dBm and 7.5 dBm in the D-band. The measured USB/LSB gain and output power versus RF/IF frequencies are measured and shown in Fig. 7.5 and Fig. 7.6. The mixer exhibits up to 9.8 dB conversion gain and 19 dB image rejection ratio. The measured 3-dB IF bandwidth of the chip is 13 GHz, which is well in line with simulation. The 3-dB RF bandwidth is 33 GHz from 119 GHz to 152 GHz.

![Figure 7.5: Modulator measured conversion gain (a) versus IF frequency at 126 GHz LO, (b) versus LO frequency at 1 GHz IF [G].](image)

![Figure 7.6: Modulator measured (a) conversion gain versus input power at IF 1 GHz and RF 131 GHz (b) output P1dB versus RF frequency at 1 GHz IF [G].](image)
7.3 D-band direct conversion I/Q demodulator

The schematic of the designed direct quadrature downconverting mixer is shown in Fig. 7.7. The design of this circuit is similar to the demodulator circuit described in Chapter 4, but all parts are redesigned in a SiGe BiCMOS process and described in detail in Paper [G]. A collector voltage of 2.7 V is applied to the two mixing cells and emitter follower, with mixing cells drawing 9.5 mA and the emitter follower requiring 17 mA of collector current. The voltages applied to the bases of the switching and transconductance transistors are 2 V and 1.4 V, respectively. The chip photo of the fabricated circuit is shown in Fig. 7.8. The quadrature demodulator is characterized as an image-reject downconverting mixer and performance parameters like image rejection ratio, conversion gain, noise figure and RF bandwidth are measured and shown in Fig. 7.9 and Fig. 7.10.
Figure 7.8: Chip photograph of the demodulator chip. The active chip size is 620 µm x 480 µm including the RF/LO baluns and the LO hybrid [G].

Figure 7.9: Demodulator (a) conversion gain and image rejection ratio versus LO frequency at IF 1 GHz (b) conversion gain and output power at 1 GHz versus RF power at 138 GHz [G].

Figure 7.10: Demodulator (a) conversion gain versus RF frequency at different LO frequencies, (c) simulated SSB noise figure versus RF frequency at 1 GHz IF [G].
7.4 Data transmission measurement on I/Q modulator

The experimental setup photo and illustration are shown in Fig. 7.11 and Fig. 7.12, respectively. The modulator MMIC is probed on-wafer and a D-band receiver module which is presented in Sec. 6.3 of Chapter 6 is used at the receiver side. The I/Q modulator and I/Q receiver are used as a single sideband up-converting mixer and image reject receiver, respectively. An Arbitrary Waveform Generator (Keysight M8195A 65 GSample/s) is used to generate high order QAM signals centered at 5 GHz IF. The generated signal is fed to the

![Figure 7.11: Photo of the experimental setup for data transmission test on I/Q modulator circuit.](image1)

![Figure 7.12: Illustration of experimental setup for data transmission test on I/Q modulator. Received signal constellation diagram for 4 Gbit/s 16QAM, 3 Gbit/s 8PSK, 12 Gbit/s QPSK is also shown [H].](image2)
modulator which up-converts the IF input signal to RF at 131 GHz. A variable attenuator is inserted between the modulator and receiver in order to attenuate the RF signal to the receiver preventing the receiver to saturate. The receiver downconverts the incoming RF signal to IF before sampling by a real-time oscilloscope (Lecroy) with a fixed 80 GSample/s sampling rate. A constellation diagram and measurement of the total modulator-to-receiver error vector magnitude (EVM) for 16 QAM, 8PSK and QPSK are shown in Fig. 7.12.

**7.5 Integration of demodulator into RX chip**

The demodulator circuit in Sec. 7.3 is integrated with a low noise amplifier (designed by Prof. Herbert Zirath). A chip photo of the integrated RX is shown in Fig. 7.13 and occupies an area of 1.4 mm x 0.8 mm (including all pads). The LNA gain and 1 dB compression point are
Chapter 7. SiGe BiCMOS Front-end Circuits Design and Implementation

shown in Fig. 7.14. The measured gain of the LNA is 20 dB and the simulated noise figure is 7 dB.

RX gain versus IF frequency is varied at a fixed LO frequency of 140 GHz and is plotted in Fig. 7.15 (a). The RX chip demonstrates a maximum conversion gain of 19 dB at 140 GHz LO and 141 GHz RF. The measured 3-dB IF bandwidth is larger than 20 GHz. The RF frequency in the D-band is swept with LO frequency to have a fixed IF of 1 GHz in Fig. 7.15 (b). A maximum gain of 19 dB is measured at 138 GHz. These measurements are not calibrated and the RX chip performs better than the results shown in Fig. 7.15.

The RX (I/Q demodulator + LNA) in Fig. 7.13 is further integrated with an X6 multiplier chain (designed by Dr. Mingquan Bao from Ericsson) at the LO port and is shown in Fig. 7.16 (a). In the third round of fabrication, the RX chip in Fig. 7.16 (a) was integrated with an on-chip microstrip to waveguide transition (designed by Dr. Zhongxia He) at the RF port. The chip photo is shown in Fig. 7.16 (b). At the time of writing this thesis, only initial measurements had been performed on these RX chips and detailed measurements are in progress.

7.6 Performance summary

A fully integrated multifunctional D-band direct I/Q modulator/demodulator circuits in a SiGe BiCMOS process were designed, fabricated and verified experimentally. Paper [G] summarizes the performance of this work with some recently published results in a similar frequency range. The modulator measured 3-dB RF bandwidth extends beyond 33 GHz from 119 to 152 GHz and the 3-dB IF bandwidth is 13 GHz with a maximum conversion gain of 9.8 dB. The demodulator exhibits 10 dB conversion gain with 3-dB RF and IF bandwidths of 36 GHz (from 117 GHz to 153 GHz) and 16 GHz, respectively. It can nevertheless be seen that the presented designs demonstrate outstanding performance in terms of conversion gain, and RF/IF bandwidth for the given technology. The demodulator circuit is further integrated with low noise amplifier, and microstrip to waveguide transition at the RF port as well as a D-band amplifier and X6 multiplier at the LO port.
Figure 7.16: I/Q demodulator integrated with (a) LNA and X6 LO multiplier chain (b) LNA, X6 LO multiplier chain and on-chip microstrip to waveguide transition at RF port.
Chapter 8

Conclusions and Future Work

Conclusions

Today’s main driving parameters for radio transceiver research is their ability to provide high capacity while maintaining low cost, small form factor, and low power consumption. Direct conversion architectures are feasible for single chip integration at millimeter-wave and have attracted a large amount of interest in recent years due to their potential to meet these demands. The mm-wave has large bandwidth for data transmissions that can achieve high data rate communication. The communication system operating over 100 GHz enabling 10-100 Gbit/s wireless communication is of interest in various applications ranging from personal area networks for portable electronic devices, 4G and 5G mobile communication infrastructure, high data rate backhaul, real-time transmission of high-definition videos, chip to chip communication (short-range) links in form factor constrained devices (wireless in a box), in data centers for cloud computing and also for long-range high-speed communication (using phased arrays). However, it is a challenge to design and implement millimeter-wave transceivers that can utilize such wideband effectively for the data transmission.

Three main topics considered in this thesis are the design and characterization of front-end building blocks, integration of TX/RX chipsets and demonstration of real-time transmission and reception of wireless signals on these chipsets. Design emphasis is made on simple, yet robust direct conversion architecture that can be integrated on single chip. The theoretical principles derived can be applied over a broad range of frequencies. The circuits are implemented in both III-V (0.25 µm InP DHBT) and silicon (130 nm SiGe BiCMOS) technologies operating at D-band. State-of-the-art performances have been achieved with several of the circuits mentioned in this thesis.

The thesis presents the design and implementation of quadrature up and downconverting mixer circuits in Paper [A] and Paper [B]; balanced frequency multipliers with respect to their major performance parameters; and the design of on-chip passive structures in the D-band frequency range in Paper [C]. The mixer circuits achieve state-of-the-art IF/RF bandwidths while maintaining a high LO-to-RF isolation with low LO power requirement. The critical design and layout issues are also discussed together with the comparison with state-of-the-art reported work in recent literature. The mixer can be used for direct modulation/demodulation of the I and Q data from baseband, as well as secondary up/downconversion of a modulated IF frequency signal. The modulator/demodulator circuits are the key component in modern wireless transceivers.
Accurate measurement of such complex circuits at high frequencies proved to be challenging. Standard instruments do not yet exist for this frequency band which means signal sources have limited output power, and harmonic mixers have high conversion loss. Data presented for the downconverting mixer was verified by comparing CW and NF.

After describing design methodologies and mm-wave building blocks (modulator, demodulator, and frequency multipliers), the thesis focuses on the system integration. The design, characterization and implementation of TX/RX chipset consisting of an X3 LO frequency multiplier integrated with an I/Q modulator/demodulator and a low-noise amplifier/power amplifier is discussed in Paper [D].

The validation of the functionality and effectiveness of the TX/RX chipset in a transmit/receive wireless link in both direct-modulation or zero-IF architecture as well as in heterodyne architecture of front-end systems are described in Paper [D-E]. For QPSK and 64 QAM modulation schemes, the maximum measured data-rates using this chipset are 48 Gbit/s in homodyne mode and 18-Gbit/s in heterodyne mode, respectively. These tests indicate that the presented MMICs are especially well suited for transmission and reception of wireless signals at data rates which exceed the present state-of-the art in the D-band by a factor of two.

Figure 8.1: Summary of data transmission results from appended papers [D-H].

Figure 8.2: Real-time data transmission and detection experiments beyond 100 GHz.
Fig. 8.1 summarizes the data transmission experiment performance achieved for different circuits in terms of data rate and spectral efficiency.

The InP TX/RX front-end circuitry is incorporated in split-block waveguide modules in a collaborative teamwork. The TX/RX front-end modules were integrated into radio units to demonstrate a real-time wireless data transmission in Paper [F] and compared to state-of-the-art published results in Fig. 8.2.

At a distance of 10 m and using 40 dBi gain antennas, the data rate achieved was 5.3 Gbit/s using 64 QAM modulation over a 1 GHz channel with spectrum efficiency of 5 bit/s/Hz. Given the TX/RX module performance in Chapter 6, we expect it to support higher modulation over longer distances (>200 m). At the time of writing this thesis, outdoor experiments in different weather conditions were in progress and initial measurements had demonstrated error-free transmission over a 200 m hop length.

The design and implementation of quadrature upconverting and downconverting mixer circuits is also described in the thesis using a commercial 130 nm SiGe BiCMOS process in paper [G]. The competitive measurement results are obtained together with the transmission experiment using QPSK and multi-level QAM modulation formats in Paper [H]. The demodulator circuit is further integrated with low noise amplifier, and microstrip to waveguide transition at RF port as well as D-band amplifier and X6 multiplier at LO port in to a multifunctional RX chip.

This thesis successfully builds and demonstrates spectrum efficient mm-wave wireless links for the next generation high-speed communication applications.

**Future work**

During the work with this thesis, several interesting topics for future work have emerged and are hereby listed:

- **Phased array transceivers**
  - The extension of the mm-wave transceivers developed in this thesis is to design phased-array transceivers. The phased-array technology results in higher immunity to unwanted interference and therefore achieves a superior overall system capacity in a shared environment.

- **Integration of VCO**
  - Integration of an adequate VCO on the same chip as presented front-ends can be implemented. The LO signal can be generated with an integrated voltage-controlled oscillator (VCO), which must be designed properly to minimize LO leakage into other parts of the circuits. This issue can be alleviated by choosing a VCO running frequency that is not an integer multiple of LO signal.

- **Digital calibration in the RF front-end**
  - With the aid of integrated advanced digital signal processing (DSP), there can be auto-tuning and digital calibration in the RF front-end. The functions may include I/Q matching calibration, band pass filter tuning, and VCO/PLL calibration. In this way, the RF front-end will be able to withstand process, voltage and temperature (PVT) variations.

- **Improvement in real-time system demonstration**
- The noise figure in LNA and the output power of the PA could be improved along with the linearity of mixer circuits. Phase noise contribution on the degradation of the SNR of the system needs to be studied and should be implemented to improve link margin.
Chapter 9

Summary of Appended Papers

This chapter presents a brief summary of each of the appended papers together with an abstract and a paragraph describing my contribution. Although most of the work was completed by the first author, the contributions from the other authors have been of invaluable help and importance. This chapter summarizes the publications which are included in this thesis.

Paper A


In order to meet the performance requirements and increased capacity of wireless communication systems, such systems have to operate with amplitude and phase modulation. Quadrature modulators and demodulators are therefore essential components in the future millimeter-wave systems. This paper presents a quadrature up and down converting mixer circuit with on-chip RF and local oscillator (LO) baluns for the 110-170 GHz band. The mixers require an external LO signal and can be used as direct carrier quadrature modulator and demodulator to implement higher order quadrature amplitude modulation formats. The circuits cover the entire D-band, which is the widest bandwidth reported up to date.

My contribution- I contributed the design, simulations and characterization of the mixer circuits, and the writing of the paper.

Paper B


This paper presents the design and characterization of a direct quadrature modulator in 0.25 μm InP DHBT technology. The modulator design is based on a double balanced Gilbert-cell topology and operates over the frequency range of 115 to 155 GHz. The results show state-of-the-art performance in terms of conversion gain, LO to RF isolation and sideband supression with low LO power requirement and DC power consumption.

My contribution- I designed the circuit, performed measurement, analyzed the data, and wrote the paper.
Chapter 9. Summary of Appended Papers

**Paper C**


Integrated frequency sources are the key components for millimeter-wave applications. At lower frequency, the oscillator has a better tuning range and phase noise and is often cascaded with frequency multipliers to generate the desired output at higher frequencies. This paper presents the design and characterization of an active balanced frequency doubler for the D-band and tripler for the G-band. The balanced topologies are employed in the designs for harmonic suppression and broadband operation. The circuits are implemented in a 250 nm InP DHBT technology with $f_T/f_{MAX}$ 350 GHz/600 GHz respectively. The measurement results highlight the significant potential of the presented balanced active frequency multipliers for mm-wave frequency synthesis chains.

**My contribution-** I contributed the design, simulations and characterization of the multiplier circuits, and the writing of the paper.

**Paper D**


This paper presents design and characterization of a single-chip 110–170 GHz (D-band) direct conversion in-phase/quadrature-phase (I/Q) transmitter (TX) and receiver (RX) monolithic microwave integrated circuits (MMICs), realized in a 250 nm indium phosphide (InP) double heterojunction bipolar transistor (DHBT) technology. The chipset is multifunctional and can be used in both homodyne and heterodyne architectures. The TX consists of an I/Q modulator, a frequency tripler, and a broadband three-stage power amplifier. The RX includes an I/Q demodulator with a D-band amplifier and X3 multiplier chain at the LO port. This work demonstrated a high data rate of 48 Gbit/s using quadrature phase-shift keying (QPSK) modulation in homodyne mode and a spectrum efficient 18 Gbit/s 64 quadrature amplitude modulation (QAM) signal in heterodyne mode over carrier frequency in the D-band.

**My contribution-** The I/Q modulator and demodulator circuits were designed by me. The LO tripler was designed by Dr. Mingquan Bao and the D-band amplifier was designed by Prof. Herbert Zirath. I contributed the integration and simulations of the above circuits into the transmitter and receiver chipset. I built the experiment setup, performed measurements and analyzed the data to characterize the transmitter and receiver chipset. The data transmission experiment and radio link demonstrator work was carried out together with Zhongxia Simon He. The QAM transmission measured data was analyzed together with D. Nopchinda. I wrote the paper.
Chapter 8. Summary of Appended Papers

**Paper E**


The communication system operating over 100 GHz enabling 10–100 Gbit/s wireless point-to-point communication is of interest after the E band. The frequency range from 120 to 160 GHz is particularly interesting due to its low atmospheric loss (1dB/km). This paper presents the data transmission on an InP DHBT transceiver chipset using QPSK modulation with a data rate of 44 Gbit/s which exceed the present state-of-the art in the D-band by a factor of 2.

**My contribution**- I designed the data transmission experiment, performed measurements and analyzed the results together with Z. Simon He. I wrote the paper together with co-authors.

**Paper F**


This paper presents the results of the first real-time transmission of data at 143 GHz at a distance of 10 m using a fully integrated chipset incorporated in split-block waveguide modules. At a distance of 10 m and using 40 dBi gain antennas, the highest data rate achieved was 5.3 Gbit/s using 64 QAM modulation over a 1 GHz channel with spectrum efficiency of 5bit/s/Hz.

**My contribution**- The packaging of the TX/RX chipset and characterization of the TX/RX modules as well as initial data transmission experiments on modules were performed together with V. Vassilev and Z. Simon He. Real-time data transmission was performed in a team with Ericsson AB. Paper is written by V. Vassilev.

**Paper G**


This paper presents the design and characterization of a SiGe BiCMOS quadrature upconverting mixer/modulator and quadrature downconverting mixer/demodulator in 110-170 GHz. The SiGe HBT BiCMOS technology has potential for low cost systems and large-scale integration of analog and digital functions on a single die. State-of-the-art results are measured on I/Q modulator/demodulator circuits in terms of RF and IF bandwidths. These circuits can be further integrated with LO multiplier and amplifier circuits to implement complete transceivers with spectrum efficient modulation and high data rate capability.
My contribution- I designed the circuits, performed measurement, analyzed the data, and characterized the modulator and demodulator circuits. I performed the data transmission experiment together with Z. He. I wrote the paper.

**Paper H**


In this paper, a 110-170 GHz quadrature upconverting mixer is designed in a commercial 130 nm SiGe BiCMOS technology. The mixer is used for direct modulation of the I and Q data from baseband, as well as secondary upconversion of a modulated IF frequency signal. The design is based on a double-balanced Gilbert mixer cell topology and is capable of transmitting more than 12 Gbit/s QPSK signal. This multifunctional modulator circuit is characterized as a single side band mixer.

My contribution- I contributed with design, simulations and characterization of the modulator circuit, and the writing of the paper.
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Bibliography


[130] https://www.infineon.com