Correlators for Interferometric Radiometry in Remote Sensing Applications, a Scaling Perspective.

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Abstract

Correlators are extensively used in the field of radio interferometry. Two different types are considered for two applications; autocorrelators for spectrometry and cross-correlators for aperture synthesis. We concentrate on satellite-based applications where power budgets are very restrictive. Several satellites are already employing correlators for interferometric measurements, and future projects are targeting even larger systems in terms of spectral channels in the case of spectrometry and baseline counts in the case of aperture synthesis. Thus, it is important to develop correlators with increasing channel count, either using ASIC technology scaling or by constructing larger systems from several ASICs.

Building on earlier ASIC designs, we examine how larger correlator systems can be constructed and the implications this has, in terms of power dissipation, system complexity, and ASIC count. Our findings indicate that, for large systems, having a very high channel count per ASIC is indeed of interest for keeping system complexity and power dissipation down by reducing both ASIC and I/O count, especially for cross-correlators.

I. INTRODUCTION

Remote sensing in the radio spectrum is becoming increasingly important for both metrology and climatology as well as for interplanetary missions [1]. Correlators are used for performing interferometry for both spectral analysis and for aperture synthesis imaging. CMOS technology scaling has made digital correlators increasingly competitive by both increasing their bandwidth capability and by reducing power dissipation per operation.

Autocorrelation is an efficient way of performing spectrometry. It was invented in 1963 [2] and used for discovering the first interstellar OH molecule [3]. Since then it has been widely adopted and used in, e.g., the Odin satellite launched in 2001 [4]. The autocorrelator for Odin was among the first to be optimized for power efficiency. One of the advantages with autocorrelation spectrometers is their flexibility; the bandwidth and, hence, spectral resolution can be modified by changing the sampling frequency. Taking the Fourier transform of the autocorrelation function, the power spectrum is calculated, using the Wiener-Khinchin theorem [5].

A relatively new application for correlators in remote sensing is aperture synthesis. Here, imaging is performed using an array of many antennas and performing cross-correlation between antenna pairs (baselines), sampling the UV-plane. By using the inverse 2-D Fourier transform, a brightness temperature image is achieved. While aperture synthesis is nothing new[1], the first, and so far only aperture synthesis array implemented on a satellite was the Microwave Imaging Radiometer with Aperture Synthesis (MIRAS) launched to low Earth orbit (LEO) with the Soil Moisture and Ocean Salinity (SMOS) satellite as late as 2009 [6]. Several initiatives of placing an aperture synthesis imager in geostationary orbit (GEO) is currently ongoing; in the USA with the Geostationary Synthetic Thinned Aperture Radiometer (GeoSTAR) [7], in Europe with the Geostationary Atmospheric Interferometric Sounder (GAIS) [8], and in China with the Geostationary Interferometric Microwave Sounder (GIMS) [9].

While the time-limited, digital cross-correlation function, as shown in Eq. 1, is performed on two signals, f and g, autocorrelation is the cross-correlation of a signal with itself ($f = g$). The signals are multiplied and averaged over a time, M, for a number of different time delays (lags), n, applied to one of the signals. Here, f^* is the complex conjugate of f.

$$(f \star g)[n] \overset{\text{def}}{=} \sum_{m=0}^{M} f^*[m]g[m+n]$$

We have previously presented two cross-correlator application-specific integrated circuits (ASICs) [10, 11] developed using full-custom design in a 65-nm CMOS process technology. The first cross-correlator implemented 64 2-level input channels, while the second can be configured as either a 96-channel 2-level correlator or as a 48-channel 3-level correlator. A separate, 8-channel analog-to-digital converter (ADC) has also been custom made for these cross-correlators [12] in a 130-nm BiCMOS process. The motivation behind using a separate ADC was two-fold; it made channel isolation of below 30-40dB much easier to achieve and it also meant bipolar transistors could be used, while the CMOS-based cross-correlator could be implemented in significantly more advanced (65-nm) technology nodes. The choice of bipolar logic for the ADC improved device matching properties [13] and made it easier to implement a high-precision comparator without using automatic offset cancelation techniques. The ADC together with the 64-channel cross-correlator have been assembled into a complete cross-correlator system [14].

We also implemented an ADC and an autocorrelator ASIC for spectrometry using full-custom design. The autocorrelator

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[1] Aperture synthesis has long been used for achieving high resolution in radio astronomy such as VLA, LOFAR and ALMA.

ADC was implemented using a 130-nm BiCMOS process technology, which was also used for the cross-correlator ADC, and was designed to support two 3-level channels. To obtain higher bandwidth, the autocorrelator ADC uses a time-division (TDM) scheme: We use four times the number of digital streams (TDM4), each outputting data at a rate of a fourth of the sample rate. The autocorrelator was implemented in a 28-nm fully-depleted silicon-on-insulator (FD-SOI) process technology and supports up to 8638 lags.

In this paper, we will evaluate different design methodologies of implementing cross-correlator and autocorrelator systems and their impact on system complexity and power dissipation, for design scenarios where we expand the number of baselines or spectral channels of the systems beyond the capabilities of the implemented ASICs. Our main focus is in on-satellite applications where size, weight, and power budgets are very restrictive, however, other applications such as security scanning applications [15], balloon experiments, etc. may have similar restrictions.

II. EXPANDING CORRELATOR DESIGNS

When construction correlators with high channel-count requirements, one have to consider the tradeoff between chip scaling and system scaling, i.e., the number of ASICs vs the number of channels per ASIC. These tradeoffs affect system complexity and, thus, size, weight, cost, and power dissipation. We will investigate implementation styles and system architectures, for both autocorrelators and cross-correlators, to handle system level-scaling based on a fixed number of channels per chip.

A. Autocorrelators

For autocorrelator systems, two approaches to increasing the resolution beyond a single ASIC are investigated; serialization and parallelization. We further divide the parallelization methods into two sub-categories, i.e., either using alias sampling or using multiple local oscillators (LO) to divide the band before analog-to-digital (AD) conversion. The three different schemes are shown in Fig. 1.

The serial scheme has historically been more common due to the very limited number of channels that could be achieved on-chip. It is the simplest solution of the three to achieve greater resolution. In the serial scheme, the entire band is sampled by a single ADC, after which the digital autocorrelator ASICs are linked, one after another.

Parallel schemes have usually been motivated by their ability to extend the total bandwidth beyond what ADCs and CMOS logic could handle. In the parallel alias-sampled approach, the band of interest is split, using power splitters, after down-conversion. Filter banks are used for sub-band division. Each sub-band is sampled by an ADC at a rate that is the Nyquist rate for the full band, divided by the number of ADCs used. For the multiple-LO scheme, the signal is split before down-conversion. A different LO frequency for each mixer divides the band into sub-bands along with low-pass filtering before each ADC. The sample rate here is the same as for the alias-sampling version. There is also the possibility to

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² The implemented ADCs use CML buffers for digital outputs.

mix the serial scheme with any of the parallel ones. We will, however, not explore any such schemes in this paper.

(a) Serialization, using additional I/Os.

(b) Parallelization, using alias sampling.

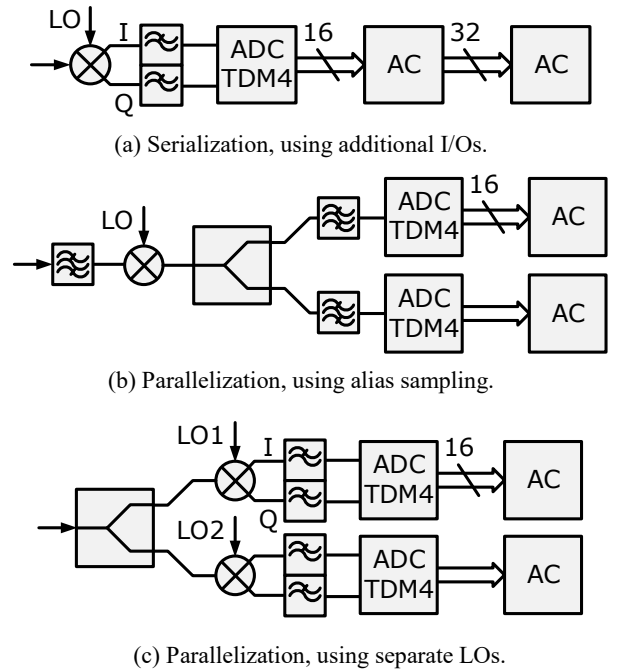(c) Parallelization, using separate LOs.

Figure 1: System architectures for connecting multiple autocorrelators (AC).

While the parallel approaches may infer a significant extra cost, in terms of additional ADCs, splitters, filters and mixers, the serial scheme requires additional I/Os for the autocorrelator ASIC. To be able to serially link ASICs, instead of one IQ input pair, an additional delayed input and output for both non-delayed and delayed data are required, which leads to a total of four times as many I/Os as for a non-linkable design.

B. Cross-Correlators

For cross-correlators, the ASICs have to be connected in parallel, and signals have to be split to multiple cross-correlator ASICs for full baseline coverage. Still, we have the option of where to perform signal splitting; before or after AD-conversion. Two examples are shown in Fig. 4. Power splitters are used for the analog split, while current-mode logic² (CML) splitters are used for digital splitting. The difference in number of ADCs required for the shown case is a factor of two.
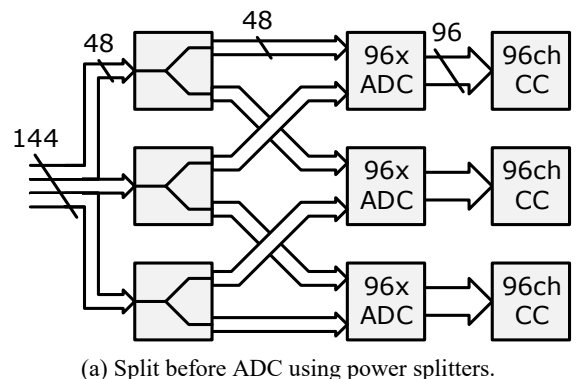
(a) Split before ADC using power splitters.

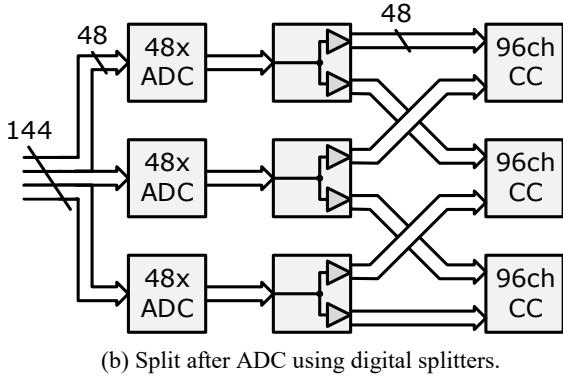(b) Split after ADC using digital splitters.

Figure 2: System architectures for connecting multiple cross-correlators (CC).

III. System Scaling Estimations

A. Autocorrelators

The number of autocorrelator ASICs required naturally scales linearly with the number of spectral channels needed, and for the parallel schemes so does the ADC count.

Apart from complexity in terms of chip count, the different systems have very different advantages and disadvantages. If not only resolution is to be expanded, the case with separate LOs gives an advantage since the analog bandwidth requirement of the ADC is much lower than for the alias-sampled and serial schemes, where ADCs have to cover the entire analog band. In addition, with separate LOs, the sub-bands can be arranged and rearranged freely, ideal in cases where a large band has to be covered, but where continuous coverage is not necessary.

The serialized scheme does impose a vulnerability if any of the circuits becomes faulty. A faulty ASIC in the chain could break the data flow and make remaining ASICs inoperable. The parallel schemes exhibit a more graceful degradation for broken correlator and ADC ASICs, giving more redundancy. The scheme using separate LOs gives an additional advantage in that any channel can potentially cover for any other broken one by switching the frequency. Even backup channels could be implemented this way.
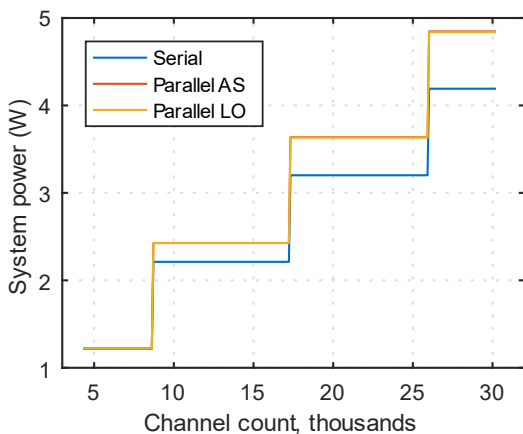

Figure 3: Estimated autocorrelator system power, including signal and clock splitters, ADC and autocorrelators, for three cases: Serial, Parallel with alias sampling (AS), and parallel with separate mixers (LO).

System power estimation, shown in Fig. 3, is based on measured results from the fabricated autocorrelator ADC, and simulated results including wire parasitics for the autocorrelator ASIC. Included are also mixer power, CML interface power and input power requirement, based on filter, splitter, and mixer losses. As shown, the two parallel schemes dissipate nearly the same amount of power and this is because total power dissipation is dominated by ADCs and correlators, which are identical for the two parallel schemes.
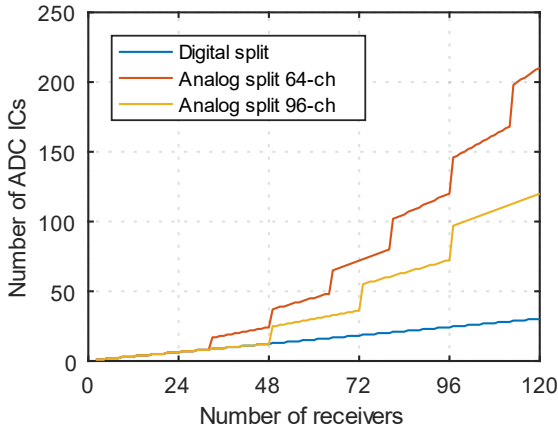
B. Cross-Correlators

The number of required n-input ASICs grows as $[N/n \cdot 2] \cdot [N/n \cdot 2\text{-}1]/2$, where N is the number of input channels from the front-ends. The number of cross-correlator ASICs, for two different input count alternatives, 64 and 96 2-level channels as in [10, 11], is shown in Fig. 4a. The numbers increase dramatically with higher input channel count requirements.

The number of ADCs when performing signal split after conversion, as shown in Fig. 4b, is naturally linear with the input count, but grows much quicker when splitting before AD-conversion. We base these estimations on an 8-channel ADC, as in [12]. With very large cross-coupling networks, the peak bandwidth may be reduced due to timing issues, and sub-banding may also be required, further exacerbating system complexity issues. Thus, it is clear that a high single-chip channel count is of the essence for keeping system complexity down, especially considering the cross-coupling that has to be performed for the cross-correlator application.

The power dissipation of cross-correlator systems with split before and after ADC, operating at 1.5 and 3GHz, is shown in Fig. 5. Calculations include power dissipation for ADCs, cross-correlators, splitter circuitry and for additional input gain required when using power splitters. With the ADCs taking a large part of the complete system power dissipation, the split-after-ADC approach is clearly advantageous.
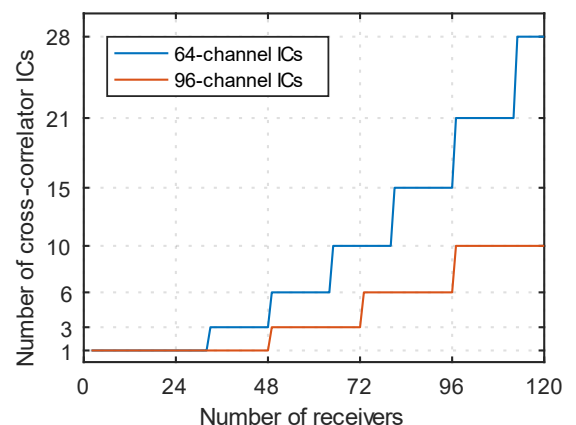
(a) Number of 64- or 96-channel cross-correlator ASICs for systems with different number of receivers.

(b) Number of 8-channel ADCs for systems with different number of receivers.

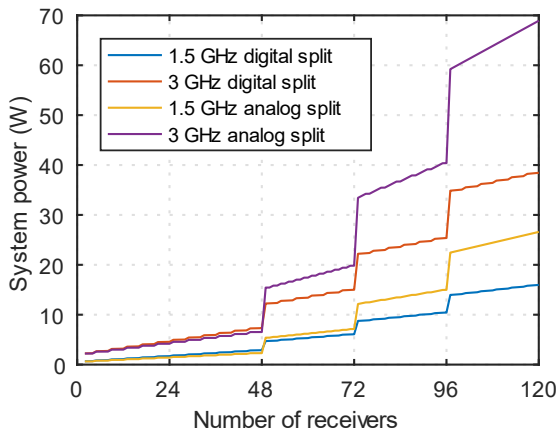Figure 4: Resource requirements for larger correlator systems.

Figure 5: Estimated cross-correlator system power, including signal and clock splitters, ADC and cross-correlators, for four cases.

III. CONCLUSION

We have explored a few different correlator systems focusing on expanding channel counts beyond single ASICs; three for autocorrelators and two for cross-correlators. For autocorrelators, it is clear that the serial approach dissipates less power with the currently studied components, however, disadvantages such as less reliability, flexibility and significantly increased chip I/O-count means this is not necessarily the best option. For cross-correlators, we find that of the two schemes explored, splitting signals after AD-conversion is significantly more power efficient, at least with our current ADCs. It is also clear that the system complexity in terms of ASIC and I/O count scales dramatically worse for cross-correlators than for autocorrelators. With these results in mind, we find that there is great motivation for implementing large channel counts already at ASIC level to reduce system design complexity, especially for cross-correlators. This is further motivated by the significant reduction in cost of MOS devices, in terms of price per transistor, that has been achieved since the early correlators.

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