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A GaN–SiC hybrid material for high-frequency and power electronics

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We demonstrate that 3.5% in-plane lattice mismatch between GaN (0001) epitaxial layers and SiC (0001) substrates can be accommodated without triggering extended defects over large areas using a grain-boundary-free AlN nucleation layer (NL). Defect formation in the initial epitaxial growth phase is thus significantly alleviated, confirmed by various characterization techniques. As a result, a high-quality 0.2- μm thin GaN layer can be grown on the AlN NL and directly serve as a channel layer in power devices, like high electron mobility transistors (HEMTs). The channel electrons exhibit a state-of-the-art mobility of $>2000\text{ cm}^2/\text{V}\cdot\text{s}$, in the AlGaIn/GaN heterostructures without a conventional thick C- or Fe-doped buffer layer. The highly scaled transistor processed on the heterostructure with a nearly perfect GaN–SiC interface shows excellent DC and microwave performances. A peak RF power density of 5.8 W/mm was obtained at $V_{\text{DSQ}} = 40\text{ V}$ and a fundamental frequency of 30 GHz. Moreover, an unpassivated 0.2- μm GaN/AlN/SiC stack shows lateral and vertical breakdowns at 1.5 kV. Perfecting the GaN–SiC interface enables a GaN–SiC hybrid material that combines the high-electron-velocity thin GaN with the high-breakdown bulk SiC, which promises further advances in a wide spectrum of high-frequency and power electronics. *Published by AIP Publishing.* <https://doi.org/10.1063/1.5042049>

Structural defects in epitaxial layers dictate semiconductor device performance and reliability. Dislocation annihilation in GaN is typically a slow process that largely relies on an undesired thick layer growth.¹ As a wide-bandgap semiconductor, GaN is being widely used in power devices, yet still suffers from this issue, due to a fundamental heteroepitaxial challenge, the large lattice mismatch to substrates.^{2,3} For GaN-based high electron mobility transistor (HEMT) heterostructures used in high-frequency and power applications, semi-insulating (SI) SiC remains the best choice of substrates, owing to its high thermal conductivity and high resistivity and the maturity in large-wafer mass production (up to 150 mm). Nevertheless, since the first GaN-on-SiC epitaxy was realized by the use of an AlN interlayer more than two decades ago, there has been limited progress in the epitaxial growth.^{4–7} The AlN interlayers/nucleation layers (NLs) typically exhibit grain-like morphology and then evolve into column-like growth as the thickness increases, due to the low mobility of Al adatoms. Structural defects like voids and dislocations generated at the interfaces of GaN/AlN/SiC introduce a thermal boundary resistance (TBR) that results in an additional 30%–40% channel temperature rise in HEMTs.^{8,9} Moreover, the threading dislocations in the GaN layer can only be effectively reduced by increasing the thickness, typically to 1.5–2.0 μm , in order to reach a structural quality sufficient for device performance. Consequently, the thick GaN layer, as a buffer layer, must be doped by acceptor-like impurities such as carbon or iron to eliminate the parasitic conduction below the GaN channel layer, which in turn introduces another grave issue — charge trapping.^{10–12} Charge trapping in deep levels

within the thick buffer layer leads to a current collapse at the device level, which is a major factor limiting the RF output power. Recently, we developed the growth of high-structural-quality AlN NL for low thermal boundary resistance (low-TBR) by hot-wall metalorganic chemical vapor deposition (MOCVD).^{13,14} The typical full width at half maximum (FWHM) value of X-ray diffraction rocking curves (XRC) for the AlN (002) and (102) reflections is around 100 arcsec. In the present work, we additionally find that with the low-TBR AlN NL, the structural quality of a 0.2- μm -thin unintentionally doped (UID) GaN layer is as mature as that of the typical 2.0- μm thick GaN layers grown on SiC substrates. This enables a thin HEMT (T-HEMT) heterostructure, which is based on a concept of a GaN–SiC hybrid material, where the thin GaN epilayer serves as the high-electron-mobility channel layer and the low-defect bulk SiC substrate functions as the voltage blocking layer, as proposed in Fig. 1(a). This results in several potential advantages for the T-HEMT heterostructure, compared to traditional HEMT heterostructures with a thick, doped buffer layer: First, the thermal resistance of the T-HEMT devices is expected to be considerably reduced, provided that the formation of structural defects in the GaN–SiC interface is suppressed. The joule heat generated in the thin GaN channel would thus dissipate more efficiently into the substrate, so that the issue of device self-heating could be alleviated; Second, by avoiding a thick doped buffer layer, there would be less trapping effects since the entire T-HEMT heterostructure is unintentionally doped; Third, the AlN NL could effectively serve as a back barrier to enhance the carrier confinement in the channel for high-frequency applications; Finally, the aggressive thickness reduction reduces 90% raw materials including precursors and gases

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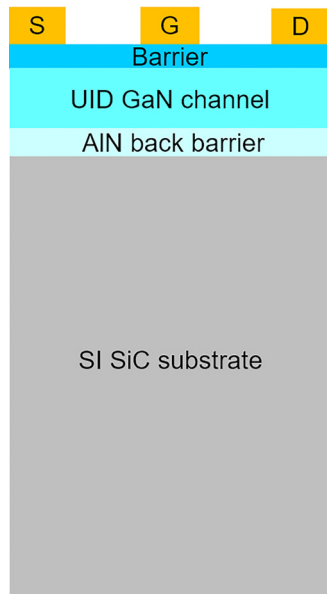


FIG. 1. Schematic thin HEMT (T-HEMT) heterostructure based on the GaN–SiC hybrid material concept.

and dramatically reduces the deposition time, thus minimizing the manufacturing cost and increasing MOCVD uptime. All the potential advantages mentioned above were investigated and confirmed in this work.

The III-nitride epitaxial layers were all grown on Si-face 4H on-axis SiC substrates in a commercial hot-wall MOCVD reactor using trimethylgallium (TMGa), trimethylaluminum (TMAI), and high-purity ammonia (NH_3 , >99.999%) as the precursors. The growth was initiated with a normal 60-nm low-TBR AlN NL. On the top of it, the growth was followed by a T-HEMT heterostructure that consists of 2-nm GaN cap/10~14-nm AlGa_{0.29}Ga_{0.71}N barrier/0~1.5-nm AlN/200-nm GaN channel layer. The Al content in the barrier is around 0.29~0.30. The heterostructure was grown at a high temperature to reduce residual impurities. The levels of Si, O, and C are close to the detection limits of secondary ion mass spectroscopy, which is $\sim 1.0\text{E}+16\text{ cm}^{-3}$. An interface sharpening technique was employed to enhance the transport properties of the channel electrons. The details of the heterostructure growth can be found in Refs. 15 and 16. A high-resolution X-ray diffractometer (Philips X'Pert MRD) with $\lambda = 0.154\text{ nm}$ of Cu $K_{\alpha 1}$ radiation was employed to measure the structural parameters of the III-nitride layers. A line focus mode was used, which provides a probe area of $2 \times 5\text{ mm}^2$. An atomic force microscopy (AFM) system (Veeco Dimension 3100) was employed to characterize the sample surface morphology. Transmission electron microscopy (TEM) cross-sectional samples were prepared by ion milling in a Gatan Precision Ion Polishing System using argon ions at 5 kV for 2 h, 2 kV to electron transparent, and finally polishing at 500 V for 2 h. FEI Tecnai G2 TF 20 UT with a field-emission gun operated at 200 keV and a point resolution of 1.95 \AA was used for TEM characterization.

We examined the properties of a thin HEMT heterostructure for a model high-frequency power device, consisting of 2-nm GaN cap/14-nm Al_{0.29}Ga_{0.71}N barrier layer/200-nm GaN channel layer/60-nm low-TBR AlN NL grown on a 100 mm semi-insulating (SI) 4H SiC substrate by using several material

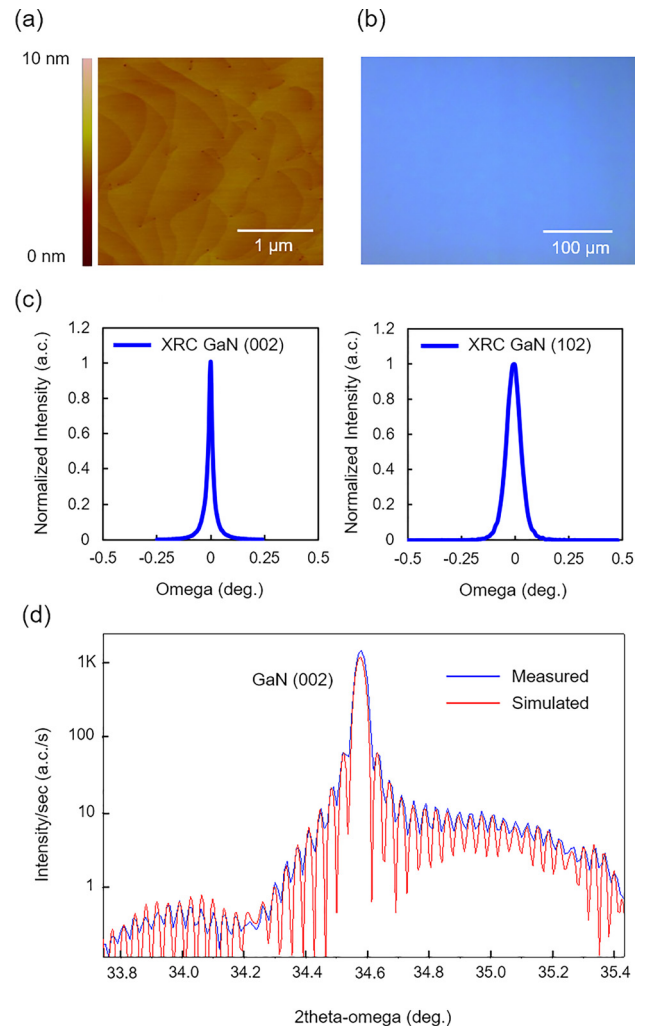


FIG. 2. (a) $3 \times 3\text{ }\mu\text{m}^2$ AFM image, (b) OM image, (c) GaN XRCs of the T-HEMT, and (d) XRD 2theta-omega of the thin GaN (002).

characterization techniques. Figures 2(a) and 2(b) show the images of a small and a large surface area by atomic force microscopy (AFM) and Nomarski optical microscopy (OM), respectively. A root-mean-square surface roughness of 0.235 nm was measured over a $3 \times 3\text{ }\mu\text{m}^2$ area. Both images indicate that the heterostructure has a fully coalesced and atomically flat morphology. Furthermore, the crystalline quality of the GaN layer was evaluated by X-ray diffraction rocking curve measurements for the (002) and (102) reflections to assess screw-type and edge-type dislocations, respectively. As shown in Fig. 2(c), the thin GaN channel layer exhibits a full width at half maximum of 86 and 268 arcsec for the GaN XRC (002) and (102) reflections, respectively. The threading dislocation density in the GaN layer is estimated to be in the range of low 10^8 cm^{-2} , based on the FWHMs of the XRCs.¹⁷ This defect density is two orders of magnitude less than that of the typical GaN layers with the same thickness.¹ Besides, in Fig. 2(d), one can see that the thin GaN layer exhibits strong Kiessig fringes, from which a channel thickness of 220 nm is extracted. It should be noted that this feature is pronounced only when the thin layer has a high-quality and sharp heterojunctions. Contactless Hall measurements revealed that the epiwafer has a two-dimensional electron gas (2DEG) density of $9.8 \times 10^{12}\text{ cm}^{-2}$ and a 2DEG

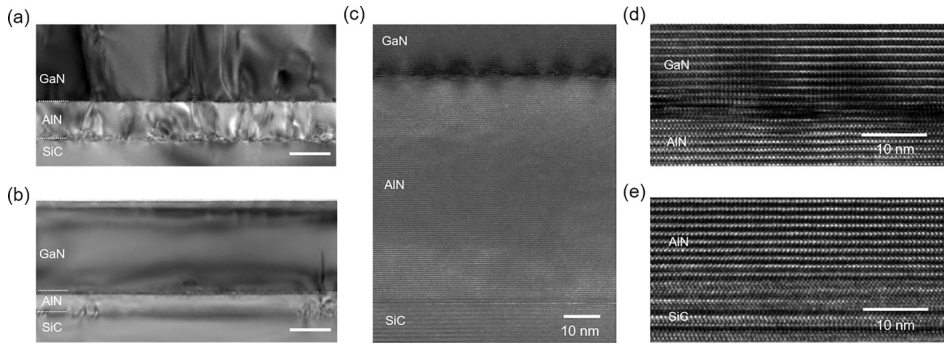


FIG. 3. Cross-sectional TEM images along $[11\bar{2}0]$ at the GaN/AlN/SiC interface using (a) a conventional AlN NL and (b) the low-TBR AlN NL. (c) High-magnification image of GaN/low-TBR AlN NL/SiC. (d) High-resolution image at the interface of GaN/low-TBR AlN NL. (e) High-resolution image at the interface of low-TBR AlN NL/SiC. The scale bar is 100 nm in (a) and (b).

mobility of $2050\text{ cm}^2/\text{V}\cdot\text{s}$, which results in a sheet resistance (R_{sh}) of $315\text{ ohm}/\text{sq}$. The uniformity of the R_{sh} measuring 17 points over the 100 mm epiwafer is 1.8% (S1). All the structural and electrical properties achieved above are unprecedented for such a thin III-nitride HEMT heterostructure. It is also worth emphasizing that these properties are on par with those of the state-of-the-art GaN-on-SiC epiwafers with the conventional thick buffer layers. To gain further insights into the epitaxy, the high-resolution TEM was deployed to investigate the GaN–SiC interface.

Figures 3(a) and 3(b) show cross-sectional TEM images in the GaN/AlN/SiC interface region of the HEMT heterostructures using a conventional AlN NL¹⁵ and our here presented low-TBR AlN NL, respectively. It confirms that the low-TBR AlN NL has a very high structural integrity and is visibly free of grain boundaries, as highlighted in Fig. 3(c). Large defect-free regions up to $300\sim 400\text{ nm}$ wide are dominant in the low-TBR AlN NL, which is in stark contrast to the conventional AlN nucleation layer that has a high grain/defect density. The noticeable defects in the low-TBR AlN NL actually originate from the SiC surface region. This shows that besides the AlN NL growth, the surface condition of the SiC and its crystalline quality are also of importance to minimize the defect formation. Moreover, a closer look at the GaN/AlN interface and the AlN/SiC interface, as shown in Figs. 2(d) and 2(e), respectively, reveals that the lattice mismatch between GaN and SiC can be well accommodated with the periodic misfits at the GaN/AlN interface, given that part of the strain is released inevitably through the generation of threading dislocations. The reason that the periodic misfits only appear at the GaN/AlN interface, not at the AlN/SiC interface, is likely due to the fact that the lattice mismatch of the former interface (2.5%) is much larger than that of the latter (1%). On the other hand, this result also suggests that the formation of threading dislocations can be considerably suppressed in the initial epitaxial growth through the formation of the periodic misfits.

The test transistor devices were fabricated on a T-HEMT heterostructure consisting of similar active layers (2-nm GaN cap/10-nm $\text{Al}_{0.30}\text{Ga}_{0.70}\text{N}$ barrier layer/1-nm AlN/0.2- μm GaN channel) with gate lengths of 0.1- and 0.2- μm and a source-drain spacing of 2.0 μm . The details of the device processing for the AlGaN can be found in Ref. 18. A contact resistance of $0.3\text{ }\Omega\text{ mm}$ was obtained using recessed Ta-based contact.¹⁹

Figure 4(a) shows the DC I-V characteristic of the 0.1 μm T-HEMT device measured using a parameter analyzer (Keithley 4200-SCS). The device exhibited a high

current density of $1.1\text{ A}/\text{mm}$ and a low on-resistance of $1.3\text{ }\Omega\text{ mm}$. It was noticed that the high saturation current can be sustained at a V_{DS} up to 30 V without a noticeable degradation due to self-heating. This confirms the merit of the thermal management in the thin heterostructure. Moreover, the transfer characteristics at $V_{\text{DS}} = 10\text{ V}$ in Figs. 4(b) and 4(c) show that the device has a sharp pinch-off and a very high transconductance of $500\text{ mS}/\text{mm}$. The subthreshold swing (SS) was estimated to be 250 and 130 mV/decade at $V_{\text{DS}} = 10\text{ V}$, for the 0.1- and 0.2- μm T-HEMT devices, respectively. These results indicate that the channel electrons are

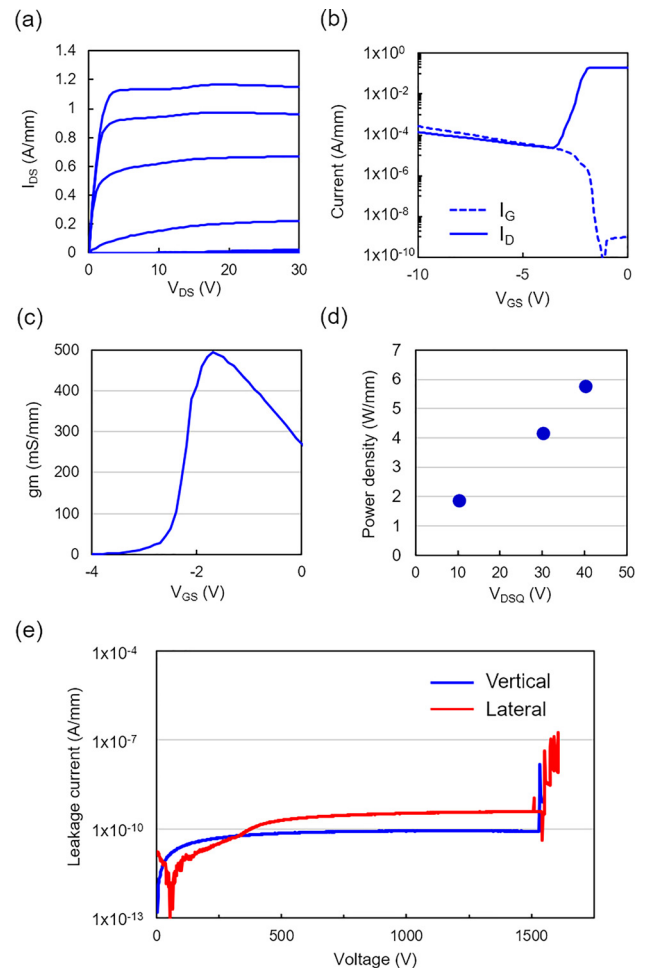


FIG. 4. (a) DC I-V characteristics, (b) transfer characteristics and gate and drain current at $V_{\text{DS}} = 10\text{ V}$ as a function of gate voltage, (c) transconductance as a function of V_{GS} , and (d) RF output power density as a function of V_{DSQ} of the T-HEMT device. (e) Vertical and lateral breakdown characteristics of the T-HEMT heterostructure without the top active layers.

well-confined in the T-HEMT heterostructures assisted by the AlN NL as a back barrier, which is essential for high-frequency applications. Meanwhile, the measured breakdown voltage of the 0.1- and 0.2- μm T-HEMT devices is 70 and 140 V, respectively. The linear relationship between the breakdown voltage and the gate length suggests that the breakdown was taking place laterally due to the limited dimension of the gate length and the gate-to-drain spacing. The typical gate length and the gate-to-drain spacing used in lateral power devices are in the ranges of 1–2 μm and 10–20 μm , respectively. Therefore, this result reveals the great potential of the T-HEMTs for lateral power devices.³

The microwave power performance was evaluated through continuous wave (CW) large signal measurements using a passive load-pull setup at a fundamental frequency of 30 GHz. The output power density of the 0.1- μm T-HEMT was measured with a quiescent current of 15% of the saturation current and biased at $V_{\text{DSQ}} = 10, 30$, and 40 V, respectively. The output power density as a function of the bias is plotted in Fig. 4(d). It is obvious that the T-HEMT is capable of delivering very high RF power. A peak RF power density of 5.8 W/mm was obtained at $V_{\text{DSQ}} = 40$ V. We attribute the high RF power to the absence of the intentional acceptor-like dopant in the T-HEMT heterostructure. Without the need to grow a thick doped buffer layer, the T-HEMT heterostructure opens up a broad opportunity to further reduce charge trapping effects.

As sparked by the previous breakdown result, we additionally measured another sample to further explore the potential of T-HEMT heterostructures for lateral power devices. The sample has the same T-HEMT heterostructure but without the top active layers, i.e. a stack of 0.2- μm GaN channel/60-nm AlN NL/500- μm SiC substrate. Figure 4(e) shows the two-terminal breakdown characteristics of the sample, measured laterally with the substrate floating (the two-terminal spacing is ~ 1.5 mm) and vertically with the substrate grounded, at room temperature. Surprisingly, the breakdown voltage in both the lateral and vertical configurations is as high as ~ 1.5 kV for the stack containing such a thin GaN layer. In both cases, the breakdown was due to the bad delineation of the contacts. Therefore, the real breakdown voltage of the stack is expected to be higher. In other words, the breakdown has been limited by the surface and it confirms that there are no interface carriers. To obtain this high vertical breakdown voltage, the SI SiC substrate must be effectively acting as a voltage blocking layer as we proposed earlier. This can be understood from GaN-on-Si lateral power devices,²⁰ in which it has been evident that the device breakdown is limited vertically. This is why the breakdown voltage can increase from 200 V to 650 V as the buffer layer thickness increases from 3.2 μm to 5.5 μm , and the breakdown voltage is further increased if the Si substrate is removed. These results indicate that the thick buffer layer and the Si substrate are the breakdown-limiting places, not the surface. Meanwhile, we noticed that there is a leakage current dip at ~ 60 V in the lateral breakdown test. The mechanism is unclear at the moment. Albeit that a detailed study of the T-HEMT heterostructure for lateral power devices is still ongoing, the result of the vertical breakdown voltage of 1.5 kV has shined the light on the future of T-HEMT

heterostructures for lateral power devices. With proper surface passivation, it holds promise to block substantially higher voltage.

In summary, we report that a nearly perfect GaN–SiC interface can be realized by using a grain-boundary-free AlN NL, which enables us to remove the conventional thick C- or Fe- doped buffer layer in GaN-based HEMT heterostructures. This provides alternative routes to tackle the buffer-trapping issues that have been prevailing in the field over the last two decades. The excellent DC and microwave device characteristics plus the extraordinary high breakdown confirm the competence of the proposed T-HEMT heterostructure that is based on the GaN–SiC hybrid material concept, for the use in both high-frequency and power applications.

See [supplementary material](#) for the R_{sh} map of the T-HEMT heterostructure grown on a SI 100 mm SiC substrate.

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