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THE EUROPEAN PROJECT "MERLIN" ON MULTI-GIGABIT, ENERGY-EFFICIENT, RUGGEDIZED LIGHTWAVE ENGINES FOR ADVANCED ON-BOARD DIGITAL PROCESSORS

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I. INTRODUCTION

Modern broadband communication networks rely on satellites to complement the terrestrial telecommunication infrastructure. Satellites accommodate global reach and enable world-wide direct broadcasting by facilitating wide access to the backbone network from remote sites or areas where the installation of ground segment infrastructure is not economically viable. At the same time the new broadband applications increase the bandwidth demands in every part of the network - and satellites are no exception. Modern telecom satellites incorporate On-Board Processors (OBP) having analogue-to-digital (ADC) and digital-to-analogue converters (DAC) at their inputs/outputs and making use of digital processing to handle hundreds of signals; as the amount of information exchanged increases, so do the physical size, mass and power consumption of the interconnects required to transfer massive amounts of data through bulk electric wires.

Optical interconnects that employ multimode optical fibre, vertical cavity surface emitting laser (VCSEL) and photo-detector (PD) arrays are now considered the enabling technology which will allow to transfer massive amounts of data between equipment, boards, modules and ASICs, quickly, efficiently and at low cost. Especially inter-board and inter-equipment connectivity through optical interconnects is of outmost importance for next generation OBPs. ASICs and ADC/DAC modules with fibre optic interfaces will effectively support the bandwidth required to the high-speed links whilst removing any distance limitation and better preserving signal integrity. This technology is expected to introduce flexibility in the architectural design by enabling, for instance to shift the ADC/DAC modules closer to the antenna elements, or to partition the OBP into several equipment as well.

MERLIN is a European research initiative that aims to develop an optical multi-channel transceiver technology for the realization of multi-gigabit on-board connectivity that will hit the right speed, size, power consumption and cost targets of next generation telecom satellite payloads.

The MERLIN technical objectives from component to system are:

- Fabrication of high-speed and extended temperature 850 nm VCSEL arrays. VCSELs are integrated in 2-D circular array configuration to enable coupling with multi-core radiation hardened fibers.
- Fabrication of high speed and extended temperature 850 nm PD circular arrays. Similar to the VCSELs, PDs are fabricated in 2-D circular array configurations.
- Fabrication of high-speed (25 Gb/s) radiation hard, multi-channel BiCMOS VCSEL driver and TIA integrated circuits.

- Fabrication of radiation hard multimode multi-core fiber. The use of the multi-core fiber enables the transmission of 6x optical channels through a single fiber feed-through, which accommodates the development of compact, ruggedized and hermetic transceiver modules.
- Fabrication of fully-packaged and ruggedized multi-core digital transceiver module.
- Module functional testing to demonstrate high-speed point to multi-point interconnectivity.
- Module environmental testing to assess performance under space environment constraints.

In what follows we report the project progress on the design, fabrication and testing of low power, high bandwidth circular VCSELs and PD arrays. Specifically we report the development of 6-channel VCSEL circular arrays with measured 3dB bandwidth >21 GHz (25°C) and >19 GHz (85°C), good uniformity, sub-mA threshold current, high slope efficiency (0.7 W/A) and high output power (8 mW). Additionally we report the development of 6-channel circular PD arrays with a temperature independent 0.6 A/W responsivity and 3dB cut off frequency of around 16 GHz at room temperature for 26μm diameter PDs. The development and experimental verification of these high speed photonic chipsets is an important step toward the realization of the MERLIN lightwave engines.

II. 6-CHANNEL MULTI-CORE VCSEL ARRAYS

Two different versions of 6-channel VCSEL arrays were fabricated on the same wafer (separated by ~1 mm) and characterized at RT and 85°C by CHALMERS University of Technology. The arrays were designed for direct butt-coupling to the outer six cores of an MCF provided by OFS, where seven 26 μm diameter graded index cores are arranged in a hexagonal array with 39 μm center-to-center spacing. The version 1 array (v1) consists of six 24 μm diameter top mesas (etched through the p-DBR) matched to the MCF on top of 30 μm diameter bottom mesas (etched through the n-DBR to the n-contact layer).

In the version 2 array (v2), the same diameter and geometry top mesas are placed on a large, common 125 μm diameter bottom mesa. Both VCSEL arrays are planarized with BCB and have a common ground (cathode) for all VCSELs. A ground-signal-ground (GSG) 80 x 80 μm^2 contact pad configuration with 100 μm pitch is used

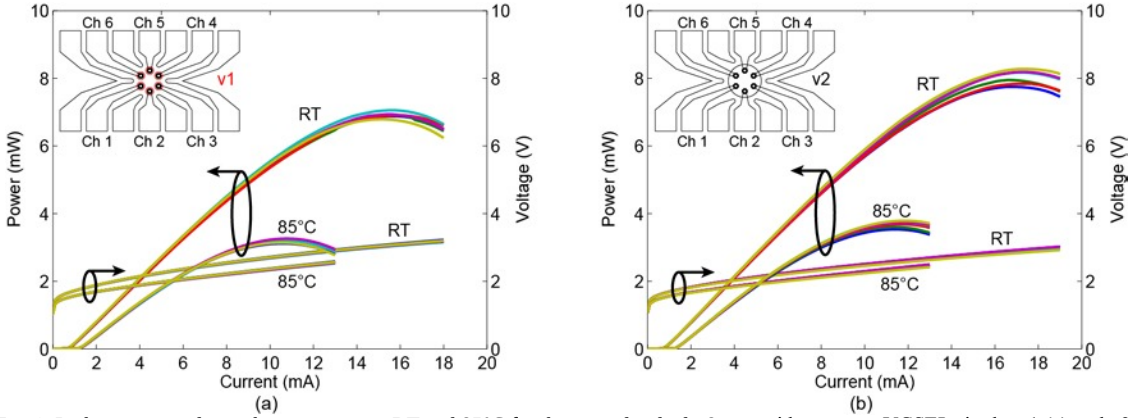


Fig. 1. Light-current-voltage characteristics at RT and 85°C for the six individual ~8 μm oxide aperture VCSELs in the v1 (a) and v2 (b) arrays. Insets: schematic layout of the respective hexagonal VCSEL array and contact pads.

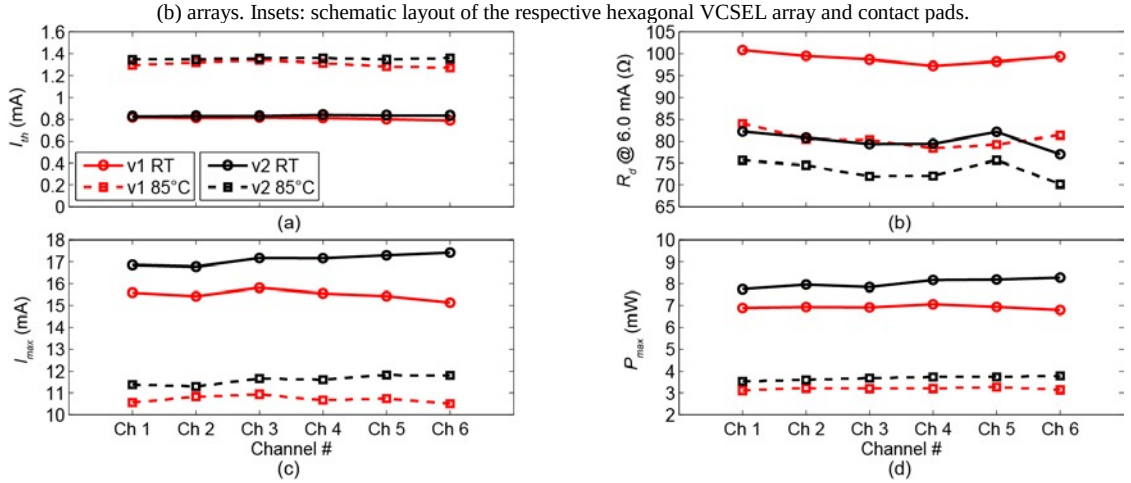


Fig. 2. (a) Threshold current, (b) differential resistance at 6.0 mA, (c) rollover current, and (d) maximum output power for the six individual VCSELs of the v1 and v2 arrays at RT and 85°C.

to enable on-chip contacting of individual VCSELs using a standard GSG RF probe or simultaneous contacting of VCSELs 1-3 or VCSELs 4-6 using a GSGSGSG three channel multiprobe. The two hexagonal array layouts and contact pad configurations, where final chip size is 720 x 420 μm^2, are illustrated in the insets of Fig. 1.

Fig. 1(a) and (b) show the light-current-voltage (LIV) characteristics for the individual ~8 μm oxide aperture diameter multimode VCSELs. The LIV curves reveal uniform performance within the arrays with a power variation < 0.5 dB over the entire current range, regardless of temperature. Fig. 2 plots the threshold current (I_{th}), the differential resistance (R_d) at 6.0 mA bias, the rollover current (I_{max}), and the maximum output power (P_{max}) for all VCSELs of both arrays at RT and 85°C. I_{th} is approximately the same for both array types and uniform over all VCSELs, indicating that the oxide aperture diameter is the same, irrespective of VCSEL and array type. Fig. 2(b) reveals that R_d is notably higher for the VCSELs in the v1 array at RT. This is probably due to that the 30 μm diameter bottom mesas in v1 are small enough for the heterobarriers in the n-DBR to contribute significantly to the total VCSEL resistance. With the temperature increased to 85°C, transport of electrons over the barriers in the n DBR is facilitated. The difference in resistance between v1 and v2 VCSELs is then reduced as the temperature induced reduction of mobility causes transport of holes through the oxide aperture in the p-DBR to become the dominating source of resistance for both design. Higher R_d has implications for the performance of the v1 VCSELs as more power is being dissipated as heat. This manifests itself in a lower I_{max} and P_{max} for v1, as seen in Fig. 2(c) and (d).

Fig. 3 shows the RT small signal modulation response for the channel 1 VCSEL in both arrays at increasing bias currents. The maximum 3 dB bandwidth for all VCSELs at RT and 85°C is displayed as insets. Again, the performance is uniform across the arrays. The v2 VCSELs reach a slightly higher maximum bandwidth than the v1 VCSELs: the mean maximum bandwidth is 21.6 GHz at RT for v2 compared to 20.8 GHz for v1. This is because of the delayed thermal saturation of the v2 VCSELs with respect to the v1 VCSELs (higher I_{max} and P_{max}). However, since the resonance frequency (f_r) scales sublinearly with output power, and since gain compression effectively reduces f_r at high photon densities, the net improvement in maximum bandwidth compared to v1 is only minor. compared to v1 is only minor.

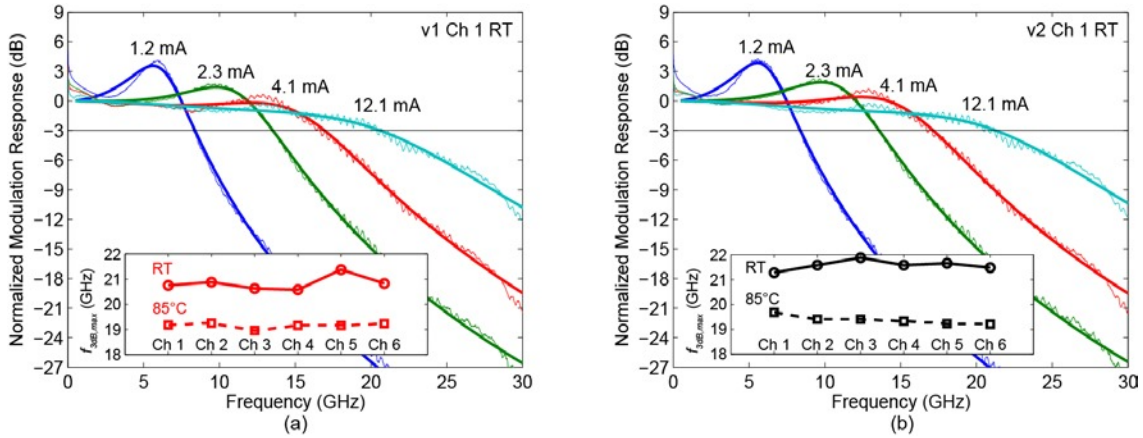


Fig. 3. Measured small signal modulation response (S_{21}) at RT for increasing bias currents for the v1 channel 1 VCSEL (a) and for the v2 channel 1 VCSEL (b). Insets: the extracted maximum 3 dB modulation bandwidth for the individual VCSELs at RT and 85°C for the v1 (a) and v2 (b) arrays.

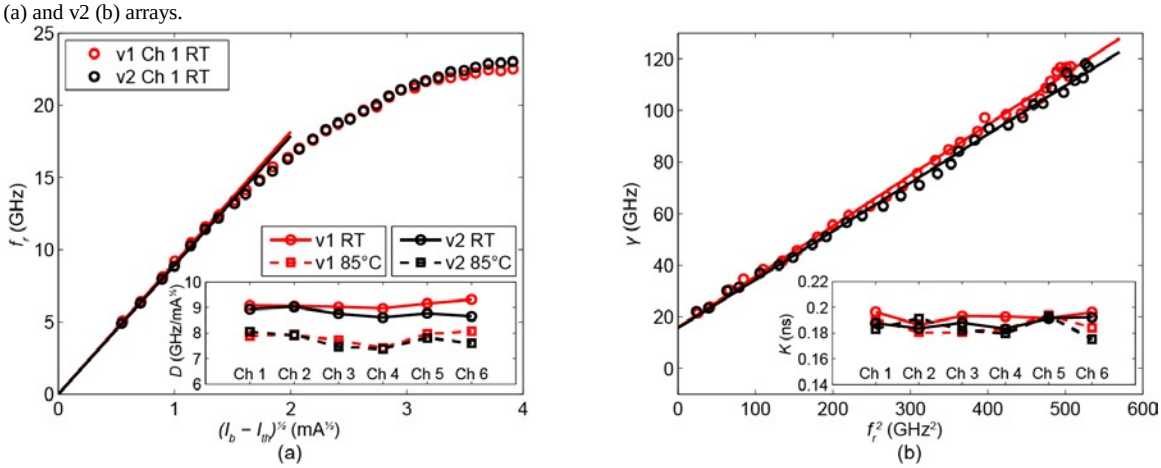


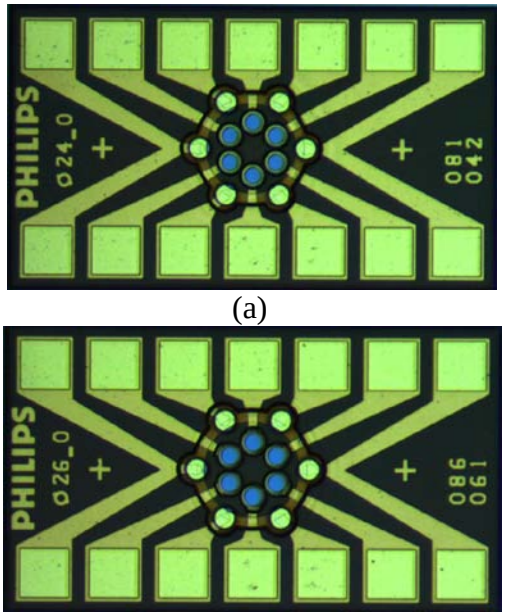
Fig. 4. (a) Resonance frequency (f_r) versus square root of bias current (I_b) above threshold for the v1 and v2 channel 1 VCSELs at RT with the inset showing the *D*-factor for channel 1-6 VCSELs at RT and 85°C. (b) Damping rate (γ) versus resonance frequency squared for the v1 and v2 channel 1 VCSELs at RT with the inset showing the *K*-factor for channel 1-6 VCSELs at RT and 85°C.

Fig. 4(a) plots f_r as function of the square root of bias current above threshold for the channel 1 VCSEL of the v1 and v2 VCSEL arrays. The figure also shows the zero intercept linear fit used to extract the *D*-factor which is plotted for all VCSELs in the arrays at RT and 85°C in the inset. Also the *D*-factor is uniform over the arrays. It is approximately the same for v1 and v2 (within measurement and fitting error), which is to be expected as the fits are made to the linear part of the curve, before f_r begins to saturate.

Fig. 4(b) shows the damping rate (γ) plotted against resonance frequency squared at RT for the channel 1 VCSEL of the v1 and v2 arrays together with linear fits to extract the *K*-factor. The inset shows the extracted *K*-factors for all VCSELs in the arrays at RT and 85°C, revealing uniform characteristics within the arrays and very similar values for v1 and v2. As has been previously observed, the *K*-factor is relatively insensitive to temperature variations.

III. 6-CHANNEL MULTI-CORE PD ARRAYS

Arrays of high speed photodiodes (PDs) matched to the multi-core fiber (MCF) geometry were designed, fabricated, and characterized in Philips ULM during the first year of the MERLIN project for 25 Gbps data transmission. Microscope images of typical 24 µm and 26 µm PD arrays after processing are shown in the figure below.



(a)

(b)

Fig. 5 Microscope views of typical (a) 24 µm and (b) 26 µm PD arrays.

PD array characterization involved an automated static measurement on one element per array for all arrays on the wafer to extract parameters such as dark current and responsivity at 25°C and 85°C.
Dark current at 25°C and bias voltage of -2 V is measured to be as low as 10-20 pA for a 26 µm PD. However, dark current is highly temperature dependent and at 85°C can be as high as ~200 pA at -2 V and 1-2 nA at higher bias voltages.

PD responsivity is given by the ratio of the measured photocurrent to the power of the incident laser beam on the PD surface. This parameter is estimated to be around 0.6 A/W and is relatively temperature independent.

High speed performance of PDs was tested by measuring S_{21} to extract the bandwidth and its uniformity over the array elements as well as S_{11} to estimate the equivalent circuit model (ECM) elements which can be used to model the load behavior of the PD for transimpedance amplifier (TIA) design.

PD bandwidth is directly measured by illuminating the PD surface by a high speed modulated VCSEL. The VCSEL used in this measurement has an approximately 17 GHz 3dB bandwidth and thus set a limit to the frequency response measurement of PDs. This limitation can somehow be compensated by subtracting the VCSEL frequency response from the total measured response. Figure 6 shows measured frequency responses of the VCSEL and PD pair at different bias voltages along with the compensated response at -5 V.

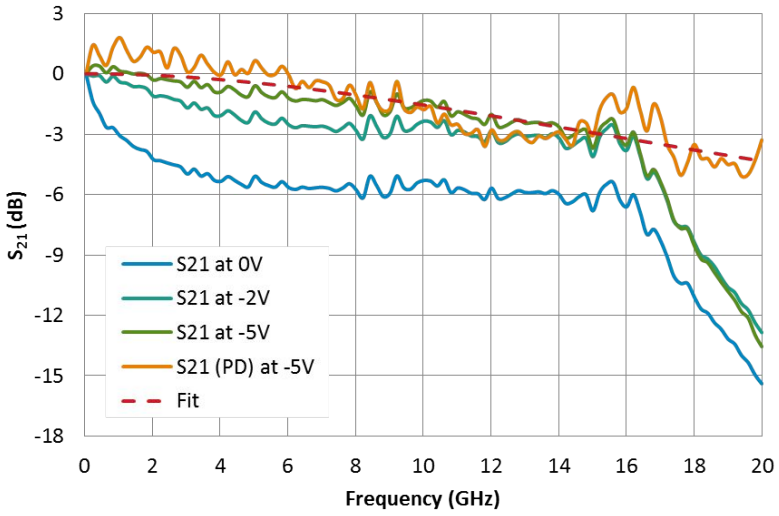


Figure 6 Frequency response of one channel within a 26 µm PD array at 25°C.

IV. ACKNOWLEDGMENT

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V. REFERENCES

[1] Online: http:// www.space-merlin.eu