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A RF-DAC based 40 Gbps PAM Modulator with 1.2 pJ/bit Energy Efficiency at Millimeterwave Band

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Abstract—A PAM-4 modulator is designed and fabricated in a 0.25 μm indium phosphide (InP) double heterojunction bipolar transistor (DHBT) technology. The modulator is verified to have a 3-dB bandwidth of 60-90 GHz and a peak output power of -5 dBm at 75 GHz. This modulator can support 40 Gbps data transmission with a bit error rate of $3.7 \times 10^{-6}$, the energy efficiency is better than 1.2 pJ/bit. This modulator is suitable for application such as low power, short range, ultra high data rate wireless communication.

Index Terms—Modulator, pulse amplitude modulation, InP, DHBT, RF-DAC, energy efficiency, wide-band, internet of things

I. INTRODUCTION

The era of integrated internet of things (IoT) has arrived, most of electronic products already featured with wireless connectivity in one way or another. This great rush to make devices wireless has produced a flood of different wireless technologies and protocols. Nevertheless, high data rate wireless connection is urgently needed even at short distance, to move data from one device to another. One of the major consideration of short distance connectivity is the power consumption, due to the fact that most mobile devices are battery driven. High data rate wireless link would reduce the transmission time and reduce the on-time of the transceiver therefore enables longer operation time of the device.

Millimeterwave bands can offers wide available bandwidth which can support ultra high data rate transmission beyond 10 Gbps. A 25 Gbps transmission is demonstrated at 113 GHz with 0.38 pl/bit [2] using On-Off Keying modulation. A 12 Gbps data transmission at 80 GHz band was presented with 4.5 pJ/bit energy efficiency. In this paper, a 40 Gbps data transmission is presented using pulse amplitude modulation (PAM) modulation. A wide band PAM modulator is designed and fabricated in a 0.25 μm InP DHBT process. This modulator has a 3-dB bandwidth of 30 GHz centred at 75 GHz and consumes 47 mW power which yields a energy efficiency of less than 1.2 pJ/bit. The proposed modulator can be used for short distance device to device communication and/or board-to-board communication via plastic waveguide [1].

The paper is structured as following: after introduction, the circuit design detail is presented in section II; the measurement setup and result in frequency- and time-domain are given in section III; section IV is the conclusion and discussion.

II. DESIGN OF THE RF-DAC

A wide band operation high data rate RF-DAC is designed and fabricated using indium phosphide (InP) double hetero-junction bipolar transistor (DHBT) technology with 0.25 μm emitter width developed by the Teledyne Scientific Company. Transistors can operate at an emitter current density of up to 12 mA/μm² with a maximum collector-emitter voltage of 2 V. Measurements on a 10 μm emitter length transistor indicate an extracted of $f_t$ and $f_{max}$ of 350 and 600 GHz and minimum noise figure of 4.3 dB. To enable low power operation, the design topology adopts emitter coupled pair (ECP) as adjustable attenuator. By using two of such ECP structure, the local oscillator (LO) input can be converted into PAM modulated millimeterwave output. The ECP structure can regulate the output amplitude at a high switching rate (high data rate) as well as ensure good output linearity for PAM operation. The simplified schematic of the proposed modulator is illustrated in Fig. 1. Two ECP structures are used for most significant bit (MSB), D0, and the least significant bit (LSB) D1 respectively. The ECP for MSB includes transistor E1-E4 (transistor size: 3 μm for E1 and E4, 8 μm for E2 and E4), and the transistors E5-E8 (transistor size: 3 μm for all) are used for LSB. The LO input signal is given at the base of E1 and E5, while both E1 and E5 are configured as emitter followers, R7=R9=100 Ohm are used to achieve wide band matching after power split.

Figure 1. A simplification of the schematic that is used for the RF-DAC

The design of the RF-DAC is based on using differential pairs as a way to control the output power of the signal. The process using InP-based DHBTs is chosen due to the wide bandwidth and high power handling capability, as well as a low noise figure. The advantages of this technology makes it possible to get a high signal-to-noise ratio which is required to be able to utilize the advantages of PAM4 modulation without
compromising the bit rate. The result is a high-data rate, power efficient as well as wide band operational modulator. When MSB bit '1' (0 V as logic '0' and 0.3 V as logic '1') is presented at the base of E4, it would steer the current away from E2 therefore reduce the output amplitude. Similar mechanism is applied to the other ECP, however with scaling of the transistor E6 and E7 act as LSB. The collectors of E2 and E6 are connected and shared a common inductor L1 (realized by a 240 µm microstrip line) to generate RF output. The photo of the fabricated MMIC is shown in the Fig. 2.

![Fig. 2. The photo of the RF-DAC. The chip size is 800µm x 800µm.](image)

III. MEASUREMENT RESULTS

A. Frequency Domain Measurement

The proposed modulator is verified in frequency domain using Anritsu VectorStar Vector Network Analyzer (VNA) ME7838A. A continuous sinusoidal wave is provided at the LO input port of the modulator, the frequency is swept from 30 to 130 GHz at a constant -5 dBm power level. The output power is monitored when different binary code is presented at the data input ports. The measured output power versus frequency is shown in Fig. 4. It can be seen the operational bandwidth of this modulator covers 55-100 GHz and at 75 GHz, the modulator gives maximum -6.2 dBm output power under 0 dBm LO drive. With different input bits the output power is attenuated, comparing the output power difference between data '11' and data '00' are modulated, it can be seen that this modulator yields 10-dB dynamic range (DR) between 30-70 GHz. Simulation result at LO=75 GHz is also given in Fig. 5, where MSB (D0) voltage is swept with different LO driven power. The output power level is monitored and plotted. The DR is about 7 dB at 75 GHz which agrees with measurement result.

The matching at the LO port (denote as S11) and the output matching at the RF port (denote as S22) are measured using the same setup. The measurement result is plotted in Fig. 3.

![Fig. 3. Measured input and output matching at LO and RF port](image)

B. Time Domain Measurement

The modulator is also on-wafer tested in time domain measurements on a probe station. A Keysight M8195A arbitrary waveform generator (AWG) is used to provide binary data input to the modulator and a Lecroy LabMaster 10-100Zi real-time oscilloscope is used to capture output RF signal.

![Fig. 4. Measured output power at different frequencies with different digital input](image)

![Fig. 5. Simulated output power for different data input voltages of the MSB, with different input power (LO). The LSB is set to 0 V and the LO frequency is 75 GHz.](image)
The modulator is first tested as amplitude shift keying (ASK) modulator. A single PRBS-9 binary stream from AWG is fed into the modulator MSB port, the output is captured by the oscilloscope when LO=50 GHz. The data rate of the PRBS-9 stream is change from 10 Gbps up to 20 Gbps and bit-error-rate (BER) is measured using the oscilloscope. The BER of 20 Gbps transmission is measured to be $1.2 \times 10^{-8}$. The time domain waveform of the 20 Gbps ASK RF signal is plotted in Fig. 6 and the received constellation diagram is shown in Fig. 7(a). The modulator is also tested for PAM-4 signal generation. Two independent binary streams (a PRBS-9 and a PRBS-10) are input to the MSB and LSB ports on the modulator. The symbol rate of the PAM-4 signal is changed from 10 Gbaud up to 20 Gbaud. For 20 Gbaud, PAM-4 signal support a data rate of 40 Gbps with a symbol error rate (SER) of $3.7 \times 10^{-6}$ and the received constellation diagram is shown in Fig. 7(b).

![Fig. 6. Measured 20 Gbps ASK modulated waveform in time-domain at 50 GHz center frequency](image)

**TABLE I**

<table>
<thead>
<tr>
<th>Technology</th>
<th>Frequency (GHz)</th>
<th>Data Rate (Gbps)</th>
<th>Energy Eff. (pJ/bit)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 nm InGaAs</td>
<td>113</td>
<td>25</td>
<td>0.38</td>
<td>[2]</td>
</tr>
<tr>
<td>HEMT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65 nm HEMT</td>
<td>77</td>
<td>12</td>
<td>0.75</td>
<td>[3]</td>
</tr>
<tr>
<td>CMOS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.25 μm InP</td>
<td>100-150</td>
<td>14</td>
<td>3.35</td>
<td>[4]</td>
</tr>
<tr>
<td>DHBT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50 nm InP</td>
<td>87.8-98.2</td>
<td>18</td>
<td>5.6</td>
<td>[5]</td>
</tr>
<tr>
<td>mHEMT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65 nm CMOS</td>
<td>80</td>
<td>12</td>
<td>4.5</td>
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<tr>
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<td>11.5</td>
<td>1.1</td>
<td>[7]</td>
</tr>
<tr>
<td>0.25 μm InP DHB</td>
<td>60-90</td>
<td>40</td>
<td>1.2</td>
<td>This Work</td>
</tr>
</tbody>
</table>

IV. DISCUSSION AND CONCLUSION

In Table. I, the modulator presented in this paper is compared with previously reported high data rate modulators. It can be seen from [3], [7] that good energy efficiency can be achieved with CMOS process. A state-of-the-art energy efficiency is achieved in [2] with a 50 nm HEMT processes.

![Fig. 7. Received constellation diagram after demodulation: (a) 20 Gbps ASK; (b) 40 Gbps PAM-4](image)

This work presents a modulator with highest data rate of 40 Gbps as well as a competitive energy efficiency of 1.2 pJ/bit.

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REFERENCES