Electrical properties of 4H-SiC MIS capacitors with AlN gate dielectric grown by MOCVD

Solid State Electronics 153 (2019) 52–58

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Electrical properties of 4H-SiC MIS capacitors with AlN gate dielectric grown by MOCVD

R.Y. Khosa[a,b], J.T. Chen[c], K. Pálsson[a], R. Karhu[c], J. Hassan[c], N. Rorsman[d], E.Ö. Sveinbjörnsson[a,c,*]

[a] Science Institute, University of Iceland, 107 Reykjavik, Iceland
[b] Department of Physics, University of Education Lahore, Dera Ghazi Khan Campus, 32200 D. G. Khan, Pakistan
[c] Department of Physics, Chemistry and Biology (IFM), Semiconductor Materials Division, Linköping University, SE-58183 Linköping, Sweden
[d] Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Göteborg, Sweden

ARTICLE INFO

The review of this paper was arranged by Prof. A. Zaslavsky

Keywords:
MIS capacitors
Gate dielectrics
AlN/4H-SiC interface

ABSTRACT

We report on the electrical properties of the AlN/4H-SiC interface using capacitance- and conductance-voltage (CV and GV) analysis of AlN/SiC MIS capacitors. The crystalline AlN layers are made by hot wall MOCVD. CV analysis at room temperature reveals an order of magnitude lower density of interface traps at the AlN/SiC interface than at nitrided SiO_2/SiC interfaces. Electron trapping in bulk traps within the AlN is significant when the MIS capacitors are biased into accumulation resulting in a large flatband voltage shift towards higher gate voltage. This process is reversible and the electrons are fully released from the AlN layer if depletion bias is applied at elevated temperatures. Current-voltage (IV) analysis reveals that the breakdown electric field intensity across the AlN dielectric is 3–4 MV/cm and is limited by trap assisted leakage. By depositing an additional SiO_2 layer on top of the AlN layer, it is possible to increase the breakdown voltage of the MIS capacitors significantly without having much impact on the quality of the AlN/SiC interface.

1. Introduction

4H-Silicon carbide (SiC) can be thermally oxidized to yield its native silicon dioxide (SiO_2) but the drawback is a rather poor interface quality of the SiO_2/SiC interface. This results in a low electron channel mobility in 4H-SiC MOSFETs due to electron trapping and scattering at the interface. The quality of the SiO_2/SiC interface has been improved by various oxidation and nitridation methods which has enabled the commercialization of high voltage (> 900 V) MOSFETs [1–3]. These high voltage devices can tolerate lower channel mobilities than the low voltage ones because the current there is limited by the resistance of the low doped SiC used in these devices. However, for low voltage devices a further reduction in the interface state density near the SiC conduction band edge is needed to achieve an acceptable electron channel mobility. In an attempt to overcome this limitation, various high-*k* gate dielectrics (e.g. Al_2O_3, HfO_2, AlN) are being explored for SiC metal-insulator-semiconductor (MIS) technology [4–12]. The wide bandgap (~6.2 eV) AlN is a potential substitute for SiO_2 in SiC MIS devices [13–15]. The lattice mismatch between SiC and AlN is less than 1%, which enables a single crystalline growth of AlN films on SiC substrates [16]. AlN has been investigated on 4H-SiC and the reported conduction and valence band offsets are 1.7 eV and 1.3 eV respectively as determined by X-ray photoelectron spectroscopy (XPS) [17]. SiC MISFETs with crystalline AlN as a gate dielectric grown by molecular beam epitaxy (MBE) have been reported but the structures were leaky and the channel mobility was very low (< 1 cm^2/Vs) [10]. A channel mobility of 10–20 cm^2/Vs is recorded for 6H-SiC MISFETs with MBE grown AlN dielectric layer while an excessive gate leakage is recorded as well most likely due to relaxation of the AlN film [18]. Pre-treatment of the SiC substrate by HCl gas etching and by atomic nitrogen irradiation before AlN growth have been used to improve the quality of AlN films grown by MBE [6,19]. A crystalline AlN has also been grown by MOCVD on both 4H- and 6H-SiC but studies showed a high density of fixed charge within the AlN and high density of interface traps [8,16].

In this study, we grow crystalline AlN by hot wall MOCVD on n-type 4H-SiC. This method has provided high quality AlN nucleation layers for GaN growth [20,21]. In addition, we investigate the effect of adding other wide bandgap dielectrics on top of the AlN layer. The interface traps at the AlN/4H-SiC interface are investigated by capacitance-voltage (CV) measurements on MIS capacitors. The AlN samples are found to be sensitive to electron injection during accumulation bias stress and the emission of trapped electrons is carefully examined by CV measurements using depletion bias stress at elevated temperatures. Furthermore, the dielectric breakdown properties are extracted from

* Corresponding author at: Science Institute, University of Iceland, 107 Reykjavik, Iceland.
E-mail address: einars@hi.is (E.Ö. Sveinbjörnsson).

https://doi.org/10.1016/j.sse.2018.12.016
Received 29 September 2018; Received in revised form 29 November 2018; Accepted 17 December 2018
Available online 18 December 2018

current-voltage (IV) measurements. We find that the AlN/4H-SiC interface contains very low density of interface traps and the detrimental traps observed at the SiO_2/4H-SiC interface are practically absent at the AlN/4H-SiC interface.

2. Experimental methods

The SiC MIS samples used in this study have 10 μm thick n-type epitaxial layers with a net doping concentration of $\sim 1 \times 10^{16}\,cm^{-3}$ grown on 4 degrees off-axis (0 0 0 1) highly doped n-type 4H-SiC substrates. The dielectric is AlN either as a single layer or in a stack with SiO_2, Al_2O_3 or Si_3N_4. The purpose of using dielectric stacks is to compare the leakage properties and electron injection into such stacks to a single layer AlN. The single crystalline AlN layer was grown in a horizontal hot-wall MOCVD reactor at 1100 °C [20,21]. Ammonia and $Al_2(CH_3)_6$ are used as a precursor for nitrogen and aluminium respectively. Prior to the growth, the SiC surface was exposed in H_2 ambient at 1320 °C, in order to obtain an oxide-free surface. The details of the SiC surface cleaning and AlN growth process are given in Ref. [21]. The morphology of the AlN/SiC samples was characterized by atomic force microscopy (AFM). Afterwards, the additional layers of SiO_2, Al_2O_3 or Si_3N_4 were deposited by different methods. The SiO_2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) at 300 °C using source gases of nitrous oxide and silane. The Al_2O_3 was grown by atomic layer deposition (ALD) at 300 °C via thermal decomposition of $Al_2(CH_3)_6$ in water ambient. In addition, Si_3N_4 layer was made by low pressure chemical vapor deposition (LPCVD) at 770 °C using source gases of ammonia and chlorosilane. The MIS capacitors were made by sputtering 0.5 μm thick aluminum as a gate metal, patterned by lithography and etching to form circular capacitors. Aluminum served as a backside contact as well.

The MIS samples investigated are summarized in Table 1. Reference samples with 32 nm or 37 nm thick SiO_2 grown in dry oxygen or in N_2O at 1240 °C were analyzed. Nitrided oxides (made by oxidation or annealing in N_2O or NO ambient) are the currently used gate dielectrics in SiC MOSFETs [3]. Another reference SiO_2 film was investigated which was made by intentional sodium contamination typically called sodium enhanced oxidation (SEO). Such oxides contain very low densities of interface traps but mobile sodium ions present within the oxide prevents their practical use in SiC MOSFETs [22]. In the SEO method, a 100 nm oxide was grown in O_2 ambient at 1240 °C and densified in nitrogen medium at 1000 °C for 5 h. This whole oxidation process was performed in alumina furnace tube with carrier boat made of sintered alumina. The alumina contains trace amounts of sodium which are responsible for increase in oxidation rate and for the reduction of interface traps [22]. All the reference samples were cleaned with HF for 1 min, prior to the deposition of SiO_2, in order to remove the native oxide of SiC.

CV measurements are performed on 300 μm circular Al pads of each sample using an Agilent E4980A LCR meter. The test frequencies were between 1 kHz and 1 MHz. Traps in a dielectric are generally classified into interface, near-interface (or border) and bulk traps with respect to their location in dielectric [23]. These traps can easily be detected by performing CV measurements under different conditions. The first estimate of the number density of interface and near-interface states in MIS capacitors is done by investigating the frequency dispersion of the CV curves. Electron capture into interface states is most often a fast process while electron emission from interface traps is normally much slower and is a thermal process which depends on the difference $E_c - E$ (where E is the energy level of the interface trap and E_c denotes the SiC conduction band edge). If an electron is captured and not emitted again this is detected as a shift of the CV curve to higher gate voltages. If the test frequency is high (1 MHz) then more traps will not emit their electrons and the curve is shifted to higher gate voltage as compared to the low frequency (1 kHz) curve [24]. Our samples have bulk traps as well that are located some distance into the dielectric and capture electrons from the semiconductor during accumulation bias stress which is detected as a shift in the CV curves. The trapped electrons do not return unless the temperature is raised and reverse electric field is applied for a long-time period. The number density of trapped electrons can be determined by using the expression [24]:

$$N_{it} = \frac{C_d(V_{FB(f)} - V_{FB(s)})}{qA} \quad (1)$$

where $V_{FB(f)}$ and $V_{FB(s)}$ are the flatband voltages of a fresh and of a stressed MIS sample respectively, C_d is the dielectric capacitance and A is the area of the circular MIS capacitor.

IV measurements are made on 100 μm circular pads of sample 1 and sample 3 as well as on reference MIS samples using Keithley 617 electrometer. IV is used to determine the dielectric breakdown strength and the tunneling barrier height of these samples. All CV and IV measurements are performed in vacuum of 10^{-3} mbar in liquid nitrogen cooled cryostat.

3. Results and discussion

3.1. Density of interface traps at the AlN/SiC interface

CV is performed to estimate the density of interface traps at the AlN/SiC interface. Fig. 1 shows room temperature CV spectra for AlN MIS samples 1 (10 nm AlN) and 3 (40 nm SiO_2/10 nm AlN). These n-type MIS capacitors show a clear accumulation at positive voltages and depletion for negative voltages. The relative dielectric constant for AlN deduced from the accumulation capacitance is ~8.7. The flatband voltage is ~0.7 V which is close to the theoretical flatband voltage (i.e. ~0.4 V) which shows that initially the AlN layer contains insignificant amount of fixed charge. Here, CV data is shown for test frequencies between 1 kHz and 1 MHz and there is virtually no frequency dispersion in both samples which indicates that the single layer AlN and the SiO_2/AlN stack both contain low density of interface states. Leakage is observed in sample 1 above gate voltage of 3 V corresponding to an electric field intensity of approximately 3 MV/cm across the AlN while the MIS capacitor with stacked dielectric, sample 3, shows no leakage up to 40 V gate bias (maximum bias for the CV meter).

Fig. 2 shows the density of interface states as a function of energy near the SiC conduction band edge extracted from room temperature CV measurements for (a) single AlN layers and for (b) samples with dielectric stack along with three reference SiO_2 MIS capacitors. Fig. 2a

Table 1
MIS devices used in this study.

No.	MIS structures	Thickness of dielectrics	Method of dielectric deposition
1	Al/AlN/SiC	10 nm	MOCVD at 1100 °C
2	Al/AlN/SiC	30 nm	MOCVD at 1100 °C
3	Al/SiO_2/AlN/SiC	40 nm/10 nm	PECVD at 300 °C/MOCVD at 1100 °C
4	Al/SiO_2/AlN/SiC	40 nm/10 nm	PECVD at 300 °C then annealed at 900 °C for 30 min/MOCVD at 1100 °C
5	Al/Al_2O_3/AlN/SiC	40 nm/10 nm	ALD at 300 °C/MOCVD at 1100 °C
6	Al/Si_3N_4/AlN/SiC	40 nm/10 nm	LPCVD at 770 °C/MOCVD at 1100 °C
7	Al/SiO_2/Si_3N_4/AlN/SiC	10 nm/40 nm/10 nm	PECVD at 300 °C/LPCVD at 770 °C/MOCVD at 1100 °C

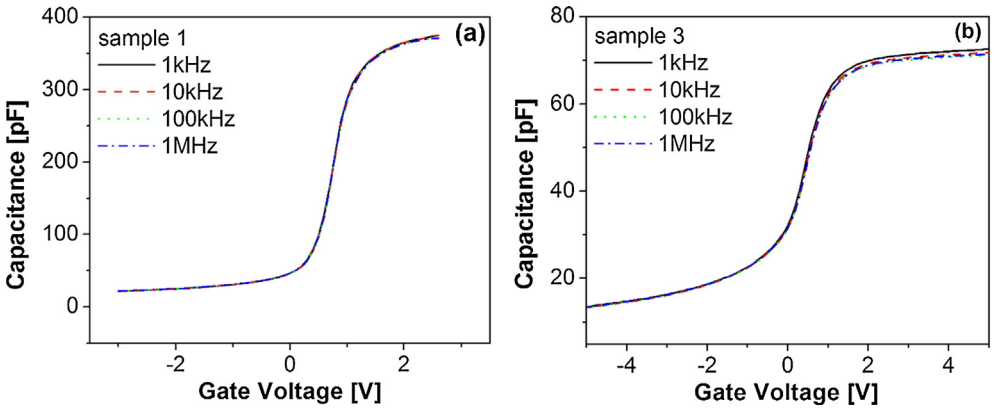

Fig. 1. Room temperature CV curves for (a) sample 1 (AlN 10 nm) and (b) sample 3 (40 nm SiO_2/10 nm AlN) at four test signal frequencies between 1 kHz and 1 MHz.

shows that sample 1, with a 10 nm thick layer AlN, has the lowest interface trap density compared to the SiO_2 reference samples. The detrimental interface states that exist within this energy range for all thermally grown oxides are practically absent at the AlN/SiC interface. The thermal oxide made in the presence of Na (labeled Na in Fig. 2) has very low density of interface states and the field effect mobility in MISFETs made with this oxide is ~150 cm^2/Vs which is among the highest reported [22].

Fig. 2a also shows that the thickness of the AlN affects the AlN/SiC interface quality. Sample 2 with a 30 nm thick AlN layer has higher density of interface states than the 10 nm thick sample but nevertheless much lower than in the thermal oxide samples. This may be connected to the different morphology of the 10 nm and 30 nm AlN layers, as shown in Fig. 3. This is not surprising since the density of misfit dislocations increases with increasing AlN thickness and above approximately 30 nm they can cause a deterioration of the insulating properties of AlN films in MIS devices [25].

It is clear in Fig. 2b that the dielectric stack does in general have higher interface state densities than a single AlN layer (by comparing with Fig. 2a). So, the addition of different dielectric layers on the top of AlN affects the AlN/SiC interface quality. The Si_3N_4/AlN stack (sample 6) has the highest interface trap density. This can be a result of the high temperature (770 °C) growth of Si_3N_4. The SiO_2/AlN stack (sample 3) has the best result for a stack in terms of density of interface states and is comparable to a 30 nm single AlN layer (sample 2 shown in Fig. 2a). It is evident by comparing Fig. 2a and b that sample 1 with 10 nm single AlN layer has the lowest interface trap density compared to all the AlN samples investigated including the SiO_2 reference samples.

Fig. 4a shows 100 kHz GV curves for sample 3 performed at 298 K and 77 K. In the GV profile, the conductance peak occurs near flatband conditions and is due to response from interface traps near the fermi level [24]. The conductance peak height gives a rough estimate of the density of interface traps near the fermi level. There is a striking difference in the height of the conductance peak at 298 K and 77 K. This indicates that the AlN sample has very fast shallow traps, located close to the SiC conduction band edge, which escape detected during CV at room temperature. Therefore, the interface trap density was also extracted from CV data at 77 K and the result is shown in Fig. 4b. At 77 K, a high density of interface traps is seen in all AlN MIS samples. The AlN samples even have higher shallow trap density than the reference SiO_2 samples. The interface trap density results of the AlN samples expressed in Figs. 2 and 4b (for 298 K and 77 K respectively) show good agreement with the conductance peak height observed in Fig. 4a. The impact of these shallow traps on channel mobility in MISFETs is not known but they are very fast at room temperature compared to the detrimental interface traps at the SiO_2/SiC interface.

3.2. Electron injection into AlN

A sensitivity to electron injection is observed in the AlN samples. This is detected as a positive flatband voltage shift in subsequent CV curves when the sample is repeatedly biased into accumulation at room temperature. Bidirectional CV sweeps (not shown) reveal that most of the injected electrons are not released from the AlN when the capacitor is swept to depletion. The voltage hysteresis in such sweeps is only of the order of 100 mV compared to positive flatband voltage shifts of 8 V when the samples are swept to accumulation (see Fig. 5a). Dislocations are reported to appear in AlN films thicker than 6 nm [25]. In our case the thickness is 10 nm so this flatband shift can be a result of trapping of electrons in dislocations or deep level defects within the AlN [26,27]. Similar electron injection is also observed in the dielectric stacks containing AlN. The trapped electrons are released back to the SiC if

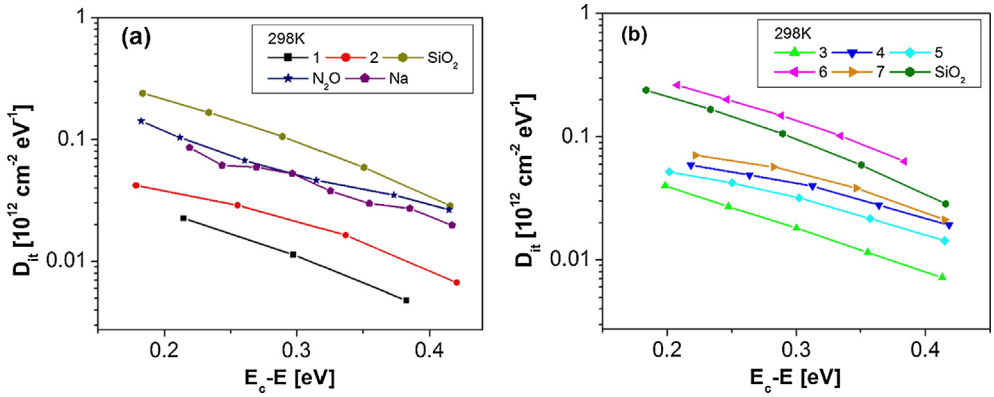

Fig. 2. Comparison of the density of interface states (D_{it}) estimated from CV measurements (at 298 K) as a function of energy for (a) single AlN layers and for (b) AlN stack MIS capacitors along with reference SiO_2 MIS capacitors.

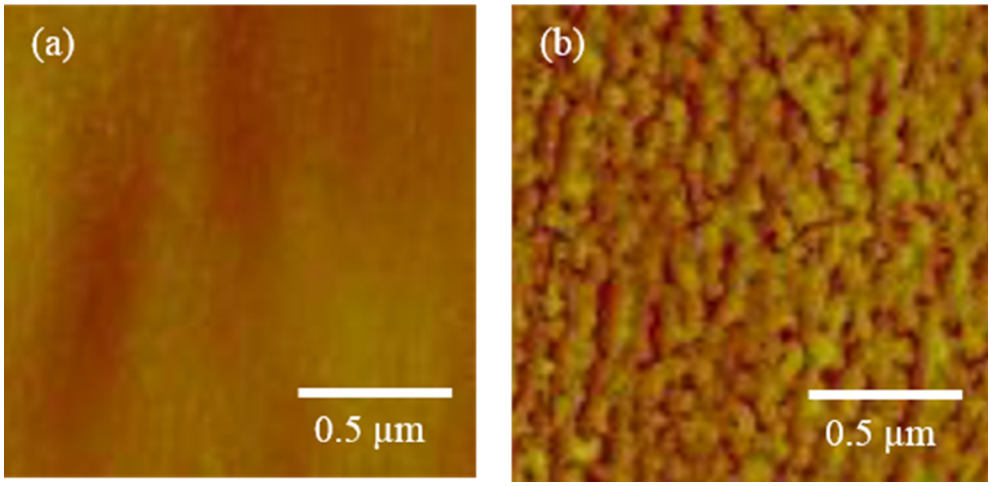

Fig. 3. AFM images of the AlN layers with the thickness of 10 nm (a) and 30 nm (b) grown on the SiC substrate.

depletion bias is applied to the MIS capacitors at elevated temperatures.

Fig. 5a and b show the electron injection into the AlN layer in sample 3 at room temperature and at 77 K respectively. The shift of the CV curve saturates after several gate voltage sweeps from depletion to accumulation (−10 V to 10 V respectively). However, the magnitude of the shift depends on the maximum applied accumulation voltage (which in this case is 10 V). It is evident that the shift is because of electron capture within the AlN under accumulation bias and the electron do not return when the sample is biased to depletion. It is seen that the shift of the CV curve saturates at lower gate voltage at 77 K (in Fig. 5b) compared to room temperature (in Fig. 5a). This indicates the electron injection to traps within the AlN is temperature dependent. Charge trapping in AlN is commonly reported in literature [8,16]. In our case, the flatband shift after stressing at 298 K and 77 K is here (in Fig. 5a and b) about 8 V and 5 V respectively which corresponds to an effective negative trapped charge of $\sim 4 \times 10^{12}\,cm^{-2}$ and $\sim 2 \times 10^{12}\,cm^{-2}$ respectively. The insets of both figures show that the CV curves coincide if one assumes that the shift is only due to electrons trapped in bulk dielectric traps within the AlN layer. This shows that the observed electron trapping is neither because of interface traps nor near-interface traps since these traps cause stretch in the CV curves that is not seen [28]. The observed positive shift is therefore mainly due to electron trapping in bulk traps within the AlN. The trapped electrons can be completely released back to the SiC by applying a depletion bias (−10 V gate voltage) at elevated temperatures to the MIS capacitor. An example of such an experiment is shown in Fig. 6.

Fig. 6 shows electron re-emission from traps located within the AlN layer. To examine such emission, the experiment is performed in a such way that the traps within the AlN are first intentionally filled with electrons by cooling the sample from room temperature down to 77 K while maintaining an accumulation bias of 20 V on the gate. Thereafter, the subsequent CV sweeps at different temperatures are made from depletion to weak accumulation (< 20 V) at different time intervals after applying a depletion bias stress (−10 V) and the flatband voltage is monitored. This experiment is performed at five different temperatures of 77 K, 250 K, 298 K, 350 K and 390 K applying a depletion bias stress at −10 V to find the temperature needed for the emission of electrons from the traps located within AlN layer. Electron emission from AlN traps starts at room temperature but quickly saturates with time indicating a limited emission of electrons at this temperature. No significant emission is seen for temperatures below 298 K. This suggests that room temperature is only sufficient for emission of electron trapped within the AlN close to the AlN/SiC interface. However, electrons trapped deeper within the AlN layer are emitted back to SiC at higher temperatures which corresponds to larger activation energies. A reliable estimate of the activation energies is not feasible from current data but there is a large spread in the activation energies. Electron trapped further away from the interface should exhibit larger activation energy than electrons located near the AlN/SiC interface [29]. This experiment demonstrates that the net negative charge observed in these AlN layers is not a permanently fixed charge but rather electrons trapped within the dielectric which can be released to the SiC using depletion bias and by raising the temperature of the sample.

A schematic of the interface, near-interface and bulk defects

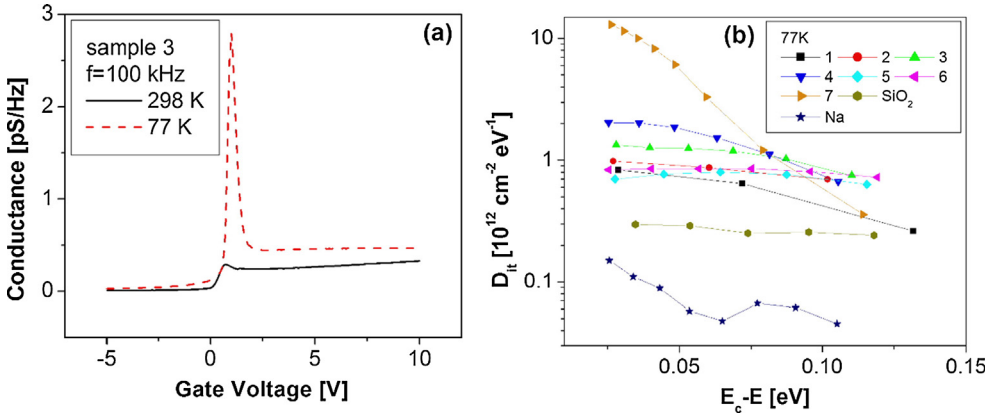

Fig. 4. (a) GV curve (100 kHz) for sample 3 at 298 K and 77 K. (b) Interface state density as a function of energy for AlN and reference SiO_2 MIS capacitors extracted from CV measurements at 77 K.

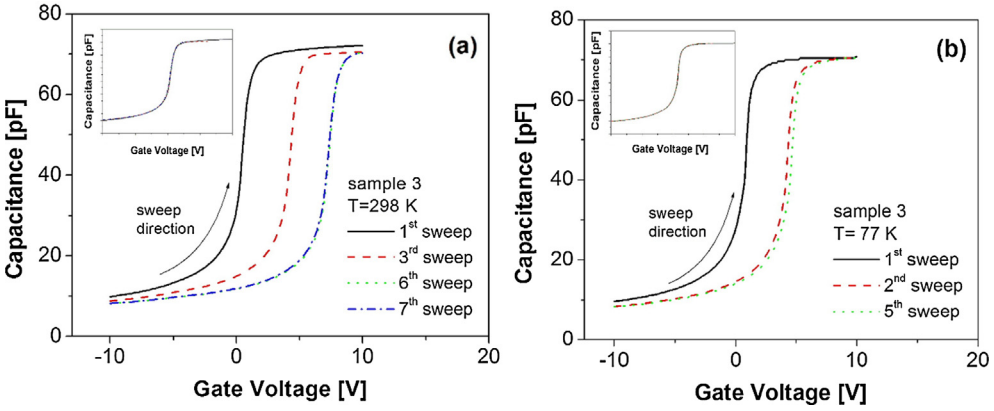

Fig. 5. (a) Subsequent 100 kHz CV sweeps for sample 3 at 298 K, (b) same for sample 3 at 77 K. Electrons are injected into the AlN layer during accumulation bias which is detected as positive flatband voltage shift. The insets of both figures show that the CV curve coincide if the shift in CV is only due to electrons trapped in bulk traps within the AlN layer.

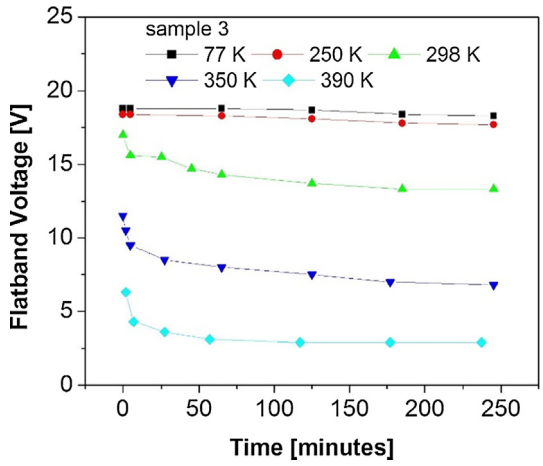

Fig. 6. Electron emission from traps located within the AlN layer. Sample 3 is first in accumulation (20 V on the gate) at room temperature and then cooled to 77 K. After that, subsequent CV sweeps are made from depletion to accumulation at different time intervals and at a given fixed temperature. Flatband voltage versus time plot extracted from the CV sweeps shows that the electrons are re-emitted from the AlN layer and detected as a reverse flatband voltage shift.

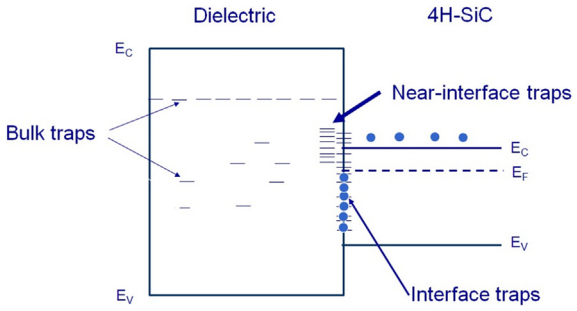

Fig. 7. A schematic of possible interface, near-interface and bulk traps in AlN/4H-SiC samples.

investigated in this study is shown in Fig. 7. The interface traps are located exactly at the AlN/SiC interface. The near-interface traps are located some distance (1–2 nm) inside the dielectric and bulk traps are deep traps within the dielectric [23]. The interface states capture electrons rapidly and their density can be estimated by conventional CV measurement. However, bulk traps are slow traps and the density of trapped electrons in these traps depends strongly on the field across the dielectric [23,24]. The slow and fast interface traps in AlN are detected by conventional CV analysis at room temperature and at low temperature of 77 K respectively (see Figs. 2 and 4). Near-interface traps, if present, are also detected to a certain degree in conventional CV analysis at room temperature. The bulk traps are detected at elevated temperature in the studies shown in Fig. 6.

A brief summary of our CV analysis is that the room temperature CV shows a very low density of interface and near-interface traps at the AlN/4H-SiC interface. However, a high density of shallow interface traps close to the conduction band edge of SiC is observed in low temperature CV measurement. The CV measurements at elevated temperatures after applying depletion bias stress show a high density of bulk traps from unknown origin within the AlN.

3.3. Breakdown properties of AlN and dielectric stacks containing AlN

IV measurements are used to estimate the critical breakdown field and the tunneling barrier height of AlN and its stacks. About 20 MIS capacitors on each sample were investigated with diameters in the range 100–500 μm. The most reliable and reproducible data was obtained for the smallest capacitors (100 μm in diameter) and results of such measurements are shown in Fig. 8. Fig. 8(a) compares the dielectric breakdown field of samples 1 and 3 along with thermally grown dry SiO_2 reference sample based on current density measurement as a function of the electric field intensity (J-E) across the gate dielectric. The single layer AlN (sample 1) shows abrupt leakage with increasing electric field and no clear abrupt breakdown is observed. If one uses the current density needed to obtain breakdown in the other samples as a guideline then the AlN layer can withstand about 3 MV/cm. However, the leakage is already unacceptable above 1 MV/cm and the data suggests that trap assisted leakage through electron injection is causing this behavior. Similar observations are made for sample 2 (not shown).

In Fig. 8(a), IV measurements on sample 3 are done at 298 K and 77 K to see the effect of temperature on the dielectric breakdown. A slight decrease in the current leakage is observed when the temperature is lowered to 77 K. For sample 3 composed of AlN and SiO_2 (room temperature red dashed curve in Fig. 8a), the effective electric field intensity, $E_{eff} = \frac{V_G - V_{FB}}{t_{D,total}}$, if we consider the dual dielectric as a single dielectric [30], is ~8 MV/cm. Here V_G, V_{FB} and $t_{D,total}$ are the gate voltage, flatband voltage and the total thickness of the dielectric stack respectively. The electric field intensity, however, across the required dielectric layer, AlN, in sample 3 is determined by taking into account the mismatch in dielectric constants using the expression: [30]

$$E_{AlN} = \frac{V_G - V_{FB}}{t_{AlN}} \times \frac{C_{ox,SiO2}}{C_{ox,SiO2} + C_{D,AlN}} \quad (2)$$

Here t_{AlN} denotes the thickness of AlN. $C_{ox,SiO2}$ and $C_{D,AlN}$ are the calculated capacitances of SiO_2 and AlN respectively by taking into account the corresponding dielectric constant and thickness of the dielectric. This expression gives a breakdown field value of ~4 MV/cm across the AlN dielectric in the stack. This shows that addition of the wide bandgap dielectric, SiO_2, on the top of AlN layer slightly improves

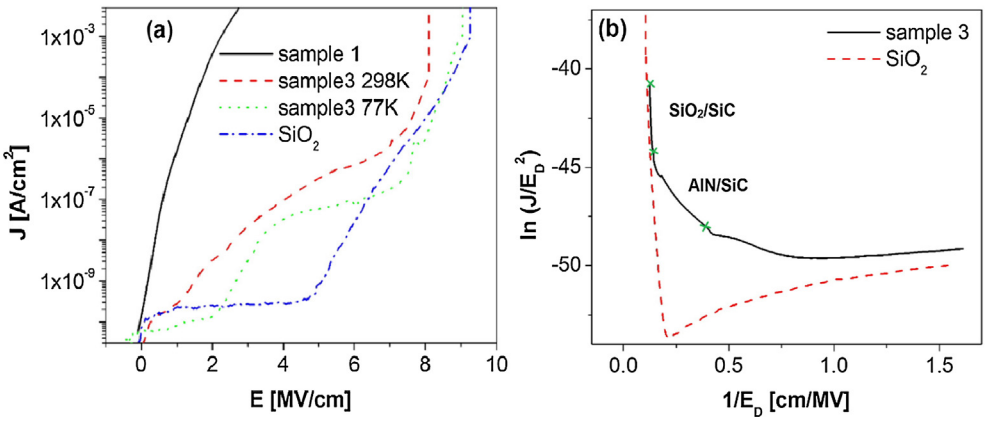

Fig. 8. (a) Comparison of leakage current density versus electric field intensity (J-E) of sample 1 and 3 and of dry thermal SiO_2. J-E profile of sample 3 is shown for 298 K and 77 K. (b) The F-N plot for sample 3 and for dry SiO_2 at room temperature. The cross marks on the F-N curve of sample 3 indicate the investigated regions of high and medium electric field intensity to find the barrier height of SiO_2/SiC and AlN/SiC respectively.

the breakdown field. As expected, the actual benefit of adding the SiO_2 layer is that the MIS capacitor can tolerate higher gate voltages compared to a single layer AlN.

Fig. 8a shows that the current leakage behavior across the dielectric is different in the single layer AlN and the stacked AlN MIS sample. Fowler-Nordheim tunneling behavior is seen in the SiO_2/AlN stack (sample 3) and the reference sample. The SiO_2 layer on top of the AlN layer reduces the current leakage across the AlN based stack because of the larger bandgap of SiO_2. The J-E data of the samples was analyzed further to determine the tunneling barrier heights assuming F-N tunneling mechanism. The classical expression for F-N tunneling is

$$J = AE_D^2 \exp\left(\frac{-B}{E_D}\right) \tag{3}$$

$$\mathrm{A} = \frac{q^3 m_{SiC}}{8\pi h m_D \phi_b},\ \mathrm{B} = \frac{8\pi\sqrt{2m_D}\,\phi_b^{\frac{3}{2}}}{3hq} \tag{4}$$

Here q is the electron charge, h is the Planck constant, E_D is the effective electric field intensity across the dielectric and ϕ_b is the effective barrier height in eV measured from the SiC conduction band edge to the dielectric conduction band edge. The m_{sic} and m_D are the effective electron masses in the SiC and the dielectric respectively. The effective electron mass of AlN and SiO_2 is taken to be $0.3m_o$ and $0.42m_o$ respectively [31,32]. The effective barrier height is mostly determined by parameter B by taking the slope of the straight line appearing in a F-N plot at high electric field intensity. Such a plot is shown in Fig. 8b. From the F-N curve of sample 3 (SiO_2/AlN stack), at high electric field intensity, the extracted value of ϕ_b is about 2.5 eV. This value of ϕ_b is considerably higher than the conduction band offset value of AlN and 4H-SiC reported in literature which is ~1.6 eV [11,33]. This high value of ϕ_b agrees with the conduction band offset of SiO_2/SiC. Extraction within the medium electric field intensity region gives ϕ_b of about 0.6 eV. This value of ϕ_b is approximately the same as obtained for a single layer AlN (sample 1) by applying F-N tunneling mechanism (F-N curve is not shown here). This indicates that the tunneling through AlN dielectric is trap assisted. The investigated high and medium electric field intensity region of F-N plot of sample 3 are shown by cross mark on the curve. From the F-N curve of reference SiO_2 sample, the value of ϕ_b of about 2.6 eV is obtained and the same value is reported in literature for thermally grown SiO_2/SiC interface using F-N tunneling mechanism [34].

In summary, the AlN MIS samples show some very interesting results. Based on room temperature CV analysis, the AlN/SiC interface contains very low density of interface states compared to state of the art thermal oxides. However, it is evident that the AlN/SiC interface has significant amount of fast interface states located very near the SiC conduction band edge. These interface state are detected at 77 K in capacitance analysis and could have an impact on electron channel mobility in AlN based SiC MISFETs. Overall the results are very promising in terms of interface state densities but the main obstacle here is severe electron injection into the AlN under accumulation bias. The physical origin of the bulk electron traps within the AlN is unknown. Our speculation is that the AlN layer has either very high density of intrinsic point defects (e.g silicon and oxygen point defects) or extended defects like dislocations causing the current leakage through the AlN layer [26]. If the latter is the case, then the structural defect density could be reduced by growing thinner layers of AlN (2–3 nm) and then depositing SiO_2 on top of the AlN to complete the dielectric stack.

4. Conclusions

CV analysis at room temperature reveals an order of magnitude lower density of interface traps at the AlN/SiC interface than at nitrided SiO_2/SiC interfaces. It is evident that the interface traps that are held responsible for electron channel mobility reduction in 4H-SiC MISFETs are practically absent at the AlN/SiC interface in this study. The AlN/SiC structures do have a large density of fast interface traps located very near the SiC conduction band edge that are revealed by CV analysis at 77 K and could have some impact in MISFETs. Electron trapping within the AlN is significant when the MIS capacitors are biased into accumulation resulting in a large flatband voltage shift towards higher gate voltage. This process is reversible and the electrons are fully released from the AlN layer if depletion bias is applied at elevated temperatures. This is connected to the relatively low breakdown field (3–4 MV/cm) of the AlN layers. It is possible to improve the breakdown field slightly by depositing a SiO_2 layer on top of the AlN. For future studies, we propose growing a few nm thin AlN layer followed by a thick layer of deposited SiO_2 in an attempt to decrease the electron trapping within the AlN layer. More work is needed on such dielectric stacks to reveal if they can be an alternative to SiO_2 as a gate dielectric in 4H-SiC MIS devices.

Acknowledgements

This work was financially supported by The Icelandic Research Fund. We also acknowledge support from the Swedish Foundation for Strategic Research (SSF), and the Knut and Alice Wallenberg Foundation (KAW).

References

[1] Jia Y, Lv H, Song Q, Tang X, Xiao L, Wang L, et al. Appl Surf Sci 2017;397:175.
[2] Kodigala SR, Chattopadhyay S, Overton S, Ardoin I, Gordon BJ, Johnstone D, et al. Appl Surf Sci 2015;330:465.
[3] Kimoto T. Japanese J Appl Phys 2015;54:040103.
[4] Afanasev VV, Ciobanu F, Dimitrijev S, Pensl G, Stesmans A. J PhysCondens Matter 2004;16:S1839.
[5] Avice M, Grossner U, Pintilie I, Svensson BG, Servidori M, Nipoti R, et al. J Appl Phys 2007;102:054513.
[6] Onojima N, Suda J, Matsunami H. Appl Phys Lett 2002;80:76.

[7] Tanner CM, Perng Y-C, Frewin C, Saddow SE, Chang JP. Appl Phys Lett 2007;91:203510.
[8] Zetterling CM, Östling M, Nordell N, Schön O, Deschler M. Appl Phys Lett 1997;70:3549.
[9] Hatayama T, Hino S, Miura N, Oomori T, Tokumitsu E. IEEE Trans Electron Devices 2008;55:2041.
[10] Horita M, Noborio M, Kimoto T, Suda J. IEEE Trans Electron Devices 2014;35:339.
[11] M. Nawaz, Hindawi publishing corporation active and passive electronic components 2015, 1; 2015.
[12] Taube A, Gierałtowska S, Gutt T, Małachowski T, Pasternak I, Wojciechowski T, et al. Acta Phys Pol A 2011;119:696.
[13] Yoder MN. IEEE Trans Electron Devices 1996;43:1633.
[14] Aboelfotoh MO, Kern RS, Tanaka S, Davis RF, Harris CI. Appl Phys Lett 1996;69:2873.
[15] Vispute RD, Patel A, Baynes K, Ming B, Sharma RP, Venkatesan T et al., MRS online proceedings library 595, F99W11.3; 1999.
[16] Ponce FA, Krusor BS, Major JS, Plano WE, Welch DF. Appl Phys Lett 1995;67:410.
[17] Choi J, Puthenkovilakam R, Chang JP. Appl Phys Lett 2005;86:192101.
[18] Zetterling CM, Östling M, Yano H, Kimoto T, Matsunami H, Linthicum K, et al. Mater Sci Forum 2000;338–342:1315.
[19] Onojima N, Kaido J, Suda J, Kimoto T, Matsunami H. Mater Sci Forum 2004;457–460:1569.
[20] Chen JT, Bergsten J, Lu J, Janzén E, Thorsell M, Hultman L, et al. Appl Phys Lett 2018;113:079903.
[21] Chen JT, Pomeroy JW, Rorsman N, Xia C, Virojanadara C, Forsberg U, et al. J Crystal Growth 2015;428:54.
[22] Allerstam F, Ólafsson HÖ, Gudjonsson G, Dochev D, Sveinbjörnsson EÖ, Rödle T, et al. J Appl Phys 2007;101:124502.
[23] Fleetwood DM. Microelectronics Reliab 2018;80:266.
[24] Nicollian EH, Brews JR. MIS (metal oxide semiconductor) physics and technology. New York, USA: John Wiley & Sons; 1982.
[25] Suda J, Matsunami H, US Patent 2006/0194379 A1; 2006.
[26] Gordon L, Lyons JL, Janotti A, Van de Walle CG. Phys Rev B 2014;89:085204.
[27] Ligatchev V, Rusli, Pan Z. Appl Phys Lett 2005;87:242903.
[28] Bhuiyan MA, Zhou H, Jiang R, Zhang EX, Fleetwood DM, Ye PD, et al. Dev Lett 2018;39:1022.
[29] Dou C, Lin D, Vais A, Ivanov T, Chen HP, Martens K, et al. Microelectronics Reliab 2014;54:746.
[30] Southwick RG, Reed J, Buu C, Butler R, Bersuker G, Knowlton WB, et al. Device Mater Rel 2010;10:201.
[31] Rinke P, Winkelnkemper M, Qteish A, Bimberg D, Neugebauer J, Scheffler M. Phys Rev B 2008;77:075202–75211.
[32] Kodigala SR, Chattopadhyay S, Overton C, Ardoin I. Solid State Electron 2016;114:104.
[33] Lelis AJ, Scozzie CJ, McLean FB, Geil BR, Vispute RD, Venkatesan T. Mater Sci Forum 2000;338–342:1137.
[34] Gutt T, Przewlocki HM, Piskorski K, Mikhaylov A, Bakowski M. ECS J Solid State Sci Technol 2015;4:M60.

Einar Örn Sveinbjörnsson received the B.Sc degree in Physics from University of Iceland, Reykjavik, Iceland in 1986, the MSEE degree in Electrical Engineering from University of Southern California, Los Angeles, CA in 1987 and the Ph.D. degree in Electrical Engineering from Chalmers University of Technology, Göteborg, Sweden in 1994. He worked at Max-Plank-Institute for Solid State Research in Stuttgart, Germany 1995-1996. He joined Solid State Electronics Department of Chalmers University of Technology, Göteborg, Sweden as Assistant Professor in 1997 and was promoted to Professor in 2004 at the Microwave Electronics Laboratory at Chalmers University of Technology. In 2008, he returned to University of Iceland. Since 2013, he is adjunct professor within the Divison of Semiconductor Materials at Linköping University, Linköping, Sweden. His main research interest is defect engineering in semiconductor devices.