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Graphene field-effect transistors with high extrinsic f_T and f_{max}

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***Abstract*— In this work, we report on the performance of graphene field-effect transistors (GFETs) in which the extrinsic transit frequency (f_T) and maximum frequency of oscillation (f_{max}) showed improved scaling behavior with respect to the gate length (L_g). This improvement was achieved by the use of high-quality graphene in combination with successful optimization of the GFET technology, where extreme low source/drain contact resistances were obtained together with reduced parasitic pad capacitances. GFETs with gate lengths ranging from 0.5 μm to 2 μm have been characterized, and extrinsic f_T and f_{max} frequencies of up to 34 GHz and 37 GHz, respectively, were obtained for GFETs with the shortest gate lengths. Simulations based on a small-signal equivalent circuit model are in good agreement with the measured data. Extrapolation predicts extrinsic f_T and f_{max} values of approximately 100 GHz at L_g=50 nm. Further optimization of the GFET technology enables f_{max} values above 100 GHz, which is suitable for many millimeter wave applications.**

***Index Terms*— graphene, field-effect transistor, maximum frequency of oscillation, transit frequency, scaling**

I. Introduction

THE two-dimensional material graphene is a promising candidate for application in high-frequency devices due to its high charge carrier saturation velocity [1]. Until recently, the realization of graphene field-effect transistors (GFETs) for high-frequency electronics was hindered by extrinsic limitations caused by impurities that reduced the carrier velocity, large extrinsic source/drain contact resistances, and large pad capacitances [2]–[5]. Recent publications have shown that efforts to develop high-frequency GFETs have resulted in a continuous step-by-step improvement of the extrinsic transit (cut-off) frequency (f_T) and the maximum frequency of oscillation (f_{max}) [5]–[10]. However, even the best reported extrinsic values of f_T and f_{max} of GFETs are still below those of n-channel Si MOSFETs with comparable gate lengths [11]–[13]. Furthermore, the increase in f_T and f_{max} with scaling down of the gate length has been suppressed [5], [7].

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In this work, we report on GFETs that exhibit improved extrinsic f_T and f_{max} values and improved scaling behavior with the gate length in comparison to the best published data for GFETs. Furthermore, the scaling behavior is comparable to that of Si n-channel MOSFETs. The enhancement was achieved by a combination of the following improvements of the GFET design and fabrication process: i) usage of high-quality graphene films, ii) effective removal of polymer residues in the contact areas, and iii) usage of a thicker SiO_2 layer (1 μm) on top of the silicon substrate. These improvements resulted in charge carrier saturation velocities as high as 1.5×10^5 m/s (at drain fields of 1.5 kV/cm), source/drain specific edge contact resistivities as low as 90 $\Omega\mu$m, and considerably reduced extrinsic pad capacitances.

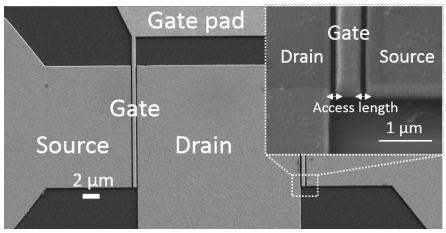

Fig. 1. SEM image of a two-finger GFET with gate length $L_g = 0.5\ \mu$m and gate width $W_g = 2 \times 15\ \mu$m. The inset shows a 70° tilted view of the gate area.

II. Fabrication

Two-finger gate GFETs (shown in Fig. 1) with the same layout as previously published in [4] were fabricated. The process flow was modified with the aim of increasing, first of all f_{max} but also f_T. The graphene film used for fabricating the GFETs was very high-quality chemical vapor deposition (CVD) graphene with a Hall mobility of up to 7000 cm^2/Vs. The graphene film was transferred to a high-resistivity silicon/silicon oxide (Si/SiO_2) substrate with an increased SiO_2 thickness of 1 μm compared to the 0.09 μm and 0.3 μm used in our previous works [4], [14]. This resulted in a reduction in the parasitic pad capacitances. After the graphene transfer, but prior to any further processing, the graphene film was covered by an 5 nm protective Al_2O_3 layer. This layer was obtained by repeating four times the process step in which 1 nm Al was evaporated and subsequently oxidized by baking on a hotplate at 160 °C for 5 min. The protective layer encapsulates graphene in the transistor

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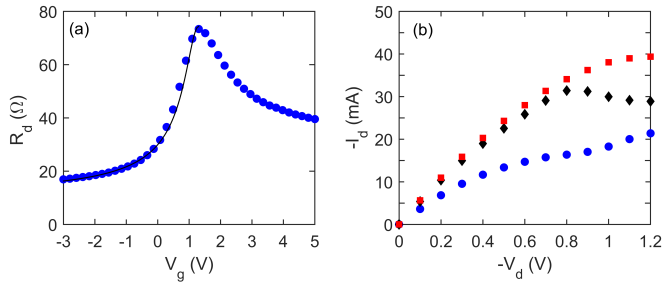

Fig. 2. Typical drain resistance (R_d) versus gate voltage (V_g) at the drain voltage $V_d = -0.1$ V (a) and output characteristics measured at V_g=-3,-1, and 0.5 V (squares, diamonds, and circles, respectively) (b) of a GFET with L_g = 0.5 μm and W_g = 2×15 μm. The solid line represents fitting by the drain resistance model [17].

channel and prevents it from contamination during further processing, thereby reducing the trap concentration at the graphene/gate dielectric interface. The graphene mesa and, subsequently, the drain and source contacts are patterned by e-beam lithography followed by etching the protective Al_2O_3 in a buffered oxide etch. Oxygen plasma was used to etch the graphene mesa. The drain/source contacts were formed by deposition of 1 nm Ti/15 nm Pd/250 nm Au and use of standard lift-off technology. Apparently, the use of a buffered oxide etch resulted in a more effective removal of e-beam resist and PMMA residues and, hence, an extremely low graphene/metal specific contact resistivity as low as 90 $\Omega\mu$m. In the next step, atomic layer deposition was used to thicken the protective Al_2O_3 layer to a total thickness of t_{ox} =22 nm in the gate area. The gate electrode was fabricated by e-beam lithography and deposition of 10 nm Ti/290 nm Au by e-beam evaporation followed by standard lift-off. GFETs with total gate widths (W_g) ranging from 2x1.25 μm to 2x15 μm and gate lengths (L_g) ranging from 0.5 μm to 2 μm were fabricated. In the final step, the gate and the drain/source contact pads were formed by e-beam lithography, deposition of 10 nm Ti/290 nm Au and lift-off.

III. MEASUREMENTS

The dc and ac performance of the GFETs was characterized using a Keithley 2612B dual-channel source meter and an Agilent N5230A network analyzer, respectively. The ac measurement system was calibrated at the ground-source-ground microwave probe tips using a CS-5 calibration substrate. The output characteristics were obtained during the S-parameter measurements with a holding time of 30 s at each bias point. This holding time is long enough for the trapping/de-trapping processes to stabilize at high fields [4]. The S-parameters were measured under different bias conditions in the frequency range of 1-50 GHz and were used to calculate the small-signal current gain (h_{21}) and the unilateral power gain (U) [15], [16]. As shown in Fig. 3(a), f_T and f_{max} are defined as the frequencies at which the magnitudes of h_{21} and U, respectively, have decreased to 0 dB.

IV. RESULTS AND DISCUSSION

Fig. 2(a) shows a typical drain resistance versus gate voltage of a GFET with $L_g = 0.5\,\mu$m and $W_g = 2 \times 15\,\mu$m. The solid line represents fitting by the drain resistance model [17], which is used to estimate the contact resistance (R_c), low-field mobility (μ_0), and residual charge carrier concentration (n_0) which are found to be 11 Ω, 1800 cm^2/Vs and 9×10^{11} cm^{-2}, respectively. The calculated graphene/metal width specific contact resistivity is 90 $\Omega\mu$m, which is in good agreement with the value of 95 $\Omega\mu$m found using transfer length method test structures fabricated on the same substrate.

Fig. 2(b) shows the typical output characteristics of GFETs. The drain current exhibits a saturation tendency at higher drain voltages (V_d). The observed so-called kink effect at $V_g = 0.5$ V is most likely associated with the reduction in the charge carrier concentration and a subsequent change in the charge carrier type at the drain side of the channel [3]. A negative differential resistance at $V_g = -1$ V can be associated with a reduction in the charge carrier density-dependent saturation velocity [18]. Both effects are consequences of the ambipolar nature of graphene. Fig. 3(a) shows the smith chart with measured S-parameters between 1 GHz and 50 GHz. Fig. 3(b) shows the small-signal current gain ($|h_{21}|^2$), maximum stable gain/maximum available gain (MSG/MAG), and unilateral power gain (U) versus frequency (f) at $V_d = -1.1$ V and $V_g = 0.5$ V. As it can be seen, the unilateral power gain reveals typical frequency dependence. The low frequency gain is approx. 18 dB. Above the roll-off frequency of approx. 5 GHz the gain starts decreasing as $1/f^2$, corresponding to 20 dB/dec slope [19]. Fig. 3(c) shows f_T and f_{max} versus V_d at different gate voltages of $V_g = 0.5, -1$, and -3 V. Both f_T and f_{max} saturate at higher drain voltages, apparently, due to velocity saturation [4], reaching values of 34 GHz and 37 GHz, respectively. To estimate the gate width and length dependence of f_T and f_{max}, expressions in terms of small-signal equivalent circuit parameters are used [20], [21]:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \frac{1}{1 + g_d R_c + \frac{C_{gd} g_m R_c}{C_{gs}+C_{gd}} + C_{pad}}, \quad (1)$$

$$f_{max} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_d(R_i + R_s + R_g) + g_m R_g \frac{C_{gd}}{C_{gs}}}}, \quad (2)$$

where g_m and g_d are the intrinsic transconductance and drain conductance, respectively; C_{gs}, C_{gd} and C_{pad} are the gate-source, gate-drain and parasitic pad capacitances, respectively; and R_g, R_s, and R_i are the gate resistance, source series resistance, and charging resistance of the gate-source capacitance, respectively. We estimated C_{gs} and C_{gd} as $C_{gs} = 0.5 C_{ox} L_g W_g$ and $C_{gd} = k_1 C_{ox} L_g W_g$, where $C_{ox} \propto 1/t_{ox}$ and k_1 is a fitting parameter taking into account the decrease in charge carrier concentration at the drain side [8]. The intrinsic transconductance was found to be $g_m = v(C_{gs} + C_{gd})/L_g$, where v is the field-dependent effective velocity of the charge carriers, with values between 1.2 and 1.5×10^5 m/s for different devices extracted from a field-dependent velocity model [4]. The intrinsic drain conductance was found by analyzing the GFET output characteristics. The resistances are estimated

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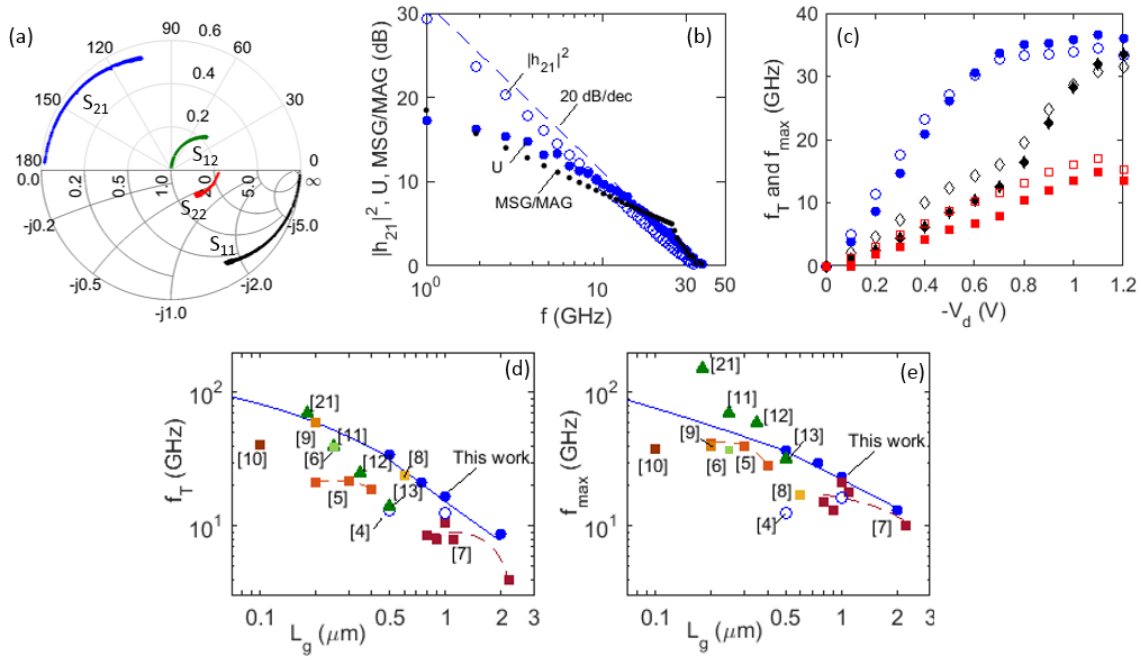

Fig. 3. (a) Smith chart with measured S-parameters between 1 GHz and 50 GHz. (b) Small-signal current gain ($|h_{21}|^2$), maximum stable gain/maximum available gain (MSG/MAG), and unilateral power gain (U) versus frequency (f) at $V_d = -1.1$ V and V_g=0.5 V. The dashed line indicates the 20 dB/dec slope. (c) Extrinsic transit frequency (f_T, open symbols) and extrinsic maximum frequency of oscillation (f_{max}, filled symbols) versus drain voltage (V_d) at different gate voltages V_g=-3,-1, and 0.5 V (squares, diamonds, and circles, respectively) of a GFET with L_g = 0.5 μm and W_g = 2×15 μm. (d) Extrinsic transit frequency (f_T) versus gate length (L_g) of GFETs measured in this work (solid circles) and simulated using (1) (solid line). (e) Extrinsic maximum frequency of oscillation (f_{max}) versus gate length (L_g) of GFETs measured in this work (solid circles) and simulated using (2) (solid line). Also shown are the highest published extrinsic f_T and f_{max} values of GFETs [5]–[10] (squares) and Si MOSFETs [11]–[13], [22] (triangles) and our previous published work (open circles) [4] for comparison. Dashed lines are polynomial fitting curves.

as $R_i = 1/(3g_m)$ and $R_g = 1/3R_{shg}W_g/L_g$, where R_{shg} is the gate electrode sheet resistance [21]. The source series resistance R_s is assumed to be $R_c/2$. The parasitic gate pad capacitance, formed between the gate pad and low-conductivity surface of Si, is taken as 3 times less than that found in [4] by delay-time analysis ($\approx$ 27 fF) due to the three times thicker SiO_2 layer.

Fig. 3(d-e) shows the measured and simulated extrinsic f_T and f_{max} values versus gate length for GFETs with $W_g = 2 \times 15\,\mu$m. The simulations and measurements are in good agreement. Also shown are the extrinsic f_T and f_{max} values obtained in our previous work and the best values published in the literature. It can be seen, that the GFETs in this work reveal higher f_T and f_{max} values than that of the best reported GFETs [3], [7], including the GFETs fabricated by our prior technology [4], and even Si MOSFETs [12] at similar gate lengths. The scaling behavior of the GFETs published in [5] and [7] is suppressed, as indicated by the polynomial fitting lines, whereas the GFETs in this work show a promising scaling trend. At $L_g = 0.5\,\mu$m, the GFETs in this work reveal higher extrinsic frequencies of $f_T = 34$ GHz and $f_{max} = 37$ GHz than the GFET counterpart in [5] at $L_g = 0.4\,\mu$m, which is most likely due to its larger width specific contact resistivity of 550 $\Omega\mu$m.

The small-signal simulations, using the same model parameters used for the GFET with $L_g = 0.5\,\mu$m, indicate that f_T and f_{max} values of up to 100 GHz can be achieved at $L_g = 50$ nm. The intrinsic value of f_T is estimated to exceed 400 GHz which is competing well with the best published intrinsic values of f_T [23], [24]. To compete with the shorter-gate-length Si MOSFETs shown in Fig. 3(d-e), further optimizations are required. It follows from the analysis of (1) and (2) that further improvement of the performance can be achieved with extrinsic f_T and f_{max} values above 100 GHz at $L_g = 0.1\,\mu$m by i) increasing the saturation velocity of the charge carriers in the GFET channel, e.g., by replacing the SiO_2 with another dielectric material with a higher optical phonon energy, such as Al_2O_3 or hexagonal boron nitride [4]; ii) reducing the gate oxide thickness if the condition $C_{gs} = 0.5C_{ox}L_gW_g$ applies; and iii) reducing the gate resistance, and iv) reducing the part of the contact resistance associated with the access areas. The last two approaches can be realized, for example, by applying the self-aligned T-gate technology.

V. CONCLUSIONS

GFETs with high extrinsic frequency values of $f_T = 34$ GHz and $f_{max} = 37$ GHz at $L_g = 0.5\,\mu$m are presented. The GFETs also exhibit a promising scaling behavior versus gate length. The performance enhancement was achieved by minimizing the extrinsic limiting parameters by modifying the fabrication process. Analysis of the small-signal model shows that further optimization of the GFET design and fabrication will allow even better performances to be achieved with f_{max} above 100 GHz for L_g below 100 nm and will further exploit the potential of GFET transistors integrated in devices for high-frequency applications.

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