

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

**On integrity assessment of IGBT-based power stacks used  
in magnet power supplies for particle accelerators**

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Gothenburg, Sweden, 2019

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## Abstract

This thesis analyses an electrical testing method for assessing the integrity of an IGBT-based power stack assembly during factory acceptance tests and service stops. The method combines  $v_{ce}$  measurements with high current in the Zero Temperature Coefficient (ZTC) operating region and with low sensing current within a specific current cycle using a proposed sampling and filtering technique. Two circuits are presented for the  $v_{ce}$  measurement. The value of this method is the ability to validate the power stack assembly and to detect IGBT aging without the need for power stack modifications for the  $v_{ce}$  measurement with sensing and load current. Additionally, no dedicated current control of the IGBTs is required. The aging mechanisms that are targeted with this method are the bond-wire lift-off and the solder delamination. As a part of the method, an on-the-stack  $v_{ce}$  calibration technique at the sensing current level is proposed for the IGBTs avoiding the need to un-mount and characterize them in a thermal chamber. The reference application is a power electronic converter that is used as a magnet power supply in particle accelerators at CERN, the European Organization for Nuclear Research. Based on the specialized application, the levels of ambient air, junction and cooling water temperature change that could have an impact on the method's precision are defined. Experimental results, which are obtained with the power stack of a power magnet supply, are presented and are compared favorably with results obtained using Finite Element Method (FEM) and Lumped Parameter Network (LPN) simulations to demonstrate the methods applicability. For the high-current IGBT module of the application, it is shown that the measurement in the ZTC operating region could detect bond-wire lift-offs when more than half of the bond-wires of the chip have been lifted. A measurement in the Positive Temperature Coefficient (PTC) operating region can be used to detect the early stage aging of a bond-wire lift-off, but the measurement precision is, highly, influenced by temperature. Moreover, the detection of manufacturing issues, such as errors in thermal paste application, is proven to be possible with the help of  $v_{ce}$  measurements with sensing current.

As a potential improvement of the future power stack designs for lifetime prolongation, this work investigates the possibility for IGBT module's thermal stressing mitigation using

the specialized application as a reference. This investigation is based on LPN simulations. Prior to the LPN modeling, the extensive operation of the magnet power supply in the Negative Temperature Coefficient (NTC) operation region is, experimentally, examined. It is demonstrated that the current and thermal stressing unbalances among the chips inside the Soft Punch Through (SPT) IGBT module operating in the NTC operating region can be neglected and do not have to be considered for the thermal modeling. Moreover, the impact of the material, of the thickness and of the heat convection of the cooling plate on the junction temperature variation and maximum junction temperature is evaluated. It can be stated that, for long current cycles of the specialized application, a relatively thick aluminum cooling plate ( $3cm$ ) with a moderate heat convection coefficient ( $5kW/({}^{\circ}Cm^2)$ ) may exhibit almost the same performance as a copper cooling plate of equal or even greater thickness ( $5cm$ ) with a high heat convection coefficient ( $10kW/({}^{\circ}Cm^2)$ ).

Two strategies are proposed with the switching frequency and the gate resistance as parameters for online thermal stressing mitigation. The first strategy reduces the switching frequency in parts of the cycle where a high precision requirement for the output current is not imposed, in order to limit the power losses and the thermal stressing of the IGBT. The second strategy combines the switching frequency reduction in one part of the cycle with the increase of switching frequency and gate resistance in another. By increasing the power losses the junction temperature fluctuation can be limited. Using four typical current profiles from the specialized application, it is shown that both strategies could prolong the IGBTs' lifetime. It is shown that the contribution of the mitigation strategy to the lifetime prolongation depends on the current profile.

**Index Terms:** power electronics, magnet power supply, IGBT, aging detection, temperature estimation,  $v_{ce}$  measurement, condition monitoring, thermal stressing mitigation

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Panagiotis  
Geneva, 2018

## List of Abbreviations

IGBT	Insulated Gate Bipolar Transistor
ZTC	Zero Temperature Coefficient
CERN	European Organization for Nuclear Research
FEM	Finite Element Method
LPN	Lumped Parameter Network
PTC	Positive Temperature Coefficient
SPT	Soft-Punch-Through
TSEP	Temperature Sensitive Electrical Parameters
LHC	Large Hadron Collider
DC	Direct-Current
NTC	Negative Temperature Coefficient
PT	Punch-Through
NPT	Non-Punch-Through
DBC	Direct-Bond Copper
TIM	Thermal Interface Material
SEM	Scanning Electron Microscopy
DUT	Device Under Test
MOSFET	Metal-Oxide-Semiconductor-Field-Transistor
DAQ	Data Acquisition
ADC	Analog-to-Digital Converter
DCCT	Direct-Current Current Transformer
RMS	Root-Mean-Square
IPSIA	IGBT Power Stack Integrity Assessment
PWM	Pulse Width Modulation
PS	Proton Synchrotron
SPS	Super Proton Synchrotron

## List of Symbols

$v_{ce}$	IGBT collector-emitter voltage
$v_F$	diode forward voltage
$n_i$	intrinsic carrier concentration
$D_a$	ambipolar diffusion constant
$v_{ge}$	gate-emitter voltage
$V_{th}$	threshold voltage
$\mu_{EFF}$	mobility

$T$	temperature
$\lambda$	thermal conductivity
$R_{th}$	thermal resistance
$C_{th}$	thermal capacitance
$d$	thickness of layer
$\rho$	density of material
$A$	surface area
$c$	specific heat capacity
$V_{ce,0}$	IGBT zero current collector-emitter voltage
$r_c$	IGBT equivalent resistance
$i_c$	IGBT collector current
$p_{con,i,in}$	IGBT instantaneous conduction losses
$P_{con,i,av}$	IGBT average conduction losses
$I_{c,av}$	IGBT average current
$L_{G,\sigma}$	gate parasitic inductance
$P_{sw,i,av}$	IGBT average switching losses
$I_{c,rms}$	IGBT RMS current
$V_{cc}$	IGBT full blocking voltage
$v_{g,on}$	IGBT nominal gate-emitter voltage
$E_{sw,i,on}$	IGBT energy loss of a switching-on event
$E_{sw,i,off}$	IGBT energy loss of a switching-off event
$E_{sw,i,on,ref}$	reference IGBT energy loss of a switching-on event
$E_{sw,i,off,ref}$	reference IGBT energy loss of a switching-off event
$E_{sw,i,ref}$	IGBT switching losses measured at a reference current and voltage
$I_{ref}$	IGBT reference current
$V_{DC,ref}$	IGBT reference voltage
$K_i$	current factor
$K_v$	voltage factor
$TC_{sw}$	temperature coefficient
$T_j$	IGBT junction temperature
$T_{j,ref}$	IGBT reference junction temperature
$f_{sw}$	switching frequency
$p_{block,i}$	instantaneous power losses at blocking state
$P_{block,i,av}$	average power losses at blocking state
$D$	Duty cycle
$i_{ces}$	IGBT collector cut-off current
$T_d$	temperature constant for blocking losses
$V_{F,0}$	diode zero current forward voltage

$i_F$	diode forward current
$r_D$	diode equivalent resistance
$I_{F,av}$	diode average forward current
$I_{F,rms}$	diode RMS forward current
$E_{rec,D}$	diode reverse recovery energy
$E_{sw,D}$	diode switching energy loss
$E_{sw,D,ref}$	IGBT switching losses measured at a reference current and voltage
$T_{j,max}$	maximum junction temperature
$T_{j,min}$	minimum junction temperature
$T_{j,mean}$	mean junction temperature
$\Delta T_j$	junction temperature variation
$t_{on}$	heating time
$D_b$	bond-wire diameter
$N_f$	number of cycles
$E_\alpha$	activation energy
$k_B$	Boltzmann's constant
$t_{on,d}$	turn-on delay time
$t_{off,d}$	turn-off delay
$I_{sc}$	short-circuit current
$R_{par}$	module parasitic resistance
$R_{int}$	gate internal resistance
$R_{ext}$	gate external resistance
$T_c$	case temperature
$Z_{th}$	thermal impedance
$P_{loss}$	power losses
$v_{gs}$	MOSFET gate-source voltage
$t_{settling}$	settling time
$t_{sampling,DAQ}$	DAQ sampling time
$V_o$	average output voltage
$T_{on}$	conduction time
$T_{sw}$	switching period
$V_{dc}$	DC-link voltage
$I_{o,rms}$	RMS output current
$Re$	Reynolds number
$u$	cooling medium velocity
$d_h$	inner pipe diameter
$\nu$	kinematic viscosity
$Q$	cooling medium flow rate

$C_p$	cooling medium thermal capacity
$V_{i,max,op-amp}$	maximum allowable input voltage of operational amplifier
$V_z$	Zener voltage
$V_{DAQ}$	DAQ voltage
$R_{th,j-a}$	thermal resistance junction-to-ambient
$P_z$	Zener power loss
$I_{z,av}$	Zener average current
$\Delta T_{j,z}$	zener temperature variation
$R_{meas}$	measuring resistance
$I_{z,leak}$	Zener leakage current
$V_{i,error}$	error in input voltage of operational amplifier
$V_{R_{meas}}$	measuring resistance voltage drop
$R_{op-amp}$	operational amplifier input resistance
$V_{op-amp}$	operational amplifier input voltage
$V_{ce,max,1A}$	IGBT maximum voltage at 1A
$v_s$	supply voltage
$T_{1,1}$	Upper left switch of H-bridge
$T_{2,2}$	Lower right switch of H-bridge
$R_{CC+EE}$	the terminal-chip leads resistance
$\alpha$	temperature coefficient of resistance of conductive material
$R_{ref}$	reference resistance of conductive material
$R_{th,j-w}$	thermal resistance from junction-to-water
$\Delta T_{j-w}$	temperature difference between junction and water inlet
$I_{s,ref}$	substrate reference current
$I_{s,1}$	substrate 1 reference current
$I_{s,2}$	substrate 2 reference current
$R_{(th,Al/Cu)}$	Ratio of thermal resistance of aluminum over thermal resistance of copper
$C_{(th,Al/Cu)}$	Ratio of thermal capacitance of aluminum over thermal resistance of copper
$h$	heat convection coefficient
$R_g$	general term for gate resistance
$R_{g,on}$	on-gate resistance
$R_{g,off}$	off-gate resistance

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# Chapter 1

## Introduction

### 1.1 Background

Power electronic converters are the main medium for electric power conversion and adaptation in a vast range of applications, such as electrical transportation, power generation from renewable and conventional sources, power transmission and distribution, supply of home appliances, industrial machinery and many others [1]. The core of power electronic converters are the semiconductors that either allow or block the current flow to the load. The semiconductor type that is preferred for medium to high power applications is the Insulated Gate Bipolar Transistors (IGBT) [2], [3]. The package type that is used for current levels up to  $3000A$  and voltage levels up to  $6500V$  is, commonly [3], an IGBT module like the one illustrated in Figure 1.1.



Figure 1.1: IGBT module (ABB property).

Apart from the benefits, such as the ease of assembly and interconnection at power electronic converter level, a critical issue in the application of IGBT modules is their reliable

operation. They are often considered as the component that is the most prone to fail during the operation of a power electronic converter [4]. For offshore wind farms, the operation and maintenance cost accounts for approximately 18% to 23% of the total cost of energy with the power electronic converters being the second least reliable sub-assembly after the pitch mechanism [5]. It is apparent that the monitoring of the health status of IGBT modules becomes a priority towards the optimal operation of a power electronic converter.

The thermal stressing, resulting from power losses [1] that are produced by the IGBTs themselves, is often responsible for their degradation. The aging mechanisms that have mostly drawn the attention are the bond-wire lift-off and the solder delamination [6]. During the development stage, it is of utmost importance to scrutinize the thermal aspect of the design of power electronic converters and to predict the thermal stressing of the semiconductor devices during operation. Additionally, it is of equal importance to monitor the condition of the semiconductor devices during their operating lifetime.

## **1.2 Application at the European Organization for Nuclear Research**

The reference application for this work is a magnet power supply that is used in particle accelerators at CERN, the European Organization for Nuclear Research. At CERN, high-power electronic converters are, extensively, used as magnet power supplies with predetermined current profiles, in order to control the particle beam's trajectory in the accelerators. Figure 1.2 illustrates the accelerator complex at CERN. The beam starts from linear accelerators, such as LINAC2, and is transferred with an increasing particle energy to the circular accelerators until it reaches the flagship of the complex that is the Large Hadron Collider (LHC).

For this task high-performance electromagnets are supplied by power electronic converters. The main requirements for this specialized application are high precision of the current output and long lifetime of at least twenty years with planned scheduled intervals, in order to avoid unscheduled stops of operation. Given that power electronic converters must all operate concurrently from the first to the last accelerator, the cost saving from unscheduled service interventions will be significant, if prognostics of IGBT failure could be obtained during scheduled service stops.

CERN power electronic engineers are involved in the technical specifications of the power electronic converter, however the manufacturing and assembly of power magnet supplies are assigned to external suppliers. The power electronic converter's part of interest for

## 1.2. Application at the European Organization for Nuclear Research

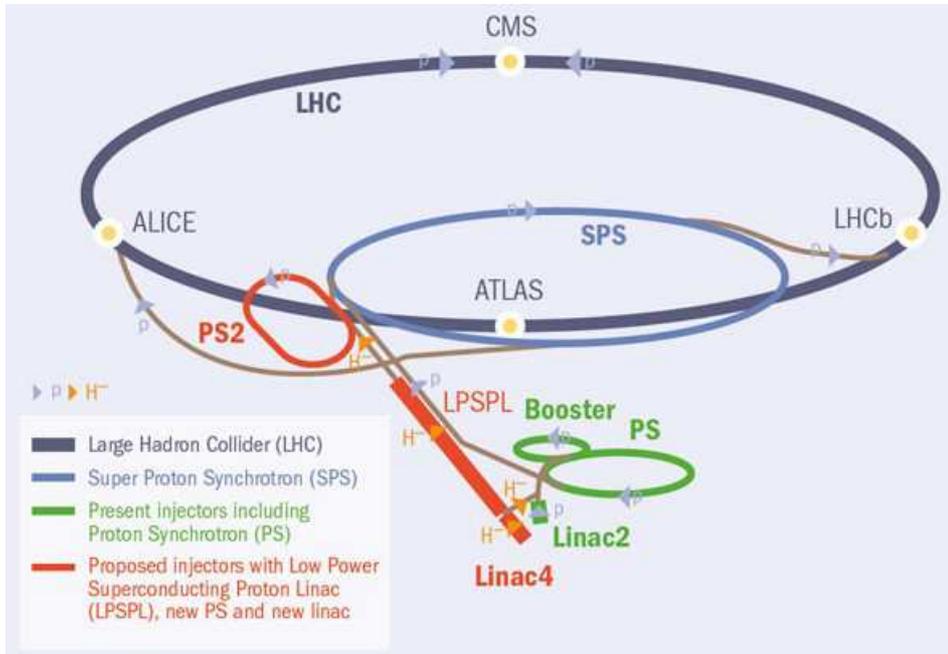


Figure 1.2: CERN accelerator complex [7].

this work is the power stack that comprises the DC-link and the power semiconductor devices with their cooling system. The evaluation from CERN side of the power stack's thermal performance and of its aging could be carried out in two phases. Further analysis is presented in Chapter 3. The first phase, which targets the thermal performance verification, is during the factory acceptance tests of series of power stacks at the supplier's premises.

The second phase targets the aging detection through condition monitoring made during service stops. Since the load profiles for this application are predefined, the thermal stressing of the IGBT modules can be predicted. Therefore, offline condition monitoring during scheduled service stops could be sufficient for this application and continuous, online condition monitoring is not needed. The long lifetime requirement and the high number of power electronic converters, reaching several thousands of units in operation for the specialized application at CERN creates the need for tracking and documentation of IGBT modules failures and aging mechanisms. Moreover, the collected data from several thousands of units operating at CERN could be important for future power stack designs, not only for the present application but, also, for other applications such as traction.

To sum up, a methodology which utilizes planned scheduled stops with minimum additional equipment would be of great value for a highly reliable but still financially reason-

able solution.

### 1.3 Previous work

The temperature estimation at IGBT chip level helps to assess the thermal stressing and the remaining lifetime of the IGBT module [8], [9], [10]. It may, also, provide an indication of aging as a condition monitoring feature [11]. To the author's knowledge, the temperature and the condition monitoring of IGBTs are, mainly, applied and tested at accelerated lifetime tests with the aim to monitor the evolution of aging. The dominant parameters that are monitored for thermal stressing evaluation and condition monitoring are electrical as well as highly dependent on temperature and are defined as Temperature Sensitive Electrical Parameters (TSEPs), [12]. There are methods for temperature estimation based on measurements that can be implemented online by recording TSEPs, such as  $v_{ce}$  with high current [13], the threshold voltage  $V_{th}$  [14], the internal gate resistance [15], as well as switching dynamics [16] and [17]. These methods require no circuit modifications but, in some cases, fast measuring systems, such as in [16] and [17], and precise calibration of the IGBT module, for instance in terms of current and temperature. Other methods are offline and may require less effort for calibration but circuit modifications are needed such as the method based on  $v_{ce}$  with sensing current [18] or on the short-circuit current [19].

The aging detection of IGBT modules with the help of temperature estimation could be implemented online such as in [13], [14], [15] [20] and [21]. Similar to the TSEP-based temperature estimation methods, the online aging detection methods have the advantage of aging detection during operation but, also, the constraint of high calibration effort. Other methods propose offline aging detection or, differently expressed, condition monitoring that could be limited by necessary circuit modifications and connection of extra components, such as in [22], [23] and [24] or specific IGBT switching patterns without the possibility for detection of different aging mechanisms such as in [25].

The present work is focused on offline aging detection methods. The application at CERN has pre-defined profiles that result in expected IGBT temperature profiles. Scheduled stops can be defined to check the aging status of the IGBT modules. Therefore, the additional calibration effort of the online methods can be avoided. A critical review of the TSEPs and their change with aging, as well as of the existing aging detection methods follows in Chapter 2. Special interest is, also, noticed for the development of measuring circuits that are capable of monitoring TSEPs, especially  $v_{ce}$ , with precision. A part of Chapter 2 is dedicated to their analysis.

Up to now, the temperature and condition monitoring remains at research level targeting to

#### *1.4. Purpose of the thesis and contribution*

future online or offline monitoring systems in the field. The field implementation of monitoring encounters practical issues that need to be further investigated. The monitoring should be independent of testing conditions such as ambience or cooling medium temperature. Ideally, it should be realized with minimum additional equipment and minimum calibration effort per semiconductor device. The calibration effort could become an obstacle for the application of some of the proposed methods. These characteristics become crucial, if a large series of power electronic converters have to be monitored at industrial scale, such as the application at CERN, either online or offline. Although many valuable contributions are published, missing in the existing literature is a complete method that exhibits the following combination of features:

- robustness in terms of precision taking into account the testing conditions
- ease of implementation and calibration for a series of power electronic converters
- follow-up of power electronic converter's condition along its lifetime, from the thermal evaluation phase to the power stack validation testing phase and, finally, to its service stops.

### **1.4 Purpose of the thesis and contribution**

The main purpose of this work is to propose a method that could contribute to the reliable operation of a magnet power supply without unscheduled service stops due to unexpected failure incidents. This method should assess, with adequate precision and ease of implementation, the thermal performance and the condition of the IGBT modules in the high-power stack from the factory acceptance phase until the end of their lifetime. A second purpose, after studying the thermal impact of the specialized application on the power stack, is to investigate methods that could, potentially, mitigate the thermal stressing of IGBT modules.

The contributions of this work in terms of IGBT module aging detection can be listed as follows:

- a method for the integrity assessment of an IGBT-based power stack. It can be, directly, applied at the manufacturer's facility during factory acceptance tests to control the assembly quality; namely the correct thermal path from chip to water. Moreover, it can be used in scheduled service stops to detect and evaluate the aging of the semiconductors in terms of bond-wire lift-off and solder delamination. This

## Chapter 1. Introduction

method requires no additional power components, no current control, and employs an on-the-stack technique for  $v_{ce}$  calibration as a function of temperature without the need for IGBT unmounting and characterization in a thermal chamber (publication II)

- the development of two  $v_{ce}$  measuring circuits that are easy to calibrate and to use with complete power stacks. For the first circuit that is based on an existing proposal in the literature, extensive sensitivity analysis of the critical components, design methodology and testing are added. Based on the principle of desaturation detection circuit used in IGBT gate drivers, the second circuit comprises reduced number of components and less calibration effort compared to similar solutions. Moreover, a filtering technique is proposed for the application of the integrity assessment method (publication I).

The following are considered as contributions with more focus on thermal stressing mitigation:

- the quantification and evaluation of current asymmetry among substrates in the same IGBT module through experiments in the low current region with Negative Temperature Coefficient, if temperature difference occurs among the IGBT module substrates (publication IV)
- a discussion of thermal stressing mitigation possibilities for the CERN application: (i) at the design phase considering the cooling plate material, thickness and water flow, (ii) during operation with the online modification of the switching frequency and gate resistance for the regulation of the IGBT's thermal stressing during predefined current profiles for the application of interest (publications III, VI).

During the period as a Doctoral student, the author has contributed with the following relevant scientific publications:

- I. P. Asimakopoulos, K. Papastergiou, T. Thiringer, M. Bongiorno and G. LeGodec, "On  $v_{ce}$  method: in-situ temperature estimation and aging detection of high-current IGBT modules used in magnet power supplies for particle accelerators", *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 551-560, Jan. 2019
- II. P. Asimakopoulos, K. Papastergiou, T. Thiringer and M. Bongiorno, "IGBT Power Stack Integrity Assessment Method for High-Power Magnet Supplies", under second review round in *IEEE Transactions on Power Electronics*

#### 1.4. Purpose of the thesis and contribution

- III. P. Asimakopoulos, K. Papastergiou, T. Thiringer and M. Bongiorno, “Thermal stressing mitigation possibility intended for a DC-current magnet supply based on high power IGBT modules”, 19th European Conference on Power Electronics and Applications, EPE’18 ECCE Europe, Warsaw, Poland, Sep. 2017, poster presentation
- IV. P. Asimakopoulos, K. Papastergiou, T. Thiringer and M. Bongiorno, “Current sharing inside a high power IGBT module at the negative temperature coefficient operating region”, 17th European Conference on Power Electronics and Applications, EPE’16 ECCE Europe, Karlsruhe, Germany, Sep. 2016, oral presentation
- V. P. Asimakopoulos, K. Papastergiou, “High Voltage Supply for Particle Accelerators based on Modular Multilevel Converters”, International Particle Accelerators Conference, IPAC16, South Korea, 2016, poster presentation
- VI. P. Asimakopoulos, K. Papastergiou, T. Thiringer and M. Bongiorno “Heat sink design considerations in medium power electronics applications with long power cycles”, 16th European Conference on Power Electronics and Applications, EPE’15 ECCE Europe, Geneva, Switzerland, Sep. 2015, oral presentation

Additionally, before the Doctoral Studentship period the author has contributed to the following publications:

- P. Asimakopoulos, T. Thiringer and M. Bongiorno “Design of a Modular Multilevel Converter as an Active-Front End for a magnet supply application”, 15th European Conference on Power Electronics and Applications, EPE’14 ECCE Europe, oral presentation
- P. Asimakopoulos, T. Boumis, E. Patsias, A. Safacas, E. Tatakis and E. Mitronikas, “Conversion of a conventional vehicle to a hybrid electric vehicle - Step by step design and experimental investigation”, in 24th International Battery, Hybrid and Fuel Cell Electric Vehicle Symposium Exhibition, EVS 24, May 13-16, 2009, poster presentation
- P. Asimakopoulos, T. Boumis, E. Patsias, A. Safacas and E. Mitronikas, “Experience derived from the conversion of a conventional car to a hybrid electric vehicle - Analysis of the powertrain”, in 20th International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM, June 14-16, 2010
- P. Asimakopoulos, T. Boumis, E. Patsias and A. Safacas, “Design and construction of a propulsion system for application in experimental hybrid car”, Energy Point, FIPP-8079, vol. 25, July - August 2009

## 1.5 Outline of this thesis

Chapter 2 presents the necessary theoretical background for this work. As an introduction, it, briefly, describes the operation of the IGBT and of the diode, its dependence on temperature, the structure of the IGBT module and the power losses calculation. The introduced topics are the foundation for a critical review of the temperature estimation method. Among the presented methods, the appropriate method is selected for temperature estimation and condition monitoring. Moreover, a review of the suitable power and measuring circuits is presented. Finally, it, briefly, describes the dominant IGBT power stack thermal modeling methods that are the Lumped Parameter Networks (LPN) and the Finite Element Method (FEM).

Chapter 3 introduces the specialized application at CERN with electrical simulations for the operation of the magnet power supply. It presents the thermal stressing with a typical magnet current profile using LPN and FEM. The main experimental set-ups used in this work are, also, presented.

Chapter 4 investigates with the help of experiments and calculations the behavior of the chips inside the IGBT module, in terms of current unbalance, if the semiconductor operates at a current level that is low compared to its nominal ratings.

Chapter 5 proposes an integrity assessment method for the assembly verification at the initial stage and the aging detection in later stages of the power stack's lifetime. It, analytically, presents the development of two measuring circuits for the implementation of the method. Finally, it, experimentally, validates the method with a magnet power supply and compares the results with those from LPN and FEM simulations.

Using the LPN thermal modeling of Chapter 3, Chapter 6 provides thermal stressing mitigation methods for the extension of the power stacks useful lifetime. These methods are proposed as measures at the design phase of the power stack to delay the aging of the IGBT module as detected with the integrity assessment method that is presented in Chapter 5. The thermal stressing mitigation methods can be applied at the power stack design phase and online during operation. Considering the power stack design phase, it investigates the impact of the cooling plate's material, thickness and heat convection coefficient on the thermal stressing for long current cycles. Two strategies are proposed for the online thermal stressing mitigation. These strategies employ the gate resistance and the switching frequency and their usability is demonstrated. Finally, the conclusions and ideas for future work are provided in Chapter 7.

# Chapter 2

## Methods for IGBT modules temperature estimation and aging detection

### 2.1 Introduction

This chapter introduces the structure and operation principles of the power semiconductor devices used in this work, namely the pin-diode and the IGBT. It demonstrates the method that is, usually, used for the power losses calculations. This chapter describes the structure of a typical IGBT module and presents the main aging mechanisms resulting from the thermal stressing. Additionally, an overview of methods for the junction temperature estimation of the IGBT is presented. The critical review on the existing measuring circuits based on the  $v_{ce}$  method for the junction temperature estimation is published in publication I, whereas the critical review on the power circuits using the  $v_{ce}$  method is published in II.

### 2.2 Power diode structure and operation principle

The power pin-diode is created by a p-n junction, [26], with a low doped region n-, called the epitaxial layer, between p and n+ forming the pn-n+ structure, as illustrated in Figure 2.1a. For the power diodes with blocking voltage capability at the level of 1200 V and above, the n- region has increased thickness compared to low voltage diodes and the other two regions are created by diffusion from the n- layer.

As a freewheeling device, the conducting state of the power diode cannot be controlled. If a small positive voltage of a certain level is applied between the anode and the cathode, in

Figure 2.1a, the diode is forward biased and becomes conductive. With negative voltage applied to it it becomes reverse biased and prevents the current flow, only allowing a very small leakage current. In case the negative diode voltage reaches the breakdown voltage it conducts an avalanche current which with the presence of the breakdown voltage can destroy the device. The characteristic of the diode's operation is shown in Figure 2.1b.

Focusing on the forward characteristic in Figure 2.1b, the operation of the diode is highly dependent on temperature. For a certain current range below the nominal ratings of the semiconductor, the power diode is a Negative Temperature Coefficient (NTC) device meaning that the forward voltage drop  $v_F$  at the conducting state decreases with an increase of temperature, as illustrated in Figure 2.1. In the Positive Temperature Coefficient operating region (PTC), for current values close to the nominal ratings or above, the forward voltage drop  $v_F$  at the conducting state increases with the increase of temperature. Finally, there is the inflection point that belongs to the Zero Temperature Coefficient operating region (ZTC), where there is no influence of temperature on the conductivity of the semiconductor. The influence of temperature on  $v_F$  around the inflection point is smaller than for low current or for current close to the nominal ratings.

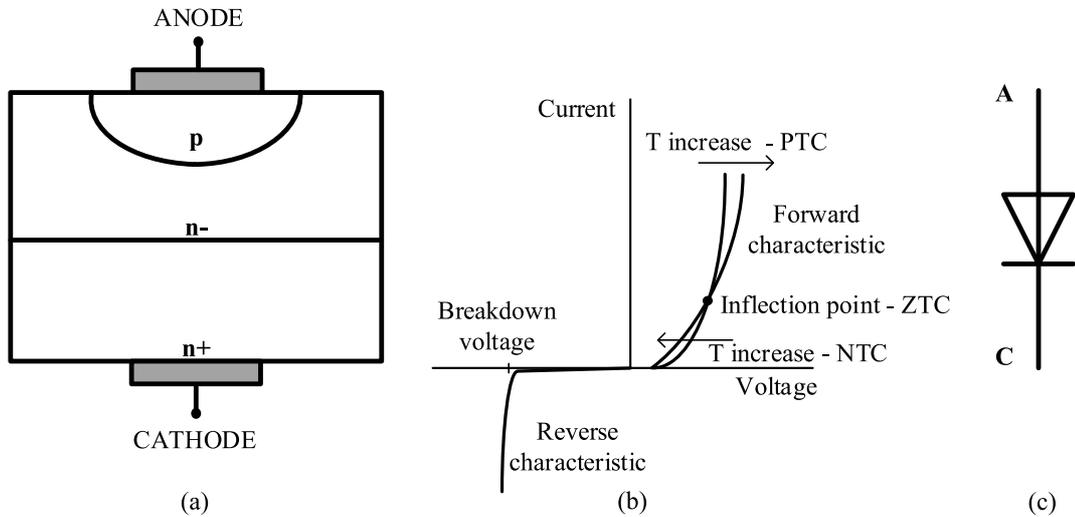


Figure 2.1: (a) Diode structure, (b) characteristic curve and (c) circuit symbol.

The influence of temperature in  $v_F$  can be demonstrated with [27]

$$v_F = \frac{2kT}{q} \ln\left(\frac{J_F W_d}{2q D_a n_i F \left(\frac{W_d}{L_a}\right)}\right) \quad (2.1)$$

### 2.3. Insulated Gate Bipolar Transistor structure and operation principle

and if the temperature derivative of  $v_F$  is calculated

$$\frac{dv_F}{dT} = \frac{2k}{q} \left( \ln\left(\frac{J_F W_d}{2q D_a n_i F\left(\frac{W_d}{L_a}\right)}\right) - \frac{T}{D_a n_i} \left( D_a \frac{dn_i}{dT} + n_i \frac{dD_a}{dT} \right) \right) \quad (2.2)$$

Focusing on the parameters that are influenced by temperature  $T$  in (2.2), the intrinsic carrier concentration  $n_i$  in  $\frac{dn_i}{dT}$  has a positive temperature coefficient and the ambipolar diffusion constant  $D_a$  in  $\frac{dD_a}{dT}$  has a negative temperature coefficient [28]. The behavior of the device with temperature along the current range is a result of the balance between these two parameters.

## 2.3 Insulated Gate Bipolar Transistor structure and operation principle

The Insulated Gate Bipolar Transistor (IGBT) [26] is a controllable device that allows unidirectional current flow. It has a pnpn structure formed by two cascade connected p-n junctions, as illustrated in Figure 2.2.

By only applying a positive voltage between the collector and the emitter leads, the device remains in the blocking state. If, additionally, a positive gate-emitter voltage  $v_{ge}$  that is at least at the level of the threshold voltage,  $V_{th}$ , of the device is applied to the gate-emitter leads, the IGBT allows current to flow. Except for direct voltage blocking capability the IGBT exhibits reverse blocking voltage capability and it can be designed for high reverse voltage levels. On the other hand, this is not a main design criterion. In fact, the IGBTs are, usually, connected with anti-parallel pin-diodes. Therefore, in many applications the negative voltage blocking capability is not a priority and can affect more important performance characteristics of the IGBT, such as the level of on-state voltage called saturation collector-emitter voltage,  $v_{ce}$  [1].

Figure 2.3 shows the IGBT characteristic curve for different  $v_{ge}$  values. During the turn-on phase of the semiconductor, the application and the increase of  $v_{ge}$  leads to a decrease of  $v_{ce}$  and the change in operation from the active region to the linear region. The device, finally, operates in saturation mode, where  $v_{ce}$  becomes smaller than  $v_{ge} - V_{th}$ . During the turn-off phase,  $v_{ce}$  increases as  $v_{ge}$  decreases and the current in the device goes to zero.

As illustrated in Figure 2.2a, the Punch-Through IGBT (PT-IGBT), [26], [29] is manufactured with an additional n region that is called buffer layer, in contrast to the Non-Punch-Through IGBT (NPT-IGBT) in Figure 2.2b where this layer is missing. The differences

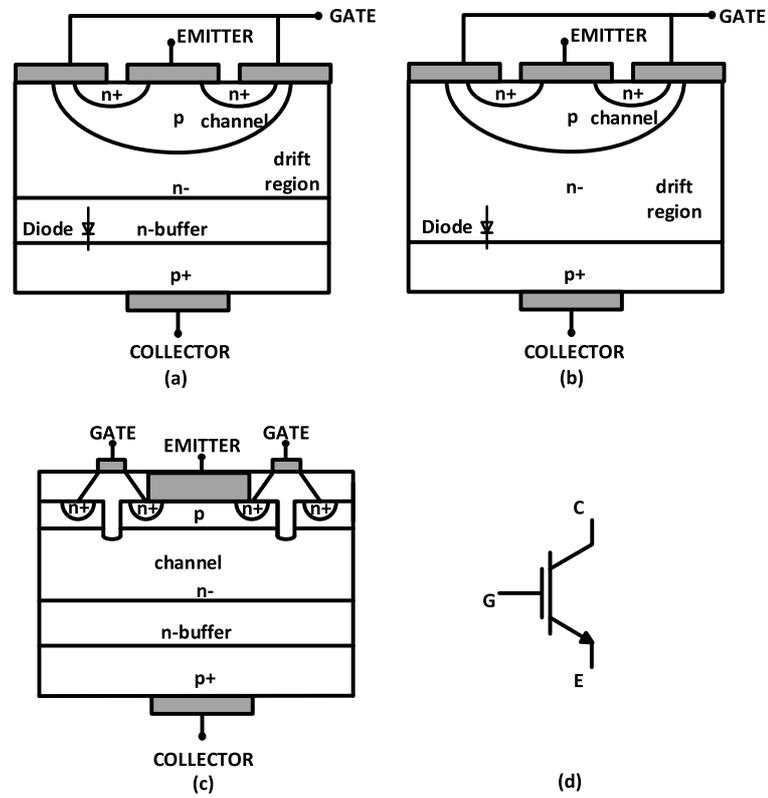


Figure 2.2: IGBT structure; (a) PT, (b) NPT, (c) Trench and (d) circuit symbol.

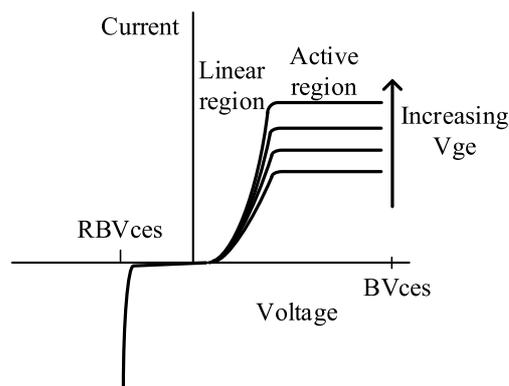


Figure 2.3: IGBT characteristic curve.

## 2.4. IGBT module structure

between the two planar-structured IGBT categories are summarized in Table 2.1. A PT-IGBT is not designed to block high reverse voltage due to the n+ buffer layer. In addition to the previous planar gate IGBT structures, the trench-gate IGBT [30] was proposed and developed by some manufacturers, Figure 2.2c. The advantage of this IGBT type compared to the PT structure is the reduced saturation voltage, while keeping switching losses low. Advancements of all these IGBT types are under ongoing research.

TABLE 2.1: Comparison of PT and NPT IGBT

Characteristic	PT	NPT
Relation with Temperature	NTC for low current, PTC for current close to nominal	mainly PTC
Conduction losses		higher for NPT at current close to nominal due to PTC
Short-circuit capability		higher for NPT
Parallelization	recommended only for high currents	Possible
Blocking voltage capability	low	high

In this application, IGBT of Soft-Punch-Through [31] technology is used that belongs to the PT family, has a structure with thinner buffer layer than a PT device and exhibits lower conduction and switching-off power losses than a NPT device [32]. For IGBTs [27], the dependence of  $v_{ce}$  on temperature resembles the pin-diode's that is, already, presented in the forward characteristic part of Figure 2.1b.

$$v_{ce} = \frac{2kT}{q} \ln\left(\frac{J_F W_d}{2q D_a n_i F\left(\frac{W_d}{L_a}\right)}\right) + \frac{p L_{CH} J_{CH}}{\mu_{EFF} C_{ox} (V_{gs} - V_{th})} \quad (2.3)$$

Similar to the diode case, focusing on the parameters that depend on temperature,  $n_i$  has positive temperature coefficient and  $D_a$  has negative temperature coefficient, whereas, from the second term of the sum, the mobility  $\mu_{EFF}$  and the threshold voltage  $V_{th}$  have positive temperature coefficients. Again, the behavior of the device with temperature change is a result of the balance between these temperature dependent parameters. For low current values, commonly up to the level of 1/4 of the nominal rating the device exhibits NTC behavior, whereas for higher current values it exhibits PTC behavior. Similar to the diode, the inflection point exists for the IGBT as well.

## 2.4 IGBT module structure

The module as a means of packaging for the IGBTs is used for applications at the medium-to-high power range and, usually, at a voltage level up to 6.5 kV. For higher voltage lev-

## Chapter 2. Methods for IGBT modules temperature estimation and aging detection

els and high-power applications the series connection of press-pack devices is a well-established solution [2] . The power module provides protection of the semiconductor devices and facilitates the mounting on the cooling plate, as well as the interconnection of the power electronic converter parts.

A typical structure of a silicon (Si) IGBT module with integrated anti-parallel diodes is illustrated in Figure 2.4.

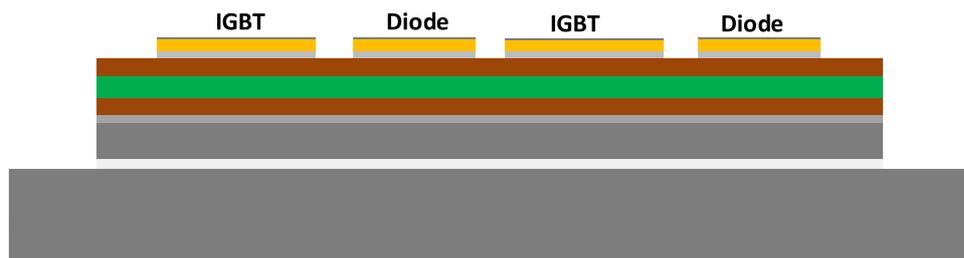


Figure 2.4: Power module structure.

A 3300V and 1200A open power module is illustrated in Figure 2.5. It consists of 6 substrates similar to the one in Figure 2.6. Each substrate consists of 4 IGBT chips and 2 diode chips. In Figure 2.6 the two springs at one side of the substrate correspond to the gate and emitter leads for the gate driver and the single spring at the left side is for the collector connection with the driver.

## 2.4. IGBT module structure

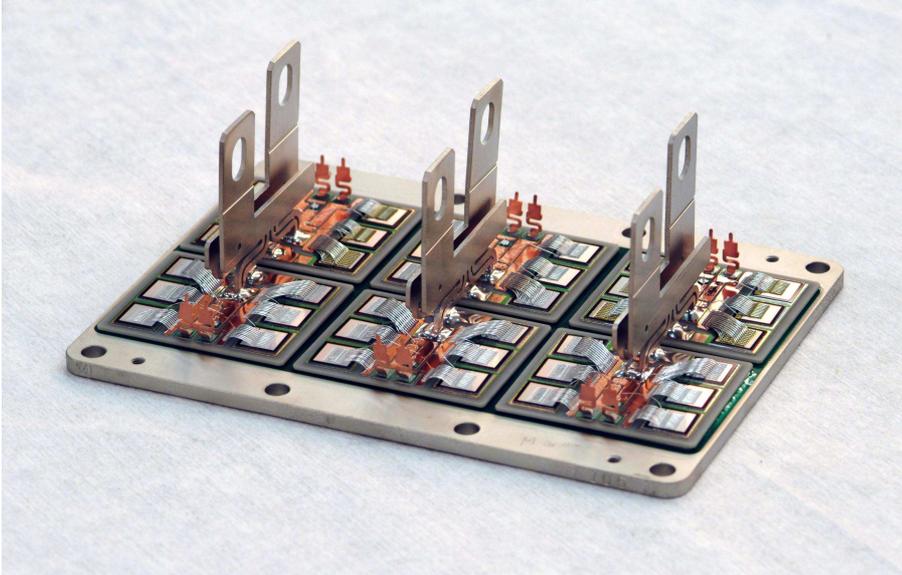


Figure 2.5: HiPak 3300 V/1200 A module (ABB property).

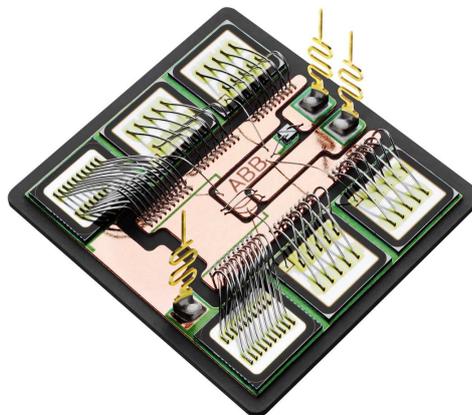


Figure 2.6: Substrate of HiPak 3300 V/1200 A module (ABB property).

The IGBT module is formed by the following layers that are illustrated in Figure 2.4 from top to bottom [33]:

- A thin aluminum metallization layer on top of the silicon chip assisting the chips

## Chapter 2. Methods for IGBT modules temperature estimation and aging detection

interconnection and the connection with the gate with the help of bond-wires, see, also, Figure 2.6

- Silicon chips as semiconductors
- Solder, usually an alloy of SnAg or Pb-Sn, for the connection of two consecutive layers. A replacement for the solder layers in some new power modules is the Ag sintered layer that exhibits a higher mechanical resistance and, also, ability to withstand higher temperatures than the conventional solder layer.

The next three layers compose the Direct-Bond Copper (DBC) part of the module:

- Copper (Cu) for the heat conduction produced at the silicon chip layer
- Insulation layer, for the IGBT module of this work it is an Aluminum Nitride (AlN) ceramic that withstands a high breakdown voltage to electrically isolate the different substrates and the cooling plate
- Copper for the heat propagation facilitation after the insulation layer
- Solder
- Baseplate, although it does not exist in all modules, usually AlSiC or Cu depending on the application. Normally, it is the thickest layer with the greatest heat storage capability among the layers. At the baseplate layer, the material selection depends on the load profile. The AlSiC baseplate exhibits the best heat storage capability and it is designated for current profiles with long duration, commonly traction applications.
- Thermal Interface Material (TIM) or thermal paste, for instance Si for the uniform contact between the baseplate and the heat sink or cooling plate surface to avoid air trapped in.

The three most important parameters for the material selection are the thermal conductivity, the heat storage capability and the thermal expansion coefficient. Table 2.2 lists these three thermal characteristics for the IGBT module layers. The materials with the worst thermal conductivity are those of the TIM with a thermal conductivity of  $1W/(mK)$ , the DBC insulating and the solder layer. The interconnections inside the module among the silicon chips and the gate and emitter pads for the control of the device are, traditionally, implemented with Al bond wires.

## 2.4. IGBT module structure

TABLE 2.2: Thermal characteristics for each of the power module layers at 25°C [33]

Material	Thermal conductivity [W/(m * K)]	Heat storage characteristic [kJ/(m <sup>3</sup> * K)]	Thermal expansion coefficient [10 <sup>-6</sup> /K]
Silicon	148	1650	4.1
Copper	394	3400	17.5
Aluminum	230	2480	22.5
Silver	407	2450	19
Molybdenum	145	2575	5
Solders	70	1670	15-30
Al <sub>2</sub> O <sub>3</sub> – DBC	24	3025	8.3
AlN DBC	180	2435	5.7
AlSiC (75% SiC)	180	2223	7

Among the materials in the structure of the IGBT module, the three dominant conductive materials in terms of thickness are Si, Cu and Al. The thermal conductivity of Si is significantly dependent on temperature, whereas for the other two the variation of thermal conductivity with temperature is very small. Table 2.3 shows the change of thermal conductivity for the usual operation temperature range between 25°C to 125°C for the three materials [34].

TABLE 2.3: Variation of thermal conductivity for the three dominant conductive materials in the IGBT module

	25°C	125°C
Silicon	148	98.9
Copper	401	396
Aluminum	237	240

Focusing on Si, this relation is described as [26]

$$\lambda = 24 + 1.87 * 10^6 T^{-1.69} \frac{W}{mK} \quad (2.4)$$

where the temperature  $T$  is illustrated in Figure 2.7

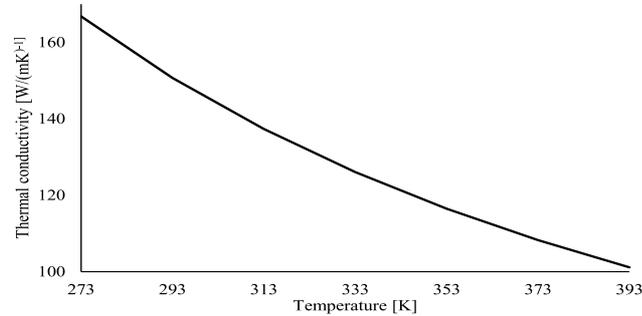


Figure 2.7: Relation of thermal conductivity with temperature for Si.

The thermal resistance and thermal capacitance defining the thermal conductivity and the heat storage characteristic of the material, respectively, are expressed

$$R_{th} = \frac{d}{\lambda A} \quad (2.5)$$

$$C_{th} = c\rho dA \quad (2.6)$$

where  $d$  is the thickness of the layer,  $\rho$  the Si density,  $\lambda$  the thermal conductivity of the material,  $A$  the chip surface area and  $c$  the specific heat capacity of the material.

## 2.5 Thermal stressing of IGBT modules

The thermal stressing of IGBT modules is caused by the power losses, comprising the switching and conduction losses produced by the IGBT and the anti-parallel diode. The following sections present the common method for power losses calculations and the main thermal stressing factors and aging mechanisms.

### 2.5.1 IGBT power losses calculation

#### IGBT conduction losses

The voltage drop of the IGBT at on-state is defined by the potential along the pn-junction, the p-channel and the drift region, Figure 2.2, [28],[26]. In the NTC operating region

## 2.5. Thermal stressing of IGBT modules

compared to the nominal ratings of the device the voltage drop is, mainly, caused by the pn-junction. At a higher current level belonging to the PTC operating region, the drift region is considered to have a resistive behavior and the voltage drop across it dominates the IGBT collector-emitter voltage. A general model for the IGBT collector-emitter voltage is expressed as

$$v_{ce} = V_{ce,0}(T) + r_c(T, i_c)i_c \quad (2.7)$$

where  $V_{ce,0}$  the zero-current voltage drop across the pn junction is linearly dependent on  $T$ ,  $r_c$  the equivalent resistance of the drift region and the p-channel depending on the temperature and the collector current  $i_c$ . The instantaneous conduction losses of an IGBT-based power module are, typically, calculated

$$p_{con,i,in} = V_{ce,0}i_c + r_c i_c^2 \quad (2.8)$$

For the average conduction losses

$$P_{con,i,av} = \frac{1}{T} \int_0^T v_{ce} i_c dt \quad (2.9)$$

where  $T$  is the time period for the losses calculation. With the help of (2.7) the average conduction losses along a cycle are expressed as

$$P_{con,i,av} = V_{ce,0}I_{c,av} + r_c I_{c,rms}^2 \quad (2.10)$$

where  $I_{c,av}$  and  $I_{c,rms}$  are the average and RMS current of the semiconductor, respectively.

The value of  $V_{ce,0}$  and of the channel resistance can be calculated with the help of the datasheet using the slope of the  $i_c(v_{ce})$  curve at a current close to nominal, provided that the semiconductor operates at this current level [35]. The  $i_c(v_{ce})$  curve is typically provided at least for 2 temperature levels, usually, 25C° and 125C°.

The datasheet, often, lacks the  $v_{ce}$  values for current levels at the low current NTC operating region. A linearization is, often, used for this operating region. The approximation is illustrated in Figure 2.8b using the datasheet of the IGBT module ABB 5SNA 1600N170100 [36]. The value of  $v_{ce}$  with a sensing current at the level of 1A for this IGBT module that is used for this work can be used for the estimation of  $V_{ce,0}$ .

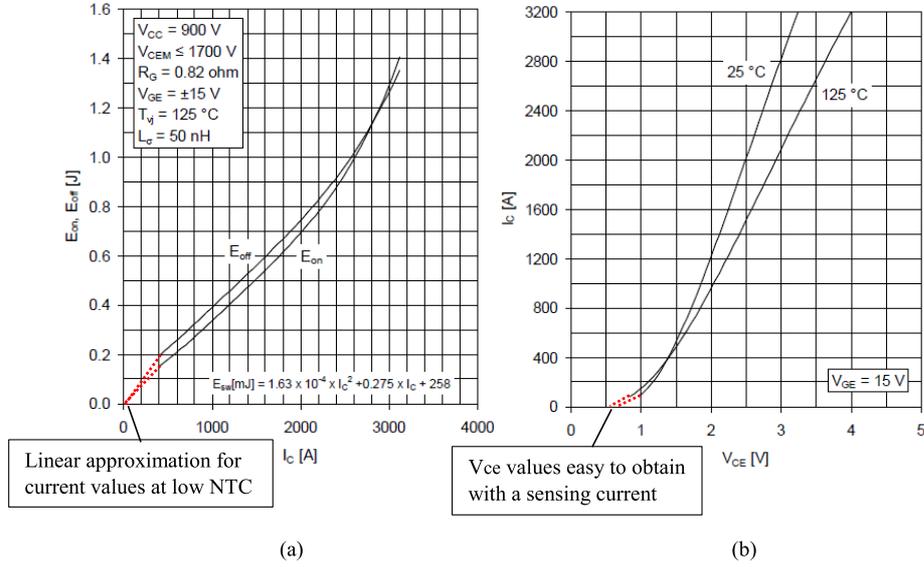


Figure 2.8: (a) Switching energy losses curves as a function of  $i_c$  for ABB 5SNA 1600N170100 and approximation for low NTC operating region current value and (b)  $i_c$  as a function of  $v_{ce}$  curve for ABB 5SNA 1600N170100 and approximation for low NTC operating region current value.

### IGBT switching losses

The switching losses are defined as the energy produced during the semiconductor device turn-on and turn-off phase, as shown in Figure 2.9. For the switching losses measurement, it is needed to define the time window in which the voltage and current are recorded. According to [37], the losses are measured within the time instants of Figure 2.9 that are presented in Table 2.4.

The reverse recovery effect of the diode that is part of the commutation process [38] between the diode and the IGBT of the same leg results in an over-current of the IGBT at the turn-on phase. The over-voltage at the IGBT turn-off phase is caused by the leakage inductance of the power circuit.

TABLE 2.4: Turn-on and off measuring instances.

Turn-on energy loss		Turn-off energy loss	
$t_{on,1}$	$t_{on,2}$	$t_{off,1}$	$t_{off,2}$
$v_{ge} = 0.1v_{g,on}$	$v_{ce} = 0.02V_{cc}$	$V_{ge} = 0.9v_{g,on}$	$I_c = 0.02i_c$

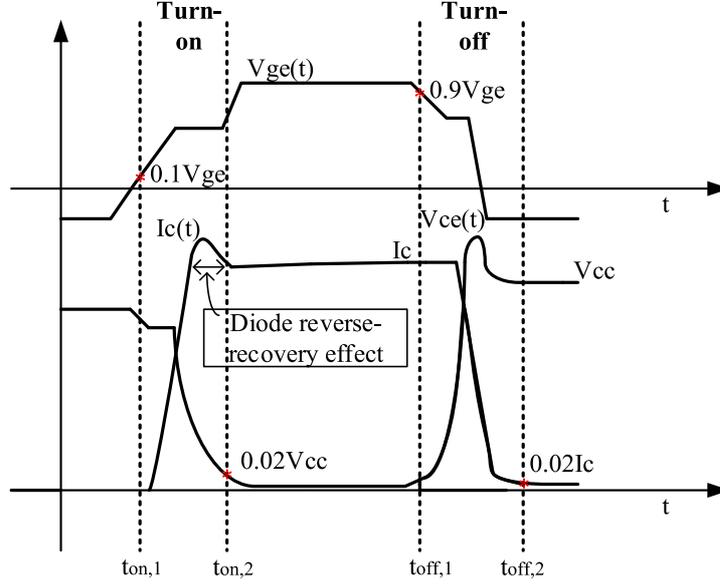


Figure 2.9: Switching power losses measurement.

As an example, the energy loss of a switching-on event can be calculated

$$E_{sw,i,on} = \int_{t_{on,1}}^{t_{on,2}} v_{ce} i_c dt \quad (2.11)$$

where the time interval between the time instants  $t_{on,1}$  and  $t_{on,2}$  is considered for the losses estimation. The turn-off energy loss per switching event  $E_{sw,i,off}$  is calculated accordingly using the time instants of Figure 2.9 and Table 2.4.

The switching energy loss can be calculated based on the power module datasheet information, where the reference values for the switching voltage and current are provided, or with the help of the curves such as Figure 2.8a. The calculation at the voltage and current level of the application is defined by [35]

$$E_{sw,i} = E_{sw,i,ref} \left( \frac{I}{I_{ref}} \right)^{K_i} \left( \frac{V_{DC}}{V_{DC,ref}} \right)^{K_v} (1 + TC_{sw}(T_j - T_{j,ref})) \quad (2.12)$$

where  $E_{sw,i,ref}$  is the value of switching losses measured at a reference current and voltage  $I_{ref}$  and  $V_{DC,ref}$ , respectively, current factor  $K_i$  that is considered equal to 1, voltage factor  $K_v$  that ranges from 1.2 to 1.4,  $I$  and  $V_{DC}$  the values of current and voltage of the actual

application,  $TC_{sw}$  the temperature coefficient equal to 0.003,  $T_j$  the junction temperature and  $T_{j,ref}$  the junction temperature at reference conditions. Similar to the conduction losses case, the IGBT module datasheet lacks the switching losses values for current levels at the low current NTC operating region. If there is no prototype converter to measure the losses, a linearization is a commonly used for the switching losses estimation at different voltage and current levels [39], and, especially, in the low NTC operating region, as shown in Figure 2.8a.

It is deduced that even using the datasheet values, the results cannot match exactly with the operation, since almost no parameter in the actual application will have the same value as the one in the measuring process. For instance, the increase of external gate resistance values leads to longer switching dynamics and, as a result, to higher switching losses [40].

The average switching power losses can be calculated with the help of (2.19) for a given switching frequency  $f_{sw}$

$$P_{sw,i,av} = f_{sw} \left( \int_{t_{on,1}}^{t_{on,2}} v_{ce} i_c dt + \int_{t_{off,1}}^{t_{off,2}} v_{ce} i_c dt \right) \quad (2.13)$$

### IGBT blocking losses

The instantaneous power losses at blocking state can be calculated with the help of [41]

$$p_{block,i} = V_{ces} i_{ces} 2^{\frac{T_j - T_0}{\Delta T_d}} \quad (2.14)$$

where  $T_j$  is the junction temperature,  $T_{j,ref}$  is the reference temperature from the datasheet and  $T_d$  is the constant with the rule of thumb that states that  $i_{ces}$  doubles with every increase of 11 C° and considering the duty cycle  $D$  the average blocking losses become

$$P_{block,i,av} = V_{cc} i_{ces} 2^{\frac{T_j - T_{j,ref}}{\Delta T_d}} (1 - D) \quad (2.15)$$

The IGBT blocking losses are not considered for the voltage and the temperature level of this work. Based on the example [41] for a 6.5kV IGBT module, the blocking losses due to the collector cut-off current or leakage current  $i_{ces}$  could be considerable with a junction temperature close to the upper operating limit in case of insufficient cooling or inappropriate IGBT module mounting on the cooling plate.

## 2.5.2 IGBT antiparallel-diode switching and conduction losses

Similar to the IGBT conduction losses, the diode forward voltage  $v_F$  and the conduction instantaneous and average losses are calculated [35]

$$v_F = V_{F,0} + r_D(T, i_F)i_F \quad (2.16)$$

$$p_{con,d,in} = V_{F,0}i_F + r_D i_F^2 \quad (2.17)$$

$$P_{con,D,av} = V_{F,0}I_{F,av} + r_D I_{F,rms}^2 \quad (2.18)$$

where  $V_{F,0}$  the zero current voltage drop,  $r_D$  the equivalent resistance,  $i_F$  the diode forward current,  $i_{F,av}$  the average forward current and  $i_{F,rms}$  the RMS forward current.

The diode reverse-recovery energy losses of a switching instant, as illustrated in Figure 2.9, are calculated with the help of

$$E_{rec,D} = \int_{t_{rr,1}}^{t_{rr,2}} v_F i_F dt \quad (2.19)$$

where the integral is defined for the time duration of the reverse-recovery effect in Figure 2.9.

The switching energy loss can be calculated based on the power module datasheet information, where the reference values for the switching voltage and current are provided. The calculation at the voltage and current level of the application is defined by [40]

$$E_{sw,D} = E_{sw,D,ref} \left( \frac{I}{I_{ref}} \right)^{K_i} \left( \frac{V_{DC}}{V_{DC,ref}} \right)^{K_v} (1 + TC_{sw}(T_j - T_{j,ref})) \quad (2.20)$$

where  $K_i$  that is considered equal to 0.5 to 0.6,  $K_v$  that is equal to 0.6,  $TC_{sw}$  equal to 0.005 to 0.006. Similar to the IGBT case, a linear approximation is usually the choice for the calculation at different current and voltage levels.

### 2.5.3 Main thermal-stressing factors and aging mechanisms

The thermal stressing of power electronic modules that is caused by their own power losses during operation is one of the factors that determine their lifetime. Several studies, which are based on accelerated testing of IGBT modules, demonstrate that the three main thermal stressing parameters are the maximum, minimum or mean temperature level,  $T_{j,max}$ ,  $T_{j,min}$  or  $T_{j,mean}$ , respectively, the temperature variation during the power cycle  $\Delta T_j$  and the power pulse duration  $t_{on}$  or heating time, [42], [43], [44], [45].

The relation of lifetime in terms of number of cycles for a specific temperature profile at junction level is expressed with the following equations. Firstly, in chronological order, is the equation proposed in [8] which, additionally to the aforementioned parameters, includes structural characteristics of the IGBT module such as the diameter of each bond-wire  $D_b$ , the current level per bond-wire  $I$  that depends on the number of bond-wires per chip and the blocking voltage of the chip  $V$ .

$$N_f = A \Delta T_j^n \left( \frac{\beta_2}{T_{j,min}} \right) t_{on}^{\beta_3} I^{\beta_4} V^{\beta_5} D_b^{\beta_6} \quad (2.21)$$

where  $A$ ,  $\beta_2$ ,  $\beta_3$ ,  $\beta_4$ ,  $\beta_5$  and  $\beta_6$  are constants.

The most recent equation by Semikron adds extra structural characteristics such as the bond-wire aspect ratio  $ar$  that is the ratio between the maximum height of the bond-wire and the distance between the two connections points of the bond-wire with the module surface [46]

$$N_f = A_c \Delta T_j^{-n} (ar)^{\beta_1 \Delta T_j + \beta_0} \left( \frac{C + (t_{on})^\gamma}{C} \right) \left( \frac{E_\alpha}{k_B T_{j,mean}} \right) f_{diode} \quad (2.22)$$

where  $E_\alpha$  is the activation energy,  $k_B$  the Boltzmann's constant and  $A_c$ ,  $\beta_1$ ,  $\beta_0$ ,  $f_{diode}$ ,  $\gamma$  and  $C$  are constants. This model concerns sintered chips.

Figure 2.10 illustrates extrapolated IGBT lifetime curves based on [42]. It shows the relation between the IGBT number of cycles and the temperature variation for two levels of maximum junction temperature. The influence of  $\Delta T_j$  in lifetime is greater than the influence of  $T_{j,max}$ .

The main aging mechanisms originating from thermal stressing are [43]:

- Bond wire lift-off or heel-cracking illustrated in Figure 2.11. It results from the heating cycles when current is flowing in the bond-wires that are usually made of

## 2.5. Thermal stressing of IGBT modules

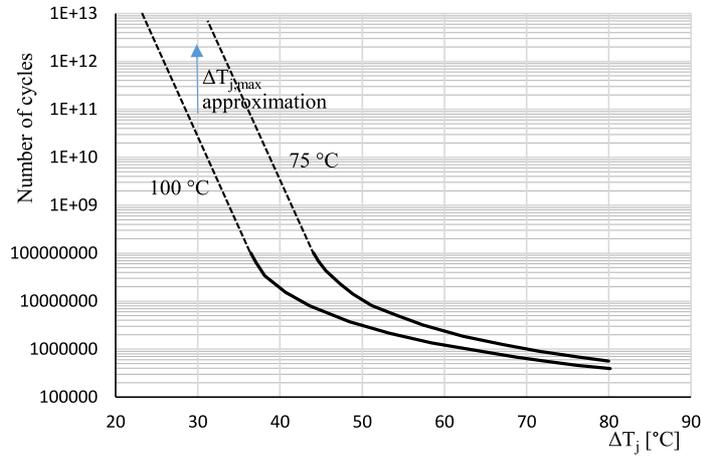


Figure 2.10: Lifetime curves of IGBT modules [42]

aluminum. New products with copper bond wires have been proposed by manufacturers [47] providing lower thermal expansion coefficient and higher electrical and thermal conductivity. However, the material cost and ecological footprint is a disadvantage of this solution [48].

- Chip-DBC or DBC-baseplate solder fatigue due to crack formation, as illustrated in Figure 2.12. The solder cracks result from the different thermal expansion coefficients between two consecutive layers.

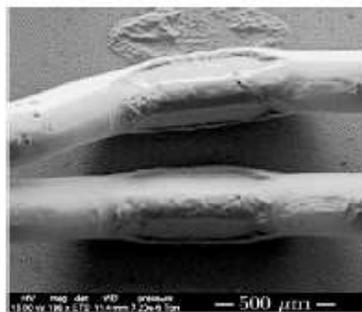


Figure 2.11: Bond-wire lift-off captured with Scanning Electron Microscopy (SEM) [49].

According to [43], the solder fatigue has a strong connection with  $t_{on}$  and a weaker connection with  $\Delta T_j$ . Bond-wire lift-offs have a strong connection with  $\Delta T_j$  but  $t_{on}$  does not

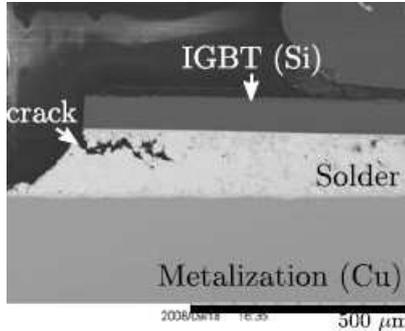


Figure 2.12: Chip solder fatigue captured with SEM [49].

seem to be critical judging from the results of the accelerated lifetime tests. The impact of  $T_{j,mean}$  seems to be the less significant for the main aging mechanisms. The greater impact of  $\Delta T_j$  compared to the impact of  $T_{j,mean}$  or  $T_{j,max}$  is evident from lifetime curves of manufacturers demonstrating the number of cycles for different levels of  $\Delta T_j$  and  $T_{j,max}$ , for instance [42]. It is crucial to form all the layers with thermal expansion coefficient values as close as possible to each other, as presented in Table 2.2, in order to have a uniform expansion and contraction for the materials and avoid solder cracks.

## 2.6 Experimental methods for indirect IGBT junction temperature measurement

The junction temperature estimation is necessary for the thermal stressing evaluation and the lifetime estimation of the IGBT modules, as described in the previous section. As already mentioned in Chapter 1, the temperature estimation can be obtained with measurements of TSEPs [12]. The IGBT module is characterized in the expected operating temperature range, in order to obtain the relation between the TSEP and the temperature. The temperature estimation with the help of TSEP is considered as an indirect temperature measurement method.

The main TSEPs that are presented so far in the literature are the saturation voltage  $v_{ce}$  with load current [13],  $v_{ce}$  with sensing current [18], the threshold voltage  $V_{th}$  [14], the internal gate resistance  $R_{int}$  [15], the short-circuit current  $I_{sc}$  [19], the turn-on delay  $t_{on,d}$  and the turn-off delay  $t_{off,d}$  or  $dv/dt$  [16], [17]. The main characteristics of each method are presented in Table 2.5. The sensitivity of the  $v_{ce}$  method with load current varies with the current level depending on the operating region, as illustrated with the help of (2.1).

## 2.6. Experimental methods for indirect IGBT junction temperature measurement

This method requires a high calibration effort due to the dependence to many parameters such as  $v_{ge}$ , current and the temperature dependence of the module parasitic resistance  $R_{par}$ . The sensitivity of the  $v_{ce}$  method with sensing current is at the level of  $2mV/^\circ C$ . The method exhibits high accuracy because it is, practically, independent of the DC-link voltage and of the load current as well as of the modules parasitics due to its low level current at the level of 1/1000 of the nominal current [26]. It has a simple calibration procedure by using a thermal chamber, setting the temperature at different levels and measuring  $v_{ce}$  with a specific sensing current at every temperature level. However, the  $v_{ce}$  measurement with sensing current and without load current flowing in the semiconductor can, only, be realized, if the semiconductor is isolated from the rest of the power circuit. Therefore, it is necessary to modify the power circuit and to stop the power electronic converter's normal operation. The  $V_{th}$  method can, potentially, have low calibration requirements, but it is dependent on gate parasitic inductance  $L_{G,\sigma}$ , gate internal  $R_{int}$  and external resistance  $R_{ext}$ . The measurement requires precise timing and high bandwidth of the measuring circuit. The peak gate current method is based on the temperature dependence of  $R_{int}$ . The sensitivity depends on the manufacturer and the semiconductor technology, since the value  $R_{int}$  varies. The measurement needs precise timing and the design of the measuring circuit is linked to the gate driver's design.

TABLE 2.5: Main methods for indirect IGBT junction temperature of measurement based on TSEP

TSEP	Sensitivity / calibration effort	Measuring circuit particularities	Power circuit modifications	Dependence
$v_{ce}$ load current	depends on operating region / high	-	-	$v_{ge}, i_c$ , module parasitics and power leads
$v_{ce}$ sensing current	$2mV/^\circ C$ / low	-	necessary for IGBT isolation	-
$V_{th}$	$4mV/^\circ C$ / high	precise timing	-	$R_{int}, R_{ext}, L_{G,\sigma}$
Peak gate current	depends on manufacturer, $3mV/^\circ C$ / low	precise timing	-	Depends on gate driver design
$I_{sc}$	$0.345A/^\circ C$ / High	-	By-pass switch	-
Switching time ( $t_{on,d}, t_{off}$ )	$2ns/^\circ C$ / high	fast and precise timing	-	gate drive design circuit parasitics

The method that is based on the short-circuit current  $I_{sc}$  has a sensitivity of approximately  $0.3A/^\circ C$  meaning that it needs very precise measurement for high currents. The short-circuit current has a cumulative degradation effect on the gate oxide. Additionally, this method requires additional by-pass switches, in order to create the short-circuit path. This method depends on  $v_{ge}$  and the configuration for short-circuit protection of the gate driver as well as on the parasitics of the circuit. Finally, the methods that are based on the switch-

ing of the semiconductor have a sensitivity of  $2nS/^{\circ}C$  that sets the requirement for a very fast and precise measuring circuit. Additionally, the calibration effort is high.

In conclusion, all the methods except for the  $I_{sc}$  method and  $v_{ce}$  with sensing current can be applied without power circuit modifications. They can potentially monitor the temperature online and without intermissions of the power electronic converter's operation. On the other hand, the methods based on  $V_{th}$ , on the peak gate current and on the switching times put extra requirements on the gate driver and cannot be directly applied to a power stack after its development phase has finished. To use  $v_{ce}$  with high current is promising but the dependence on many parameters causes a high calibration effort. The  $v_{ce}$  method with sensing current seems to offer great accuracy without significant calibration effort due to the absence of dependence parameters provided that non-intermittent operation of the power electronic converter is not a requirement. As mentioned in Chapter 1, for the specialized application at CERN, where a series of power electronic converters have to be tested during factory acceptance tests and service stops throughout their lifetime, the  $v_{ce}$  method with sensing current can be applied. For this application, the online monitoring due to the predefined load profiles is not necessary. The calibration of the IGBT modules is simple with this method, but it is an issue if it has to be implemented in an already assembled power stack. In Chapter 4, a solution is proposed for fast calibration using the  $v_{ce}$  method with sensing current.

### 2.6.1 Aging detection of IGBT modules with $v_{ce}$ measurement

The second challenge for this work, after estimating the junction temperature, is the aging detection of the IGBT modules and the separation of the aging mechanisms. The aging detection in this work is focused on the aging mechanisms of bond-wire lift-off and solder delamination. An indicator of bond-wire lift-off, which is, extensively, tested in laboratory conditions, is the small increment of  $v_{ce}$  with high current at the level of a few  $mV$  [50], [24], [23], [13] and [51]. A great advantage of this method is that it can be implemented with the same measuring circuit as the  $v_{ce}$  method with sensing current, benefiting in terms of measuring circuit development and power stack testing effort.

The effect of resistance increase is amplified at a current level close to the nominal rating. This increment results from the increase of the parasitic resistance, when a few bond-wires serving as parallel current paths are lifted off [24]. On the other hand,  $v_{ce}$  measurement in a current close to the nominal rating is highly dependent on junction temperature affecting the precision of the measurement even with a small temperature change

Solder crack results in a change of the thermal path reducing the module's ability to trans-

## 2.6. Experimental methods for indirect IGBT junction temperature measurement

mit the produced heat from chip level to the cooling medium. The junction temperature under the same operating conditions increases, if solder crack occurs. Solder delamination detection leads, also, to a  $v_{ce}$  increase for current levels in the PTC operating region, whereas it leads to a  $v_{ce}$  reduction in the NTC operating region. By using  $v_{ce}$  with load current as an aging indicator, the aging mechanisms are more difficult to distinguish when operating in the NTC operating region. In the NTC operating region, the bond-wire lift-off and the solder delamination electrical effects can overlap and disguise each other due to the fact that the former aging mechanism leads to an increase of  $v_{ce}$  whereas the latter results in a  $v_{ce}$  reduction [52], due to the increase of the thermal resistance in the heat propagation path. As a result, the  $v_{ce}$  reduction due to solder delamination may not be detected if bond-wire lift-offs occur causing  $v_{ce}$  to increase. At the same time a  $v_{ce}$  increase in the PTC operating region could not be directly linked to anyone of the two aging modes.

The TSEP-based methods that are presented in section 2.6 can, potentially, detect, even online, the junction temperature change due to solder crack. Another proposed method for the solder crack detection uses a baseplate temperature sensor [53], in order to calculate the temperature at junction level with the help of electro-thermal models called Lumped Parameter Network (LPN) models. The LPN models are presented later in this chapter. This method requires a very accurate sensor and precise power loss estimations, in order to calculate the temperature at junction level. Additionally, the temperature dynamics at junction level are filtered out at the baseplate level.

The results in [53] have shown that a typical increase in the IGBT module thermal resistance  $R_{th}$  of 20% leads to a case temperature rise of about  $1.5^{\circ}C$  for the inverter system tested, and this corresponds to a maximum  $9^{\circ}C$  increase of the junction temperature. The junction temperature increase of  $9^{\circ}C$  is significant and an earlier aging detection would be necessary. Therefore, more accurate baseplate temperature measurements that can be, clearly, related to the solder cracks should be conducted.

The methods using  $v_{ce}$  with sensing or high current are selected in this work to be the most suitable for the detection of the two main aging mechanisms, if the non-intermittent operation is not a requirement for the application. The characteristics of the specialized application are presented in Chapter 3. The  $v_{ce}$  method with sensing current can provide an adequate level of accuracy for the temperature estimation needed for the solder crack detection, whereas the  $v_{ce}$  method with load current provides clear indications of bond-wire lift-off.

## 2.6.2 Power circuits for aging detection using $v_{ce}$ measurement

Recent methods have been presented in the literature for the IGBT modules' aging detection by using  $v_{ce}$  measurements with sensing or load current. These methods are used in accelerated lifetime tests or they are presented as potential solutions for field applications.

A circuit incorporating  $v_{ce}$  measurements with both high and sensing current measurements, Figure 2.13a, has been proposed in [24]. The measurement at high current is followed by a measurement with sensing current, in order to make the necessary corrections for the high current  $v_{ce}$  method and to indirectly measure the junction temperature. By combining again  $v_{ce}$  measurements with sensing and high current and by using the same set-up as in Figure 2.13b, it is proposed in [54] that a solder delamination can be detected based on the thermal resistance  $R_{th}$  estimation with sensing current. The thermal impedance is calculated

$$Z_{th}(t) = \frac{T_j - T_c}{P_{loss}} \quad (2.23)$$

where  $T_j$ ,  $T_c$  is the junction and case temperature, respectively, and  $P_{loss}$  are the power losses produced by the device.

The requirement of a high current source and a blocking IGBT module in series as well as the need for an extra sensor at the baseplate level for  $R_{th}$  calculation makes this method less suitable for already developed power stack designs. Depending on the application the high-current source may have to have several times higher ratings than for the low power application in [54] and [24], as it is the case for the application of interest.

In Figure 2.13b [22], the DUT disconnection for the  $v_{ce}$  method with sensing current becomes complicated by adding four switches, their driving circuits and logic for the switching sequence, in order to redirect the load current for a few switching periods. Accordingly, it is inconvenient to connect and control switches in series with an inductive load during technical visits to suppliers. Using the same principle, the method in [23] combines the  $v_{ce}$  methods with sensing and load current for aging detection due to bond-wire lift-off or solder delamination. In this case, the calculation of the thermal resistance for the aging evaluation requires measurements with high current, at the same point of a sinusoidal current profile and at the same temperature conditions, as well as a sensor at baseplate level. To produce a sinusoidal output it is required to control the power electronic converter and to have an output filter.

As already mentioned, the  $v_{ce}$  measurement with high current for bond-wire lift-off detection is highly dependent on temperature and, in addition, the influence of the inter-

## 2.6. Experimental methods for indirect IGBT junction temperature measurement

connections resistance to the measurement has to be defined. The method in [55] that is illustrated in Figure 2.13c is proposed for bond-wire lift-off detection in low power IGBT devices based on  $v_{ce}$  measurement in the ZTC operating region. The detection in the ZTC operating region for low power IGBT devices was, also, demonstrated in [56] and [57]. No temperature estimation can be achieved in this current operating region, therefore this method does not detect solder cracks. For all the aforementioned methods, an additional difficulty that has not been brought out in the literature is the calibration of the IGBT modules at sensing and at load current in an already assembled power stack and without modifying the circuit.

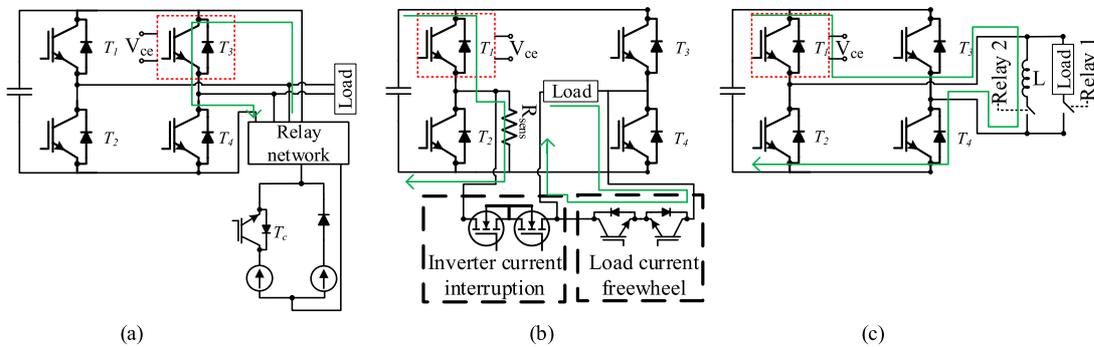


Figure 2.13: Power circuits for aging detection of IGBT modules using the  $v_{ce}$  method with sensing or load current: (a) power circuit with additional high-current source and relays for  $v_{ce}$  method with sensing and load current [24], (b) power circuit with current redirection for  $v_{ce}$  method with sensing and load current [22], (c) power circuit with test inductor only for  $v_{ce}$  method with load current in the ZTC operating region [55].

For the application of interest, a method offering adequate precision with minimum dependence to other parameters, as well as ease of implementation without power stack modifications and connection of extra power components is desired for the assessment of the power stack's integrity along its lifetime.

### 2.6.3 Circuits for $v_{ce}$ measurement with load and with sensing current

#### State-of-the-art of $v_{ce}$ measuring circuits

The design of a  $v_{ce}$  measuring system is an important step for the aging and temperature monitoring of IGBT modules. The structure of a  $v_{ce}$  measuring system generally comprises the protection stage, the isolation stage and the signal adaptation stage. Figure 2.14

presents the trends for the circuits that have been proposed so far. The circuit in Figure 2.14a [22] is based on the connection of the DC-link in series with the DUT (IGBT1 or IGBT2). A MOSFET (AS2 or AS1), is connected in series with a precision resistor to bypass the IGBT in parallel and to adjust the sensing current flowing through the other IGBT of the leg. No extra current source is needed, but the DC-link voltage value must remain constant to guarantee the correct sensing current value. It is not oriented to real applications with a varying DC-link. The input voltage to the measuring system is clamped with the use of ASC1-Rc1 and ASC2-Rc2 for the upper and lower IGBT, respectively, to protect the measuring circuit from the DC-link voltage that is applied to the IGBT when it is at off-state. This measuring system requires synchronized switching of three MOSFETs and the appropriate resistors per DUT. The circuit in Figure 2.14b like the circuit Figure 2.14a, uses extra switches, in this case depletion MOSFETs, to protect the measuring stage from the power circuit [25]. The resistor in series to the MOSFET guarantees that the potential  $v_{gs}$  becomes negative and the switch is turned-off when the DUT stops conducting. Similarly, another measuring system is patented based, again, on transistors for the high-voltage blocking and on resistive voltage divider, see Figure 2.14g [58].

## 2.6. Experimental methods for indirect IGBT junction temperature measurement

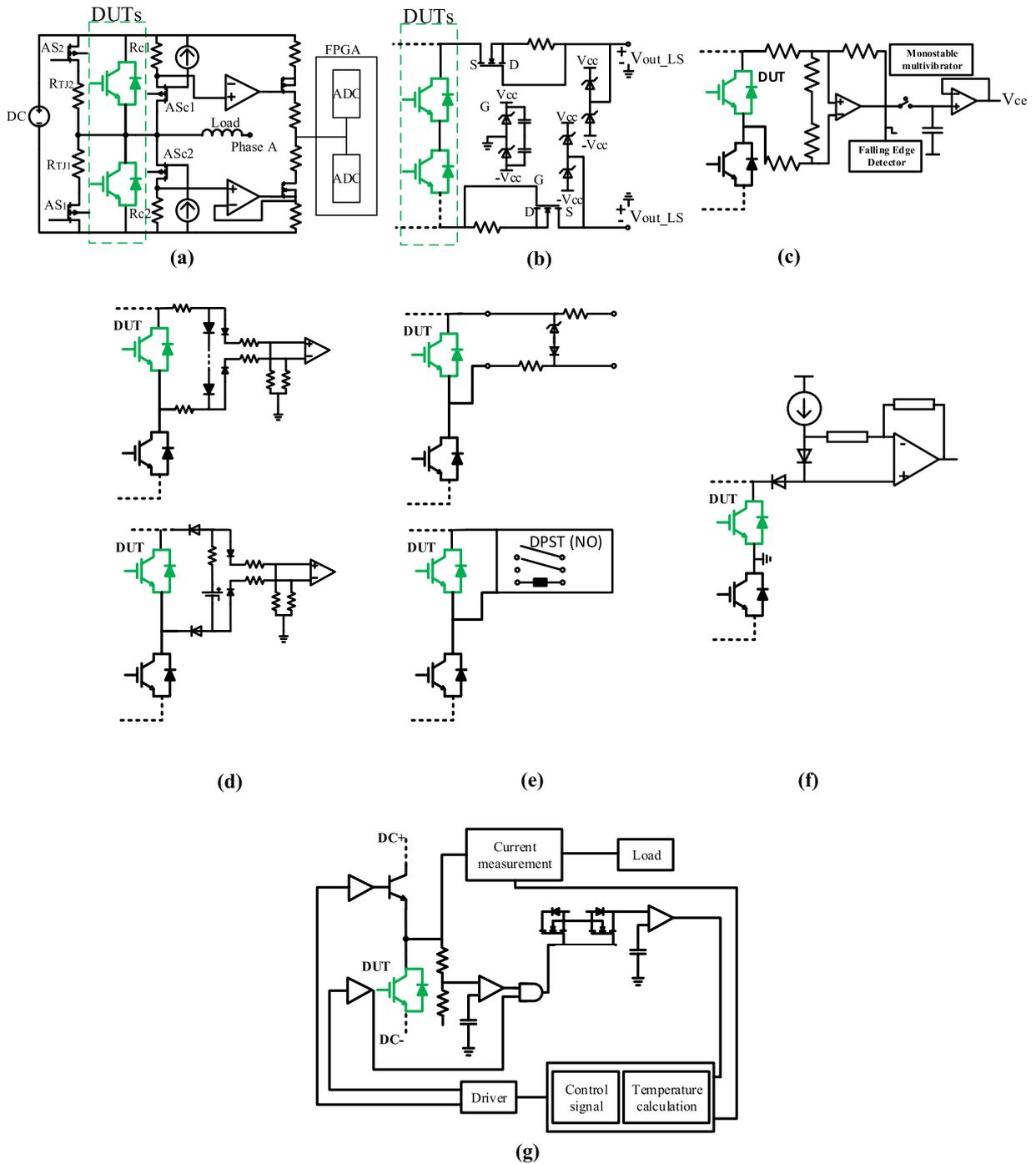


Figure 2.14: Trends of  $v_{ce}$  measuring systems for medium and high voltage IGBT modules- With green the DUTs used for  $v_{ce}$  measurement. Circuits in Figures (a), (b), lower (e), and (g) use additional switches whereas (c), (d), upper (e) and (f) use passive elements.

This circuit is developed to provide the calculated temperature at load current to the controller and adapt the control action according to the thermal stressing of the device. It comprises a voltage divider that is used for the detection of the IGBT entrance into saturation and two MOSFETs for the high-voltage blocking that connect the IGBT collector to the input of an amplifier.

The circuit in Figure 2.14c consists of two voltage dividers to limit the input to the operational amplifier, a falling edge detector to detect when the DUT is conducting and a monostable multi-vibrator to give the command for the measurement to start [59]. The main concern for this circuit is the right choice of the voltage dividers values and of the correct gain tuning for the operational amplifier, in order to be able to measure the saturation voltage, the voltage dividers frequency response and the delay configuration of the multi-vibrator. No current source is needed for this solution, if it is targeted for the  $v_{ce}$  method with load current.

The upper circuit of the pair of circuits in Figure 2.14d is based on a series of diodes to clamp the high voltage [60]. When the DUT is conducting, the measured  $v_{ce}$  is lower than the sum of the forward voltage drops of the diodes. The rise of the current through the diodes with the DC-link voltage increase leads to the proposal of the lower circuit voltage in Figure 2.14d, where a voltage source is applied across the DUT when it is conducting. The  $v_{ce}$  measurement results from the subtraction of the voltage source level and the forward voltage of the two diodes. The upper circuit of the pair of circuits in Figure 2.14e is based on a Zener diode and two resistors that limit the current, when the DUT is blocking [61]. One of the circuits proposed in this work is based on the same principle and is analyzed in Chapter 4. As an alternative for the measuring system protection and in order to avoid the power losses produced by the Zener diode, when the DUT is blocking, a relay is proposed for operation at high DC-link voltage levels.

The circuit of Figure 2.14f [62] is based on the desaturation protection circuit that is integrated into the IGBT drivers as an overcurrent and short-circuit protection [63]. It is designed for the  $v_{ce}$  measurement with high current. A current source is injecting a constant low current of  $10mA$  to the blocking diodes D1 and D2 creating a current loop when the DUT is conducting. The operational amplifier outputs  $v_{ce}$  by subtracting two times the voltage drop of one blocking diode from its input voltage. The main concern for this circuit is the calibration and the thermal coupling of the two diodes, in order to ensure equal forward voltage values for the same injected current. Furthermore, two precision current sources with fast settling time comparing to the switching period would be needed, if this circuit was used for the  $v_{ce}$  method comprising a sensing current.

Considering the implementation complexity, the measuring systems that are based on Zener or pin-diodes are advantageous in terms of number of components that are needed.

## 2.6. Experimental methods for indirect IGBT junction temperature measurement

Concerning the measurement precision and the calibration effort, the characterization effort can be limited by using components which exhibit well defined characteristics in the operating region of interest. It is a key element for the specialized application to develop measuring circuits that require minimum effort of calibration and simple operation.

### Critical factors for $v_{ce}$ measurements

Observing the measuring circuits of the previous section, it is concluded that the  $v_{ce}$  measurement imposes several requirements extending to three main aspects; the protection and isolation, the speed and, finally, the precision of the total measuring system.

#### Protection of measuring system

The measuring circuit has to be capable of measuring a voltage below  $1V$  for the case of the sensing current, at the level of up to a few volts for the load current method and withstand a fluctuation that can be at the kilovolt level. Common methods for the protection at the input of the measuring system are a voltage divider, a blocking or a Zener diode or, finally, an additional switch. The isolation of the Data Acquisition System (DAQ) is, often, realized with digital isolators connected with the output Analog to Digital Converter (ADC) or with analogue isolation operational amplifiers. Each option exhibits requirements in terms of precision.

#### Precision of measurement

The precision of the measuring system has to be in the  $mV$  scale, due to the sensitivity of  $v_{ce}$  with sensing current that is about  $2mV$ . If the signal adaptation circuit is omitted, the main factors that influence the precision are the high voltage blocking elements and the sensing current source or the high current measurement. The voltage divider as well as the resistor values have to be selected properly, in order to be able to measure the saturation voltage with a resolution of  $2mV/^\circ C$ . Regarding the blocking diode, it has to be thermally and electrically characterized for the current imposed to it. At least one current source is needed in most of the circuits, if the  $v_{ce}$  method is used. The current source precision and output ripple are crucial for the measurement. The gate voltage level  $v_{ge}$  is an extra parameter to be considered, especially for the high current method. As described in [64],  $v_{ce}$  at high current is sensitive to  $v_{ge}$ . It is necessary to wait until  $v_{ge}$  stabilises in order to initiate the measurements. This delay may hinder the measurement, in case of a high switching frequency with a narrow measuring window.

#### Speed of measurement

The online measurement within a measuring window that is equal to the duty cycle of the switch is challenging in terms of:



## 2.7. Junction temperature estimation with thermal modeling

TABLE 2.6: Overview of the main considerations for the design of a  $v_{ce}$  measuring circuit

Design aspect	Requirements	Main concerns
Protection	Blocking voltage at $kV$ level	<ul style="list-style-type: none"> <li>-Resistive voltage divider selection and gain of amplifier for signal adaptation</li> <li>-Blocking diode characterization</li> <li>-Zener diode characterization</li> <li>-Extra circuitry for additional switch for voltage clamping</li> <li>-Additional switch calibration</li> </ul>
Precision	maximum $2mV$ corresponding to $1^{\circ}C$	<ul style="list-style-type: none"> <li>-Current source ripple, accuracy not better than 2%</li> <li>-Independent of <math>v_{ge}</math> over <math>10V</math></li> <li>-The concerns mentioned for the protection</li> </ul>
Speed	for online measurements: meas. window $< D$	<ul style="list-style-type: none"> <li>-Current source rise time</li> <li>-Conditioning circuit settling time</li> <li>-Resistive voltage divider dynamics</li> <li>-Zener/measuring resistor matching</li> <li>-<math>v_{ge}</math> level stabilization</li> <li>-Electron recombination</li> </ul>

## 2.7 Junction temperature estimation with thermal modeling

Apart from the experimental methods, the estimation of the temperature can be achieved with the help of thermal modeling. The two widely applied methods for the thermal modeling of IGBT modules and of their cooling system are the Finite Element Method (FEM) for off-line temperature estimations and the Lumped Parameters Network (LPN) for on-line and off-line temperature estimations.

### 2.7.1 Finite Element Method modeling

The Finite Element Method requires as an input the geometry of the modeled system for the temperature calculation at each point of the volume [66]. The principle is the splitting of the geometry in small pieces. The dimensions of the pieces define the results' precision.

This procedure is called meshing. For all the nodes forming the pieces, the unknown variables are solved with the help of heat transfer and fluid mechanics equations. FEM provides precise results at every point of the volume and offers a visual demonstration of the modeled effects. However, it is necessary to know the detailed geometry and the computation can have a long duration and be demanding in terms of resources.

### 2.7.2 Lumped Parameters Network modeling

The method of Lumped Parameters Network defines the equivalence between thermal and electrical parameters [67]. The thermal resistance, the thermal capacitance and the heating power resulting from the semiconductor power losses correspond to the electrical resistance, the electrical capacitance and the current, respectively. Finally, the temperature is the thermal equivalent of voltage. The thermal resistance  $R_{th}$  and the thermal capacitance  $C_{th}$  of a layer of the geometry can be calculated, respectively,

$$R_{th} = \frac{d}{\lambda A} \quad (2.25)$$

$$C_{th} = c\rho dA \quad (2.26)$$

where  $d$  is the material thickness,  $\rho$  is the material density,  $\lambda$  is the thermal conductivity,  $A$  the surface area and  $c$  the specific heat capacity. If the dimensions of each layer of the geometry and the heat propagation angle from each layer to the next are known, a LPN comprising a sequence of RC blocks can be developed, as illustrated in Figure 2.15a. Each RC block corresponds to a layer of the geometry. This is the Cauer thermal model that models the physical behavior of each layer if heat is applied. The semiconductor' datasheets typically include the Foster model of Figure 2.15b. It is a relatively simple mathematical tool to calculate the junction temperature but, in this case, the RC blocks do not correspond to the physical layers of the geometry.

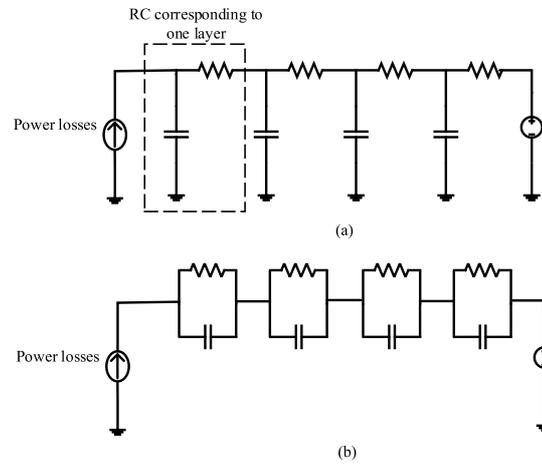


Figure 2.15: (a) Cauer thermal model representing the geometry, (b) Foster thermal model.

The Foster model is obtained from the thermal impedance curve. In the power modules' datasheets, the waveform of the thermal impedance as a function of time shows the change of the capability of the power module to extract the produced heat to the cooling system as a function of the time and for a dc current step. For the thermal impedance measurement by the manufacturers, the junction temperature, the reference temperature that, often, is the case temperature and the conduction losses of the power module are measured. According to [37], the IGBT is heated with a DC-pulse until it reaches thermal steady state and  $v_{ce}$  with sensing current is measured during the cooling-down time of the IGBT switch, immediately after the DC-pulse is cut. The advantage of this method is that it offers a precise value of the power losses since the IGBT conducts with constant current and constant  $v_{ce}$  at thermal steady state before the cooling down occurs. Practically, the cooling temperature curve is the inverse of the heating temperature curve, but the turn-on effects of the gate voltage that influence the conduction losses are avoided. The Foster model that is obtained from the thermal impedance curve can be transformed to a Cauer model, but the RC blocks of this Cauer model do not represent the physical layers of the geometry.

## 2.8 Summary

After comparing the available methods for junction temperature estimation, it is concluded that a combination of  $v_{ce}$  measurements with sensing and with load current is a suitable method to estimate the junction temperature and to detect aging of an IGBT module throughout its lifetime. The aging detection in this work is targeted to the two main ag-

## *Chapter 2. Methods for IGBT modules temperature estimation and aging detection*

ing mechanisms, the bond-wire lift-off and the solder delamination. The  $v_{ce}$  method with sensing current provides great accuracy and ease of calibration but it requires circuit modifications, whereas the  $v_{ce}$  method with load current can be implemented with the same measuring circuit as the method with the sensing current and provides clear evidence of bond-wire lift-offs. On the other hand, it is highly dependent on temperature. To apply these methods, measurements circuits of high accuracy and minimum calibration, as well as power circuits that enable  $v_{ce}$  measurement with sensing current without modifications are of great importance. The description of the characteristics of the specialized application in Chapter 3 is going to further justify the selection of these methods.

# Chapter 3

## Case set-up for magnet power supply

### 3.1 Introduction

This chapter introduces the application of interest and the power electronic converter that is used as a reference for this work. It presents the functionality of the converter and the main experimental set-ups that are used. The special characteristics of the application are analyzed with the help of calculations and thermal simulations with LPN models and FEM.

### 3.2 Reference power electronic converter

The power electronic converter that is used as a reference belongs to a family of magnet power supplies [68]. It is a medium-power electronic converter that exhibits the ratings presented in Table 3.1.

TABLE 3.1: Magnet power supply operating characteristics

Characteristic	Value
Peak output current [A]	450
RMS output current [A]	200
Peak output voltage [V]	+/- 450
Switching frequency [Hz]	6500

It can be connected as a module in various configurations, such as in series or in parallel depending on the ratings and characteristics of the magnet, namely the inductance and

Chapter 3. Case set-up for magnet power supply

parasitic resistance, as well as on the current profile. The power circuit is illustrated in Figure 3.1. The power electronic topologies that are used in the magnet power supply are a diode bridge and an H-bridge. The H-bridge is built with four single-switch HiPak SPT IGBT modules by ABB with ratings 1600A/1700V [36]. The brake chopper is used in case of excessive energy recuperation from the magnet.

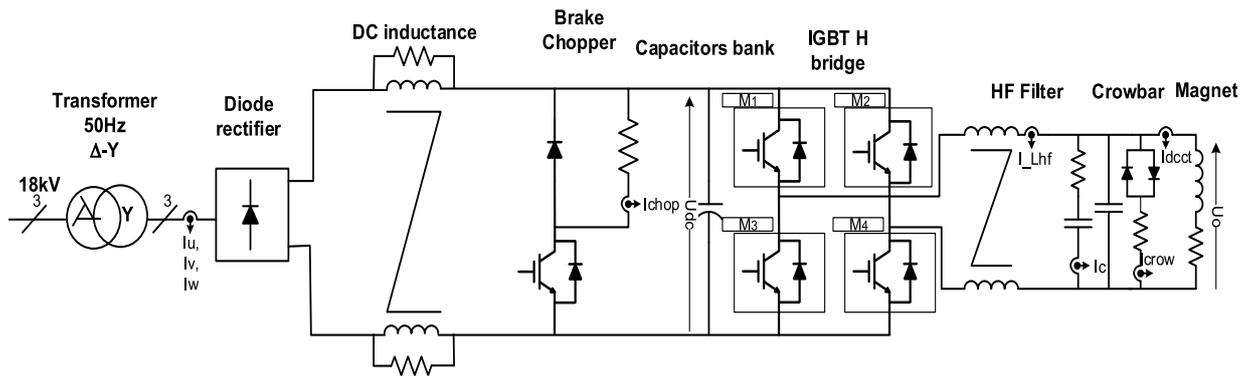


Figure 3.1: Converter power circuit.

The typical current profiles of the reference magnet power supply are of trapezoidal shape varying in ramp-up, ramp-down and flat-top time durations, see Figure 3.2 for pulse definition and Figure 3.3 for different profile forms. The current amplitude per module remains at 450A that is slightly above the NTC operating region for the IGBT modules of the application [36]. The greatest parts of the current ramp-up and ramp-down belong to the NTC operating region. The H-bridge operates as a DC-DC current converter to supply the DC current to the magnet.

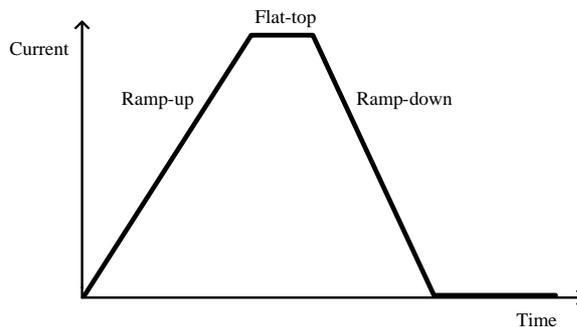


Figure 3.2: Magnet current pulse shape.

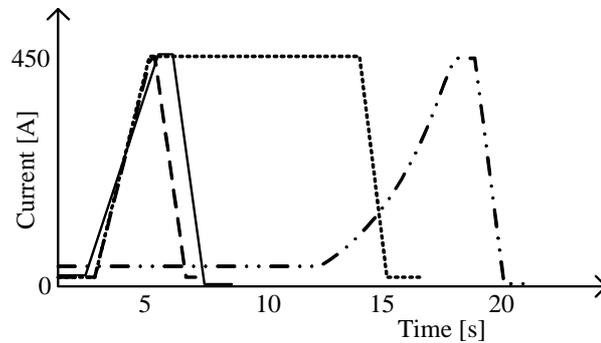


Figure 3.3: Different output current profiles of the magnet supply.

The requirements for the magnet power supplies at CERN are long lifetime of at least 20 years without unscheduled maintenance stops and high precision of the output current. This work focuses on the assessment of the power stack's condition throughout its lifetime. With the help of the method called IGBT Power Stack Integrity Assessment (IPSIA) that is proposed in this thesis, the assessment of the power stack's integrity is realized even before the commissioning phase during factory acceptance tests and during scheduled service stops. To this direction, thermal design validation and preventing maintenance can be achieved. Applying a specific current profile, this method requires a  $v_{ce}$  measuring circuit for measurements with sensing and with load current to achieve temperature and condition monitoring based on the analysis in Chapter 2. The existing inductor of the output filter of the magnet power supply is a perfect example of a load that can be used for the implementation of the method. In this case the load of the magnet power supply has to be short-circuited. Further theoretical investigations in this work propose thermal stressing mitigation with appropriate design of the cooling system and with online strategies engaging operation parameters such as the switching frequency and the gate resistance. These investigations are presented in Chapter 6. Figure 3.4 illustrates the different phases in the lifetime of the power stack together with the corresponding actions proposed in this work. Figure 3.5 introduces the concept of the method that will be, analytically, described in Chapter 5.

Chapter 3. Case set-up for magnet power supply

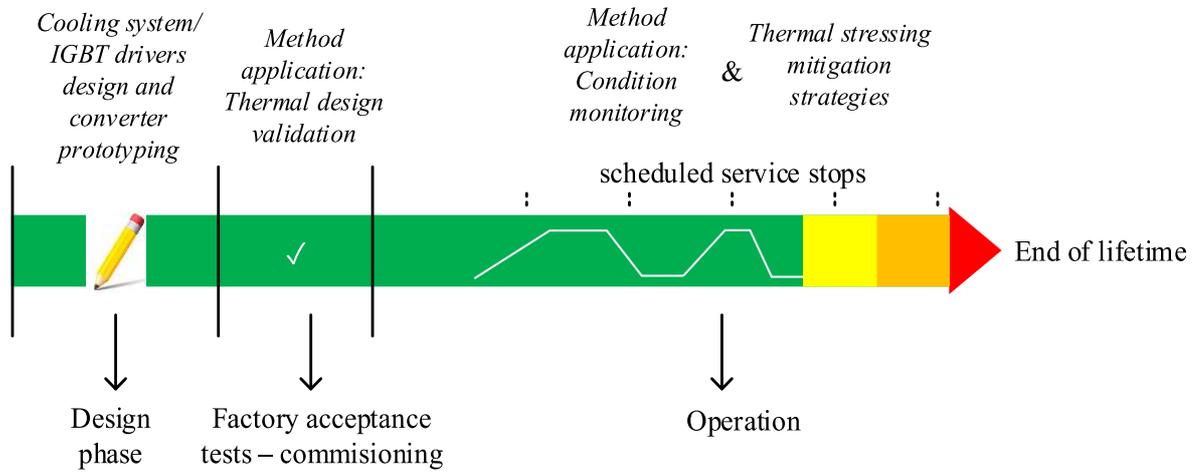


Figure 3.4: Different phases in the lifetime of the power stack and corresponding actions proposed in this work.

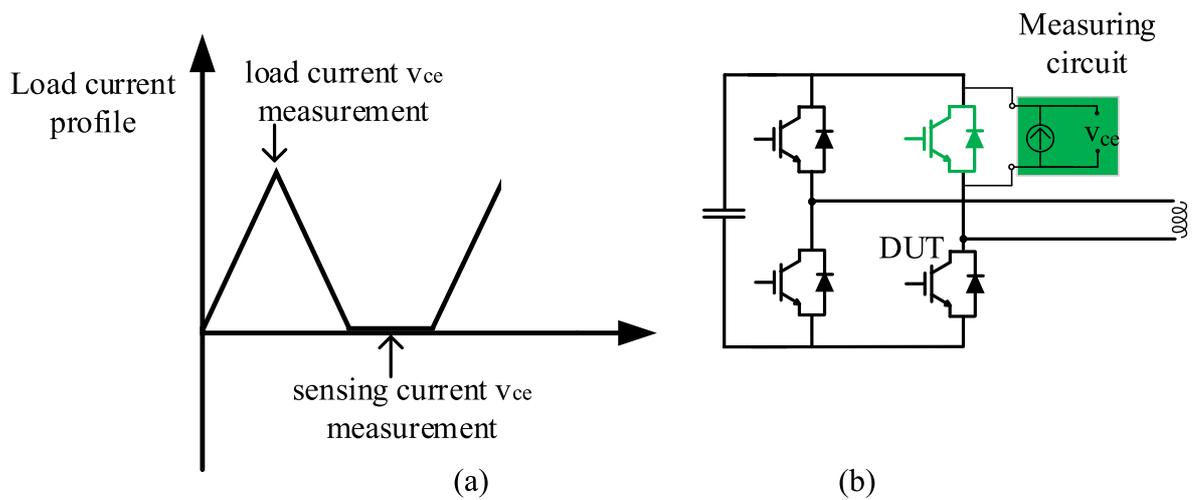


Figure 3.5: Overview of integrity assessment method.

Figure 3.6 shows the magnet voltage and current waveform for a 1.2s pulse for a magnet of 100mH and 0.1Ω. The flat-top voltage drop is caused by the parasitic resistance of the magnet. During the ramp-up and ramp-down the magnet voltage is constant as a consequence of the inductive load.

The current loop inside the H-bridge, in a simplified form, is illustrated in Figure 3.7, if

### 3.2. Reference power electronic converter

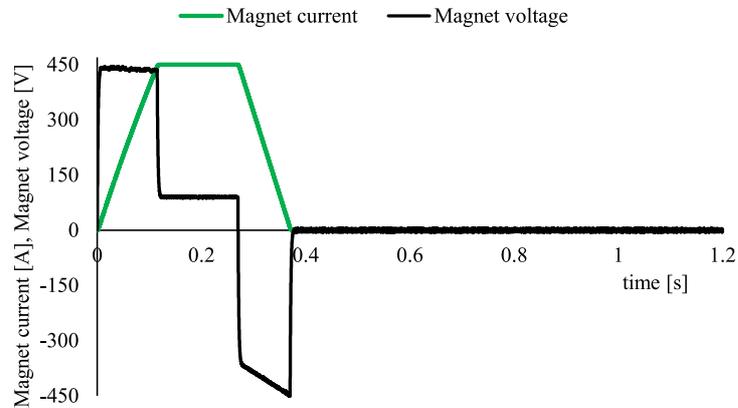


Figure 3.6: Magnet current and voltage.

the output filter is neglected. The unipolar output current causes the unbalanced operation of the H-bridge semiconductor devices. The devices that are in the current loop are the diagonal IGBTs M1, M4 that control the output current, otherwise the freewheeling diodes of the switches M2, M3 create a path for the current to circulate. Theoretically, the converter can still operate by omitting the diodes of M1, M4 and the IGBTs of M2, M3. The switches M2, M3 provide the possibility for the reset of the magnet's flux density to a specific point in the magnetic flux density and magnetic field curve or B-H curve by applying negative current.

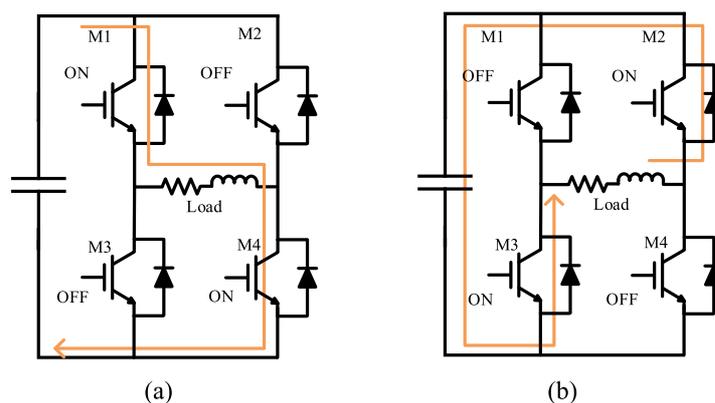


Figure 3.7: H-bridge operation: (a) IGBTs conducting, (b) Freewheeling diodes conducting.

### Chapter 3. Case set-up for magnet power supply

The average output voltage  $V_o$  of the H-bridge is calculated for the application of interest and for a conduction time  $T_{on}$  within a switching period  $T_{sw}$  [69]. For a bipolar switching operation, if  $D$  is the duty cycle of the switch M1,

$$D = \frac{T_{on}}{T_{sw}} \quad (3.1)$$

$$V_o = V_{an} - V_{bn} = V_{dc}D - V_{dc}(1 - D) = V_{dc}(2D - 1) \quad (3.2)$$

Accordingly, the average current at M1 and the anti-parallel diode of M2, respectively, are

$$I_{c,av} = DI_o \quad (3.3)$$

$$I_{F,av} = (1 - D)I_o \quad (3.4)$$

where  $I_o$  is the output current and the RMS current values are calculated

$$I_{c,rms} = \sqrt{D}I_o \quad (3.5)$$

$$I_{D,rms} = \sqrt{(1 - D)}I_o \quad (3.6)$$

The specialized application of the H-bridge as a magnet power supply, mainly, exhibits three special characteristics:

- in some cases, the long heating time or long  $t_{on}$  that can cause solder delamination, according to the thermal stressing factors of Chapter 2, and is an additional thermal stressing factor according to [9] and [8]
- the asymmetrical operation of the topology by exploiting only two IGBT switches and two anti-parallel diodes out of four for each device type
- the operation, during the greatest part of the ramp-up and ramp-down, in the NTC operating region

The operation in the NTC operating region is investigated in the Chapter 4, in order to find any thermal stressing unbalance among the parallel connected IGBT chips. This unbalance could be considered in the thermal models.

### 3.3 Experimental set-ups

This section presents the main experimental set-ups that were used for the different experiments conducted in this work. Three alternatives are presented:

- Set-up for current sharing investigation
- Two alternatives of the set-up for the presentation of the method for the integrity assessment of a power stack

#### 3.3.1 Set-up for current sharing investigation

Figure 3.8a and Figure 3.8b illustrate the open IGBT module that is used for these tests. The connection of the gate and emitter pads of the module with the gate driver is implemented with the construction based on spring probes that is illustrated in Figure 3.9a. The spring probes are pressed on the gate and emitter pads to maintain electrical contact. The soldering of cables on the pads was not possible due to the excellent thermal design of the module that allowed the heat to propagate to the other layers. As observed in Figure 3.8b, the four substrates of the IGBT module can be controlled independently. The temperature on the chips of the open module is monitored with the infrared camera T440 by Flir having a frame rate of  $60Hz$ . The IGBT module is painted black with a special paint that has a high emissivity. According to [70], the selected black paint was *MOTIP* – 04031 and the emissivity setting for the thermal camera was 0.95 that is the average number of the corrected emissivity for the expected junction temperature range during the IGBT operation. The infrared camera measurements were evaluated before the tests. A power resistor was painted black with the same paint as the module and it was heated with current injected by a laboratory power supply. The temperature at the surface of the power resistor was monitored with the thermal camera and compared with a thermocouple attached on the resistor. The two measurements were in accordance at the level of  $1^{\circ}C$ . The control of the substrates and the measurements acquisition is done with National Instruments Data Acquisition (DAQ) system *USB6251*. This DAQ system is used for the measurements acquisition and the control of the IGBTs for all the experimental set-ups. The module is placed on an electrically and thermally insulating surface, in order to be heated up by hindering the heat propagation below the baseplate. Eventually, temperature levels are achieved that are comparable to the real application. An overview of the power circuit of the test bench with the independent control of the substrates is illustrated in Figure 3.9.

Chapter 3. Case set-up for magnet power supply

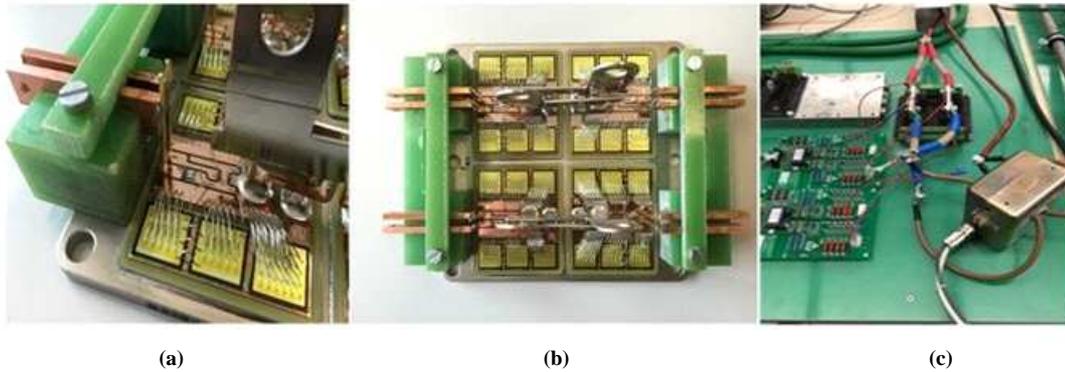


Figure 3.8: Experimental set-up for current sharing investigation (a) Driver connection to the module, (b) Open module, (c) Test set-up for current unbalance detection.

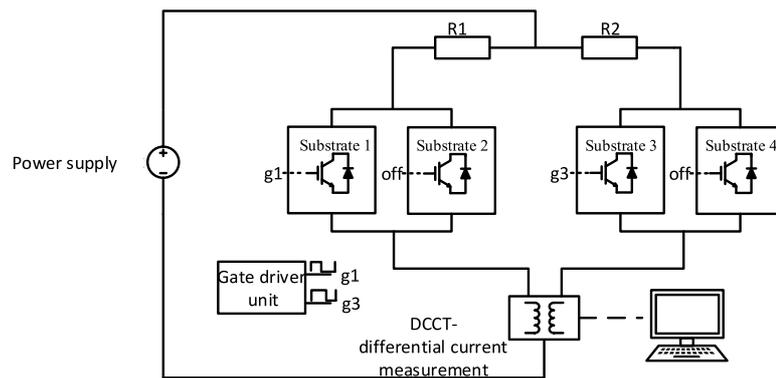


Figure 3.9: Overview of test bench for NTC operating region with non-uniform heating of substrates.

The current difference between the two substrates is measured with a Direct-Current Current Transformer (DCCT), as illustrated in Figure 3.10, that allows high precision measurements [71]. The power module that is painted black, the two gate drivers driving the two substrates and the DCCT with the current differential measurement between the two branches for the third test are illustrated in Figure 3.8c. The DCCT is a high precision instrument offering isolation with measurement uncertainty that can be down to a few parts per million (ppm) [72]. It exhibits a limited bandwidth of up to a couple of hundreds of kHz and measures current up to  $20kA$  [73]. Its principle of operation is illustrated in Figure 3.10.

The change of the primary current  $I_p$  causes a change of flux and an induced voltage on

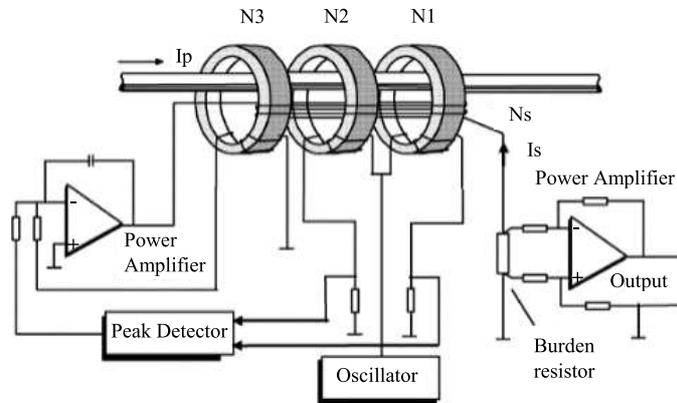


Figure 3.10: DCCT operation principle [73].

the secondary windings of the toroids. The voltage is fed to the power amplifier and the resulting current causes a flux at the secondary that opposes the initial flux change. The secondary current that is created is a mirror of the primary current with the turns ratio of the two windings relating the two currents. The DCCT can be used during the calibration and right before the use of the measuring system or even during the actual monitoring.

### 3.3.2 Set-ups for condition monitoring method

The power circuit for the demonstration of the method for the integrity assessment of the IGBT power stack comprises the power stack of the magnet power supply that is the H-bridge controlling the DC current to the magnet, the diode rectifier and the DC-link, according to Figure 3.1. An auto-transformer is used for the adjustment of the diode rectifier input voltage. Figures 3.11a and Figure 3.11b provide overviews of the two power circuits alternatives. The difference in Figure 3.11b compared to Figure 3.11a is that an open IGBT module is connected in series to the inductor. To allow a free-wheeling path for the load current in case of an accidental turn-off of the open IGBT module during operation, power resistors are connected in parallel to the inductor. The set-up of 3.11a is used for junction temperature and thermal resistance estimations, whereas the set-up of Figure 3.11b is used for the detection of bond-wire lift-offs and IGBT module incorrect mounting on the cooling plate. The results obtained from these set-ups are provided in Chapter 4. The current probe TCP404XL with a bandwidth of 2MHz and 1% precision is used for the load current measurements. The  $v_{ce}$  measuring circuits that are developed in this work as well as their calibration and testing are presented in Chapter 4.

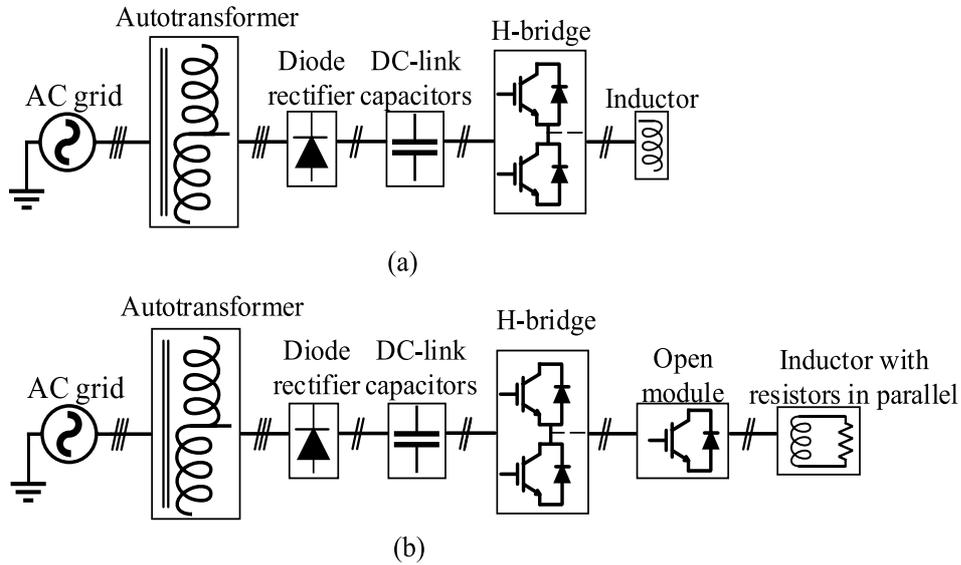


Figure 3.11: Experimental set-up variations: (a) Power circuit diagram for temperature and thermal resistance estimations, (b) Power circuit diagram for testing of thermal paste application and bond-wire lift-offs.

Figure 3.12a and Figure 3.12b illustrate the power circuit corresponding to Figure 3.11a. Figure 3.12b provides an internal view of the power stack's power circuit.

The cooling circuit has a central, manual valve for the flow rate regulation, a flow sensor and two temperature sensors at the inlet and outlet to check that the experiments are conducted under the same operating conditions. The cooling plate of the power stack is connected in parallel with an external and identical cooling plate, as illustrated in Figure 3.13. An on-off valve that is connected in series with the external cooling plate offers the possibility to cut the plate's water flow. An open and black-painted IGBT module of the same type as the power stack's switches is mounted on top of the external cooling plate. The open module is used for thermal measurements with an infrared camera.

The ratings of interest for the power circuit are provided in Table 3.2.

### 3.3. Experimental set-ups

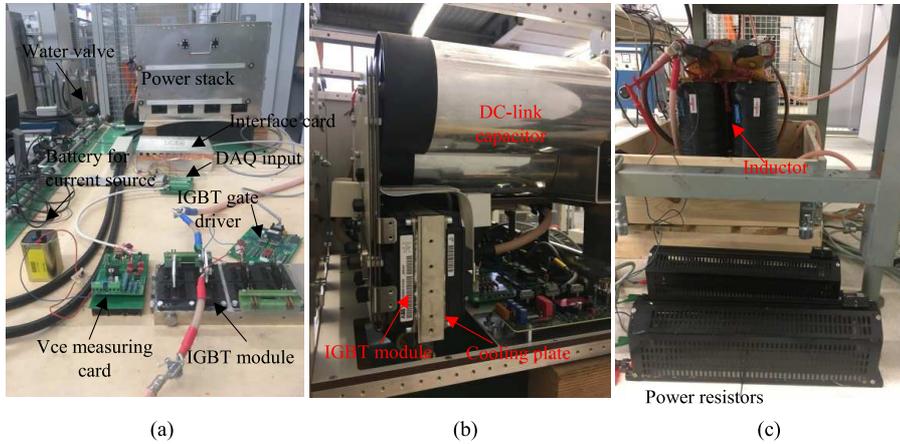


Figure 3.12: Experimental set-up pictures: (a) Experimental set-up with H-bridge output connected to open IGBT module, (b) Internal view of power stack (c) Inductive load with power resistors in parallel.

TABLE 3.2: Ratings of interest for the power circuit of the experimental set-up

Parameter	Value
DC-link voltage, $V_{dc}$ for experiment	560V
RMS output current, $I_{o,rms}$	approx. 150A
Allowable peak output current, $I_{o,peak}$	450A
IGBT switch nominal current/voltage	1600A/1700V
Nominal flow rate of water cooling system, $Q$	12 l/min
Inductive load $L_{load}/R_{load}$	approx. 120 $\mu$ H/1.1mOhm

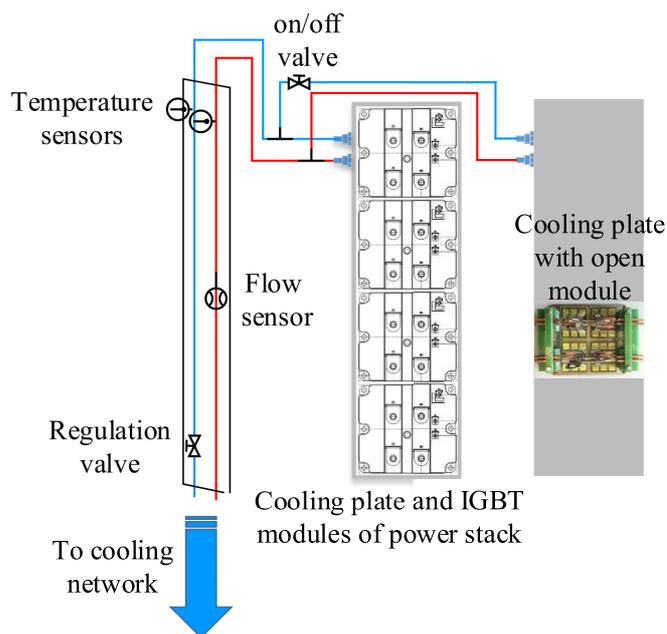


Figure 3.13: Cooling circuit of experimental set-up.

### Chapter 3. Case set-up for magnet power supply

During the testing of the experimental set-up with bipolar switching of the H-bridge, an oscillation was observed at the load voltage, as illustrated in Figure 3.14 for a DC-link of 200V. It is caused by the load inductance and the parasitic capacitance of the semiconductor switches. A ferrite toroid is placed around the power cable close to the load to damp the oscillation.

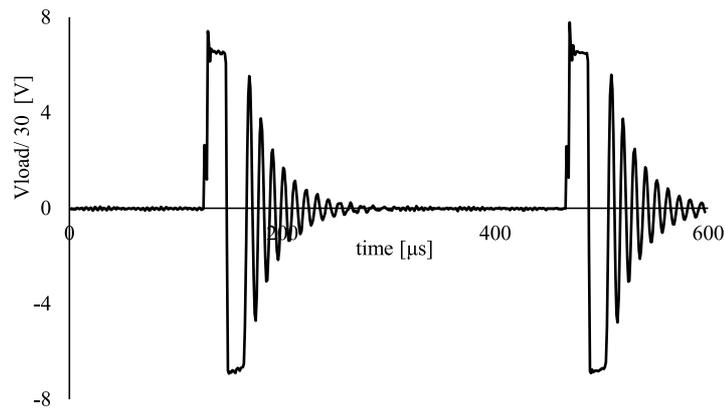


Figure 3.14: Load voltage oscillation at end of current ramp-down.

## 3.4 Thermal modeling with Finite Element Method

FEM in COMSOL environment is used to simulate both heat conduction among the solid parts of the power stack as well as heat convection to cooling water. For the cooling part of the model, the water flow is considered turbulent after calculating the Reynolds number [74] value greater than

$$Re = \frac{ud_h}{\nu} > 4000 \quad (3.7)$$

where  $u$  is the cooling medium velocity,  $d_h$  the inner pipe diameter and  $\nu$  the kinematic viscosity of the cooling medium. Turbulent flow is more efficient for convective heat transfer [74]. The power module dimensions are defined based on measurements on the open module and on literature search for chip dimensions and solder layers materials and properties [75], [76], [3] and [77]. The dimensions, the material and the characteristics of each material for every layer of the IGBT module as well as the dimensions of the cooling

### 3.4. Thermal modeling with Finite Element Method

plate are provided in Appendix A. The geometry in COMSOL environment is illustrated in Figure 3.15.

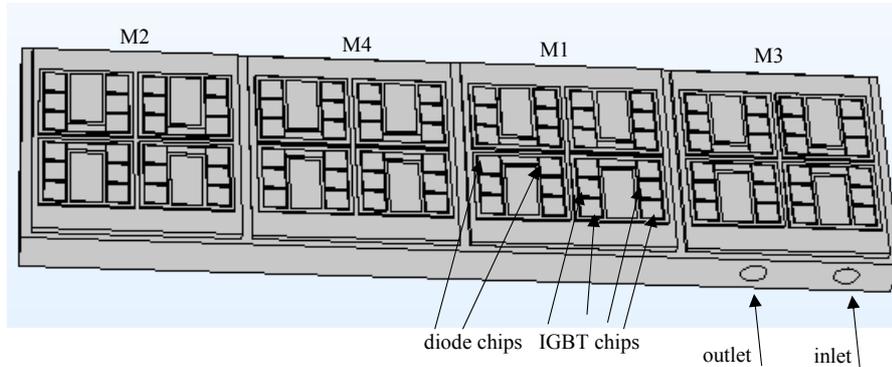


Figure 3.15: Power stack geometry in FEM.

The modeling of the IGBT module follows the method that is proposed for IGBTs of the same type as in [78]. Heating power is injected to the whole volume of the upper one third of the IGBT chip. The junction temperature of the IGBT module corresponds to the average temperature in the volume of the heated parts of the chips. For the thermal impedance calculations using FEM, the case temperature is the average temperature at baseplate level of the surfaces directly below each chip. The area of each surface is equal to the chip area that it corresponds to. As shown in Figure 3.16, the first verification step is to compare the thermal impedance characteristics of both IGBT-to-case and anti-parallel diode-to-case to the datasheet characteristics. The FEM model matches well, especially close to steady state and it is acceptable, especially for the comparison of simulations results with static temperature measurements, as it is going to be analyzed in Chapter 4.

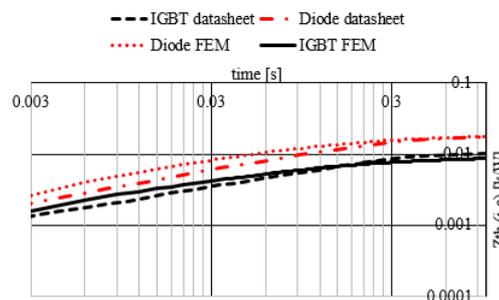
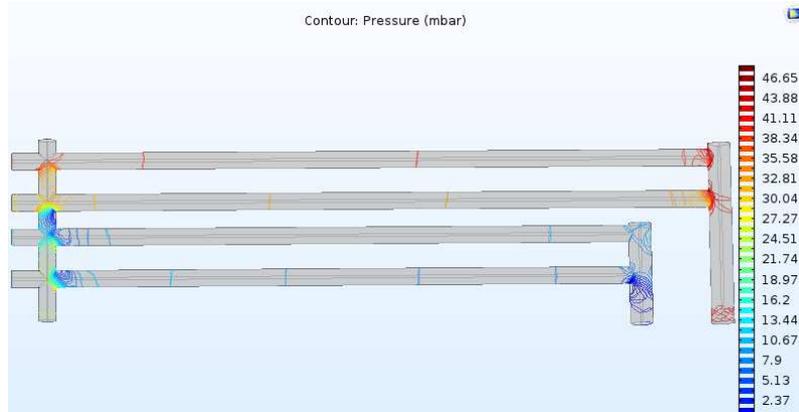


Figure 3.16: Thermal impedance of both IGBT chip-to-case and anti-parallel diode chip-to-case comparison between FEM and datasheet for IGBT and anti-parallel diode [36].

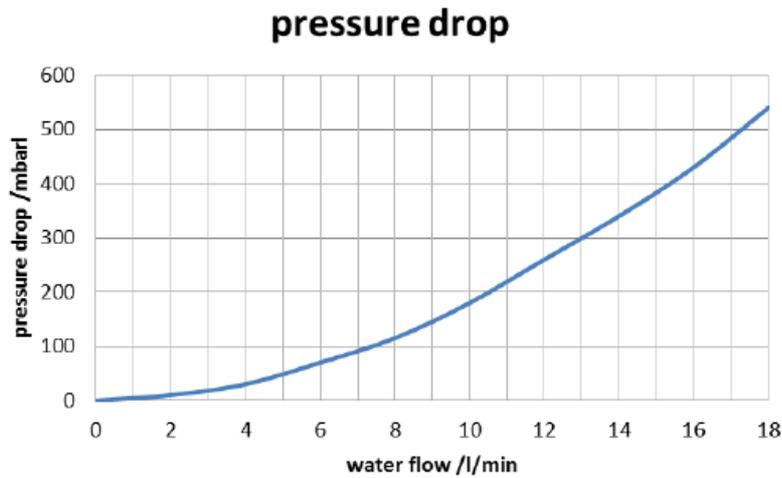
### *Chapter 3. Case set-up for magnet power supply*

The second verification step that the FEM model passed is the constant heat power injection to the chips and the comparison of the amount of the injected heat power with the heating power that arrives to water. The only path for the heat propagation is defined to be from chip level towards water and no heat is transferred to the ambient. The verification is done with the help of (3.8). The third verification step is the comparison between the FEM model and the cooling plate datasheet in terms of pressure drop between inlet and outlet. According to Figure 3.17, the total pressure drop of the cooling plate that is calculated with FEM for a cooling flow rate of  $12l/min$  is approximately  $50mbar$ . The total pressure drop value for the module that is provided by the supplier is approximately  $260mbar$ , which is close to the calculated value. The difference could result from the point of measurement for the supplier, for instance if the pressure sensors are not placed exactly at the connections points of the cooling plate and if there is an angle in the pipes connecting the cooling plate connection points with the pressure meters.

### 3.5. Thermal modeling with Lumped Parameters Networks



(a)



(b)

Figure 3.17: (a) FEM results for pressure inside the pipes of the power stack cooling system for  $12\text{ l/min}$ , (b) Supplier's data for total pressure drop of the cooling plate.

## 3.5 Thermal modeling with Lumped Parameters Networks

For the demonstration of the the thermal stressing per device for a typical magnet current, the current profile of Table 3.3 is used as a typical profile for the magnet power supply of interest. With the electrical circuit simulation software Psim by Powersim the junction temperature profile is calculated using LPN modeling along this current profile. Figure 3.19 shows the power losses of the switch M1 and of the switch M2 anti-parallel diode

that are illustrated in Figure 3.1. In the simulation, the waveforms for switch M4 and M2 anti-parallel diode are identical to the waveforms of the devices that are illustrated. For this demonstration, the simulation model uses the model in [79] as a starting reference.

TABLE 3.3: Typical profile of magnet current

Characteristic	Value
Ramp-up [s]	0.1
Ramp-down [s]	0.1
Flat-top [s]	0.17
Zero current interval [s]	0.83
Current amplitude at flat top [A]	450

The simulation software PSIM provides a thermal simulation toolbox that is coupled with the electrical simulation environment. It is possible to create components that are based on the datasheet of semiconductor devices. The IGBT switch of the application is electro-thermally simulated. The thermal model of the power stack is a series connection of Cauer models of the components, namely of the power module and of the combined thermal paste and water-cooling system. The thermal model of the IGBT power module is provided in Foster form in the datasheet. The Foster model is transformed to a Cauer model, in order to connect it with the Cauer models of the thermal paste and of the cooling plate. The Cauer model resembles more the physical response of the power module as a complete system of separate layers of different materials [67]. Therefore, the Cauer model of the IGBT module can be connected in series with the Cauer model of the thermal paste and the cooling circuit that are calculated based on their physical properties. In practice, this is a preliminary thermal stressing evaluation that is applied in the design phase and inaccuracy due to the connection of different Cauer models may occur. Figure 3.18 shows the Cauer thermal model structure and Table 3.4 the model values. The Cauer model of the combination of thermal paste and cooling plate is built based on the supplier's data. The reference temperature that is represented as a voltage source in Figure 3.18 is the inlet water temperature. The water temperature rise during the power stack operation is, often, neglected in the LPN simulations. The water temperature rise at the outlet of the power stack cooling plate comparing to the inlet can be calculated using the relation

$$\Delta T = \frac{P_{loss}}{QC_p\rho} \quad (3.8)$$

where  $Q$  is the cooling medium flow rate,  $C_p$  is the cooling medium thermal capacity and  $\rho$  is the material density. For the worst case in terms of thermal stressing, the maximum temperature at junction level would increase by an additional level of  $\Delta T$  according to (3.8),

### 3.5. Thermal modeling with Lumped Parameters Networks

if the outlet water temperature was used in the model of Figure 3.18 instead of the inlet water temperature. For the application of interest, each IGBT module is cooled along its surface by pipes with water having a temperature close to the inlet water temperature and by pipes with water temperature close to the outlet water temperature. The representation of the cooling system geometry is provided in the next section.

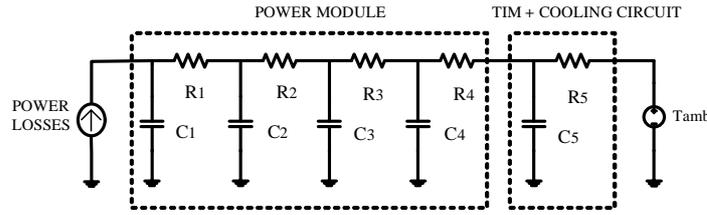


Figure 3.18: Power stack thermal model.

TABLE 3.4: Cauer thermal model values from the Foster model values per IGBT provided by the IGBT manufacturer for  $R_1$ - $R_4$  and  $C_1$ - $C_4$  and Cauer value  $R_5$ ,  $C_5$  per IGBT for the cooling plate based on power stack's manufacturer data

Thermal resistance [ $K/W$ ], Thermal capacitance [ $J/K$ ]	Value
$R_1, C_1$	0.0009, 0.8295
$R_2, C_2$	0.0009, 2.3211
$R_3, C_3$	0.003, 6.4027
$R_4, C_4$	0.0057, 24.3602
$R_5, C_5$	0.025, 1200

The energy amount that is dissipated per switching event is calculated based on the IGBT datasheet with a linear extrapolation at the lowest range of current in the switching losses graph, for the gate resistance values of the power stack and for a DC-link voltage of 700V. This case is used as it is the worst case for the IGBT switching losses as the switching energy values are provided in the datasheet for 125°C. For the diode reverse recovery energy estimation, a linear approximation for the gate on-resistance of the application based on the datasheet is used. Again the worst case of 125°C is used. The reason is that in a mix of cycles, the maximum junction temperature might be higher than for the demonstrated cycle alone. A preliminary evaluation for the IGBT total switching power losses for the  $f_{sw}$  of the application is

$$P_{sw,i,av} = (E_{on} + E_{off})f_{sw} \approx 2890W \quad (3.9)$$

### Chapter 3. Case set-up for magnet power supply

that is very close to the switching losses of approximately  $2750W$  calculated in PSIM. The total IGBT and diode losses are illustrated in Figure 3.19. It is observed that the conduction losses of approximately  $380W$  are much lower than the switching losses. A main reason is that at the flat-top the duty cycle is low because the output voltage of the power converter is equal to the voltage drop of the magnet's resistance. The output voltage in this case is approximately  $90V$ , as in Figure 3.1.

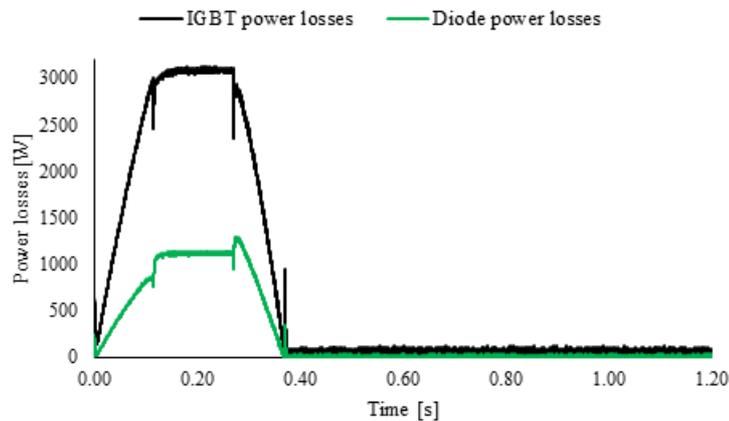


Figure 3.19: IGBT and freewheeling diode power losses for the current cycle of Table 3.3.

The temperature profiles during this cycle for the IGBT M1 and the anti-parallel diode of switch M3, according to Figure 3.7 are presented in Figure 3.20.

The maximum IGBT temperature and the temperature swing are approximately  $14^{\circ}C$  and  $9^{\circ}C$ , respectively, higher than for the diode. The switching losses of the IGBT are the main reason for the greater thermal stress of the switch comparing to the diode. For this work, the focus is on the mostly stressed device, i.e. the IGBT.

The cycle of Table 3.3 for the first  $1.2s$  is applied to the FEM model and it is compared with the results of LPN model of Table 3.4. For the LPN model, the manufacturer' value for thermal resistance from case-to-water of each IGBT module is used not including the thermal coupling between the IGBT modules. The temperature profiles for the LPN and FEM simulation models are shown in Figure 3.21.

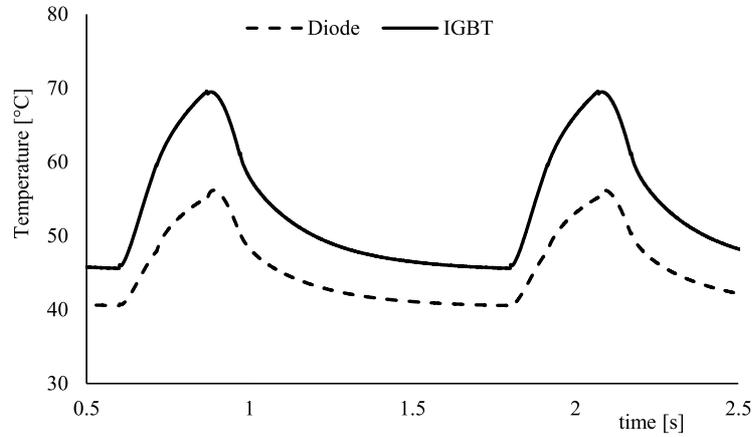


Figure 3.20: IGBT and freewheeling average junction temperature calculated with the LPN model with water-flow rate of  $12l/min$  and water inlet temperature  $27^{\circ}C$ .

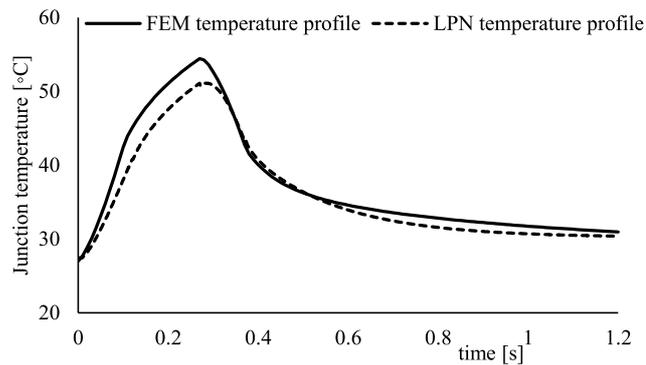


Figure 3.21: Comparison of IGBT junction temperature response during the first cycle of the 1.2s current profile based on FEM and LPN simulations

## 3.6 Summary

A typical magnet power supply has an H-bridge that is used as a DC-DC current converter. The current profile is, usually, of trapezoidal form and can vary in terms of ramp and flat-top time reaching a  $t_{on}$  time of several seconds. The operation is asymmetrical and engages only two diagonal switches and two anti-parallel diodes out of the eight semiconductor devices in total. A significant part of the current profile belongs to the NTC operating

### *Chapter 3. Case set-up for magnet power supply*

region, whereas the peak current is slightly above the ZTC operating region. It is observed with the help of LPN modeling that the thermal stressing in terms of maximum junction temperature and junction temperature variation is significantly higher for the IGBT than for the anti-parallel diode. A methodology is presented for the development of the thermal model of the power stack in FEM.

# Chapter 4

## Current sharing in high-power IGBT module in the NTC operating region

As it was presented in Chapter 3, the IGBT modules of the application operate extensively in the NTC operating region. This chapter investigates the current sharing effect in the NTC operating region of the high-power SPT IGBT module used in the magnet power supply. The current sharing between two of the module's substrates is demonstrated in case of temperature unbalance and its impact on the thermal stressing of the device is evaluated. The motivation for this investigation is the evaluation of the thermal stressing and of the necessity to include the effect of the current unbalance in the thermal modeling of the power stack. The results of this investigation are published in publication IV.

### 4.1 Research background

Previous works have demonstrated the current sharing at current levels close to the nominal ratings of the power module both at steady state [80], [81] and during switching dynamics [82], [83], [84]. In these cases, the uneven current sharing was a result of the temperature unbalance among the substrates due the cooling system, due to the deviation at the characteristics of the chips or due to asymmetry at power module or power circuit level. As it has been indicated in [80], a significant temperature difference between the chips may exist as an effect of the pipe distribution inside the cooling plate or of the degradation of the thermal paste.

## 4.2 Method for the investigation of current unbalance in NTC

The proposed method for the current unbalance investigation in NTC is to use two of the four substrates of the power module and measure the current difference between them when they operate under different temperature levels. The tests for the investigation of current unbalance were executed in three steps:

- Thermal characterization in a thermal chamber to define the relation between IGBT saturation voltage with sensing current and junction temperature for each of the two substrates.
- Test for current unbalance due to power circuit asymmetry
- Test for current unbalance due to temperature difference between the two substrates.

The first step of the experimental procedure was to thermally characterize the power module in a thermal chamber, in order to obtain the relation between the saturation voltage and the temperature at junction level for various temperature levels. The thermal characterization is done for a sensing current of  $1A$ . It is the same calibration procedure as the one that was described for the  $v_{ce}$  method with sensing current for indirect junction temperature measurement in Chapter 2. In this way, it is ensured that there is no significant inherent difference between the two used substrates of the IGBT module. Figure 4.1 depicts the relation between  $v_{ce}$  and  $T_j$  for three different measurement configurations; one series of measurements for each of the substrates and one for the two substrates operating in parallel. All the measurements are done under a controllable temperature range from  $30^{\circ}C$  to  $100^{\circ}C$ . The fact that the lines for substrate 1 and 3 coincide shows that their thermal behavior is almost identical with a maximum  $v_{ce}$  difference of  $3mV$ .

Secondly, in order to measure the current unbalance due to the circuit asymmetry, one pulse of  $1s$  each at different current level up to  $100A$  was applied to the two substrates connected in parallel with the power supply operated in current source mode. The temperature rise at chip level is considered negligible, because the current is low (nominal of  $50A$  per substrate). Moreover, the heat that is propagated to the isolating material below the IGBT module is not enough to rise the temperature for such a short time duration close to the IGBT module's time constant. The temperature difference between the two substrates was, also, considered negligible. Figure 4.2 shows the current levels of the pulses and the corresponding current unbalance that was measured. It is observed that the relation of the current unbalance and total current level in the circuit is linear. This result implies

## 4.2. Method for the investigation of current unbalance in NTC

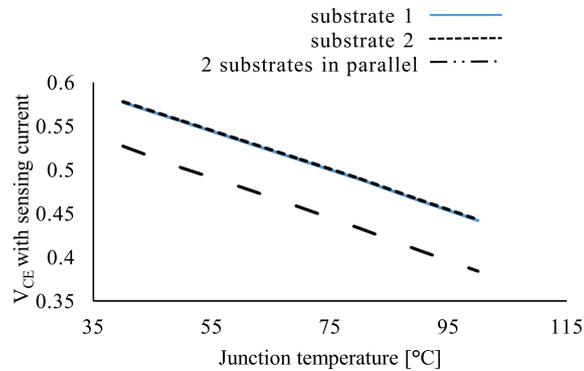


Figure 4.1: Module partial thermal characterization: two substrates separately and the two substrates in parallel.

that there is a constant circuit asymmetry that, as expected, is amplified as the current increases. The current unbalance due to the circuit asymmetry has to be subtracted from the current unbalance that is measured for different temperature conditions between the two substrates. The effect of the different temperatures for the cables of each branch can be neglected. Therefore, the effect alone of the NTC operating region can be isolated and evaluated.

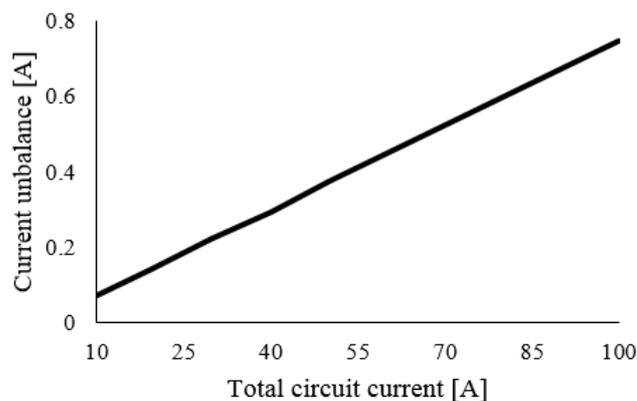


Figure 4.2: Current unbalance between the two substrates due to circuit asymmetry for different current values.

For the third step of the tests, in order to achieve a temperature difference between the two substrates, the power supply is operated as a voltage source and the current is shared between the substrates that are switched at the same switching frequency but at different

duty cycles, as illustrated in Figure 3.9. The temperature on four different chips, two for each substrate, was monitored with the infrared camera, in order to measure the temperature difference between the two substrates. The experiments are carried out only with substrates 1 and 3 that are depicted in Figure 4.3 to measure the current sharing between them for currents up to 50A per substrate and for different temperature distributions. This current value corresponds to 200A for the full module that represents the operating region where the NTC effect is mostly evident, as it can be observed in Figure 2.8b.

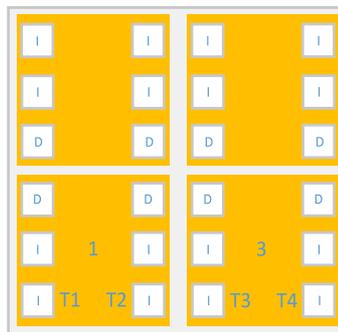


Figure 4.3: Open module drawing.

### 4.3 Results from tests in the NTC operating region with non-uniform heating of substrates

As observed in Figure 3.9b, each substrate consists of two diode chips that are indicated with the letter D and four IGBT chips that are indicated with the letter I. The infrared camera monitors the temperature at two chips on substrate 1 and on two chips on substrate 3. The current unbalance between the substrates is measured for various current levels and temperature differences. The circuit asymmetry effect is subtracted from the current measurements. Table 4.1 presents the current unbalance for various current levels and for different temperature deviations between the two substrates.

According to 3.9, the temperature difference between the chips can be explained with respect to their positions. The chip T1 is at the outer part of the module, where there is a temperature difference towards the ambience at the side of the module and the heat can propagate more easily. The temperature of chip T2 is positioned close to chip T3 that has the highest temperature, as it was observed with the thermal camera during the power cycling. The temperature difference between chips T2 and T3 is a result of the fact that

#### 4.4. Impact on thermal stressing distribution between the substrates

TABLE 4.1: Current unbalance for various current levels and temperature differences

Total current [A]	Temp. of 2 chips (T1 and T2) on subs. 1 [ $^{\circ}C$ ]	Temp. of 2 chips (T3 and T4) on subs. 3 [ $^{\circ}C$ ]	Max. temp. difference between two chips [ $^{\circ}C$ ]	Unbalance between the 2 subs. [A]
40	41, 42	46, 48	7	0.4
60	42, 44	48, 49	7	0.45
80	82, 85	90, 91	9	0.45
100	67, 71	80, 82	15	0.5

the surfaces of the insulating material and of the lower part of the IGBT module are not perfectly flat. Therefore, air can penetrate between the two surfaces changing the heat propagation in different places on the IGBT module.

Focusing on the current unbalance, the difference is between  $0.4A$  and  $0.5A$  in all cases. The highest current unbalance is measured at  $100A$ , that means at an average of  $50A$  per substrate or  $12.5A$  per chip. The temperature difference between the hottest and coldest chip reaches  $15^{\circ}C$ , which is not considered as a common condition. On the other hand, the current unbalance of  $0.45A$  at  $60A$  and  $80A$  with a temperature difference of  $7^{\circ}C$  and  $9^{\circ}C$ , respectively, is a realistic case [80]. The current unbalance does not seem to be significant even for high temperature difference between the two substrates. The junction temperature for a total current of  $80A$  is higher compared to the  $100A$  case because it is influenced by the heat stored in the insulating material below the DUT from previous tests.

#### 4.4 Impact on thermal stressing distribution between the substrates

The next step is to evaluate the impact of the measured current unbalance on the thermal stressing distribution at substrate level by taking the worst case of  $100A$  and  $15^{\circ}C$  temperature difference as an example. With the assumption of no leakage inductance unbalance that could influence the current sharing between the two substrates during the switching dynamics, a difference of the average total power losses of  $2W$  between the two substrates is calculated using a linear approximation for the low current region. The switching losses are much higher than the conduction losses for this application, as it was demonstrated in Chapter 3.

Chapter 4. Current sharing in high-power IGBT module in the NTC operating region

$$P_{loss,i,av} = (E_{sw,i,on,ref} + E_{sw,i,off,ref}) \frac{V_{DC}}{V_{DC,ref}} \frac{I_c}{I_{c,ref}} f_{sw} + DV_{ce}I_c \quad (4.1)$$

$$\Delta P_{loss,i,av} = \left( \frac{E_{sw,i,on,ref} + E_{sw,i,off,ref}}{4} \right) \frac{V_{DC}}{V_{DC,ref}} \frac{I_{s,2} - I_{s,1}}{I_{s,ref}} f_{sw} + DV_{ce}(I_{s,2} - I_{s,1}) \approx 2W \quad (4.2)$$

where  $E_{sw,i,on,ref}$  and  $E_{sw,i,off,ref}$  are the reference turn-on, turn-off losses, respectively, both according to the device datasheet for a total module current of  $200A$  divided by four, since the calculations are for one of the four substrates of the module,  $V_{dc,ref}$  the datasheet reference voltage,  $V_{dc}$  the DC-link voltage of the application equal to  $900V$ ,  $I_{c,ref}$  four times lower than the datasheet reference current,  $I_{s,2}$  is the saturation current of substrate 3 equal to  $50.25A$ ,  $I_{s,1}$  is the saturation current of substrate 1 equal to  $49.75A$  and  $V_{ce}$  the saturation voltage, respectively, at  $200A$ . The switching and conduction losses are calculated for a given temperature of  $125^\circ C$ . The calculations are for operating conditions that correspond to the actual application with a duty cycle  $D$  of approximately  $0.5$  and a switching frequency  $f_{sw}$  of  $6.5kHz$ . Based on (4.2), the difference in power losses for the two substrates is not significant. It should be mentioned that the power losses difference would be higher, if the temperature difference was taken into account for the power losses calculation. For this investigation, the focus is on the current unbalance impact at the losses and the impact of temperature unbalance is neglected.

In order to calculate the increase of power losses, if the substrate operates at  $50.25A$  compared to the balanced operation at  $50A$ , and based on (4.1), it can be found that

$$\frac{P_{loss,50.25,av}}{P_{loss,50,av}} = \frac{(E_{sw,i,on,ref} + E_{sw,i,off,ref})V_{DC}I_{c,2}f_{sw} + 4DI_{c,2}V_{ce}I_{c,ref}V_{DC,ref}}{(E_{sw,i,on,ref} + E_{sw,i,off,ref})V_{DC}I_{c,3}f_{sw} + 4DI_{c,3}V_{ce}I_{c,ref}V_{DC,ref}} \quad (4.3)$$

leading to a power losses increase of approximately  $0.5\%$ . In (4.3)  $I_{c,2}$  is the saturation current of  $50.25A$  and  $I_{c,3}$  is the saturation current of  $50A$ .

The power losses increase of  $0.5\%$  compared to the ideal case without any current unbalance means that there is no significant thermal stressing difference between the two substrates, even for a temperature difference of  $15^\circ C$ . The current unbalance in the NTC operating region as well as the impact in the thermal model of the IGBT module can be neglected.

## 4.5 Conclusions

Considering the operation in the NTC operating region, the effect of the temperature unbalance between the substrates on the current sharing in the power device was investigated. The measurements and the calculations indicate that the difference in the current between the two substrates and the additional thermal stressing at the substrate that carries the highest current are not significant. Therefore, it is not necessary to consider it for the thermal modeling of the H-bridge operating at the NTC operating region. Moreover, it does not seem to influence the lifetime of the power modules.

*Chapter 4. Current sharing in high-power IGBT module in the NTC operating region*

# Chapter 5

## Method for IGBT Power Stack Integrity Assessment

### 5.1 Introduction

This chapter proposes an electrical test for testing the integrity of an IGBT-based power stack assembly initially during factory acceptance tests and later in service stops during regular operation. The method is referred to as IGBT Power Stack Integrity Assessment (IPSIA) method, as it was introduced in Chapter 3. The following paragraphs describe how the method can be used during factory acceptance tests to detect assembly issues and verify the thermal performance of the power stack. During service stops, bond-wire lift-offs can be distinguished from solder delamination. Moreover, two measuring circuits offering ease of calibration and reduced number of components are proposed for the  $v_{ce}$  measurement. Their performance is, initially, tested with an experimental set-up that emulates a phase-leg of the considered power magnet supply. The IPSIA method is analyzed and is tested using the power stack of the power magnet supply described in Chapter 3. Experimental results are presented and compared with results from FEM and LPN simulations to demonstrate the method's applicability. The content of this chapter is based on papers I and II.

### 5.2 Developed $v_{ce}$ measuring circuits

The IGBT Power Stack Integrity Assessment method is based on combined  $v_{ce}$  measurements with sensing as well as with load current. Two  $v_{ce}$  measuring circuits are analyzed.

### 5.2.1 Zener diode-based $v_{ce}$ measuring circuit

The circuit and the working principle of the first developed  $v_{ce}$  measuring circuit are presented in Figure 5.1. The circuit comprises a measuring resistance in series with a Zener diode, as depicted Figure 5.1a. It is connected in parallel to one of the two single-switch IGBTs of a phase leg. The voltage across the Zener diode is equal to  $v_{ce}$ , if the DUT is conducting, according to Figure 5.1c. If the DUT is blocking, the voltage across the Zener diode is equal to the Zener voltage and the rest of the DC-link voltage is applied across the measuring resistor, as shown in Figure 5.1b.

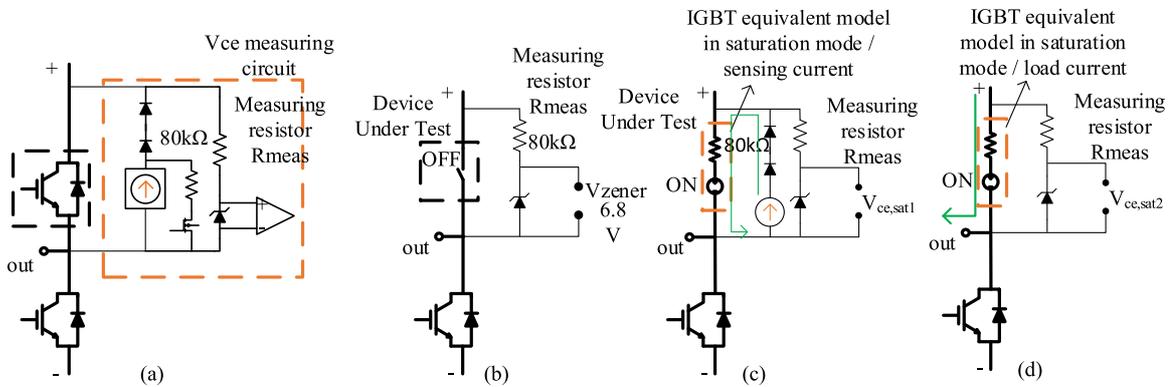


Figure 5.1: (a) Overview of proposed Zener-based  $v_{ce}$  measuring circuit, (b) Circuit output if DUT is blocking, (c) Circuit output if DUT is conducting using the equivalent of the IGBT at saturation.

The current source is protected from the high voltage with two high-voltage diodes in series. In parallel to the source, there is a MOSFET and a resistor; this parallel branch is optional, in the case that the current source is not fast enough to raise the current within the measuring window. The MOSFET path can be used for ramping-up the current in advance, i.e. during the off-time of the DUT.

### 5.2.2 Components selection for Zener diode-based $v_{ce}$ measuring circuit

The Zener voltage  $V_z$  has to, initially, fulfil two requirements

$$v_{ce} < V_z < \min(V_{i,max,op-amp}, V_{DAQ}) \quad (5.1)$$

## 5.2. Developed $v_{ce}$ measuring circuits

$$v_{ce} \ll V_z \quad (5.2)$$

where  $V_{i,max,op-amp}$  is the maximum allowable voltage of the operational amplifier and  $V_{DAQ}$  of the Data Acquisition System. The saturation of the amplifier can delay its response due to its desaturation time and has to be avoided, if the measurement requires fast dynamics in a small measuring time window. The second requirement results from the leakage current of the Zener diode, when the DUT is conducting. The voltage  $v_{ce}$  has to be significantly lower than  $V_z$  to ensure that the minimum leakage current will flow in the measuring resistor.

The measuring resistor is selected based on four criteria. The first one is the measurement dynamics due to the RC circuit created by the Zener diode capacitance and the measuring resistor. The second criterion is the maximum allowable Zener current flowing in the diode, when the DUT is blocking the voltage. The increase of the diode temperature increases this current. The Zener current value has to be kept minimum to avoid the Zener temperature increase  $T_{jz}$  according to

$$R_{th,j-a}P_z = R_{th}I_{z,av}V_z = \Delta T_{j,z}, \quad (5.3)$$

where  $P_z$  is the conduction power losses of the Zener diode,  $I_{z,AV}$  is the average Zener current during the switching of the DUT and  $\Delta T_{j,z}$  is the estimated junction temperature of the diode that has to remain as close as possible to the nominal conditions of  $25^\circ C$  in the datasheet. Thirdly, it is the leakage current of the diode with its voltage-current relation,

$$R_{meas}I_{z,leak} = V_{i,error} \quad (5.4)$$

where  $I_{leak}$  is the diode leakage current and  $V_{i,error}$  the measurement error in the operational amplifier input voltage. The leakage current can create a notable voltage drop across the resistor that has to be compensated at the circuit output. The input impedance of the operational amplifier of Figure 5.1 is considered infinite compared to  $R_{meas}$ . This assumption helps for the impedance matching of  $R_{meas}$  and of the operational amplifier input impedance. In detail, the measuring resistor has to be much smaller than the amplifier input impedance, in order to eliminate the voltage divider effect of the measuring path and to maintain a precision of  $2mV$ . For the  $v_{ce}$  method with sensing current and for a known maximum measured voltage  $V_{ce,max,1A}$  the relation of the two resistors are

$$V_{R_{meas}} = \frac{R_{meas}}{R_{meas} + R_{op-amp}} V_{op-amp} \quad (5.5)$$

## Chapter 5. Method for IGBT Power Stack Integrity Assessment

with the help of

$$V_{op-amp} + V_{R_{meas}} = V_{ce,max,1A} \quad (5.6)$$

and of

$$V_{R_{meas}} \leq 2mV \quad (5.7)$$

using the value of  $2mV$  to respect the measuring circuit's precision requirement

$$\frac{R_{meas}}{R_{op-amp}} = \frac{V_{R_{meas}}}{V_{ce,max,1A} - 2V_{R_{meas}}} \quad (5.8)$$

where  $V_{ce,max,1A}$  corresponds to the minimum operation temperature of the module. The thermal drift of  $R_{meas}$  does not have a significant impact neither on the speed nor on the precision of the measurement. For this design  $R_{meas}$  should be at least  $80k\Omega$ , in order to maintain a low temperature increase for the Zener diode due to its leakage current. The Zener diode *BZX55C6V8* with a Zener voltage of  $6.8V$  is selected for the low leakage current at the measuring range of the application. According to the datasheet [85], for a Zener voltage of up to  $2V$ , it limits the leakage current to below  $100nA$ . For the characterization of the Zener diode in terms of  $V_z$  and leakage current, the set-up of Figure 5.2a is used and the measurement error is obtained along the  $v_{ce}$  measuring range for measurements with the sensing and with load current in Figure 5.2b. For the IPSIA method the exact  $v_{ce}$  is important at the sensing current level for the temperature estimation.

For commonly available Zener diodes with a leakage current at the level of  $1\mu A$  and in the worst case in terms of leakage current at  $125^\circ C$ , the voltage drop across the measuring resistance may reach  $80mV$  or more that corresponds to almost  $40^\circ C$  error at the temperature estimation with the  $v_{ce}$  method with sensing current. The leakage current increases, as the measuring voltage approaches the Zener voltage. The Zener voltage should be much lower than the measured  $v_{ce}$ . For  $v_{ce}$  with load current, a Zener diode with a Zener voltage over  $10V$  is recommended respecting (5.1). From the thermal response graphs in [85], the expected temperature increase for the diode *BZX55C6V8* is approximately  $6^\circ C$  according to (5.3).

Additionally, the sensing current source precision and output ripple are crucial for the measurement. For a sensing current of  $1A$  injected to the  $1.6kA$  IGBT open module, the corresponding loss of accuracy in the voltage measurement and, as a result, in the temperature estimation is illustrated in Figure 5.3.

## 5.2. Developed $v_{ce}$ measuring circuits

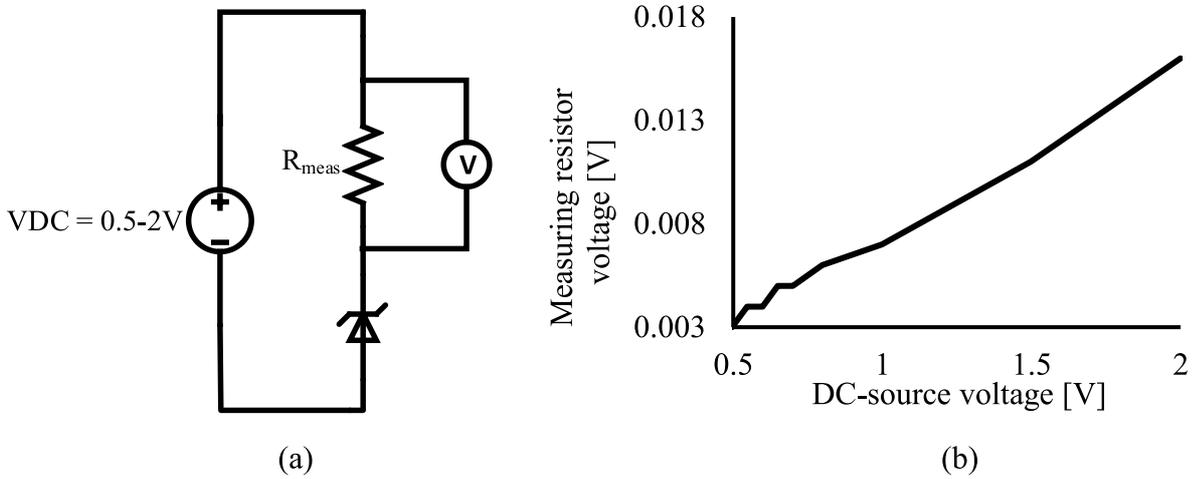


Figure 5.2: (a) Set-up for the measurement of the error due to the leakage current of the Zener diode, (b) Measured voltage drop across measuring resistor as a function of the total voltage applied across the series-connected measuring resistor and Zener diode.

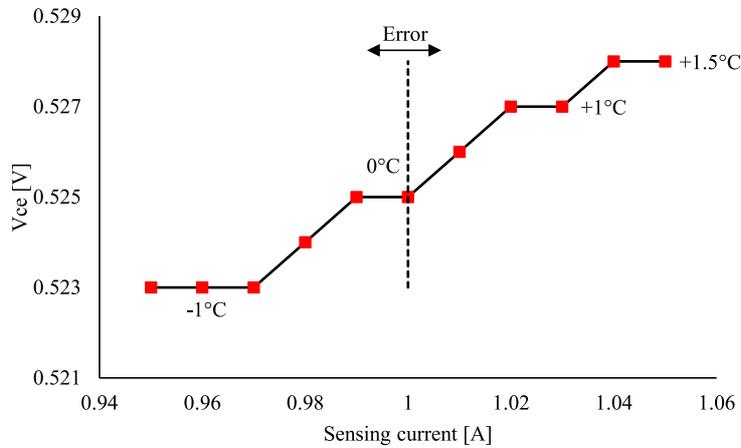


Figure 5.3: Measured sensitivity of  $V_{ce}$  with sensing current for the ABB 5SNA 1600N170100 IGBT module [36] for  $V_{ge}$  equal to 15V and a temperature of 22°C used as a sample in this work.

It is observed that for a sensing current of 1A a deviation of 20mA can cause an error of 2mV or 1°C. The required precision for the sensing current source is relatively low at 2% and can be achieved with the current sources available in the market. The characterization is done with a power module at 22°C, which is the the room temperature. The linear

## Chapter 5. Method for IGBT Power Stack Integrity Assessment

regulator LT3080 by Linear Technology with adequate precision and a current response to steady state of approximately  $1\mu s$ , as shown in Figure 5.4 with the IGBT module as a load, is used as the sensing current source, in order to avoid noise emitted by current source alternatives such as PWM switching LED current sources. The ripple level is the same as the ripple level before the current rise and is not caused by the current source.

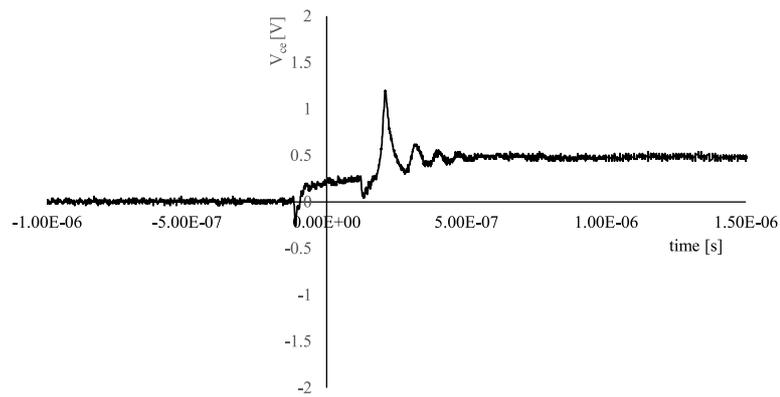


Figure 5.4: Current source response to steady state with the IGBT module used a load.

The operational amplifiers circuit consists of a precision amplifier with a high input impedance that, directly, receives the  $v_{ce}$  value and the output of this amplifier is connected to the isolation operational amplifier *ISO124* by Texas Instruments. The amplifier before the isolation amplifier is introduced because the input impedance of the latter is only  $200k\Omega$  being comparable to  $R_{meas}$  causing a voltage divider effect, as described by (5.8). The implemented measuring circuit is illustrated in Figure 5.5a and its schematic is provided in Appendix B.

The set of batteries of Figure 5.5b is used for the power supply of the card that makes the measuring device portable and eliminates any noise introduced by the supply. The number of batteries can be reduced by four units compared to Figure 5.5b if a supply voltage of  $9V$  instead of  $18V$  is used. Furthermore, the operation amplifier before the isolation amplifier has its own battery supply to avoid unbalanced supply of the isolation amplifier, if the battery voltage level is reduced during operation. Therefore, the number of batteries could be reduced even by five units. The device is enclosed in a metallic and grounded box. It can be connected directly in parallel to the DUT at the power electronic converter in the field. The advantage of this design is the simple circuitry with a low number of components and the fast and easy calibration of the Zener diode.

As an advancement to the method for the measuring circuit of [61], the effect of the Zener

## 5.2. Developed $v_{ce}$ measuring circuits

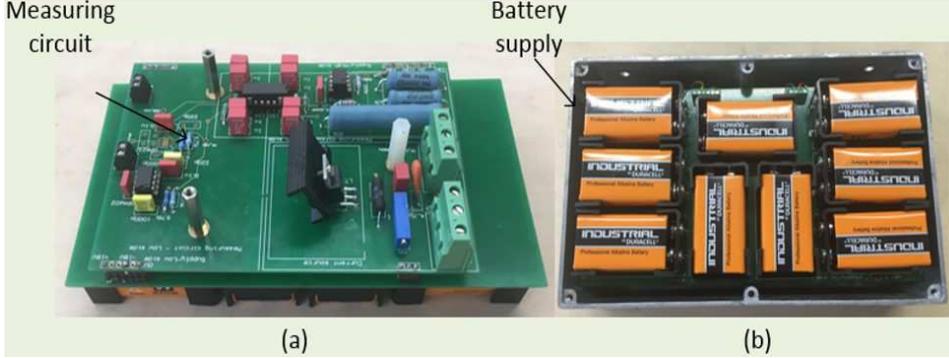


Figure 5.5: Prototype of Zener-based portable  $v_{ce}$  measuring circuit: (a) Upper side - measuring circuit, (b) Lower side - Battery supply .

diode selection and of its leakage current, especially for  $v_{ce}$  under high current, is investigated and it is considered for the accuracy improvement. A complete design procedure for the measuring circuit is proposed facilitating the development. Finally, a switch in parallel with the sensing current source is proposed in case the current source had a rising time that was slow compared to the measuring window inside the switching period of the DUT.

The Zener-based circuit for  $v_{ce}$  measurement with sensing and load current is used for the validation of the IGBT Power Stack Integrity Assessment method.

### 5.2.3 Measuring circuit for $v_{ce}$ based on desaturation detection circuit

A starting point for the typical desaturation detection circuit is shown Figure 5.6a. The blocking diode  $D_F$  is used for protection. Resistor  $R_1$  and capacitor  $C_1$  form a low-pass filter. For the  $v_{ce}$  method a measurement throughout a voltage range is necessary and a threshold voltage detection is not needed. To avoid the current source that is proposed in

The design principle is to keep the diode forward voltage  $v_F$  at a constant value. This enables to subtract a constant  $v_F$  from the measurement and obtain  $v_{ce}$ . A constant  $v_F$  requires a constant supply voltage and a  $v_{ce}$  that ranges within values that do not practically change  $i_F$ . The resistor  $R$  defines the current  $i_F$ . The value of  $I_F$  is defined by

$$i_F = \frac{V_s - v_{ce} - v_F}{R} \quad (5.9)$$

As a demonstration, this measuring circuit has been characterized for  $v_{ce}$  measurements with sensing current, but its application can be extended to  $v_{ce}$  with load current. Based on

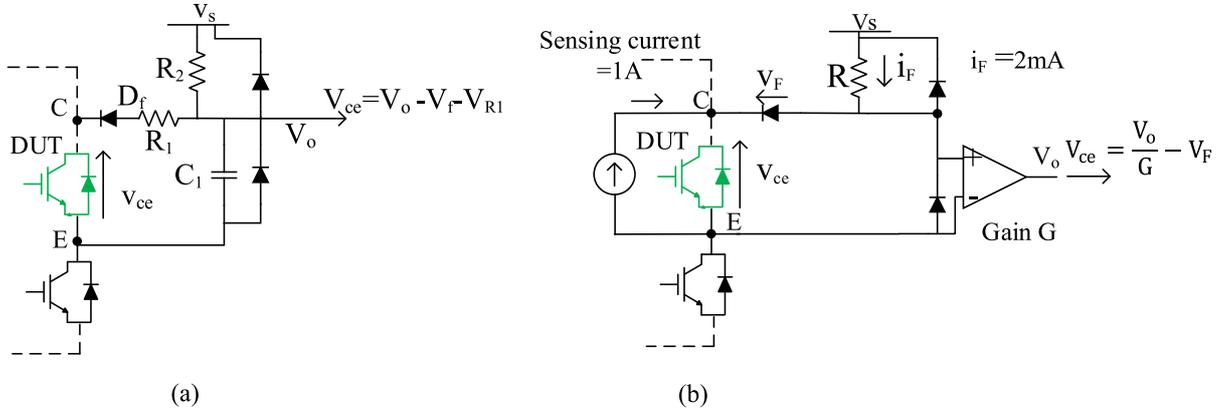


Figure 5.6: (a) Desaturation protection circuit and (b) proposed pin-diode based  $v_{ce}$  measuring circuit based on the desaturation protection principle.

the open IGBT module thermal characterization with a sensing current within the range of junction temperature levels that are expected during operation, the range of  $v_{ce}$  change is approximately from  $0.35V$  to  $0.53V$ , according to Figure 5.7. In this case,  $v_{ce}$  could exceed  $0.53V$  for low temperature values. Therefore, no essential change in  $v_F$  is caused within the defined  $v_{ce}$  range. For instance, by selecting the  $v_s$  and  $R$  values accordingly, the voltage  $v_F$  is stabilized between  $1.089V$  and  $1.09V$  for a  $i_F$  of  $2mA$  and an ambient temperature of about  $20^\circ C$  for the given range of  $v_{ce}$ . The resistor  $R$  is the most decisive factor for  $i_F$  and  $v_F$  change and not  $v_{ce}$ . The supply voltage  $v_s$  can be formed with a voltage divider from the supply of the operational amplifier connected across  $D_f$  and the IGBT emitter. It has to be a fraction of the amplifier supply in order not to drive the amplifier to saturation. The amplifier network is the same as in the Zener diode-based circuit. Concerning the variation of  $v_F$  of the pin-diode with ambient temperature, a calibration should, always, be implemented at the ambient temperature of the testing environment before a series of measurements.

The circuit in [62] is a solution to actively subtract  $v_F$  and, as an effect, cancel this ambient temperature variation. As it is shown in 2.14f, the upper diode of the measuring system is assumed to have the same electrical and thermal behavior as the lower diode. Therefore, by measuring  $v_F$  in the upper diode  $v_F$  in the lower diode is obtained. The effect of the two diodes can be subtracted from the measurement with the use of differential amplifiers to obtain  $v_{ce}$ . The advantage of the proposed circuit in this thesis, compared to the similar circuit of Figure 2.14f, [62] is that no precision current source is needed, in order to define a constant  $v_F$ . For the proposed method, there is no need to use any additional source except for the sensing current source. Moreover, it requires only one pin-diode instead of

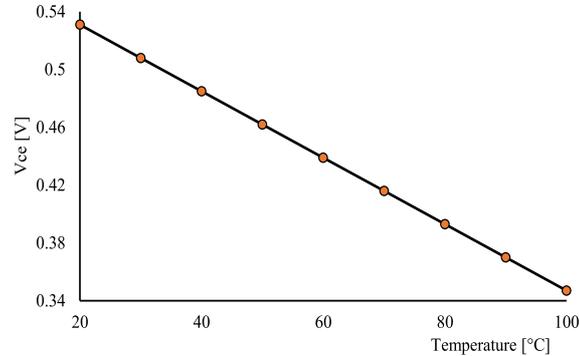


Figure 5.7: IGBT open module [36] thermal characterization.

two and it avoids the thermal coupling of two pin-diodes.

#### 5.2.4 Testing of $v_{ce}$ measuring circuits

The circuit of Figure 5.8 is used for the testing of the proposed measuring circuits. The IGBT module used for the test is intentionally uncovered to enable the independent control of the four substrates, as illustrated in Figure 3.9b. For ease, one substrate of the IGBT is the DUT and it is used as the upper switch of the phase leg and the other substrate as the lower switch, respectively. The phase-leg is connected to a DC voltage source that emulates the DC-link of a power stack, in order to test the voltage blocking capability and the dynamic performance of the measuring circuit. The two switches operate in a complementary manner that is the upper target of this application for  $v_{ce}$  measurement during the on-time within the switching period. As it will be demonstrated for the IPSIA method later in this chapter, this way of  $v_{ce}$  measurement is useful to estimate the temperature, and, as a result, the thermal impedance at specified operating points without extra power components in the power stack.

As a result,  $v_{ce}$  increases to the level of  $0.6V$  compared to the  $v_{ce}$  value in Figure 5.7 for the full module. The DAQ sampling rate for this test is  $800 \text{ ksamples/s}$ . The DUT is not heated for this test, a thermocouple is placed at the test bench to obtain the ambient temperature and compare the voltage measurement with the thermal characterization curve of Figure 5.7. This method can be more accurate for a first-stage evaluation of the measuring circuit performance than the active heating of the semiconductor with high current and the monitoring with a thermal camera within specific intervals. Due to the thermal camera's low frame rate of  $60Hz$ , the measuring circuit's full bandwidth performance cannot be

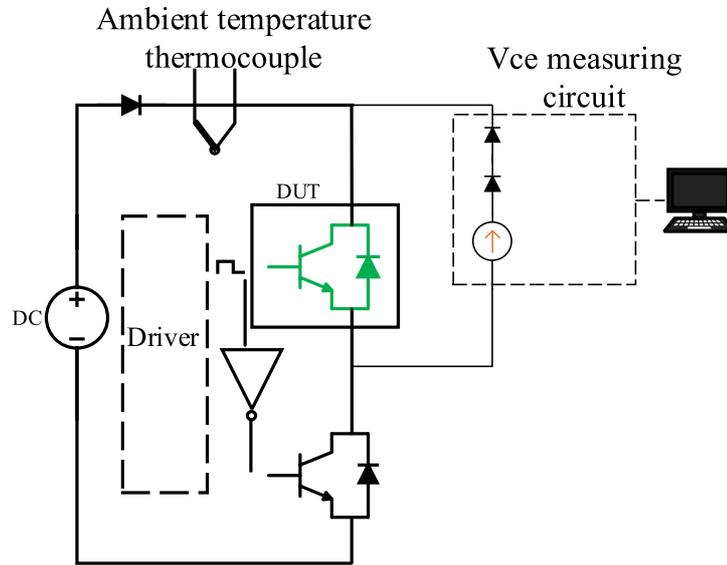


Figure 5.8: (a) Test set-up for the  $v_{ce}$  measuring circuits performance.

tested. Moreover, the thermal camera measurement can introduce measurement errors due to the black paint application and the emissivity definition, whereas the proposed test is realized under a fixed and known temperature. Therefore, the proposed evaluation method is, easily, applied and tests the measuring method's bandwidth as well. This method could be extended by inserting the DUT inside a thermal chamber and check the precision of the circuit at different temperature levels. The tests are implemented in industrial environment with several power converters operating at the same time.

The aim of the test is to evaluate the precision and the settling time of the measuring circuits under real switching frequency conditions. For the testing of the measuring circuits the operation at the nominal switching frequency of  $6.5kHz$  is selected. A second switching frequency of  $3kHz$  is chosen because this value is used for the demonstration of IPSIA method later in this chapter. A filter to eliminate the  $500kHz$  ripple produced by the modulator/demodulator for the digital-to-analog conversion of the input signal in the isolated amplifier causes the oscillation before reaching the low state.

### Testing of Zener-based circuit

The measurement for a switching frequency of  $6.5kHz$  is illustrated in Figure 5.9 for the Zener-based circuit. A duty cycle of about 0.7 is selected to allow time for the measure-

## 5.2. Developed $v_{ce}$ measuring circuits

ment settling. According to Figure 5.9b,  $v_{ce}$  at low state is processed for the last  $20\mu s$  of the DUT on-time. This time interval is adequate for the measurement after the measuring circuit settling time that is observed to be close to  $50\mu s$ . Figures 5.10a and 5.10b show the  $v_{ce}$  voltage measurement for a switching frequency of  $3kHz$ . The same duty cycle as for the  $6.5kHz$  case is used. In Figure 5.10a the  $v_{ce}$  measurement fluctuates from approximately  $4V$ , when the DUT is blocking to the value corresponding to the sensing current of  $1A$  providing  $0.618V$  at  $22^\circ C$ . The saturation voltage  $v_{ce}$  at low state is processed for the last  $50\mu s$  of the DUT on-time. For the maximum values of the Zener voltage for the  $3kHz$  and the  $6.5kHz$  case, it is noticed that at  $3kHz$  the maximum Zener voltage is higher than at  $6.5kHz$  according to Figure 5.10a and Figure 5.9a. For these testing conditions, the time interval that the DUT does not conduct is longer for the  $3kHz$  than for the  $6.5kHz$  case allowing more time for the Zener voltage to rise. As it will be shown during IPSIA demonstration with a power stack during operation with high current, the voltage rise across the Zener diode when the DUT does not conduct is much faster reaching the Zener voltage. This effect does not influence the  $v_{ce}$  measurement and it is not further analyzed in this work. In the case of  $3kHz$  in Figure 5.10b, a longer measuring window is illustrated because there is more time with stabilized  $v_{ce}$ , after the measuring circuit settling time has passed, compared to the  $6.5kHz$  case.

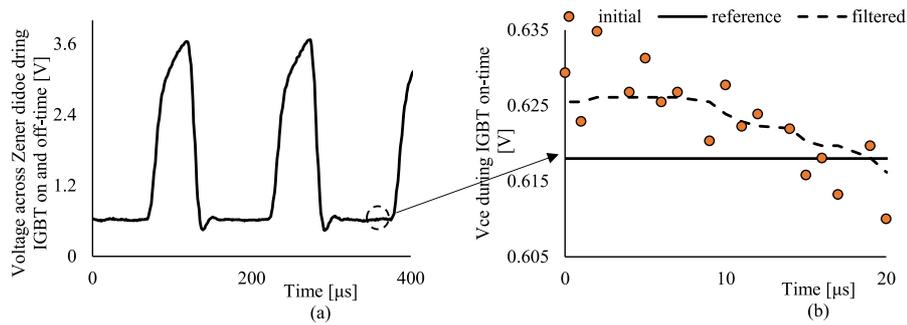


Figure 5.9: Measurements with the Zener-based circuit for a switching frequency of  $6.5kHz$  (a) Voltage across Zener diode: high value for DUT at off-state, low value for DUT at on-state, (b) measuring interval of  $v_{ce}$  in the end of the on-state.

Chapter 5. Method for IGBT Power Stack Integrity Assessment

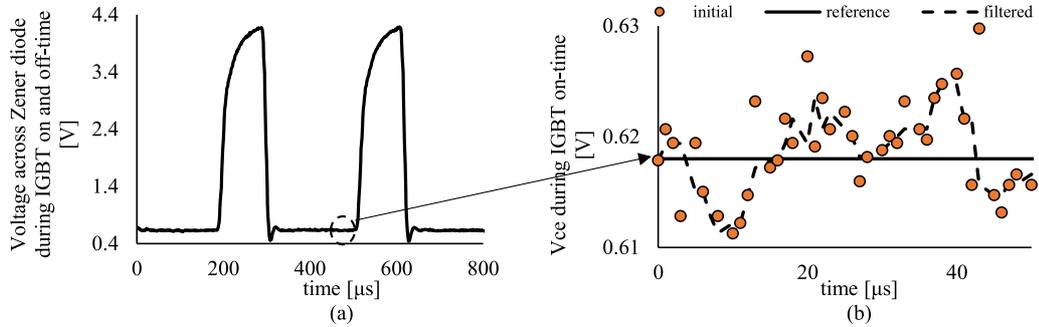


Figure 5.10: Measurements with the Zener-based circuit for a switching frequency of  $3kHz$ : (a) Voltage across Zener diode: high value for DUT at off-state, low value for DUT at on-state, (b) measuring interval of  $v_{ce}$  in the end of the on-state.

The ripple reaches  $20mV$  due to the few sparse measurements. For this application, the noise level of the proposed measuring circuit is considered acceptable. A median filter with a range of 3 samples, taking into account the next three values, is utilized to smooth out the measurement [86]. The measurement ripple is reduced to about  $15mV$  peak to peak for the worst case. The principle of the median filter for the spikes elimination is illustrated in Figure 5.11.

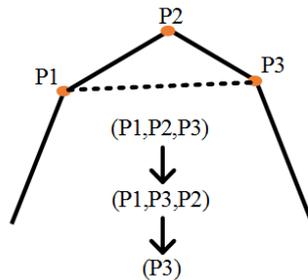


Figure 5.11: Median filter logic for eliminating the spike value P2.

The selection of the next value is within a band of samples that are ranked from the smallest to the greatest value. The median value is the output. For instance, the filtered signal at  $3kHz$  has a band of approximately  $7mV$  per side around the reference value of  $0.618V$  and its mean value per period matches with the reference. The same technique is used for a switching frequency of  $6.5kHz$ . The mean value deviates from the reference by less

## 5.2. Developed $v_{ce}$ measuring circuits

than  $1mV$ . The level of accuracy remains unchanged over the switching periods, which is satisfactory.

### Testing of pin-diode circuit

The performance of the pin-diode circuit is similar to the Zener diode circuit for the two switching frequency levels. The median filter is applied again. The performance test is again repeated and the results for the  $6.5kHz$  case are illustrated in Figure 5.12b. The mean value of the median filter output is  $3mV$  higher than the reference for the measurements at the switching frequency levels of  $3kHz$  and  $6.5kHz$ . Due to the capacitance of the anti-parallel diodes in Figure 5.6b the maximum voltage level does not have enough time to rise to the  $v_s$  level but it reaches about  $5V$  as illustrated in Figure 5.12a, whereas in Figure 5.13a the maximum voltage level has the time to stabilize. The measured value in Figure 5.12a and Figure 5.13a corresponds to the sum of  $v_{ce}$  and  $v_f$  according to Figure 5.6b. The ripple level is comparable to the Zener-based measuring circuit.

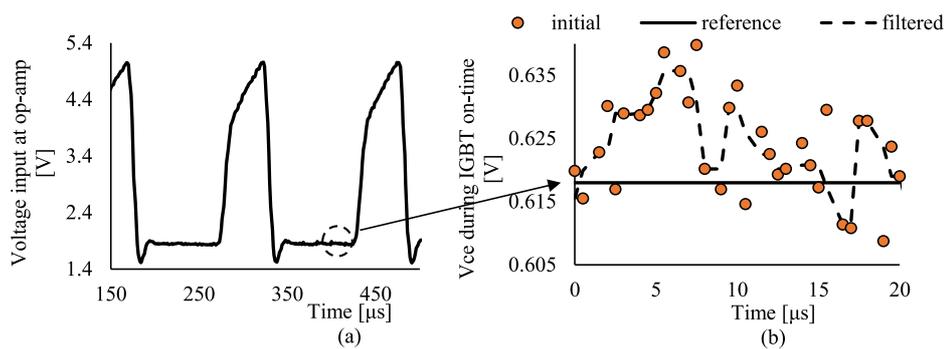


Figure 5.12: Measurements with the pin-diode based circuit for a switching frequency of  $6.5kHz$ : (a) Measured voltage at the op-amp input: high value for DUT at off-state, low value for DUT at on-state, (b) measuring interval of  $v_{ce}$  at on-state.

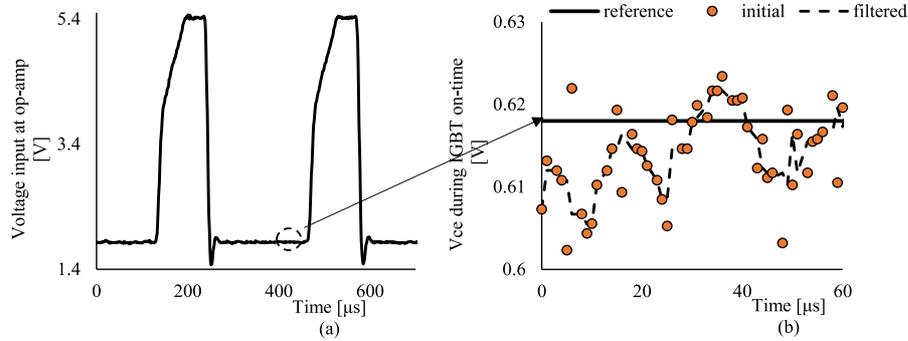


Figure 5.13: Measurements with the pin-diode based circuit for a switching frequency of 3 kHz: (a) Measured voltage at the op-amp input: high value for DUT at off-state, low value for DUT at on-state, (b) measuring interval of  $v_{ce}$  at on-state.

With the proposed testing method, the focus is on the precision of the  $v_{ce}$  measurement with sensing current. Both  $v_{ce}$  measuring circuits can be used for  $v_{ce}$  measurement with load current. A main difference in the design requirements between the two circuits is the need for an extra supply-voltage for the pin-diode circuit, in order to force the pin-diode to conduct. On the other hand, the Zener-diode circuit requires a calibration of the Zener diode, whereas the pin-diode circuit requires a calibration of the pin-diode and a total calibration of the circuit based on the expected  $v_{ce}$  variation during operation.

## 5.3 Presentation of IGBT Power Stack Integrity Assessment method (IPSIA)

### 5.3.1 Method overview

This method, primarily, targets the IGBTs, because they are the devices that are stressed the most in the specialized application, according to the analysis in Chapter 3. For the specialized application with the predefined current profiles and, as a result, thermal stressing profiles, it is not needed to monitor the temperature online and it is sufficient to check the aging status during scheduled service stops.

To date, relevant literature discusses methods for aging detection during operation in accelerated tests of the IGBT modules with the aim of field application. This work proposes a method that targets a complete high-power IGBT power stack and can be applied al-

### 5.3. Presentation of IGBT Power Stack Integrity Assessment method (IPSIA)

ready from the factory acceptance phase in order to validate the thermal path (and hence the assembly) from water to IGBT junction. Additionally, during service stops, the method can detect the aging and distinguish between the two common IGBT aging mechanisms, namely bond-wire lift-off and solder delamination. The novelty of the proposed method stems from (i) its ease of implementation by only switching two diagonal switches to create a testing current profile with only a fixed duty cycle pattern, (ii) the DUT on-the-stack calibration both with sensing and high current, (iii) the absence of power stack modifications for the DUT disconnection for the  $v_{ce}$  measurement with sensing current and for the production of the testing current cycle. The combination of the aforementioned features, as well as the measurement in the extended ZTC operating region avoiding the inflection point detection, makes this method a substantially improved sequence among the existing proposals for offline aging detection, especially for series of power stacks. The  $v_{ce}$  measurement in the extended ZTC operating region is originally presented for high-current modules together with the sensitivity analysis based on the current level, the precision of the  $v_{ce}$  measurement, as well as the junction, water and ambient air temperature. So far, the focus was only on the inflection point of ZTC operating region for IGBT devices with low and medium current ratings [55], [57] and [56].

The operation of the power stack according to the proposed method is presented in Figure 5.14. The semiconductor devices that are mostly stressed in the reference application are the diagonal switches  $T_{1,1}$  and  $T_{2,2}$ . By switching these diagonal switches and with the anti-parallel diodes of the other two diagonal switches in the H-bridge that is illustrated in Figure 5.14b, a current ramp-up and ramp-down is produced for the inductive load. A time interval of zero current remains in the end of the cycle. This cycle is repeated in every switching period. A typical output filter inductor is adequate for the implementation of the method. The dashed green line represents the shorting cable that by-passes the load for the production of the testing current cycle. In the unlike case that the output filter is not suitable, an inductive load at  $\mu H$  level should be used after disconnecting the power electronic converter from the filter and the load.

During the time interval of zero load current, one of the two diagonal switches that were previously conducting, is turned on with the other diagonal switch blocking the DC-link voltage. The sensing current is injected to the switch and the  $v_{ce}$  measuring method can provide the temperature estimation. Moreover, the  $v_{ce}$  reduction at the sensing current level between service stops is an indication of solder delamination that increases the thermal resistance and, finally, the temperature at junction level. During the current ramp-up,  $v_{ce}$  is continuously monitored and the value at the top of the ramp is stored to be compared with values during other service stops. At the top of the ramp, the current should be in the ZTC operating region, in order to detect the bond-wire lift-off, independently of temperature

Chapter 5. Method for IGBT Power Stack Integrity Assessment

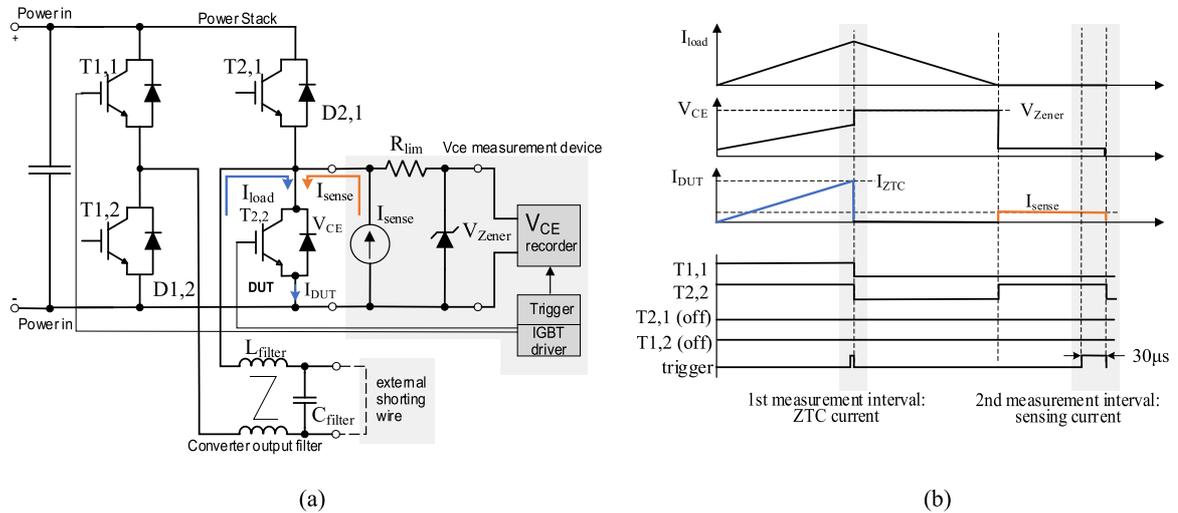


Figure 5.14: Operation during the proposed method, (a) H-bridge for  $v_{ce}$  measurement, the power components that are not used, such as the load, can be by-passed with a sorting wire (green line) (b) Waveforms of measured  $v_{ce}$ , load current, sensing current and gate pulses generated by open-loop controller with fixed duty cycle for the switches  $T_{1,1}$  and  $T_{2,2}$  during the proposed current cycle.

and of solder delamination. The resistance increment of the interconnection in the IGBT modules due to bond-wire lift-offs is amplified at a current level close to the nominal. On the other hand, at high current level,  $v_{ce}$  is highly dependent on temperature requiring very precise measurement, always under exactly the same temperature conditions. An additional reason for the selection of the ZTC operating region for the reference application is the limited current output that does not allow the operation at the level of nominal current.

According to [51], the beginning of aging and the degradation stage is detected via an increase of 3% and 10% in  $v_{ce}$ , respectively, at load current close to the nominal ratings of a high-power IGBT module. Moreover, an increase of 10% in junction-to-water thermal resistance is an indication of early failure. In [87], the junction-to-baseplate thermal resistance increase of 5% indicates the beginning of aging, 10% is an indication of degradation and 20% is an indication of failure. The thermal resistance estimation and its comparison with previous measurements is necessary, in order to prevent unscheduled stops due to unexpected failure.

### 5.3. Presentation of IGBT Power Stack Integrity Assessment method (IPSIA)

#### 5.3.2 Sampling-filtering technique and measurements utilization

For the  $v_{ce}$  measurement at sensing current a LabVIEW program is developed to acquire 30  $v_{ce}$  samples right before the current ramp-up, with a sample rate of  $1MHz$ . The maximum time duration of the measuring window is limited by the switching frequency for a given DC-link voltage and a given inductive load. Additionally, the settling time of the  $v_{ce}$  measuring circuit and the switching transients of the circuit set a minimum time length requirement. The  $v_{ce}$  value is independent of the gate-emitter voltage for  $v_{ge}$  value over  $10V$ , if the nominal  $v_{ge}$  is  $15V$ , as shown in Figure 5.15.

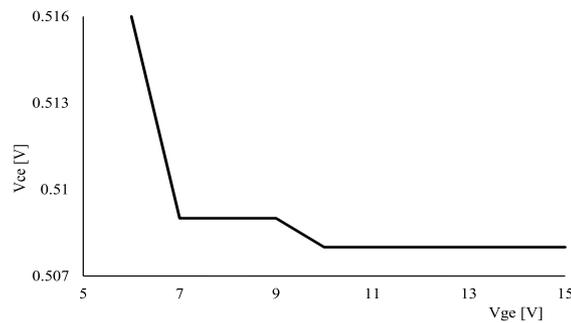


Figure 5.15: Measured sensitivity of  $v_{ce}$  with  $v_{ge}$  with a sensing current of  $1A$  for a temperature of  $30^{\circ}C$  for the IGBT module of the application.

Therefore, the settling time of  $v_{ge}$  is not adding delay. Every  $30ms$  the group of the last 30 samples belonging to a cycle is averaged and stored. The value of the averaging is the input to a median filter with a rank of 3, as illustrated in Figure 5.16. The turn-on signal for the other diagonal switch triggers the DAQ to save the last 30  $v_{ce}$  samples.

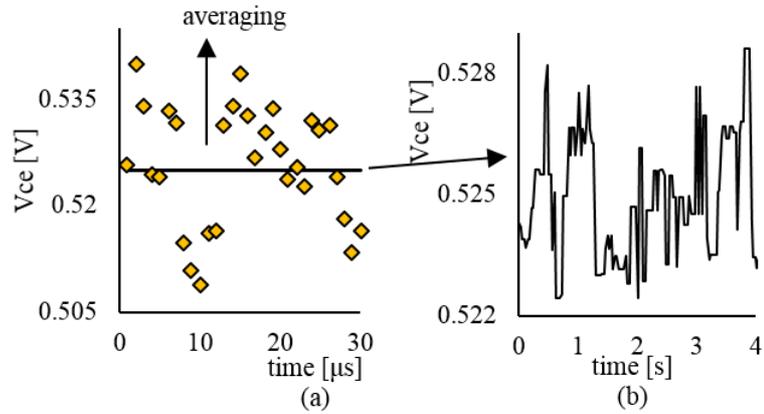


Figure 5.16:  $v_{ce}$  measurement at sensing current (a) Samples per period and averaging, (b) median filter output at steady state.

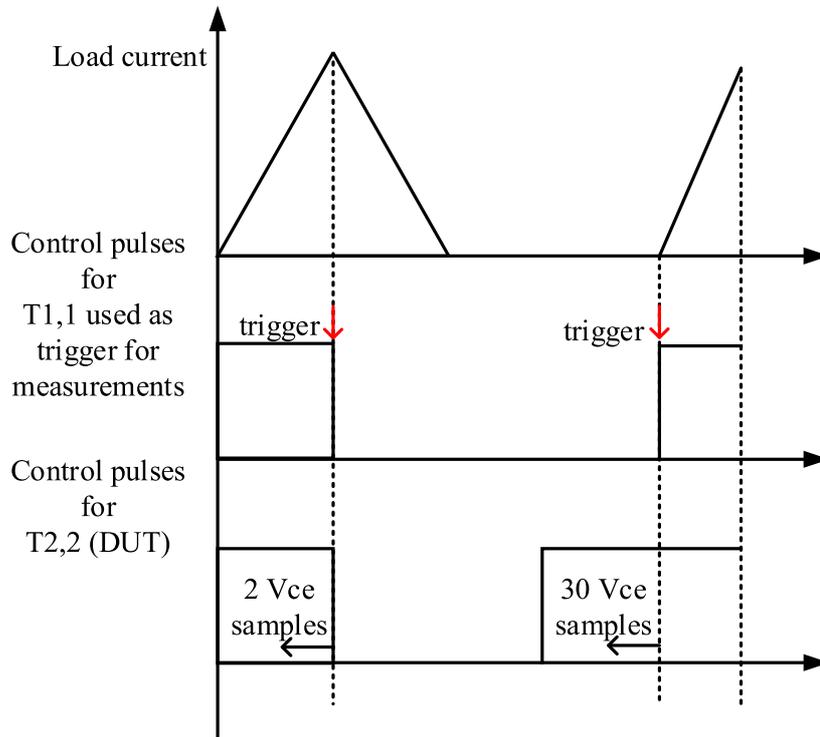


Figure 5.17: Triggering for  $v_{ce}$  measurement at high and at sensing current  $T_{2,2}$  used as DUT for demonstration.

### 5.3. Presentation of IGBT Power Stack Integrity Assessment method (IPSIA)

For the measurement at the top of the current ramp the number of samples depends on the rate of the current rise. The rate of the current rise depends on the DC-link voltage and the inductive load. For the ZTC operating region 2 samples are taken and their average  $v_{ce}$  is calculated. The ZTC operating region is defined in terms of current level in the section referring to the ZTC operating region calibration. For this application and the demonstration of the method, it is considered to be a current region with a range of  $\pm 15A$  around the inflection point. The peak current at the top of the triangle in Figures 5.14 and 5.17 belongs to this operating region. The rise time of the current is sufficient for  $v_{ge}$  stabilization [13]. The trigger signal for the DAQ to record  $v_{ce}$  is the turn-off pulse to the switches. Again, the value of the averaging is the input to a median filter. The trigger signals and the sampling technique are illustrated in Figure 5.17. Concerning the measuring circuit, the slew rate of the operational amplifiers must be adequate to follow the  $v_{ce}$  ramp-up that can be approximated as a part of a triangular waveform. The measuring circuit with a slew rate of  $2V/\mu s$  is sufficient for the needs of this application.

#### 5.3.3 On-the-stack IGBT calibration with sensing current

The thermal calibration of a single IGBT module in terms of  $v_{ce}$  at sensing current as a function of temperature is a fast procedure, as described in Chapter 2. A few measurements are enough to define the linear relation between  $v_{ce}$  and temperature that is usually around  $2mV/^\circ C$ . In the case of an already assembled power stack, the calibration of the IGBT modules in a thermal chamber becomes a non-practical solution. The proposed method for a fast-thermal calibration of an IGBT module that is, already, mounted on the cooling plate in the assembled power stack depends on the difference between ambient temperature and cooling water temperature. It is divided in the following two steps:

- measure  $v_{ce}$  for each DUT at sensing current and at ambient temperature. This is the first point in the linear relation between  $v_{ce}$  and temperature. At this stage there is no water flowing in the cooling plate.
- measure  $v_{ce}$  for each DUT at sensing current with water flow in the cooling plate. The measurement is obtained after waiting for thermal equilibrium that depends on the power stack's thermal time constant. The water temperature is assumed to be equal to the junction temperature.

The linear relation of temperature and  $v_{ce}$  at sensing current for the two switches is shown in Figure 5.18. Two measurements are obtained for each switch.

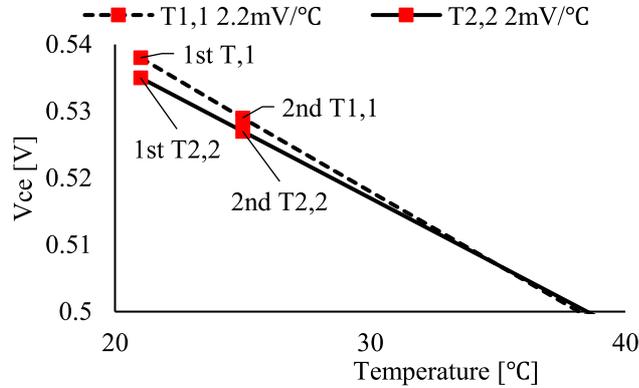


Figure 5.18: Thermal characterization of IGBT modules at sensing current with and without water flow in the cooling plate.

### 5.3.4 On-the-stack IGBT calibration in the ZTC operating region

The narrow current range of the IGBT module in the ZTC operating region can be defined with the help of the datasheet and with measurements. By applying the pulse of the proposed method in Figure 5.14a and by adjusting the current at the top of the ramp within the ZTC operating region according to the datasheet, the  $v_{ce}$  values at the top of the ramp are compared before the cooling plate reaches thermal steady state. If the change of the  $v_{ce}$  value is negligible during the time interval that the temperature at junction level changes, it means that the IGBT module operates in the ZTC operating region. Figure 5.19 focuses on the current region around the ZTC operating region with data that is taken from the datasheet. The two curves show the evolution of  $v_{ce}$  with a current change at  $25^{\circ}C$  and  $125^{\circ}C$ . The inflection point where there is no temperature influence to  $v_{ce}$  is close to  $375A$ . Around this point, it is observed that the change in  $v_{ce}$  is small at the same current level for the two temperature levels.

### 5.3. Presentation of IGBT Power Stack Integrity Assessment method (IPSIA)

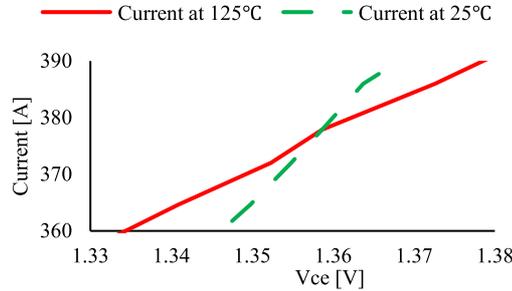


Figure 5.19: Relation of IGBT current and  $v_{ce}$  around ZTC operating region for  $25^{\circ}\text{C}$  and  $125^{\circ}\text{C}$ .

By using the datasheet values at these two temperature levels, Figure 5.20 shows the dependence of  $v_{ce}$  on temperature in  $\text{mV}/^{\circ}\text{C}$ . The change in  $v_{ce}$  as a function of temperature for a constant current is considered to be linear, as observed from measurements in [13]. It is observed that this relation is negative for current values lower than the inflection point by subtracting the  $v_{ce}$  value at  $25^{\circ}\text{C}$  from the value at  $125^{\circ}\text{C}$ . In a band of  $30\text{A}$  around the inflection point the maximum absolute value of this relation is about  $0.1\text{mV}/^{\circ}\text{C}$ . With the help of Figure 5.19 and Figure 5.20, a conclusion is that it is not critical to measure  $v_{ce}$  exactly at the inflection point, because the sensitivity of  $v_{ce}$  in temperature around this point is small. An observation that supports this analysis is documented in [56], where it is mentioned that for a tolerance of  $5\%$  in the inflection point  $v_{ce}$  differs by  $5\text{mV}$  if measured at approximately  $25^{\circ}\text{C}$  and at  $100^{\circ}\text{C}$ . For specified operating conditions, the change in temperature can be, only, caused by a change in cooling water temperature.

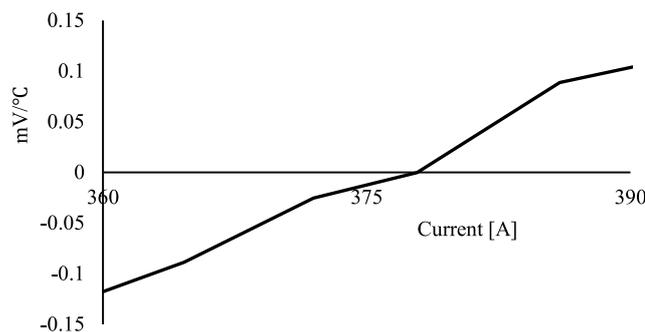


Figure 5.20: Dependency of  $v_{ce}$  on temperature around the ZTC operating region.

Based on manufacturers data [39], the impact of temperature at the resistance of bond-wires and interconnections inside the IGBT module is considered in the graph of Figure 5.19. On the other hand, a factor that is influenced by the ambient air temperature but is not considered in Figure 5.19 is the terminal-chip leads resistance  $R_{CC+EE}$ . Based on the datasheet the difference for a temperature from  $25^{\circ}C$  to  $125^{\circ}C$  is  $0.03m\Omega$ . The change in the resistance is calculated

$$R_{actual} = R_{ref}[1 + \alpha(T_{actual} - T_{ref})] \quad (5.10)$$

where  $R_{ref}$  is the reference resistance at the reference temperature  $T_{ref}$ ,  $\alpha$  is the temperature coefficient of resistance for the conducting material and  $T_{actual}$  the temperature during the measurement. Figure 5.21 shows the voltage drop change in the leads as a function of temperature for copper leads for a current at the level of the inflection point. As an example, the change of  $30^{\circ}C$  at the ambient temperature at the testing platform between two tests would lead to a change of about  $3mV$ .

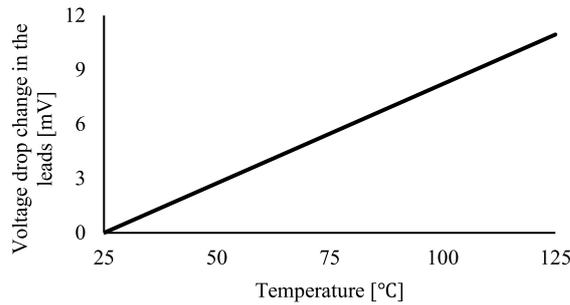


Figure 5.21: Voltage drop change at IGBT module power leads for current in the ZTC operating region as a function of ambient temperature.

### 5.3.5 Power losses estimation and thermal resistance calculation

The temperature estimation with the  $v_{ce}$  measurement at sensing current can be used for the calculation of the thermal resistance  $R_{th,j-w}$  of the IGBT module from junction to ambient, which is the water flow inlet [88]. This calculation can be used as a verification, within a certain accuracy margin, of the power stack's thermal design and of the thermal resistance value that is provided by the supplier. Moreover, it is useful for comparisons with measurements in future service stops, in order to track the  $R_{th,j-w}$  change with aging and detect solder delamination. The value of  $R_{th,j-w}$  is calculated with the help of

### 5.3. Presentation of IGBT Power Stack Integrity Assessment method (IPSIA)

$$R_{th,j-w} = \frac{\Delta T_{j-w}}{P_{loss}} \quad (5.11)$$

where  $\Delta T_{j-w}$  is the temperature difference between junction and water inlet and  $P_{loss}$  the sum of average switching and conduction losses of the IGBT module per switching period.

An advantage of this cycle is that the effort for the power losses estimation is limited. Due to the discontinuous current mode of the cycle in Figure 5.14a, there is no turn-on switching energy loss and only one measurement point is needed for the determination of the turn-off switching energy loss at the top of the current ramp. For this work, the power stack supplier's measurements at 400A, that is close to the ZTC operating region's current, as described in Figure 5.20, and 1000V for the switching energy loss are used for the calculation of turn-off energy loss, according to (2.12). For this work  $K_v$  is considered to be 1.3 that is the mean value of the provided range, as mentioned in Chapter 2. If any of the two extremes in this range was selected, the results would be influenced but the analysis would remain the same. The value of  $T_{j,ref}$  is 20°C.

The switching loss measurement is more precise than the datasheet value, thanks to the difference in the leakage inductance of the power circuit and the gate resistors that are used by the IGBT module manufacturer. For the IGBT module conduction losses the datasheet values for  $v_{ce}$  are used with a linear approximation from the lowest current value available in the datasheet down to  $v_{ce}$  at 1A, which is obtained during the IGBT module calibration.

Regarding the two anti-parallel diodes which conduct during the current ramp-down in Figure 5.14, their power losses are significantly lower than for the IGBTs. The diodes' switching losses are zero because they turn off at zero current in the end of the ramp-down. Therefore, the temperature measurements for the IGBTs are not, practically, influenced by thermal coupling with the diodes. Using (5.11) the accuracy of the method for  $R_{th,j-w}$  calculation can be compared with the accuracy of the traditional method for thermal impedance estimation at sensing current. According to the traditional method,  $v_{ce}$  with sensing current is measured for  $T_j$  estimation. The temperature measurement is measured both in the proposed method and in the traditional method with the  $v_{ce}$  method at sensing current, therefore the precision in terms of temperature estimation is considered the same. The advantage of the traditional method is that it offers precise value of the power losses because the IGBT conducts under constant current and constant  $v_{ce}$  at thermal steady state before the cooling down. The proposed method requires the measurement in dynamic conditions for the switching energy and linear approximations for the conduction energy that may lead to errors. The switching losses for the proposed cycle are significantly higher than the conduction losses, approximately five times more, therefore the error by the conduction losses linear approximations has a negligible impact. Another

difference between the two methods is that the  $R_{th,j-w}$  of the proposed method includes the thermal resistance due to the thermal coupling of the two operating IGBTs, especially if they are placed closed to each other, as illustrated in Figure 3.15 for the description of the FEM model.

Finally, the regulated inlet water temperature at each service stop eliminates any error that could occur, if two measurements were conducted at different services stops with different water temperature levels. For the specialized application, the criterion of 10% increase in thermal resistance can be adopted as an indication of degradation for the thermal resistance from junction to water assuming that no degradation will occur at the level of the thermal paste or of the cooling system due to accumulated particles in the cooling pipes. In practice, the monitoring of the water flow at the outlet and the particle filter at the inlet of the cooling plate protect the power stack from cooling degradation for the specialized application. Nevertheless, to support the aforementioned, a sensitivity analysis of  $R_{th,j-w}$  in terms of junction temperature measurement is presented in Section 5.4. Table 5.1 summarizes the main conclusions for the power losses and thermal resistance estimation with the IPSIA method.

TABLE 5.1: Power losses and thermal resistance  $R_{th,j-w}$  estimation for IPSIA

Power losses estimation	
Switching losses	only a turn-off switching instant (much higher than conduction losses)
Conduction losses	linear approximation for NTC operating region
Thermal resistance $R_{th,j-w}$ estimation	
Precision	depends on measuring circuit precision and power losses estimation
Aging criterion	10% $R_{th,j-w}$ increase

## 5.4 Results

### 5.4.1 Experimental demonstration of the method

The experimental setup of Figure 3.11a is used to obtain measurements and compare them with FEM and LPN calculations. All the measurements are conducted in an industrial environment with several high-power converters operating in the vicinity. The load current and load voltage along with collector-emitter voltage  $v_{ce}$  of switch  $T_{2,2}$  have been recorded. The load current of 365A keeps the semiconductor in the extended ZTC operating region below the inflection point in Figure 5.20. A dc-link voltage of 560V generates a

current ramp rate of approximately  $4.6A\mu s$  with the  $120\mu H$  reactor load, while a switching frequency of  $3kHz$  is adequate to generate enough switching losses as well as to allow adequate time for  $v_{ce}$  measurement with sensing current.

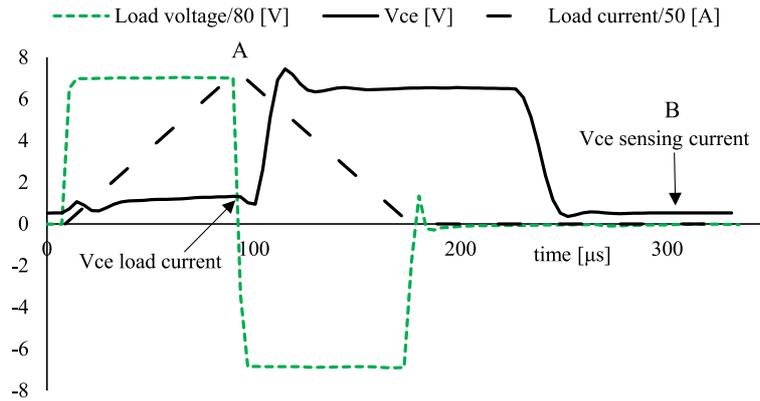


Figure 5.22: Operation overview during the cycle of the proposed method.

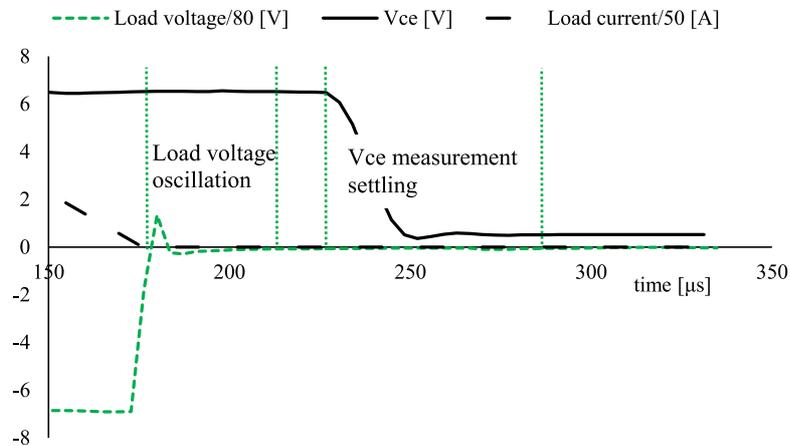


Figure 5.23: Signal settling for  $v_{ce}$  measurement at sensing current.

As can be seen in Figure 5.22 during the conduction of two diagonal IGBTs ( $T_{1,1}$  and  $T_{2,2}$ ) the current increases with a constant rate, and the  $v_{ce}$  voltage increases with the current

increase. At the top of the ramp in point A,  $v_{ce}$  is recorded under full load current. At approximately  $80\mu s$  the load current is directed to the anti-parallel diodes of the other two diagonal IGBTs. After the current ramp-down and during the operation with zero load current, the switch  $T_{2,2}$  alone that is considered as the DUT for the method explanation, is turned on and a sensing current is injected in point B of Figure 5.22. The switch  $T_{1,1}$  blocks the DC-link voltage. The voltage  $v_{ce}$  is stabilized before the  $300\mu s$  instant of the period. Figure 5.23 illustrates the signal settling for the  $v_{ce}$  measurement with sensing current. After a small load voltage oscillation, the switch  $T_{2,2}$  is turned-on and a bit more than  $50\mu s$  is the settling time for the recording to begin.

Figures 5.24 and 5.25 show the  $v_{ce}$  reduction of switch  $T_{2,2}$  with the temperature increase for a sensing current of  $1A$  and for water flow rate of  $12l/min$  and  $18l/min$ , respectively. The voltage value is recorded in the end of the cycle. The  $v_{ce}$  reduction for the case of  $12l/min$  corresponds to  $13^\circ C$  of junction temperature rise, whereas for the case of  $18l/min$  it corresponds to a  $10.5^\circ C$  rise. The operation in the low NTC operating region leads to the  $v_{ce}$  reduction with the junction temperature increase.

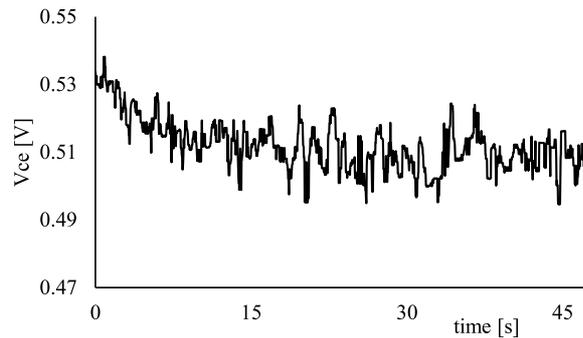


Figure 5.24:  $v_{ce}$  voltage reduction (with sensing current) as the junction temperature of switch  $T_{2,2}$  increases for water flow rate of  $12l/min$ .

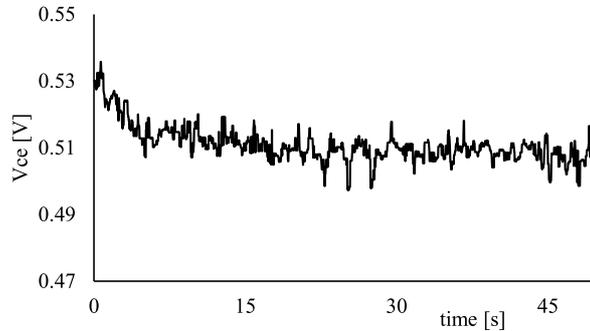


Figure 5.25:  $v_{ce}$  voltage reduction (with sensing current) as the junction temperature of switch  $T_{2,2}$  increases for water flow rate of  $18\text{ l}/\text{min}$ .

Table 5.2 provides the temperature rise for the two diagonal IGBT switches between the beginning of the cycling, which corresponds to the ambient temperature, and the thermal steady state. The proposed cycle is repeated for two cooling flow rate values at  $12\text{ l}/\text{min}$  and  $18\text{ l}/\text{min}$  and for the two diagonal switches  $T_{1,1}$  and  $T_{2,2}$ . Table 5.2 presents the temperature rise at junction temperature for the two diagonal IGBT switches obtained with the experiments, with the FEM model and the LPN model by taking into account the thermal coupling between the IGBT switches. The thermal coupling is not provided neither in the IGBT module manufacturer's data. For a more precise comparison, the FEM model is used to calculate the coupling between the two IGBTs mounted next to each other, as demonstrated in Figure 3.15. Additionally, the power losses injected to the FEM and the LPN simulation are presented. The steady-state LPN model of the power stack is used for the temperature rise calculations, as in Figure 5.26.

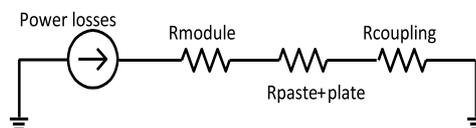


Figure 5.26: Steady-state LPN model of IGBT switch accounting for thermal coupling between the two IGBTs placed next to each other.

TABLE 5.2: Comparison of measurements, FEM and LPN simulations for temperature estimation

Flow rate [l/min]	$\Delta T$ Measurement [°C]	$\Delta T$ FEM [°C]	$\Delta T$ LPN [°C]	Power losses per IGBT [W]
12	12.7 ( $T_{1,1}$ ), 13 ( $T_{2,2}$ )	11.6	12.9	~330
18	11.8 ( $T_{1,1}$ ), 10.5 ( $T_{2,2}$ )	10.5	11.6	~330

### 5.4.2 Thermal resistance estimation and detection of solder delamination

Table 5.3 presents the estimation of  $R_{th,j-w}$  that is obtained with the experiment, the FEM and the LPN model. It is observed that the difference between the measurement and the FEM model is approximately  $0.004K/W$  for  $12l/min$ , whereas the LPN simulation matches with the measurements. The value of  $R_{th,j-w}$  from the measurements can be used as a starting reference for the comparison of thermal resistance values in the following service stops. For the specialized application the change of the inlet water temperature is expected to be kept within a range of  $1^\circ C$  that does not affect the measurement.

TABLE 5.3: Comparison of measurements, FEM and LPN simulations for thermal resistance estimation

Flow rate [l/min]	$R_{th,j-w}$ Measurement	$R_{th,j-w}$ FEM	$R_{th,j-w}$ LPN
12	0.039 ( $T_{1,1}$ ), 0.038 ( $T_{2,2}$ )	0.035	0.039 (0.036 without thermal coupling)
18	0.036 ( $T_{1,1}$ ), 0.032 ( $T_{2,2}$ )	0.032	0.035 (0.033 without thermal coupling)

As Figure 5.27 shows, for other applications, where the temperature of the cooling water changes, the thermal resistance would increase by 5% and 10% for a water temperature increase of  $20^\circ C$  and  $40^\circ C$ , respectively. This increment results from the comparison with the previous measurement with both values calculated with the power losses before the water temperature rise. Selecting the worst case, the switching losses increase is considered for the power losses because they increase with temperature, whereas the conduction losses that are much lower are assumed to remain the same. In practice the conduction losses even decrease with temperature in the NTC operating region. If the power losses at the increased water temperature were considered for the  $R_{th,j-w}$  estimation,  $R_{th,j-w}$  would, roughly, remain the same. Based on FEM, the power losses increase and not the Si thermal conductivity is the main factor for the thermal resistance rise. The water tempe-

perature change is a factor that should be considered for significant variations between the tests.

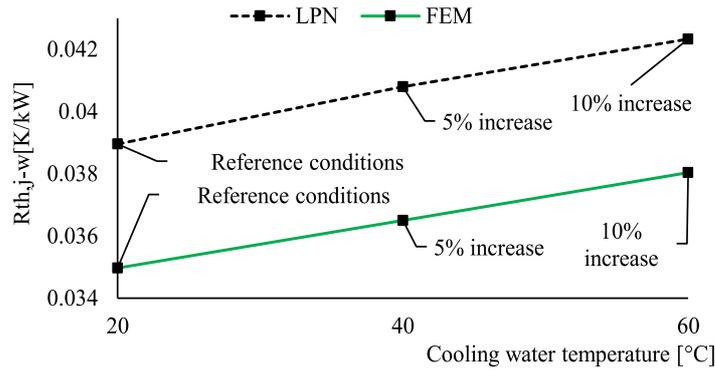


Figure 5.27: Thermal resistance estimation error with cooling water temperature increase.

The temperature decrease of the IGBT during the off-time interval of  $220\mu s$  between the current peak value and the  $v_{ce}$  measurement at sensing current is simulated using FEM. The FEM model is more accurate than the LPN model for such a short time cooling-down interval right after the heating power injection. The RC parts of the LPN dynamic model do not correspond to the physical layers of the IGBT module [67]. Moreover, no information is given below 1ms about the thermal impedance in the IGBT datasheet. The thermal time constant of the chip is, with the help of (2.5) and (2.6), approximately  $550\mu s$ , therefore the cool-down for  $220\mu s$  is limited to chip level. The initial condition for the model is the thermal steady state at this cycle and no heating power is injected to the chips. The temperature decrease after  $220\mu s$  is less than  $0.2^\circ C$ , accordingly negligible. It, slightly, affects the calculation of  $R_{th,j-w}$ . The thermal mass of the high-power IGBT module results in a high thermal capacitance and relatively slow thermal time constant compared to IGBT modules with lower power ratings. The cooling down response of the IGBT module remains the same independently of the temperature rise at current peak with the proposed current cycle. Therefore, the temperature decrease within the time interval between the current peak and the  $v_{ce}$  measurement with sensing current has in percent of the temperature at the current peak the same value, independently of the temperature value at current peak.

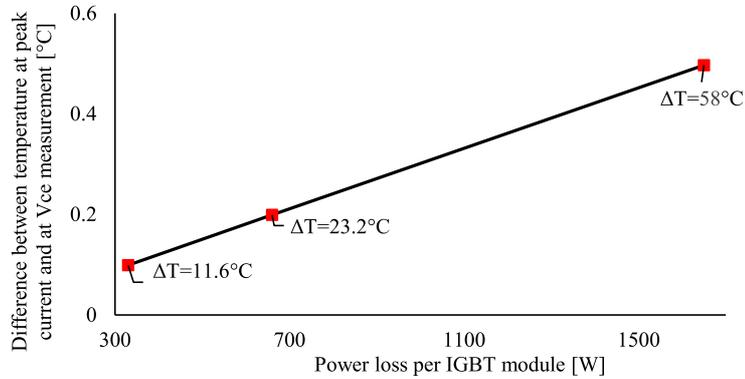


Figure 5.28: Difference of temperature at peak current and with  $v_{ce}$  measurement with sensing current as a function of power losses for different junction temperature rises at steady state.

On the other hand, the absolute temperature decrease for the relatively low temperature rise of the proposed method, as shown in Table 5.2, is smaller than it would be for a higher temperature rise. Figure 5.28 illustrates the increase of the difference between the temperature at peak current and the temperature that is estimated with  $v_{ce}$  with sensing current as the power losses increase. The temperature rise above water temperature level at peak current is written for every power losses level. The data is obtained with the help of FEM simulations. However, the relative error in the  $R_{th,j-w}$  estimation remains the same, therefore the precision in  $R_{th,j-w}$  is not affected.

The precision of the measuring circuit may affect the thermal resistance estimation at the service stops and, therefore, the health state estimation of the IGBT module in terms of solder delamination. According to (5.11), with an assumed accuracy within  $+/- 1^\circ C$  in the measuring circuit, the deviation in  $R_{th,j-w}$  estimation at the service stops can be calculated for the nominal flow rate of  $12l/min$  at the level of 7%. Therefore, a change below 7% in the value of  $R_{th,j-w}$  could be due to the measurement uncertainty and it is not considered as degradation. However, the change over 10% can be set as an indication for solder degradation. It is observed that the impact of the temperature estimation at the  $R_{th,j-w}$  is smaller, if the temperature rise is higher. It is noticed that for power losses higher than for the proposed operating conditions the temperature rise would be higher resulting in a smaller relative error in  $R_{th,j-w}$  estimation. In this case, the proposed method becomes more sensitive and detects  $R_{th,j-w}$  changes below 7%. The power losses increase could be achieved, for instance, if a double DC-link voltage value (there is a safety margin until the

1.7kV nominal rating of the IGBT module) and double inductive load value were assumed, in order to significantly increase the switching losses.

### 5.4.3 Detection of manufacturing issues

This test aims to demonstrate the detection of thermal effects caused by the wrong IGBT mounting. The detection of thermal paste deficiency is used as an example of wrong IGBT mounting. In this test, different thermal paste layer thicknesses are applied, according to the guidelines in [89], before mounting an open IGBT module on a cooling plate. The experimental set-up of Figure 3.11b is used. The current cycle of the proposed method is applied with a peak current of 450A to increase the semiconductor power losses and exhibit higher temperature variations across the thermal resistance. The open IGBT module is always turned-on, therefore it does not produce any switching losses. The current profile of the open IGBT is the same as the load's triangular load current profile in Figure 5.14a. The temperature is estimated using the  $v_{ce}$  measurement with sensing current on the open IGBT module and it is compared with the average temperature among all chips measured using infrared imaging. Table 5.4 summarizes the junction temperature estimation with the sensing current method and the infrared camera measurements for the different thermal paste cases.

TABLE 5.4: Comparison between thermal camera and  $v_{ce}$  measurements of temperature rise for different thermal paste conditions

	No thermal paste	Reduced thermal paste	Normal thermal paste
Layer thickness	$0\mu m$	$50\mu m$	$100\mu m$
Junction temperature change $v_{ce}$ method [ $^{\circ}C$ ]	13	10	6
Junction temperature change thermal camera [ $^{\circ}C$ ]	11.5	8.5	5.5

When no thermal paste is applied as well as when the thermal paste is not adequate ( $50\mu m$ ) or pumped out due to excessive mounting force, a significant increase in  $R_{th,j-w}$  is observed. The indication is the increase in the junction temperature rise. During the experiments, it was noticed that for the specific current profile, the application of thermal paste with thickness about  $200\mu m$  did not cause any detectable difference compared to the case with nominal thermal paste.

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Figure 5.29 shows as an example of a thermal camera measurement and the average temperature for each chip in the case without thermal paste and for a cooling water temperature of approximately  $23^{\circ}\text{C}$ . There is a small deviation in the average temperature among the chips that may be a result of the mounting on the cooling plate or of the cooling channels. Due to the small temperature rise and the small temperature fluctuation during the cycle, the difference between the maximum and the average temperature on the chip surface is not significant.

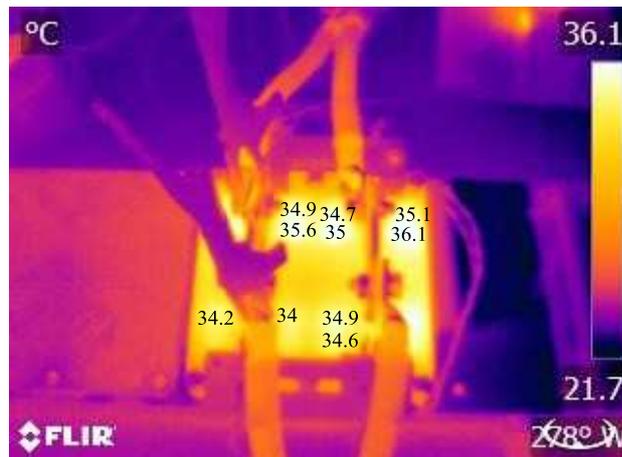


Figure 5.29: Thermal camera measurement and average temperature for each chip in the case without thermal paste for a triangular current pulse with peak of approximately 450A and for a cooling water temperature of approximately  $23^{\circ}\text{C}$ .

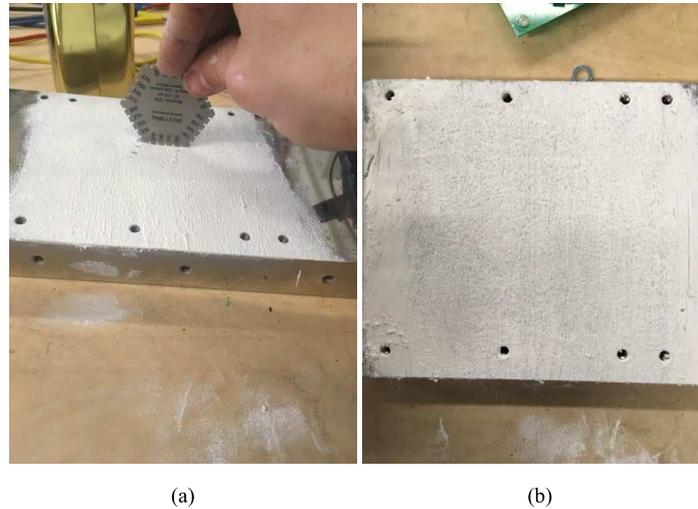


Figure 5.30: (a) Measurement of thermal paste thickness of approximately  $200\mu m$ , (b) thermal paste thickness of approximately  $50\mu m$ .

Figure 5.30 shows the measurement of the thermal paste thickness of approximately  $200\mu m$  and the thermal paste of approximately  $50\mu m$  applied on the cooling plate.

#### 5.4.4 Bond-wire lift-off detection

The experimental set-up of Figure 3.11b is used for the bond-wire lift-off detection in the ZTC operating region. The bond-wires of a chip are intentionally cut one-by-one and the change in  $v_{ce}$  voltage is registered for each cut. The measurement of  $v_{ce}$  is carried out at the top of the ramp-up by averaging the last two  $v_{ce}$  values. For these test series, only one substrate out of four is used, in order to be able to operate it in the PTC operating region and at a current level close to the rated. The bond-wire lift-off effect in both ZTC ( $92A/\text{substrate}$ ) and PTC ( $360A/\text{substrate}$ ) operation regions are evaluated. Figure 5.31 shows the  $v_{ce}$  evolution during the current ramp-up measured with an open module. The difference between the datasheet values and the measurements is due to the parasitic inductance and terminal-chip leads resistance in the measurement setup. Moreover, the measuring circuit is connected to the cables close to the IGBT module power leads with crocodile clips adding an offset to the measured voltage due to the cables resistance. The difference between the datasheet and the measured values increases with the current increase because the parasitic resistance effect is amplified at high current values.

As an additional investigation, the aging stage, in terms of bond-wire lift-off, that can be

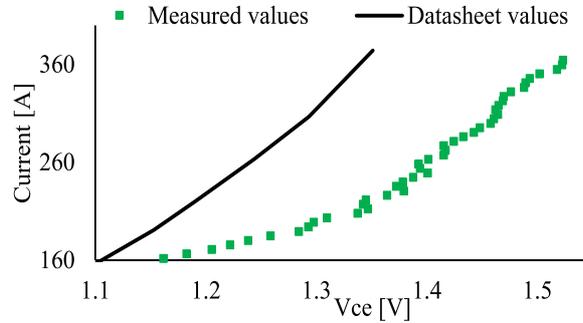


Figure 5.31:  $v_{ce}$  values at chip level during current ramp-up of approximately  $4.6A/\mu s$  according to datasheet and  $v_{ce}$  values close to power leads according to measurements.

detected with the  $v_{ce}$  measurement with sensing current is investigated with the open IGBT module. The independent control of each substrate and the switching from four-substrate to three-substrate operation demonstrates the loss of one substrate that results to a  $v_{ce}$  increase of approximately  $15mV$ , as illustrated in Figure 5.32.

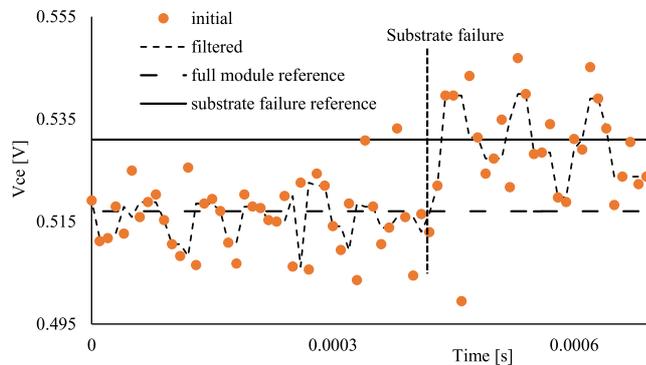


Figure 5.32: Measurements to demonstrate the detection with sensing current of a substrate failure for the 1.6kA IGBT module of the application.

Table 5.5 presents the results from the bond-wire lift-off detection in ZTC, PTC and NTC operating regions with sensing current. It, also, includes results that are documented in the literature from the bond-wire lift-off detection in ZTC and PTC operating regions.

It is observed that for the PTC operating region case, the cut-off of two bond-wires provides clear evidence of aging. Generally, the test current cycle could be applied with a

TABLE 5.5: Bond-wire lift-off detection with the  $v_{ce}$  method in the NTC, ZTC and PTC operating regions

Module ratings [V/A]	Module number of bond-wires	Bond-wires cut	Operating region	$v_{ce}$ change [mV]
1700/1600	160	8/9 /10 (chip failure)	ZTC	4/6/12
1700/1600	160	40 (1 substrate)	NTC sensing current	14
1700/1600	160	2/3	PTC	10/15
1700/1000	96	1/2	PTC	$\sim 5/10$ [13]
600/70	not available	1	ZTC	$\sim 200$ (20% $v_{ce}$ [56])

peak current value close to the nominal rating of the IGBT module. The main concerns are the slew rate of the current for the measuring circuit and the combination of DC-link voltage and inductive load that are required for such a current ramp-up. Concerning the ZTC operating region case, the relatively low current does not allow the detection of loss of a few wire bonds, but it gives a clear indication that more than half of the connections to a chip are lost. According to Figure 5.21, an increase of around  $30^\circ\text{C}$  in the ambient temperature could have the same impact at  $v_{ce}$  as the eighth lift-off on the chip.

Due to the current overrating of the IGBT module for lifetime extension, the module could, theoretically, operate even with the loss of a substrate. Therefore, the detection of a substrate loss at the service stop may be sufficient as a warning to prevent the complete failure of the module for this application. However, this method cannot be widely applicable. For a discrete device as in [24], [56] and [55], the  $v_{ce}$  measurement in the ZTC operating region is more sensitive, due to the smaller number of parallel bond-wires and can detect a single bond-wire lift-off. Therefore, the method could be more effective in terms of lift-off detection for low power devices.

It is interesting to examine if a whole chip failure influences the  $v_{ce}$  measurement with sensing current and, therefore, the solder delamination detection. The change of the average temperature among the healthy chips of the IGBT module, if a whole chip fails, is simulated with FEM for the proposed cycle. The increase in  $R_{th,j-w}$  would be about 5%, which is less than the 10 % criterion that is set for solder delamination detection. Therefore, there would be insignificant overlapping in the detection of the lift-off and solder delamination until a whole chip fails. The chip failure detection can be achieved with the high current  $v_{ce}$  measurement and can be considered for the solder delamination detection.

Based on Figure 5.20, the sensitivity of  $v_{ce}$  with temperature at this current level is approximately  $0.1mV/^\circ C$ . Finally, the water temperature is a parameter that can change in other applications. For a significant water temperature change of  $20^\circ C$ , the  $v_{ce}$  change is only  $2mV$ . Furthermore, based on FEM results, the impact of water temperature change at the thermal conductivity of silicon does not affect the measurement in the ZTC operating region.

Table 5.6 provides an overview of the parameters and their margin in the precision of the temperature estimation and of the aging detection according to the proposed method.

TABLE 5.6: Summary of sensitivity analysis of IPSIA method with the specialized application as reference

Variables	Aging parameters influenced by variables	Margin of change for variable	Impact at precision within the margin
$v_{ce}$	$R_{th,j-w}$	$\pm 1^\circ C$	7% (lower for higher power losses)
Water temperature	$R_{th,j-w}$ /solder aging	$\pm 20^\circ C$	5%
Ambient temperature	Bond-wire lift-off	$\pm 30^\circ C$	$3mV$ close to impact of 8th bond-wire lift-off
Peak current value	Bond-wire lift-off	$\pm 15A$	approx. $0.12mV/^\circ C$

Finally, Table 5.7 compares the existing methods in the literature using  $v_{ce}$  measurements for aging detection with the proposed method. The method in this work proposes the short-circuit of the load during service stops and the exploitation of the output filter inductor. The method with a power circuit similar to the presented is found in [55]. The prognostic procedure in [55] uses a different current profile and detects only bond-wire lift-off exactly at the inflection point. The rest of the methods require additional power components. The advantage of the proposed method is the reduction of the additional equipment and control complexity, the ease of calibration for already assembled power stacks and the negligible impact of junction temperature at bond-wire lift-off detection due to the operation in the extended ZTC operating region, without the need to measure at the inflection point. Among the methods, it is distinguished for its ease of implementation for a series of power stacks. However, the bond-wire lift-off detection in the ZTC operating region for the high-current modules in the experiment, is feasible when more than half of the chip's bond-wires are detached. On the other hand, the high-power IGBT modules offer redundancy due to their high number of bond-wires in parallel compared to the discrete devices with lower ratings.

TABLE 5.7: Overview of IGBT aging detection methods for assembled power stacks using  $v_{ce}$  measurements

Method	Target	Power stack modifications - extra power components	On the stack $v_{ce}$ calibration	Detection level	Temperature sensitivity lift-offs/solder del.
in PTC [24], [54] Fig. a	Lift-off and solder del.	IGBT, relay, high current source	No	Early detection for solder del., lift-offs (but for low current devices)	High to junction temperature /Low, only for significant cooling temperature change between tests
in PTC [22], [23] Fig. b	Lift-off and solder del.	2 IGBTs and two MOSFETS	No	Early detection for solder del., lift-offs	High to junction temperature /Low, only for significant cooling temperature change between tests
in ZTC [55], Fig. c	Only lift-off	Inductor and relay only if load is not suitable	No	Early detection for lift-offs (but for low current devices)	Negligible to junction temperature /not detected
Proposed method (IPSA) in ZTC	IGBT mounting lift-off solder del.	None/ $\mu H$ level inductor and relay only if output filter is not suitable	Yes, suitable for assembled power stacks	Early detection for solder del. / more than half chip failure due to lift-offs (but for high current devices)	Low to junction temperature/ considerable for more than $20^{\circ}C$ temp. change between tests

## 5.5 Summary

A method is proposed for the integrity assessment of a semiconductor power stack throughout its life-cycle; from factory acceptance to its end of useful life in operation. Additionally, for the implementation of the method, two  $v_{ce}$  measuring circuits are presented and analyzed offering ease of calibration and simple implementation. The proposed method exhibits advantages that are essential for the integrity assessment of a series of IGBT power stacks in industrial scale. Concerning the application of the  $v_{ce}$  method with sensing current, the method requires no additional circuitry for the DUT isolation and offers a fast thermal calibration of the mounted IGBT modules. Moreover, it is performed with just a fixed duty cycle pattern. It is shown, using the specialized application as an example, that the absence of the thermal paste layer can be detected during factory acceptance tests, because it causes twice the junction temperature rise compared to the case with the normal thermal paste thickness. Once the equipment is in operation, solder delamination can be detected during scheduled service intervals. Using the reference application, a temperature change of more than  $20^{\circ}C$  in the cooling water temperature would have a considerable im-

## *Chapter 5. Method for IGBT Power Stack Integrity Assessment*

pact of 5% on the thermal resistance estimation and, as a result, on the solder delamination detection. By presenting a sensitivity analysis of  $v_{ce}$  in the ZTC operating region as a function of current, junction, water and ambient temperature, it is demonstrated that the  $v_{ce}$  measurement does not have to be carried out exactly at the inflection point, since the effect of junction and ambient temperature at  $v_{ce}$  is not significant in the extended ZTC operating region. However, in the ZTC operating region for high-current modules, the detection of wire bond lift-off is only possible when more than half of the wire-bonds of the chip have failed. It is shown that the voltage drop of power leads may be important for the precision of such measurement for ambient temperature changes of at least  $30^{\circ}C$ .

# Chapter 6

## Thermal stressing mitigation possibilities for a power stack

### 6.1 Introduction

In the previous chapters the specialized application was presented in terms of thermal stressing and a method for the thermal performance evaluation and aging detection of the power stack was proposed. Focusing on the prevention of the aging due to thermal stressing, this chapter is a study investigating the possibility for thermal stressing mitigation of the power stack with actions in the design and in the operation phase. The first part investigates possible improvements in the design of the cooling system with the aim to reduce the thermal stressing of the semiconductors. It focuses on the impact of the cooling plate thickness and material on the junction temperature swing and maximum value. The second part is dedicated to the active mitigation of the thermal stressing using the switching frequency and the gate on and off resistance values as mitigation parameters. Both parts use the reference magnet power supply as a starting point for the investigation. The material of this chapter is published in publications III and VI.

### 6.2 Cooling system investigation for thermal stressing mitigation

The first part of the investigation of the thermal stressing mitigation focuses on the cooling system of the power stack. The magnet power supply including the LPN of the H-bridge

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is simulated using the software PLECS that offers the possibility for thermal modeling of semiconductors. The thermal networks are connected in series forming the total thermal network that represents the whole power stack; the power module, the thermal paste, the cooling plate and the modeled heat convection to the ambient, see Figure 6.1c. The value of the thermal paste's thermal resistance is found in the IGBT module datasheet. The IGBT module that is used is the one used in the previous chapters. The thermal coupling among different IGBT modules is at the level of the thermal paste. The position of the IGBTs on the cooling plate is assumed as having no influence in the thermal coupling among the modules, in contrast with the the actual power stack in Chapter 4. According to the analysis in Chapter 3, the mostly stressed devices are the IGBTs Q1 and Q4 that have an equal load, see Figure 6.1a. The focus is on the temperature profile of one of these diagonal IGBT switches. The losses are calculated as described in Chapter 2. The DC-link nominal voltage is 900V and the current shape provided to the magnet is considered to be a trapezoidal pulse with an increased current magnitude of 600A, a ramp-up and ramp-down time of 1s each and a total on-time of 8s within a time period of 100s. This is one of the cycles at which a magnet power supply could be expected to operate, in reality with lower current magnitude and with a shorter turn-off time to combine it with other cycles within the 100s. This profile could, also, occur in traction applications under similar circumstances. This mission profile of the semiconductor module represents a high thermal stress in terms of junction temperature swing leading to a decreased number of cycles until the end of lifetime.

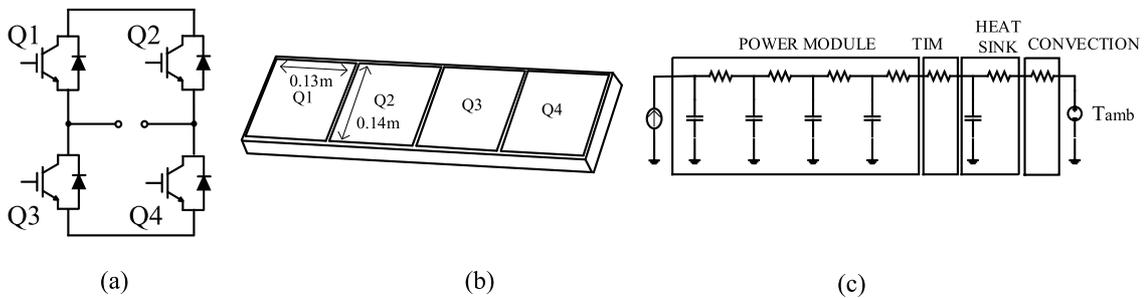


Figure 6.1: (a) H-bridge power circuit, (b) mechanical layout, (c) thermal model of IGBT/diode junction-to-ambient.

The cooling plate area is selected to be equal to the total area of the four power modules that is four times each of the modules area  $0.130m \times 0.140m$ , see Figure 6.1b. This assumption for mounting is very close to the real case in the reference power stack. For simplification, it is assumed that the geometry of the cooling plate is a simple orthogonal body. The thickness of the cooling plate at the module side is varied to observe its impact

## 6.2. Cooling system investigation for thermal stressing mitigation

on the thermal stressing of the module. The heat convection is modeled with one main water channel and it is uniform below the cooling plate layer, as illustrated in Figure 6.2. It is considered that the heat is, uniformly, spread in the baseplate and, then, into the cooling plate.

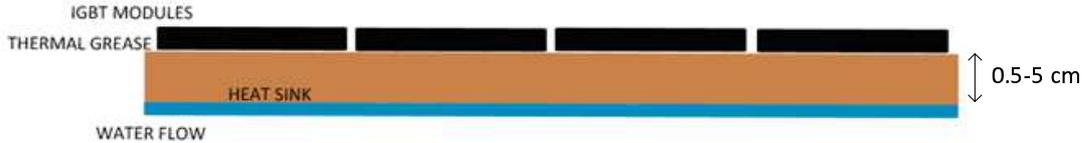


Figure 6.2: Power stack structure.

The materials under investigation are aluminum and copper. Copper is the preferred material at CERN. The existence of copper components in the cooling network prohibits the use of aluminum to avoid corrosion. However, copper is more expensive and less environmentally friendly [48]. The metallic materials in the cooling network of CERN are stainless steel and copper. Table 6.1 demonstrates the relevant material characteristics of aluminum and copper.

TABLE 6.1: Aluminum and copper thermal properties of interest

	Aluminium	Copper
Density [ $kg/m^3$ ]	2700	8960
Thermal conductivity [ $W/m^\circ C$ ]	238	400
Specific heat capacity [ $J/kg^\circ C$ ]	900	385

The thermal resistance of the aluminum cooling plate is higher than that for the copper cooling plate. The specific heat capacity of aluminum is higher than the value for copper but the thermal capacitance of the copper cooling plate is, finally, greater by approximately 40% due to its significantly larger material density. For long cycle applications, the use of a copper cooling plate could be beneficial due to its high heat storage characteristic. For stationary systems as the magnet power supply of this application, the weight disadvantage of copper is not important. The cooling plate thickness values selected are relatively high, in order to compensate for the thermal capacitance that is lost due to the limited surface area of the cooling plate. The increased thickness of the cooling plate has a negative impact on the thermal resistance of the cooling plate.

According to (2.5) and (2.6), for the same dimensions the thermal resistance and the thermal capacitance ratios of aluminum over copper are approximately

$$R_{(th,Al/Cu)} = 1.68 \quad (6.1)$$

$$C_{th,Al/Cu} = 0.70 \quad (6.2)$$

Table 6.2 shows the different thickness values and the corresponding thermal resistance and thermal capacitance values of the aluminum and the copper cooling plate body, based on (2.5) and (2.6). Copper, as expected, exhibits better thermal performance than aluminum. Copper price is, currently, higher than for aluminum, therefore the decrease of copper cooling plate dimensions, due to its high thermal performance, could make this solution attractive.

TABLE 6.2: Thermal characteristics of aluminum and copper cooling plate for different values of thickness

Thickness	Thermal capacitance [ $J/^\circ C$ ]		Thermal resistance [ $^\circ C/W$ ]	
	Aluminium	Copper	Aluminium	Copper
0.5	881	1220	$2.88 \cdot 10^{-4}$	$1.38 \cdot 10^{-4}$
1	1760	2440	$5.77 \cdot 10^{-4}$	$2.76 \cdot 10^{-4}$
3	5280	7320	$17 \cdot 10^{-4}$	$8.28 \cdot 10^{-4}$
5	8810	12200	$28.8 \cdot 10^{-4}$	$14 \cdot 10^{-4}$

The next step is to define the cooling plate convection coefficient to the ambience, similar to [90]. The heat is assumed to be extracted only from the bottom side of the cooling plate. A moderate water-cooling convection coefficient,  $h$  equal to  $5kW/(^\circ C m^2)$  [91] is, initially, used in this work. The thermal resistance from cooling plate-to-ambient is calculated with the expression

$$R_{th,hs-a} = \frac{1}{hA_{hs}} \quad (6.3)$$

where  $A_{hs}$  is the whole lower surface of the cooling plate that is in contact with the water, as illustrated in Figure 6.2.

### 6.2.1 Results on cooling system investigation

By using LPN simulations based on the copper and aluminum cooling plates, the temperature is recorded throughout the power cycle at the top of the thermal paste, representing

## 6.2. Cooling system investigation for thermal stressing mitigation

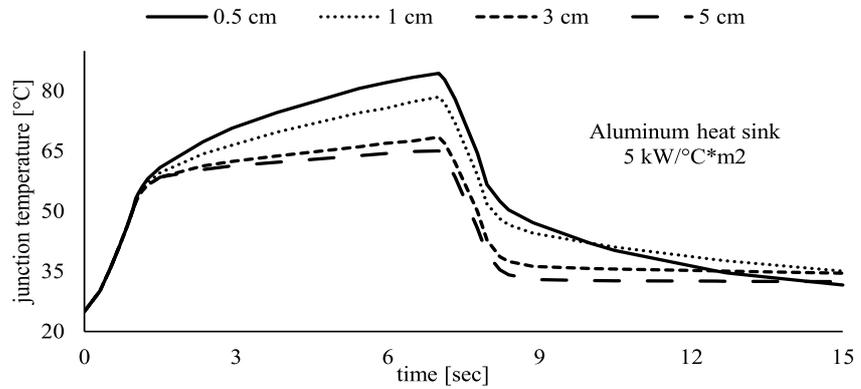
the level directly below the baseplate of the IGBT and at the junction of IGBT switch Q1. The focus is on the temperature profile at junction level that is considered to be more critical than the temperature profile at baseplate level, as it is going to be mentioned later in this section. For all figures the focus is on the first fifteen seconds of the cycle where the most interesting part of the response takes place. For every case, within the 100s cycle, the junction temperature returns to the initial level that is assumed to be the water inlet temperature of  $25^{\circ}C$ .

Figure 6.3a and Figure 6.3b illustrate the junction temperature for the different values of thickness between  $0.5cm$  and  $5cm$  for the aluminum and the copper cooling plate. The heat convection coefficient used in both cases is  $5kW/(^{\circ}Cm^2)$ . The temperature response is almost identical for all the thickness values at the first second. According to the IGBT datasheet, this time period represents, approximately, the time until thermal steady state for the module itself, therefore for pulses shorter than one second, the cooling plate makes no difference. For the  $0.5cm$  cooling plate, the thermal capacitance is very low leading to a high maximum temperature of approximately  $85^{\circ}C$  and, also, to a high temperature swing from the maximum temperature to the ambient temperature. Similar observations are valid for the  $1cm$  cooling plate, with a maximum temperature of  $78^{\circ}C$ .

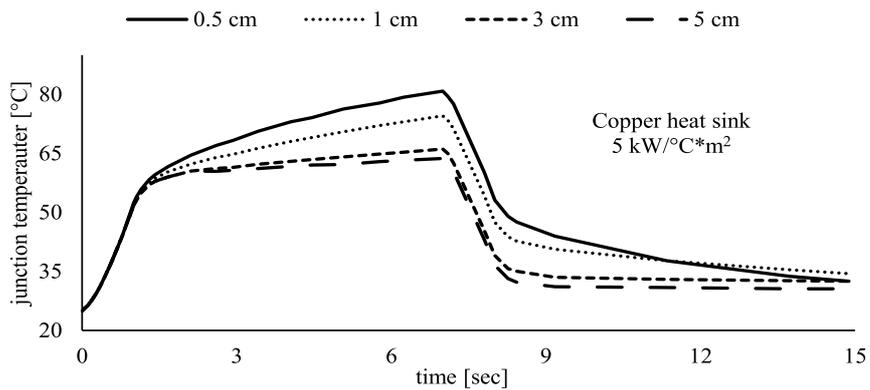
For the two thick cooling plates the difference is small, although the increase in the thickness is significant. The  $3cm$  cooling plate limits the junction temperature to a maximum of  $68^{\circ}C$  and the temperature swing to  $43.5^{\circ}C$ . In the  $5cm$  cooling plate case, the increased thermal resistance obstructs the heat extraction and the thermal capacitance is not high enough to further filter the temperature swing. For the  $5cm$  cooling plate the temperature swing is  $40.1^{\circ}C$  and the maximum temperature around  $65^{\circ}C$ . Independently of the application, the  $3cm$  cooling plate would be selected for the aluminum case, due to its dimensions and weight advantage over the  $5cm$ .

In the copper cooling plate case, see Figure 6.3b, the observations are the same as for the aluminum. Despite the better thermal characteristics of copper, its increased cost outweighs the benefit in the temperature variation. If the  $3cm$  cooling plate is compared for aluminum and copper, the lead of copper is only  $2^{\circ}C$  for the maximum temperature and for the temperature swing.

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(a)



(b)

Figure 6.3: (a) Junction temperature response for different thickness values of aluminum cooling plate, (b) Junction temperature response for different thickness values of copper cooling plate, both cases with a convection coefficient of  $5kW/({}^{\circ}Cm^2)$ .

Moreover, a second model is built to run an AC sweep analysis for the heat produced at the most stressed device of the H-bridge. This set-up can be represented again by the Cauer network of Figure 6.1c. In this way the Bode plot magnitude diagram for the power loss extracted to the ambient in relation to the power losses produced by the device is obtained covering the range of frequencies included in the application. The Bode plot diagram of

## 6.2. Cooling system investigation for thermal stressing mitigation

Figure 6.4 illustrates the heat extraction ability for the different thickness values of the aluminum case by presenting the output heat to the ambient with respect to the input heat at chip level. The focus is on the frequency range of the power magnet supply current pulses. The 0.5cm case demonstrates the highest ratio of output to input heat, due to its low thermal resistance. This is in accordance with Figure 6.3a. This heat extraction ability is not the selection criterion because it implies a low heat storage capability, a disadvantage for medium and long pulse applications. This Bode plot could, mostly, be of interest for short pulses. The final choice would be the aluminum 3cm cooling plate.

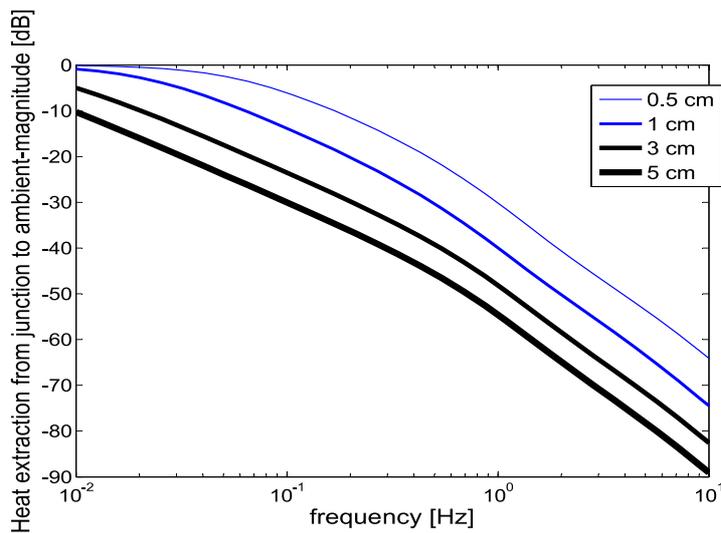


Figure 6.4: Magnitude bode diagram for the heat extracted to the ambient with respect to the heat dissipated by the chip.

The next step is to test the aluminum cooling plate with a highly effective water-cooling system, in order to identify a possible gain. Figure 6.5 shows the junction temperature response for the aluminum cooling plate, if the convection coefficient increases to  $10kW/(\text{°Cm}^2)$ .

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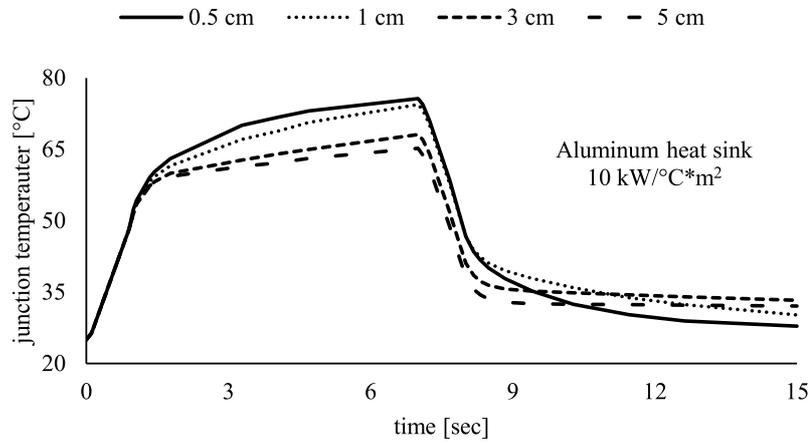


Figure 6.5: Junction temperature response for different thickness values of copper cooling plate with a convection coefficient of  $10kW/(\text{°C}m^2)$ .

For the  $0.5cm$  the temperature swing and the maximum temperature are remarkably limited compared to the  $5kW/(\text{°C}m^2)$  case. For both the  $3cm$  and the  $5cm$  case, the enhanced convection does not offer a considerable advantage for the thermal stressing at chip level. However, for the two cases with the smallest thickness values, the impact of the increased convection coefficient is important due to the reduced thermal capacitance of the cooling plate. The selected cooling system would be the one with a convection coefficient of  $5kW/(\text{°C}m^2)$ , because it could, potentially, reduce the energy consumption and the cost for the increased water flow in the cooling system.

Table 6.3 summarizes the temperature swing levels for the three cases; aluminum- $5kW/(\text{°C}m^2)$ , copper- $5kW/(\text{°C}m^2)$  and aluminum- $10kW/(\text{°C}m^2)$ . According to Chapter 2, the junction temperature variation is considered as the main thermal stressing parameter compared to maximum junction temperature, since the heating time is the same for all cases.

## 6.2. Cooling system investigation for thermal stressing mitigation

TABLE 6.3: Junction temperature swing for different materials, cooling plate thickness and convection coefficient

cooling plate thickness [cm]	aluminum for $5kW/({}^{\circ}Cm^2)$ [ ${}^{\circ}C$ ]	copper for $5kW/({}^{\circ}Cm^2)$ [ ${}^{\circ}C$ ]	aluminum for $10kW/({}^{\circ}Cm^2)$ [ ${}^{\circ}C$ ]
0.5	59.4	55.8	50.6
1	53.5	49.5	49.4
3	43.5	41.1	43.1
5	40.1	38.7	40.1

### 6.2.2 Possible failures and lifetime of the IGBT module

The aim of the design is to reduce the thermal stressing of the power module and to provide an increased lifetime according to possible future requirements. A lifetime estimation is attempted based on the thermal stressing data that were obtained from the simulations. The application note on lifetime of the IGBT modules of interest, [13], provides an estimated number of cycles to failure for the first 10% of the number of samples. The critical parameters are the junction temperature swing, the junction maximum temperature and the heating time. An alternative lifetime estimation in this application note uses the case maximum temperature and the temperature swing as critical parameters. Although the conducted lifetime tests do not have exactly the same profile as for this application, a rough conclusion can be reached for the modules lifetime and most probable aging mechanisms. Based on the simulation results, a comparison is needed between the two estimations, in order to find the worst-case scenario that is the most pessimistic approach for the expected lifetime.

If the junction-based estimation is used, two different estimations are presented for bond-wire lift off and for chip solder delamination. The long pulse application could make the chip solder the dominant failure source. Therefore, from [42], the cycle that is closer to this application has a duration of 10s, temperature swing of  $40^{\circ}C$  and maximum temperature of  $100^{\circ}C$ . The module is expected to have a lifetime of at least 328 millions cycles or 15 years, in the case that solder fatigue is used. On the other hand, if the bond-wire lift-off is used as a cause of failure, the expected lifetime is decreased to 100 million cycles with the new generation of epoxy-less modules. A suitable accelerated test of the modules with the specific load would be more accurate than these estimations.

According to the estimation based on the case temperature measurements for solder joints failures of the conductor leads or of the substrate, the simulation results of  $13^{\circ}C$  tempe-

perature swing and  $38^{\circ}\text{C}$  maximum temperature show that no failure is expected from these parts.

### **6.3 Conclusions on cooling system investigations**

From the comparison of aluminum and copper as cooling plate materials, it is observed that aluminum would be more suitable for the specialized application if the problem of corrosion did not exist for the specialized application. In spite of the fact that copper exhibits a better thermal performance than aluminum, the decrease of the maximum junction temperature and temperature swing, if a copper cooling plate is used, is minor. The high specific thermal capacity of the aluminum compensates for the rest of its thermal properties for this application. The results are improved, if the cooling plate thickness is increased, but the increase from  $3\text{cm}$  to  $5\text{cm}$  does not result in a significant advantage. The linear relation between the thermal resistance and the thickness limits the thermal performance as the thickness level increases. A Bode plot at the frequency levels of the current pulse is demonstrated as a technique for the evaluation of the heat extraction capability of the cooling system. It is considered as more useful for short pulses.

Furthermore, for mixed pulse applications, a thick cooling plate may result in a slow cooling time, due to the high thermal resistance of the cooling plate, enhancing significantly the average and maximum junction temperature. On the other hand, if the aim is the temperature swing reduction, a compromise is needed in the design for the absolute temperatures. A highly effective water cooling system would almost not change the thermal stressing at all for any of the  $3\text{cm}$  and  $5\text{cm}$  cooling plates for the tested cycle. The cooling plate thickness compensates for the convection coefficient. The convection coefficient influences essentially the system with the smallest cooling plate of  $0.5\text{cm}$ . The findings or the methodology could be extended to a module with an increased baseplate thickness cooled directly at this layer and even for customized solutions. The comparison in terms of material could be between copper and AlSiC, due to their lower thermal expansion coefficient comparing to aluminum for an improved lifetime.

### **6.4 Parameters modification for power losses regulation during operation**

This part investigates the possibility to reduce the thermal stressing of high power IGBT modules by taking the targeted magnet power supply as reference. The thermal stressing

#### 6.4. Parameters modification for power losses regulation during operation

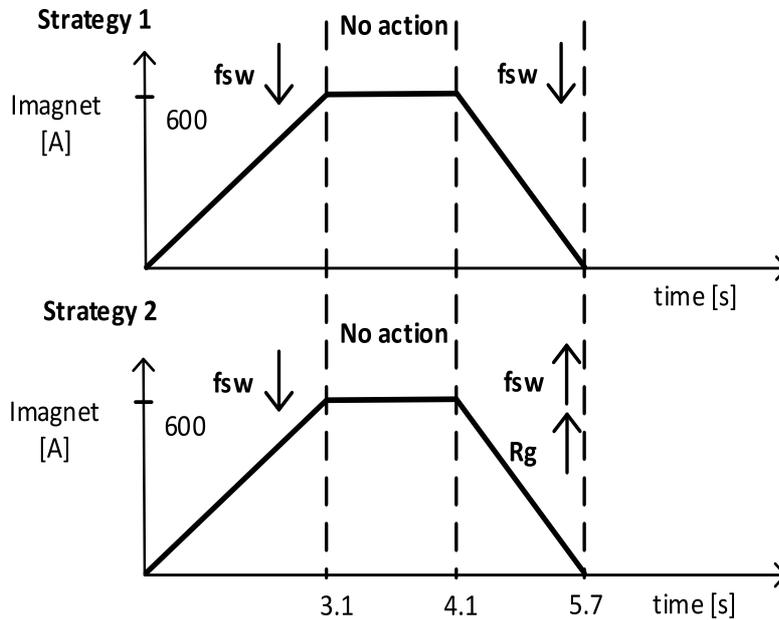


Figure 6.6: Mitigation strategies demonstrated for current cycle No. 3.

mitigation is achieved by adjusting the switching frequency and the on and off gate resistance values online. Using the pre-defined load profile of the application combined with the existing hardware capabilities of the power converter, two approaches are described. One approach is based on the reduction of the switching frequency in the part of the cycle where the output current precision is not a priority. The second approach combines the possibility to reduce the switching frequency in a part of the cycle while increasing the losses by increasing the gate resistance and the switching frequency in another part of the cycle. Figure 6.6 provides an overview of the two approaches.

Using four typical load current profiles as examples, two mitigation strategies are presented and their benefits to the power stack in terms of lifetime prolongation is evaluated. Finally, the investigation focuses on the relation between the shape of the load current and the potential for thermal stressing limitation that the proposed mitigation strategies can provide.

The motivation for this investigation can be summarized in three major reasons. The first reason is, clearly, to prolong the lifetime that is of utmost importance for this application. The second reason is to decrease the thermal stressing, in case of aging detection, by applying a mitigation strategy to decrease the temperature swing. The output power level must remain the same and the derating, meaning the reduction of the converter output

power, must be avoided. The third reason is that a mitigation strategy could be applied to achieve an increased usage flexibility of a power stack. In this case, the same power stack would have to supply a wide range of loads that were not specified from the beginning.

### Previous work

Various online methods are available in the literature to achieve a prolongation of the power modules lifetime [92], [93]. The focus has been on the reduction of junction temperature swing  $\Delta T_j$  and, secondly, of maximum junction temperature  $T_{j,max}$ . Both of them are crucial factors of thermal fatigue, as presented in Chapter 2. On the other hand, the swing reduction could lead to an increase in the mean temperature. Another possibility is the frequency reduction but with the consequence of the load current ripple increase [94]. For this work, the online parameters configuration is of interest for the lifetime prolongation and, at the same time, respecting the output requirements in terms of current precision. The temperature swing limitation is achieved by producing extra power losses, usually, with the increase of the switching frequency at the part of the load profile where the load current is reduced [95]. The power losses increase, the junction temperature remains at high level and the temperature swing is reduced. The proposed DC-link voltage increase in [96] for diode stress reduction in an inverter at rectifying mode implies an increase in the ratings of active and passive devices leading to size and cost rise. Finally, the gate voltage increase as a method to reduce the thermal stressing may lead to potential gate oxide degradation and higher dissipation at driver level [90].

#### 6.4.1 Load profile and thermal modeling of power stack

The DC-link voltage for this investigation is the nominal  $700V$  and it is assumed that the maximum current output for all the load profiles is  $600A$ . The increased current output is used, in order to make the effect of the mitigation strategies more evident. The nominal switching frequency is  $6.5kHz$ . The current profiles in Table 6.4 represent current cycles at CERN and are used for demonstration.

It is important to mention that the time interval, where there is a high precision requirement, is the flat-top. This is the case for the accelerator transfer line TT2, whereas high precision is required along the whole current cycle for the accelerators Proton Synchrotron (PS) and Super Proton Synchrotron (SPS). The requirements for PS and SPS prohibit the implementation of the proposed thermal stressing mitigation strategies. The example of TT2 is used as a reference for the analysis.

#### 6.4. Parameters modification for power losses regulation during operation

TABLE 6.4: Magnet current profiles

	Time duration [s]			
	Cycle No. 1	Cycle No. 2	Cycle No. 3	Cycle No. 4
Ramp-up	2.82	0.15	3.1	3.9
Ramp-down	1.23	0.15	1.6	1.4
Flat-top	0.16	0.17	1	0.6
Zero-current interval	1.79	0.83	1.8	1.3

The LPN that is presented in Figure 3.18 and in Table 3.4 is used for the thermal modeling.

#### 6.4.2 Proposed mitigation strategies overview

The mitigation strategies aim to reduce the junction temperature swing and, secondly, the maximum junction temperature. The dependence of the switching losses on the switching frequency  $f_{sw}$  can be considered linear, according to (2.19). The impact of the change of switching frequency in the output filter is not a part of this investigation. The gate resistor value  $R_g$  influences directly the turn-on and turn-off time of the semiconductor device. As mentioned in Chapter 2, an increase of gate resistance values increases the switching losses. The IGBT datasheet provides information for the relation of  $R_g$  values and switching power losses for a gate resistance range from  $0.5\Omega$  to  $12\Omega$ . The actual values that are used in the system are approximately  $2\Omega$  for the on-gate resistance  $R_{g,on}$  and  $7\Omega$  for the off-gate resistance  $R_{g,off}$ . These values are used as starting points for this investigation. Therefore,  $R_g$  values greater than the actual ones are needed for extra losses production. Again, the IGBT datasheet provides information for the relation between the switching energy losses at  $1600A$  and the different  $R_g$  values. Based on the IGBT datasheet, a linear approximation is used to estimate the switching losses for the new gate resistance values and for the voltage and current levels of the application. Finally, a linear approximation is used to calculate the losses for a DC-link voltage of  $700V$  that is close to the reference datasheet value of  $900V$ . With  $R_g$  equal to  $12\Omega$  for both  $R_{g,on}$  and  $R_{g,off}$ , the turn-on losses can be increased by a factor of more than 4 and the turn-off losses by a factor of 1.5. The increase of  $R_g$  comes with the cost of an increased dead time. Due to the existing output filter no output voltage loss is caused. The purpose of these calculations is to estimate the maximum switching losses that would be available with a significant increase of the gate resistance.

**Mitigation Strategy 1: Variable  $f_{sw}$  - Mitigation with reduced switching frequency**

As mentioned before, the part of the cycle with the high precision requirement for the output current is the flat-top. The first proposed mitigation strategy reduces the switching frequency by four times from the nominal value of  $6.5kHz$  to  $1625Hz$  during the ramp-up and ramp-down phases. This reduction is based on the fact that in this interval a fast controllability and a high current precision are not needed.

**Mitigation Strategy 2: Variable  $R_g$  - Mitigation with variable switching frequency and increased gate resistance**

For this strategy the power losses must be reduced during the ramp-up of the current using again a switching frequency of  $1625Hz$ . During the ramp-down, the power losses must be increased, in order to prevent the reduction of the junction temperature due to the power losses reduction. Cycle No. 3 is used again for demonstration.

Apparently, the gate resistance and switching frequency benefit can be exploited only while there is current supplied to the load. Figure 6.7 focuses on the ramp down phase of the load profile. It demonstrates the different power losses levels for a power module achieved in three different cases, namely the initial case that is by only switching the power module at  $6.5kHz$  or by increasing  $R_g$  without an  $f_{sw}$  increase or, finally, by increasing  $R_g$  to  $12\Omega$  and  $f_{sw}$  to  $15kHz$ . The purpose is to show what the maximum available power losses are that can be produced for the mitigation strategy. It is observed that the potential in the production of power losses is significant.

#### 6.4. Parameters modification for power losses regulation during operation

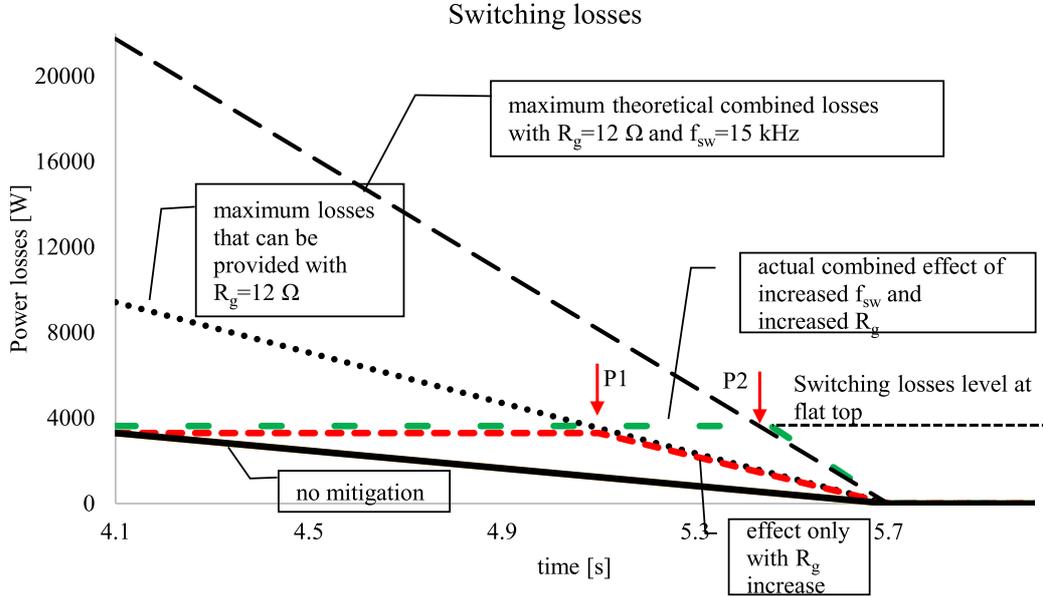


Figure 6.7: Power losses for the IGBT with focus on the ramp-down phase of the load current: From top curve to bottom: Switching losses combining maximum  $f_{sw}$  and maximum  $R_g$ , switching losses only with increased  $R_g$ , switching losses in the initial case and, finally, the mitigation with both increased  $f_{sw}$  and increased  $R_g$  or only with increased  $R_g$ .

The mitigation process for cycle No. 3 at the ramp-down begins when the current starts to decrease at the time instant equal to 4.1 s. The aim is to produce an amount of extra losses that could maintain the temperature at the level reached in the end of the flat top. In other words, the target is to be able to produce the same losses during the ramp-down as during the flat-top. With reference to Figure 6.7, the additional losses can, even, be produced with only an increase of  $R_g$  until the crossing point P1. The amount of power losses produced by the maximum  $R_g$  alone is greater than the effect of the maximum  $f_{sw}$ . In practice, a variable gate resistance must be used and, at point P1, it should reach the maximum value that is defined at the level of  $12\Omega$ . From point P1 until point P2, the maximum gate resistance with contribution by an increased switching frequency (even below  $15kHz$ ) must be used. From point P2 until the end of the ramp-down, the extra losses must be provided by both the maximum  $R_g$  as well as the maximum  $f_{sw}$  of  $15kHz$ . The green and the red dashed lines are at the same level, but there is placed below the green for illustration purposes. For the time interval when the current starts to reduce, up to P1, no difference is expected if just  $R_g$  is utilized. The difference in the extra power losses production, if both mitigation parameters are utilized, is that the flat top losses can be kept for extra time

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between P1 and P2 and that after P2 the device losses follow the line of the combined  $R_g$  and increased  $f_{sw}$  effect. The conduction losses at flat-top are significantly lower, almost 6 times lower at the level of 600W. It is considered that they have a negligible impact in the presented analysis. It is concluded that, depending on the instant of the ramp-down, the extra power losses can be provided either by increasing  $R_g$  or by increasing  $f_{sw}$  or even by the combination of the two parameters.

### Simulation model logic

In the simulation model in PSIM, the difference between the flat-top losses and the losses without mitigation strategy is calculated during the ramp-down. The calculated power losses are injected to the IGBT thermal model until point P2. From point P2 until the end of the current pulse, the extra power losses that are injected are the difference between the power losses with the combined effect of maximum  $R_g$  and maximum  $f_{sw}$  and the power losses that are produced without any mitigation strategy. The model is an average model to increase the simulation speed. A hysteresis controller is used to provide the calculated power losses, in order to keep the temperature close to the value at the beginning of the ramp-down. In this way, the temperature neither increases nor decreases further than a specified band below  $1^\circ C$ . The presented temperature control logic is applicable for pre-defined load profiles. Figure 6.8 illustrates the logic followed in the simulation model to implement mitigation strategy 2.

## 6.4. Parameters modification for power losses regulation during operation

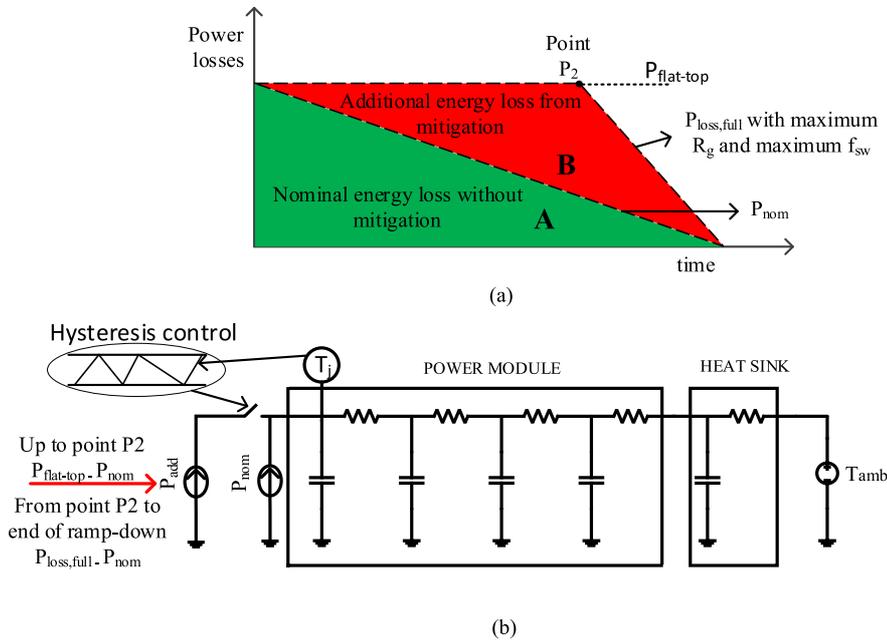


Figure 6.8: Power losses injection logic (a) Power losses partitioning during ramp down (b) Temperature regulation logic.

### 6.4.3 Mitigation strategies results - comparison and evaluation

For demonstration, Figure 6.9 illustrates the LPN simulation results for the initial temperature evolution along cycle No. 3 and with Strategy 1 and 2. During the ramp-up phase, it is observed that the rate of temperature change is smaller compared to the initial case for both strategies. During the ramp-down phase, Strategy 1 forces the temperature to be reduced abruptly, in contrast to Strategy 2 that keeps the temperature constant for a time period longer than the current flat-top.

Based on the same simulation results, Figure 6.10 provides the change in maximum junction temperature and temperature swing for the two strategies and for the four different cycles. Table 6.5 presents the thermal stress benefit for each of the strategies. For the cycles No. 1 and No. 2 the first strategy clearly leads to a lower thermal stressing compared to the second one. For profiles No. 3 and No. 4, the maximum temperature reduction is significantly greater for Strategy 1, but the swing is reduced more with Strategy 2. In all cases, the benefit is clear. Especially, Strategy 1 could, potentially, lead to the power modules downsizing in terms of current ratings.

Chapter 6. Thermal stressing mitigation possibilities for a power stack

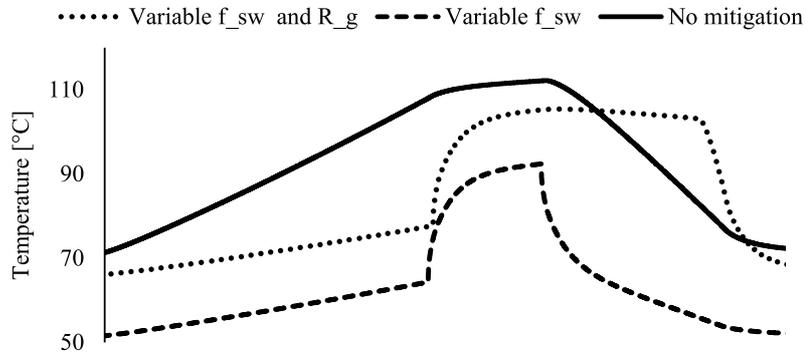


Figure 6.9: Simulation results for junction temperature in the three cases. From top to bottom: Initial case without mitigation, with variable  $f_{sw}$  and  $R_g$  and with only variable  $f_{sw}$ .

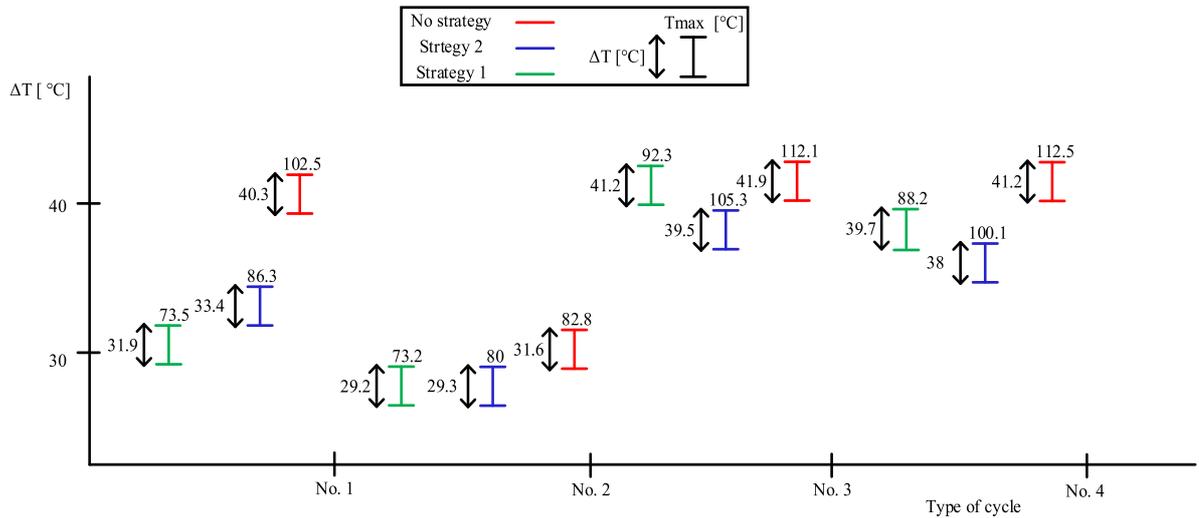


Figure 6.10: Junction temperature swing and maximum junction temperature for the four cycles before mitigation is applied and with each of the mitigation strategies.

#### 6.4. Parameters modification for power losses regulation during operation

TABLE 6.5: Thermal stressing reduction with mitigation strategies compared to initial cycle

Cycle	Strategy 1	Strategy 2
	Reduction in temp. swing/max temp. [°C]	Reduction in temp. swing/max temp. [°C]
No. 1	8.4/29	6.9/16.2
No. 2	2.4/9.6	2.3/2.8
No. 3	0.7/19.8	2.4/6.8
No. 4	1.5/24.3	3.2/12.4

Another observation from the results in Table 6.5 is that the overall impact of the mitigation strategies in terms of temperature swing is greater for cycles No. 1, No. 2 and No. 4. Especially the first two profiles have short flat-tops compared to the time constant of the IGBT thermal impedance that is  $0.3s$  (from 10% to 90% of the final value) [36]. The impact of the mitigation strategies at the temperature swing depends on the flat-top.

The application note for the life cycling capability of the used IGBT modules, [42], shows the relation between the number of cycles and temperature swing levels for different maximum temperature levels. Due to the duration of the cycles, the most probable cause of aging is considered to be the bond-wire lift-off. Lifetime curves, which are provided, reach a maximum of 100 million cycles for IGBT modules with and without epoxy filling. Figure 6.11, as, already shown in Figure 2.10, illustrates the linear extrapolation that is implemented to estimate the lifetime of the IGBT modules for more than  $10^8$  cycles and for  $T_{j,max}$  between  $75^{\circ}C$  and  $100^{\circ}C$ . The lifetime curves for IGBT modules with epoxy filling in [42] are used for the extrapolation, as they provide shorter estimated lifetime than the IGBT modules without epoxy. Table 6.6 summarizes the lifetime estimations in cycles for the three cases. The increase in lifetime for the two strategies is significant. The main disadvantages of Strategy 2 are the production of extra losses that are compensated by the losses reduction in the ramp-up phase compared to the initial case, and, secondly, the increased complexity because of the two parameters used. For a number of cycles over  $10^6$  millions, the lifetime estimation are done for the epoxy filling case.

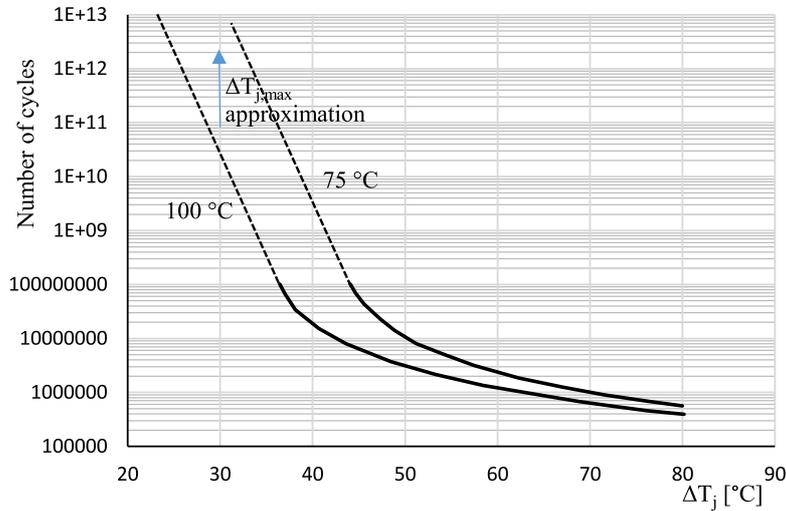


Figure 6.11: Extrapolation of lifetime curves for IGBT modules with epoxy filling [42].

TABLE 6.6: Lifetime estimation approximations in million cycles for the four cycles for the initial case and after each of the two strategies

Cycle	Epoxy filling Yes (Y)/No (N)	Initial lifetime estimation	Str. 1 lifetime estimation	Str. 2 lifetime estimation
No. 1	Y	18		
	N	109	$10^7$	$10^6$
No. 2	Y	$10^6$	$10^7$	$10^6$
	N			
No. 3	Y	8	62	9
	N	45	557	45
No. 4	Y	8	62	18
	N	45	557	109

#### 6.4.4 Impact of the mitigation based on current pulse shape

Figure 6.12a illustrates the change in temperature swing and the change in percent of the maximum temperature, if Strategy 1 is used, with the increase of flat-top length for cycle No. 1. The ramp-up, ramp-down and zero time remain the same, which implies an

#### 6.4. Parameters modification for power losses regulation during operation

increase in the RMS current for one cycle period. This cycle, already, has a long ramp-up and ramp-down time limiting the impact of the increased flat-top at the total RMS current of the cycle. There is an increase of 20% in the RMS current in the longest flat-top case. The benefit due to the  $\Delta T_j$  reduction decreases between the 0.1 s flat-top and the 0.3 s one by a factor of 2.5, whereas  $T_{j,max}$  decreases by a factor of 1.3. During the flat-top phase, the benefit in terms of  $\Delta T_j$  is almost zero, if the thermal impedance of the power module is close to its steady state value or more. The thermal impedance approaches its steady state for a flat-top length of 0.7 s. It can be concluded that the effect of the mitigation strategies at the temperature swing is greater for profiles with short flat-top. The flat-top duration is crucial for  $\Delta T_j$ , because the maximum current is continuously applied to the semiconductor device increasing the switching losses. The  $\Delta T_j$  reduction with the increase of flat-top duration is kept to higher values in the case of Strategy 2, as observed from Table 2, but with the cost of much higher maximum temperature compared to Strategy 1.

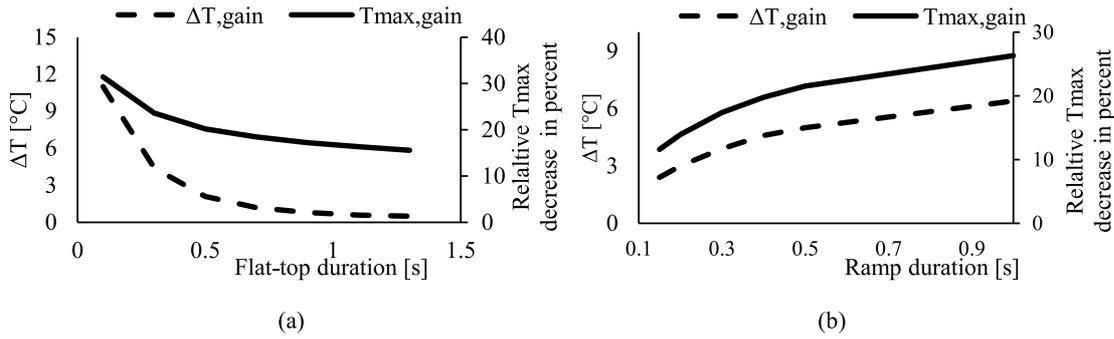


Figure 6.12: (a) Change of temperature swing and of maximum temperature in percent with flat-top increase, (b) Change of temperature swing and of maximum temperature in percent with ramp-up and ramp-down increase.

Respectively, profile No. 2 is used to investigate the impact of the mitigation for different ramp times. The ramp-up and ramp-down durations vary and the flat-top and zero-current time intervals are kept constant. The influence of the ramp durations increase in the RMS current is limited due to the relatively long zero time. The RMS current increase in the No. 2 cycle with the longest ramps is 15% compared to the initial cycle. In this profile, the ramp-up and ramp-down durations are equal. In Figure 6.12b, the relation of the ramp duration (either ramp-up or ramp-down) with  $T_{j,max}$  and  $\Delta T_j$  is illustrated by using Strategy 1 again. The mitigation leads to a more significant  $T_{j,max}$  reduction, if the profile has long ramps. There is, also, a benefit for  $\Delta T_j$ . Regarding  $\Delta T_j$ , the influence of a flat-top shorter than the thermal impedance time constant of the module seems to be greater than the ramp

duration. This is valid for the preferred mitigation Strategy 1.

## 6.5 Conclusions on online thermal stressing mitigation

This part has focused on the investigation and evaluation of two mitigation strategies that can potentially prolong the lifetime of the semiconductors in a power converter used as a magnet power supply. The mitigation strategy is based on the pre-defined nature of the load profiles in this application. Therefore, it can be adapted to various load profiles for this type of application using the same general concept. The experimental validation phase for the thermal performance of the power stack has to come first, in order to allow such a strategy. Moreover, these strategies could, also, be applied when aging is detected and there is no scheduled service stop soon enough. Between the two mitigation strategies, the reduction of the switching frequency during the ramps is found to be more effective in terms of thermal stressing limitation and more efficient thanks to the reduction of the switching losses in the converter. The second strategy leads to satisfactory results but there is a trade-off between the lifetime increase and the decrease in efficiency due to the power losses increase during the ramp-down. Both strategies result in significant lifetime increase. The flat-top of the pulse is crucial for the temperature swing and the effect of the first mitigation strategy at the temperature swing is greater for profiles with short flat-top compared to the power module time constant. The mitigation leads to a more significant  $T_{j,max}$  reduction, if the profile has long ramps, compared to the case of cycles with short ramps. An interesting observation is that by considering the mitigation strategies even from the power electronic converter development phase, the calculated ratings of the IGBTs can be reduced, potentially, leading to reduced cost and size of the power stack.

# Chapter 7

## Conclusions and future work

### 7.1 Conclusions

#### Method for integrity assessment of power stack

This thesis contributes with a method for the integrity assessment of a semiconductor power stack from the factory acceptance tests stage to the end of its lifetime using planned service stops. The presented method exhibits advantages that are essential for the integrity assessment of a series of IGBT power stacks in industrial scale. It is performed with a fixed switching pattern without the need for current control. For the temperature estimation with the  $v_{ce}$  method with sensing current previous methods used additional circuitry for the DUT isolation. This method does not need power stack modifications for the  $v_{ce}$  measurement with sensing and high current. For the  $v_{ce}$  measurement with high current it is enough to connect a shorting wire in the power electronic converter output terminals, in order to bypass the load. The measurement with high current can be obtained in the extended ZTC operating region and not necessarily exactly at the inflection point. Moreover, the method provides on-the-stack thermal calibration for the  $v_{ce}$  method with sensing current and for the  $v_{ce}$  measurement in the ZTC operating region. For the  $v_{ce}$  thermal calibration with sensing current the temperature difference between cooling water and ambience was proposed offering fast thermal characterization of the IGBT module. However, this method is proposed to be applied during stops of operation. Therefore, the types of operation that benefit the most from the developed method are the ones that include scheduled service stops.

### **Circuitry for $v_{ce}$ measurement**

Particularly, for the implementation of the proposed method, two  $v_{ce}$  measuring circuits were proposed and analyzed. During their testing, they proved a measurement precision at the level of maximum  $1.5^{\circ}C$  using the  $v_{ce}$  method with sensing current for measurements at a switching frequency of up to  $6.5kHz$ . One circuit was based on a Zener diode, whereas the other used a pin-diode for the high-voltage clamping. Both exhibited ease of implementation and calibration.

### **Specific findings for the application of the integrity assessment method to a magnet power supply**

It was demonstrated, based on datasheet values, that the  $v_{ce}$  measurement does not have to be carried out exactly at the inflection point, since the effect of junction and ambient temperature at  $v_{ce}$  was not significant in the extended ZTC operating region with a range of  $\pm 15A$ . It was shown, with the specialized application at CERN as an example, that the absence of the thermal paste layer can be detected during factory acceptance tests, because it causes twice the junction temperature rise compared to the case with the normal thermal paste thickness. Using the reference application as an example, a temperature change of more than  $20^{\circ}C$  in the cooling water temperature would have a considerable impact of 5% on the thermal resistance estimation and, as a result, on the solder delamination detection. However, the investigation for the first time of the  $v_{ce}$  measurement in the ZTC operating region as a method for bond-wire lift-offs detection for high-current modules showed that the detection of wire bond lift-off is only possible when more than half of a chip's bond-wires have failed. It was shown that the voltage drop of power leads may be important for the precision of such measurement for ambient temperature changes of over  $30^{\circ}C$ .

### **Investigation for current unbalance between substrates of the same IGBT module due to temperature difference**

The extended operation in the NTC operating region for the specialized application was a motivation for the experimental investigation of the current unbalance in a high-current IGBT module, if temperature difference occurs among the chips. The added value of the findings was that the current unbalance between two substrates operating in the NTC operating region, even with a temperature difference of  $15^{\circ}C$ , was not significant. The additional thermal stressing at the substrate that conducts the highest current was negligible. Therefore, it is not necessary to consider this unbalance in the thermal modeling of the

H-bridge operating in the NTC operating region. Moreover, it does not seem to influence the lifetime of the power modules.

### **Possibility for thermal stressing mitigation - design of cooling system**

In spite of the fact that copper as a cooling plate material exhibits a better thermal performance than aluminum, it was observed that aluminum exhibited almost the same performance as copper, in terms of maximum junction temperature and temperature swing cycle. The high specific thermal capacity of the aluminum compensated for the rest of its thermal properties for this application. The results were improved for an increased cooling plate thickness of  $3\text{cm}$  between the IGBT baseplate and water. A further thickness increase of the cooling plate to  $5\text{cm}$  does not result to a significant improvement. A highly effective water cooling system would almost cause no change to the thermal stressing for a thickness of  $3\text{cm}$  or above. A final observation is that the cooling plate thickness compensates for the convection coefficient increase from  $5\text{kW}/(^{\circ}\text{Cm}^2)$  to  $10\text{kW}/(^{\circ}\text{Cm}^2)$ , potentially, resulting in reduced energy consumption for the water circulation.

### **Possibility for thermal stressing mitigation - online strategies**

Between the two thermal stressing mitigation strategies, the reduction of the switching frequency during the ramps was found to be more effective in terms of thermal stressing limitation and more efficient thanks to the reduction of the switching losses in the converter. The second strategy investigated resulted in thermal stressing mitigation but it produces extra power losses during the ramp-down compared to the case without mitigation and to the case with the first strategy. The maximum reduction in  $T_{j,max}$  was  $29^{\circ}\text{C}$  and in  $\Delta T_j$  it was  $8.4^{\circ}\text{C}$  indicating that there is great potential for thermal stressing mitigation. The effect of the first mitigation strategy at the temperature swing is significant for profiles with short flat-top duration compared to the power module time constant. Moreover,  $T_{j,max}$  can be, substantially, reduced, if the profile has long ramps.

## **7.2 Future work**

The method for the assessment of the power stack integrity is proposed for industrial scale implementation. To this extent, two further investigations are suggested as future activity. The first is the accelerated lifetime testing of the high-current IGBT modules to study the impact of the two main failure modes on  $v_{ce}$ . Especially for the solder crack detection it is

## Chapter 7. Conclusions and future work

necessary to study the change of  $v_{ce}$  with aging in more depth, so as to be able to more precisely estimate the health status of the device and to distinguish this aging mechanism from possible thermal paste pump-out. Ideally, during service stops, the detection and separation of the thermal paste pump-out would be made within the same simple test as for the detection of the other aging mechanisms. The repeatability of the testing accuracy during service stops is critical for the aging detection. An extra investigation step would be to change the isolation stage with a digital isolator as an input to an ADC converter, in order to compare with the isolation amplifier in terms of level of noise. It was shown that the method is sensitive to the resistance of the power leads due to the ambient temperature variations. Although it was calculated that the precision would not be affected for ambient temperature variations of up to  $30^{\circ}C$ , the change of the power leads or the auxiliary leads resistance due to the skin effect in steep current ramps was not studied. The available information in the literature is limited and an analytical study would be of interest.

An optimized testing technique for a large number of power stacks that could, simultaneously, test multiple DUTs could be proposed, in order to save time during the application of this method. These proposed future steps are necessary for every new family of power stacks used. The aging criteria that are set for this work are based on previous works conducted on IGBT modules with lower power ratings. Overall, a statistical analysis with data collected during service stops for a series of power stacks could evaluate the applicability and precision of the method. Furthermore, the obtained data could provide useful information for the design trends that are more suitable for the specialized application, as well as for similar applications such as traction.

Regarding the investigation for thermal stressing mitigation, experimental verification would be of great value, especially for the online mitigation strategies. The effectiveness of the strategies for a combination of current cycles, as a normal profile for a magnet power supply, has to be proved. The actual impact of gate resistance on switching power losses has to be verified. To the author's knowledge, what does not exist in the current literature is the demonstration of the benefit in terms of lifetime, if an online mitigation strategy is used. This can be achieved with the comparison of the lifetime gain of IGBT modules with a mitigation strategy, as opposed to lifetime of IGBT modules with standard operation. It would be interesting to find suitable accelerated lifetime tests to represent the difference in thermal stressing between the mitigation cycle and the normal one. It is important to analyze if the calculated ratings of the power stack (cooling plate dimensions, water-flow rate, IGBT thermal performance) during the design phase could be reduced by considering the mitigation strategies. A design with thermal stressing mitigation could, potentially, lead to reduced cost and size of the power stack.

For the case of cooling system design, the presented findings could be extended to the

## *7.2. Future work*

modules with an increased baseplate thickness cooled directly at this layer and even for customized solutions for long pulse applications. The comparison in terms of material should be between copper and AlSiC or other materials, due to their good thermal performance and low thermal expansion coefficient for an improved lifetime. It would be interesting to estimate the energy and cost saving for a large number of power electronic converters with increased cooling plate or baseplate thickness as well as with reduced water flow rate.

## *Chapter 7. Conclusions and future work*

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## *References*

# Appendix A

TABLE A.1: Thermal characteristics for each layer of the module - FEM Comsol

Material	Thermal conductivity [ $W/(m * K)$ ]	Heat capacity [ $kJ/(KgK)$ ]
Silicon	130	700
Copper	394	385
96.5Sn/3.5Ag (chip solder)	33	220
92.5Pb/5Sn/2.5Ag (substrate solder)	70	1670
AlN DBC	170	745
AlSiC	170	800
Thermal paste	1	1200

Chapter A.

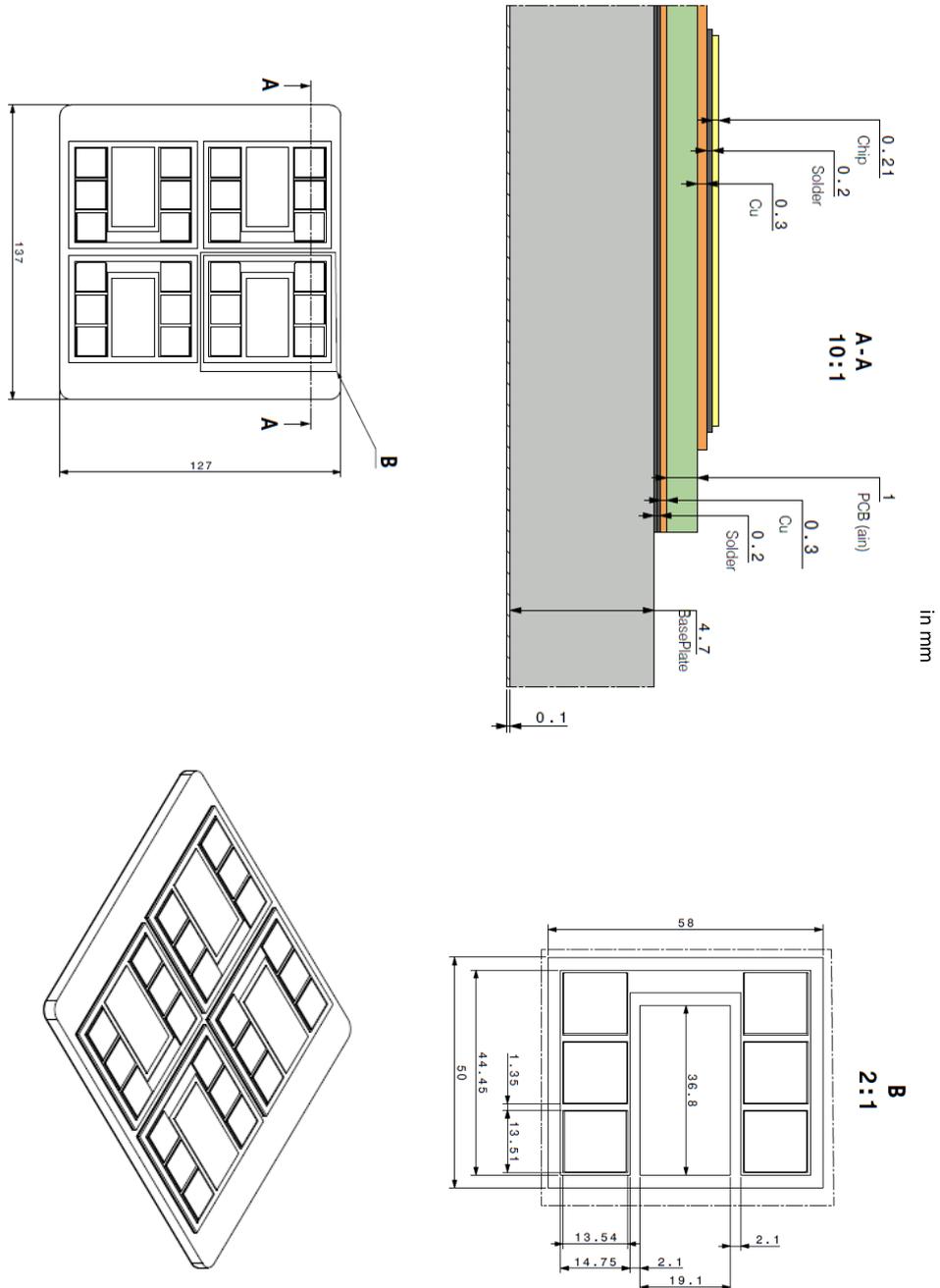


Figure A.1: IGBT module CAD drawing: The chip thickness correspond to the IGBT chip. The diode chip has a thickness of 0.385mm.

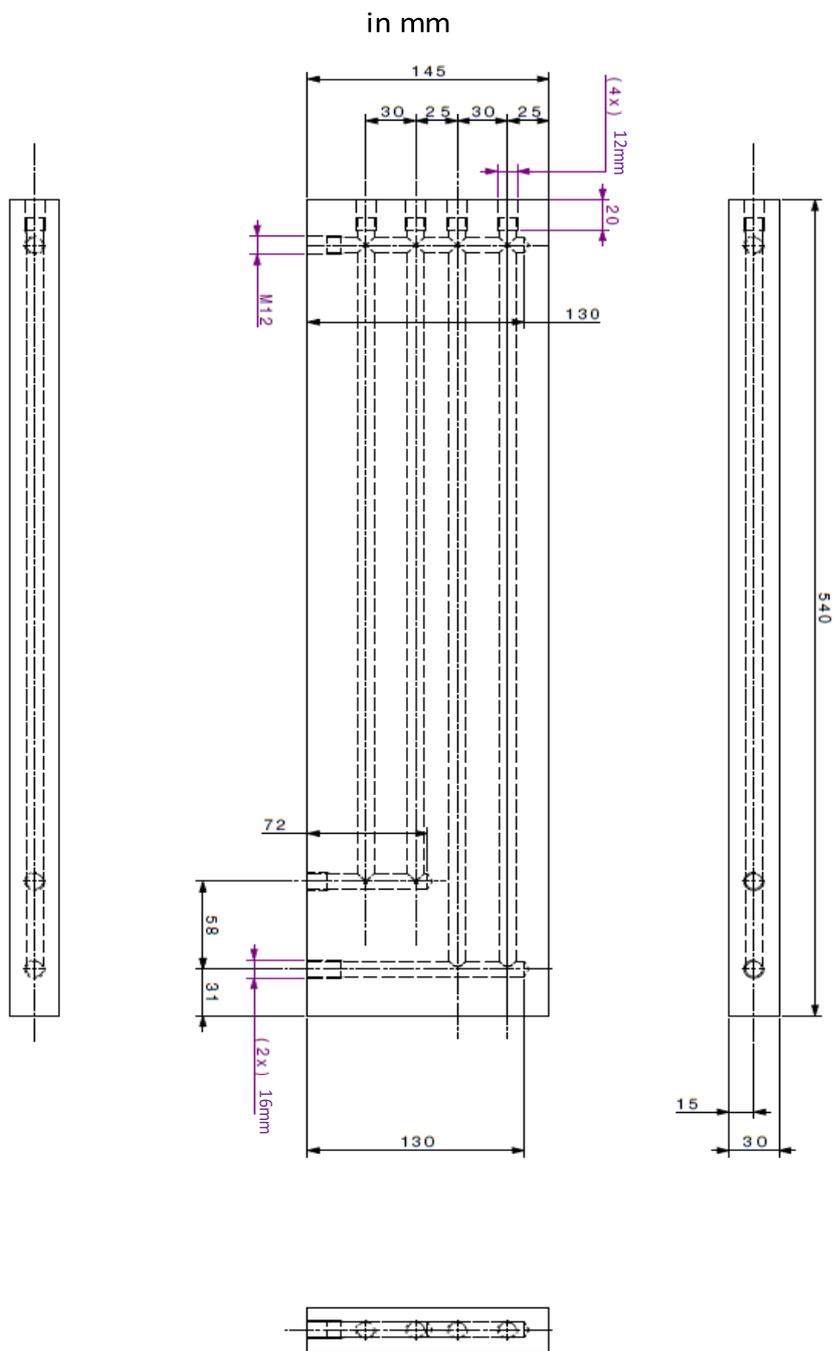


Figure A.2: Cooling plate CAD drawing.

*Chapter A.*

# Appendix B

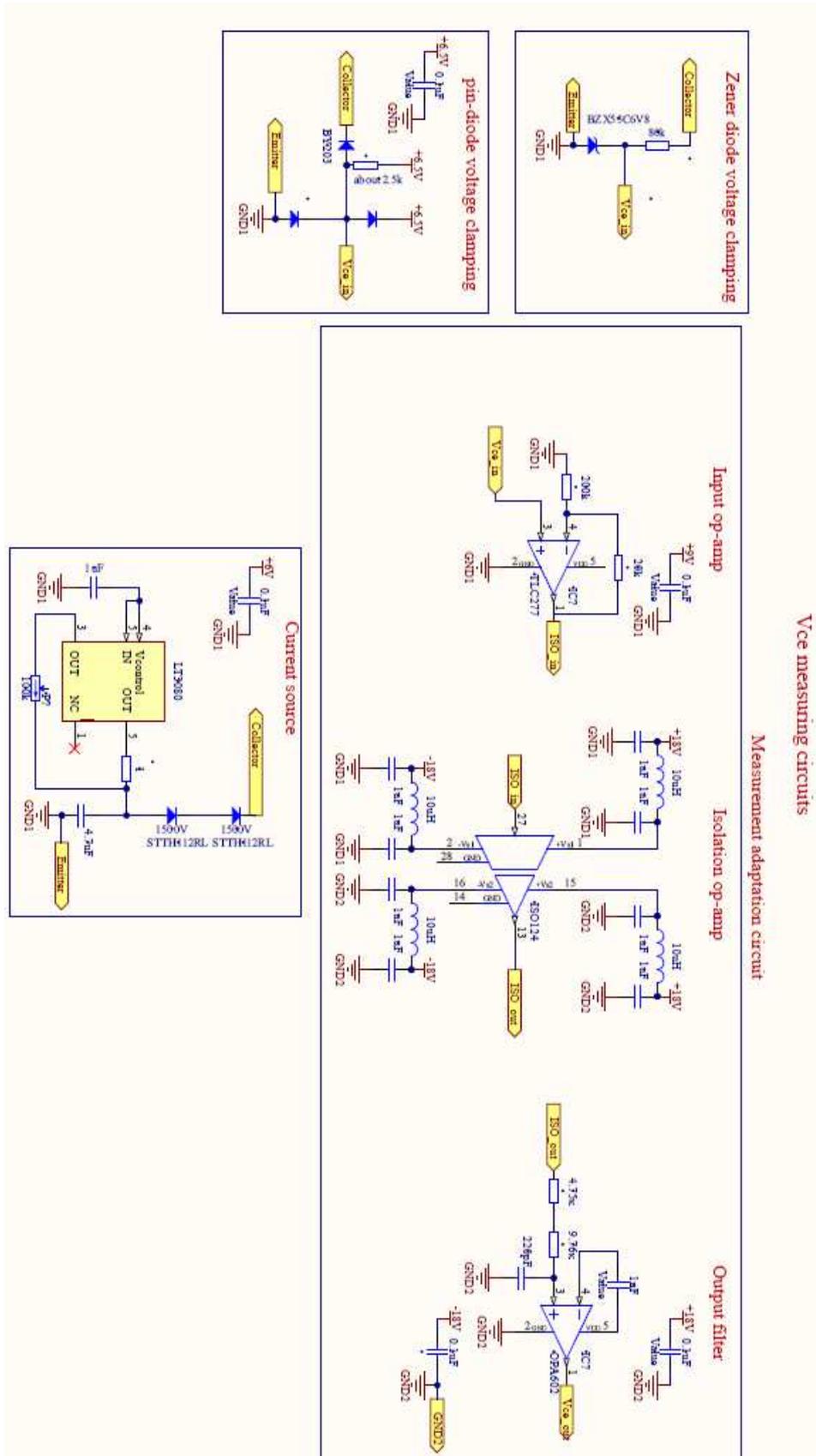


Figure B.1: Schematic of  $v_{ce}$  measuring circuits.