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# Electrical characterization of high k-dielectrics for 4H-SiC MIS devices

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ABSTRACT

We report promising results regarding the possible use of AlN or $Al_2O_3$ as a gate dielectric in 4H-SiC MISFETs. The crystalline AlN films are grown by hot wall metal organic chemical vapor deposition (MOCVD) at 1100 °C. The amorphous $Al_2O_3$ films are grown by repeated deposition and subsequent low temperature (200 °C) oxidation of thin Al layers using a hot plate. Our investigation shows a very low density of interface traps at the AlN/4H-SiC and the $Al_2O_3$/4H-SiC interface estimated from capacitance-voltage (CV) analysis of MIS capacitors. Current-voltage (IV) analysis shows that the breakdown electric field across the AlN or $Al_2O_3$ is ~ 3 MV/cm or ~ 5 MV/cm respectively. By depositing an additional $SiO_2$ layer by plasma enhanced chemical vapor deposition at 300 °C on top of the AlN or $Al_2O_3$ layers, it is possible to increase the breakdown voltage of the MIS capacitors significantly without having pronounced impact on the quality of the AlN/SiC or $Al_2O_3$/SiC interfaces.

## 1. Introduction

The great potential of 4H-SiC MISFETs for power electronics is hampered by low channel mobility mainly due to high density of interface states at the $SiO_2$/SiC interface. The quality of the $SiO_2$/SiC interface has been improved by various oxidation and nitridation methods but more reduction in interface traps is needed [1–3]. Beside $SiO_2$ as a gate dielectric, the use of high-k dielectrics on SiC has also been investigated. AlN and $Al_2O_3$ have reasonably large band gap (~ 6.2 eV and ~7 eV respectively) and high dielectric constant. The conduction band offset of AlN or $Al_2O_3$ to 4H-SiC of ~ 1.7 eV is expected to be sufficient for n-channel MISFET operation [4–9]. High quality single crystalline AlN can be grown on SiC because of only 1% lattice mismatch to SiC [10]. However, an amorphous $Al_2O_3$ is considered to be better than poly-crystalline α-$Al_2O_3$ as a gate dielectric on 4H-SiC because of leakage through grain boundaries [11].

A crystalline AlN grown by molecular beam epitaxy (MBE) has been reported as a gate dielectric for 4H-SiC MISFETs but very low channel mobility (< 1 $cm^2$/V) was obtained because of the leaky structure [12]. The irradiation of atomic nitrogen or HCl gas etching before the growth of AlN has been used to improve the quality of MBE grown AlN films [13,14]. The growth of AlN layers by MOCVD on 4H- and 6H-SiC has also been reported and a significant density of fixed charge and interface traps is observed in such AlN layers [15,16].

An amorphous $Al_2O_3$ grown by atomic layer deposition (ALD) or thermal oxidation of metallic Al has been used as a gate dielectric in graphene field effect transistors with some success [17,18]. The ALD as grown $Al_2O_3$ on 4H-SiC typically contains a large number density of negative charges which are reduced after annealing in Ar at 1000 °C but the $Al_2O_3$/SiC interface contains a high density of interface traps after such treatment due to growth of an interfacial $SiO_x$ ($0 < x < 2$) layer [19]. To improve the quality of ALD grown $Al_2O_3$, pre-deposition surface cleaning and post deposition annealing has been performed in $N_2O$ or $N_2$ ambient [20,21]. A MOSFET with ALD grown $Al_2O_3$, that was post-annealed in hydrogen at 400 °C, is reported with a field effect mobility of 57 $cm^2$/V. Even though these results are promising, large threshold voltage shifts are observed due to the sensitivity of the $Al_2O_3$ layers to electron injection [22]. There is another report on a very high peak field effect mobility of 300 $cm^2$/V in SiC MOSFETs using $Al_2O_3$ made by MOCVD with a thin $SiO_2$ interfacial layer to the SiC [23]. But, the mobility drops very rapidly with gate voltage and is less than 50 $cm^2$/V at moderate gate voltages.

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In this study, we grow crystalline AlN by hot wall MOCVD and amorphous $Al_2O_3$ by low temperature oxidation of Al on n-type 4H-SiC. On few selected samples, an additional layer of $SiO_2$ is deposited on top of the AlN or $Al_2O_3$ layer by plasma enhanced chemical vapor deposition (PECVD). The interface traps at the AlN/SiC and $Al_2O_3$/SiC interfaces are investigated by capacitance voltage (CV) measurements on MIS capacitors. The dielectric breakdown properties are extracted from current voltage (IV) measurements. We find that both the AlN/SiC and the $Al_2O_3$/SiC interface contain very low density of interface traps and the use of $SiO_2$/AlN or $SiO_2$/$Al_2O_3$ dielectric stack improves the breakdown voltage of the MIS devices.

## 2. Experimental methods

Two sets of n-type 4H-SiC MIS capacitors were made. One with single crystalline AlN and other with amorphous $Al_2O_3$ as a dielectric. The 4H-SiC used in this study have 10 μm thick n-type epitaxial layers with a net doping concentration of $\sim 1 \times 10^{16}$ cm$^{-3}$ grown on 4° off-axis (0001) highly doped $\sim 1 \times 10^{18}$ cm$^{-3}$ 4H-SiC substrates. A single crystalline 10 nm thick AlN layer was grown on 4H-SiC in a horizontal hot-wall MOCVD reactor at 1100 °C. Ammonia and $Al_2(CH_3)_6$ were used as a precursor for nitrogen and aluminum respectively. Prior to deposition of AlN, the SiC surface was exposed in $H_2$ ambient at 1320 °C, in order to obtain a native oxide-free surface. The details of the AlN growth process and structural characterization of the crystalline AlN layers are given in Ref. [24]. The amorphous $Al_2O_3$ is grown by depositing few monolayers of pure Al by electron beam evaporation at a rate of ~ 0.5 Å/s and then the sample is baked on a hot plate in room environment at a temperature of 200 °C for 5 min to form $Al_2O_3$ layer. This process of deposition and subsequent low temperature oxidation was repeated twelve times resulting in a film thickness of 15 nm as determined by X-ray reflectivity (XRR) and Atomic Force Microscopy. Prior to growth of $Al_2O_3$, the SiC was cleaned with HF in order to remove the native oxide. Further details of the $Al_2O_3$ growth process are given in Ref. [25]. An additional layer of $SiO_2$ with thickness of 40 nm was deposited on selected samples from both sets by PECVD at 300 °C using source gases of nitrous oxide and silane. Reference MIS capacitors with thermal $SiO_2$ grown in dry oxygen or in $N_2O$ ambient were also analyzed. Samples with identical reference oxides have previously been used in SiC MOSFETs [26]. The dielectric thickness of all samples was estimated using X-ray reflectivity (XRR) and the crystallinity was investigated with X-ray diffraction (XRD). Our $Al_2O_3$ and $SiO_2$ films are amorphous, no crystallization is observed by XRD apart from the AlN samples [24].

Circular MIS capacitors are made using Al as a gate metal and back contact as well. The interface quality is characterized by conventional CV analysis using Agilent E4980A LCR meter. The dielectric breakdown strength of the MIS samples is determined by IV measurements using a Keithley 617 electrometer. CV and IV measurements are performed in vacuum of $10^{-3}$ mbar in a cryostat.

## 3. Results and discussion

Fig. 1 shows CV spectra of MIS capacitors having AlN and $Al_2O_3$ dielectrics measured at room temperature and at frequencies of 1 kHz and 1 MHz. The gate bias is swept from depletion (negative bias) to accumulation (positive bias) and the capacitance signal for both frequencies is recorded simultaneously at each gate bias point. Fig. 1a shows the CV curves for AlN sample. The dielectric constant deduced from the accumulation capacitance is about 8.7. Fig. 1b shows the CV spectra of the $Al_2O_3$. The dielectric constant for $Al_2O_3$ is ~ 6.5. The flatband voltage in both AlN and $Al_2O_3$ is ~ 0.7 V which is close to the theoretical flatband voltage (i.e. ~ 0.4 V) which shows that initially the AlN and $Al_2O_3$ layers contain insignificant amount of fixed charge. A first estimate of the interface trap density is extracted from frequency dispersion of CV curves [27]. In the AlN and $Al_2O_3$ case, such dispersion is hardly visible indicating a low interface state density.

The interface quality of AlN or $Al_2O_3$ dielectric with 4H-SiC can be estimated by investigating the frequency dispersion of the CV spectra of an MIS capacitor. Electron capture into interface states is most often a fast process while electron emission from interface traps is normally much slower and is a thermal process which depends on the difference $E_c$-E (where E is the energy level of the interface trap and $E_c$ denotes the SiC conduction band edge). If an electron is captured and not emitted again, this is detected as a shift of the CV curve to higher gate voltages. If the test frequency is high (1 MHz) then more traps will not emit their electrons and the curve is shifted as compared to the low frequency (1 kHz) curve. The extraction of $D_{it}$ follows the method of Berglund [27]. The interface trap density ($D_{it}$) is determined by well-known High-Low-Capacitance method using an equation: $D_{it} = \frac{1}{q}\left(\frac{C_d C_{lf}}{C_d - C_{lf}} - \frac{C_d C_{hf}}{C_d - C_{hf}}\right)$. Where $C_d$ is dielectric capacitance, $C_{lf}$ and $C_{hf}$ are low and high frequency capacitance respectively.

Fig. 2 shows $D_{it}$ extracted from room temperature CV dispersion data for MIS samples with AlN or $Al_2O_3$ as a dielectric as well as reference $SiO_2$ samples. The single layer AlN and $Al_2O_3$ samples contain the lowest $D_{it}$. The detrimental interface states that exist within this energy range for thermally grown oxides are virtually absent at the AlN/SiC or the $Al_2O_3$/SiC interface. It is clear that the addition of a $SiO_2$ dielectric layer on the top of AlN or $Al_2O_3$ affects the AlN/SiC and $Al_2O_3$/SiC interfaces. However, the single AlN and the $SiO_2$/AlN stack both have lower $D_{it}$ than reference samples. The $D_{it}$ of the $SiO_2$/$Al_2O_3$ stack is comparable to the reference $N_2O$ grown $SiO_2$.

A sensitivity to electron injection is observed in both AlN and $Al_2O_3$ samples. This is detected as a flatband shift in subsequent 100 kHz CV curves when the samples are repeatedly biased into accumulation. The magnitude of the shift depends on the maximum applied accumulation voltage. An example of such behavior is shown in Fig. 3 for single layer AlN and $Al_2O_3$ MIS samples. Such behavior is also reported in literature for AlN and $Al_2O_3$ MIS samples [14,19]. This flatband shift can be a result of trapping of electrons in defects located within the dielectric. Similar electron injection is also observed in the dielectric stacks (not shown here).

However, in this work the process is reversible since the trapped electrons can be released back to the SiC at room temperature by applying depletion bias stress and UV illumination for a certain time to the MIS capacitors [28–30]. An example of such an experiment is shown in Fig. 4 for AlN/$SiO_2$ and $Al_2O_3$/$SiO_2$ stack samples. In the case of the AlN/$SiO_2$ sample (Fig. 4a), the MIS capacitor is initially kept in accumulation (+11 V) for 30 min at room temperature and then sequentially the bias with 100 kHz frequency is swept to depletion (−10 V) and the CV is recorded seen as the black solid curve. Electrons are intentionally injected into the AlN layer during the bias stress. Next, a UV light is shined on the sample under depletion bias of −10 V for 30 min to examine if electrons are released from AlN traps. A broken black 100 kHz CV curve is recorded directly thereafter. A stretch-out of the CV curve at gate voltage from -5 V to 7 V suggests that electrons are released from traps during UV exposure, but they are recaptured to traps as the gate voltage leads the device to accumulation. The same procedure is applied to the $Al_2O_3$/$SiO_2$ sample with accumulation and depletion bias of +5 V and -5 V respectively (shown in Fig. 4b) and the results are similar to the AlN/$SiO_2$ sample. This experiment shows that the AlN and $Al_2O_3$ layers have traps which capture free electrons during accumulation bias stress and re-emission of the captured electrons is made possible by UV illumination. Applying depletion bias in the same manner but without applying UV light results in a negligible shift of the CV curves (not shown).

IV measurements are used to estimate the critical breakdown field of the dielectrics. Fig. 5 compares the dielectric breakdown field of the AlN and $Al_2O_3$ samples as well as of reference dry $SiO_2$ sample based on current density measurement as a function of the effective electric field (J-E) across the gate dielectric. A breakdown field of ~ 3 MV/cm (solid

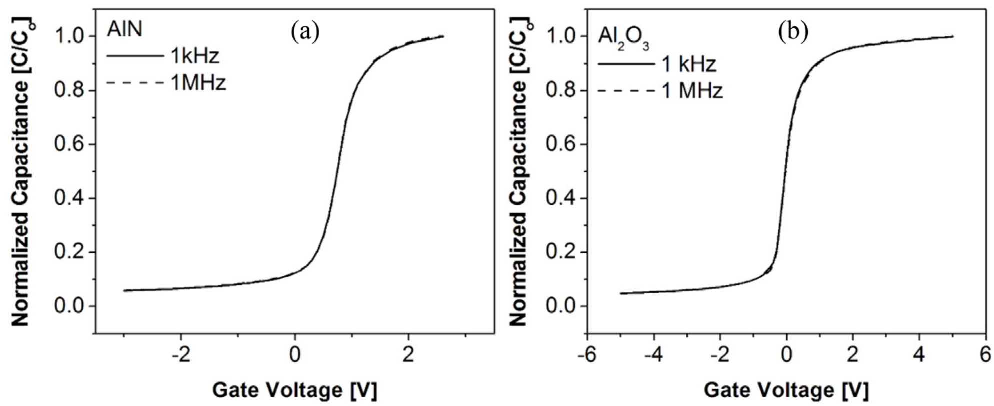


**Fig. 1.** Room temperature CV curves for (a) AlN and (b) $Al_2O_3$ samples at test signal frequencies of 1 kHz and 1 MHz.

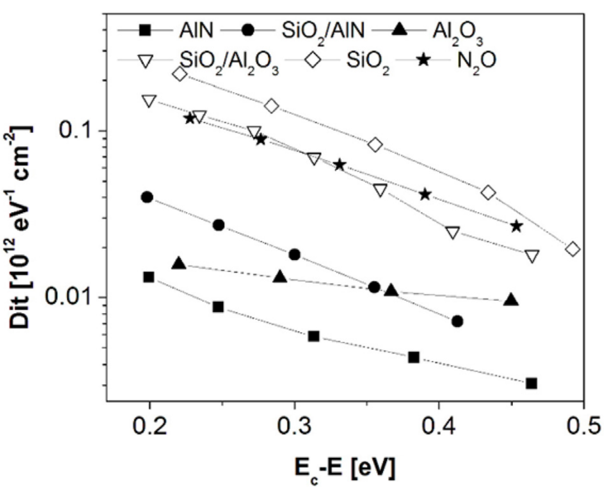


**Fig. 2.** Comparison of the density of interface states ($D_{it}$) estimated from CV (at 298 K) as a function of energy for AlN and $Al_2O_3$ based MIS capacitors along with reference $SiO_2$ MIS capacitors.

curve) or 5 MV/cm (dotted curve) is recorded for the single layer AlN or $Al_2O_3$ sample respectively. A sharp current leakage is observed for single layer AlN even at low dielectric electric fields. This suggests the AlN layers have higher density of bulk traps compared to $Al_2O_3$ that cause trap assisted leakage across dielectric. The breakdown field of the reference thermal $SiO_2$ sample is ∼ 9 MV/cm (dash double dotted curve). The physical origin of the electron traps within the AlN and $Al_2O_3$ layers is unknown. Our postulate is that the AlN layer has either very high density of intrinsic point defects (e.g silicon and oxygen point defects) or extended defects like dislocations [31]. The $Al_2O_3$ layer is expected to contain oxygen related intrinsic defects [32]. These defects are presumably the cause of the current leakage through the AlN and $Al_2O_3$ layers.

The $SiO_2$/AlN and $SiO_2/Al_2O_3$ stack samples have effective breakdown field, if we consider the dual dielectric as a single dielectric, of ∼ 8 MV/cm (dashed curve for $SiO_2$/AlN and dash dotted curve for the $SiO_2/Al_2O_3$ sample). However, the breakdown electric field across the AlN or $Al_2O_3$ layer in the stack is ∼ 4 MV/cm or ∼ 5.5 MV/cm. Addition of $SiO_2$ on the top of AlN layer does not significantly improve the breakdown properties of the AlN or $Al_2O_3$ but allows the use of higher gate voltages for device operation.

## 4. Conclusions

CV analysis at room temperature shows that single crystalline AlN and amorphous $Al_2O_3$ layer have good interface quality in terms of low density of interface states in n-type 4H-SiC MIS capacitors. A significant electron trapping is observed within the AlN or $Al_2O_3$ when the MIS capacitors are biased into accumulation resulting in a large flatband voltage shift towards higher gate voltages. This can be connected to the relatively low breakdown field (∼ 3 MV/cm or ∼ 5 MV/cm) of the AlN or $Al_2O_3$ layers. It is possible to slightly improve the breakdown field of the MIS devices by depositing a $SiO_2$ layer on top of the AlN or $Al_2O_3$. More work is needed in optimizing the growth conditions of the dielectrics and resolving the question of electron trapping within the AlN and $Al_2O_3$ layers. In summary, the AlN and $Al_2O_3$ MIS samples show very promising results in terms of interface state densities but electron injection into both layers is currently preventing their practical use.

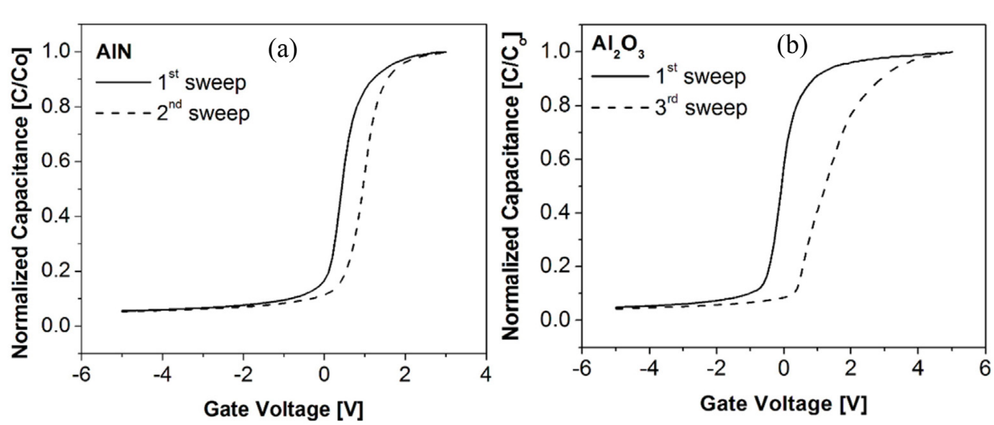


**Fig. 3.** Subsequent 100 kHz CV sweeps for single layer (a) AlN and (b) $Al_2O_3$ sample at room temperature.

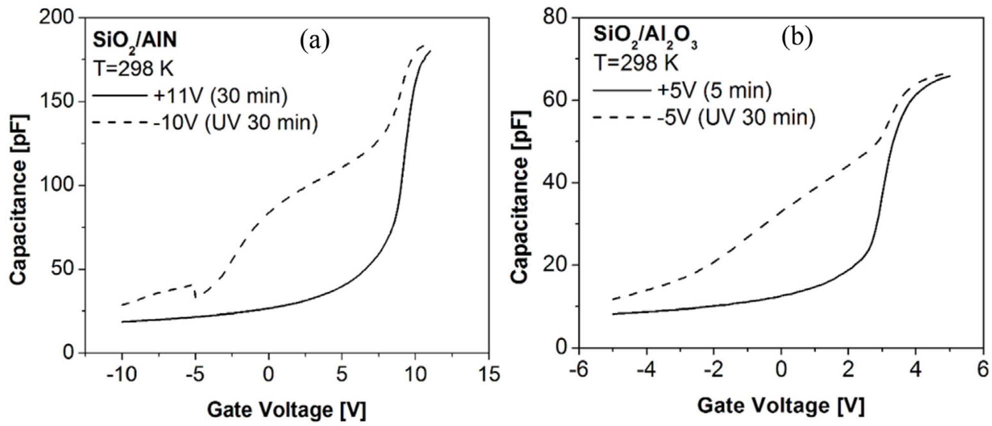


**Fig. 4.** Electron injection and emission in and out of traps located within (a) the AlN or (b) $Al_2O_3$ layer. The black solid 100 kHz CV curves are recorded after which electrons are intentionally injected into the AlN or $Al_2O_3$ by accumulation bias stress for certain period. The dotted 100 kHz CV curves are recorded after applying negative bias stress with UV illumination to the samples for 30 min.

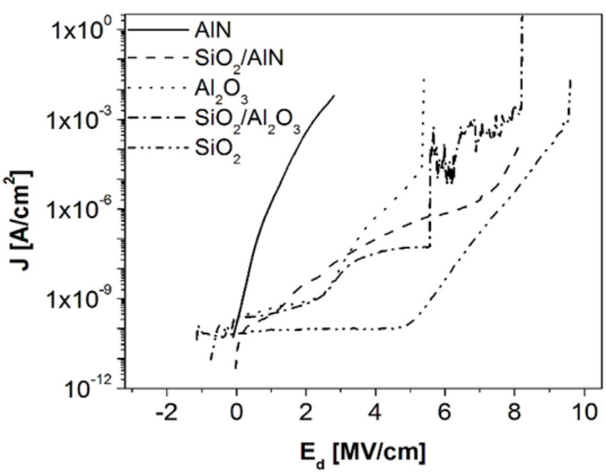


**Fig. 5.** Comparison of leakage current density versus effective electric field (J–E) for differently prepared MIS samples.


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