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Electrical characterization of high k-dielectrics for 4H-SiC MIS devices


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A B S T R A C T

We report promising results regarding the possible use of AlN or Al2O3 as a gate dielectric in 4H-SiC MISFETs. The crystalline AlN films are grown by hot wall metal organic chemical vapor deposition (MOCVD) at 1100 °C. The amorphous Al2O3 films are grown by repeated deposition and subsequent low temperature (200 °C) oxidation of thin Al layers using a hot plate. Our investigation shows a very low density of interface traps at the AlN/4H-SiC and the Al2O3/4H-SiC interface estimated from capacitance-voltage (CV) analysis of MIS capacitors. Current-voltage (IV) analysis shows that the breakdown electric field across the AlN or Al2O3 is ~ 3 MV/cm or ~ 5 MV/cm respectively. By depositing an additional SiO2 layer by plasma enhanced chemical vapor deposition at 300 °C on top of the AlN or Al2O3 layers, it is possible to increase the breakdown voltage of the MIS capacitors significantly without having pronounced impact on the quality of the AlN/SiC or Al2O3/SiC interfaces.

1. Introduction

The great potential of 4H-SiC MISFETs for power electronics is hampered by low channel mobility mainly due to high density of interface states at the SiO2/SiC interface. The quality of the SiO2/SiC interface has been improved by various oxidation and nitridation methods but more reduction in interface traps is needed [1–3]. Beside SiO2 as a gate dielectric, the use of high-k dielectrics on SiC has also been investigated. AlN and Al2O3 have reasonably large band gap (∼ 6.2 eV and ∼ 7 eV respectively) and high dielectric constant. The conduction band offset of AlN or Al2O3 to 4H-SiC of ∼ 1.7 eV is expected to be sufficient for n-channel MISFET operation [4–9]. High quality single crystalline AlN can be grown on SiC because of only 1% lattice mismatch to SiC [10]. However, an amorphous Al2O3 is considered to be better than poly-crystalline α-Al2O3 as a gate dielectric on 4H-SiC because of leakage through grain boundaries [11].

A crystalline AlN grown by molecular beam epitaxy (MBE) has been reported as a gate dielectric for 4H-SiC MISFETs but very low channel mobility (< 1 cm2/V) was obtained because of the leaky structure [12]. The irradiation of atomic nitrogen or HCl gas etching before the growth of AlN has been used to improve the quality of MBE grown AlN films [13,14]. The growth of AlN layers by MOCVD on 4H- and 6H-SiC has also been reported and a significant density of fixed charge and interface traps is observed in such AlN layers [15,16].

An amorphous Al2O3 grown by atomic layer deposition (ALD) or thermal oxidation of metallic Al has been used as a gate dielectric in graphene field effect transistors with some success [17,18]. The ALD as grown Al2O3 on 4H-SiC typically contains a large number density of negative charges which are reduced after annealing in Ar at 1000 °C but the Al2O3/SiC interface contains a high density of interface traps after such treatment due to growth of an interfacial SiOx (0 < x < 2) layer [19]. To improve the quality of ALD grown Al2O3 pre-deposition surface cleaning and post deposition annealing has been performed in N2O or N2 ambient [20,21]. A MOSFET with ALD grown Al2O3 that was post-annealed in hydrogen at 400 °C, is reported with a field effect mobility of 57 cm2/V s. Even though these results are promising, large threshold voltage shifts are observed due to the sensitivity of the Al2O3 layers to electron injection [22]. There is another report on a very high peak field effect mobility of 300 cm2/V s in SiC MOSFETs using Al2O3 made by MOCVD with a thin SiO2 interfacial layer to the SiC [23]. But, the mobility drops very rapidly with gate voltage and is less than 50 cm2/V at moderate gate voltages.

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In this study, we grow crystalline AlN by hot wall MOCVD and amorphous Alox by low temperature oxidation of Al on n-type 4H-SiC. On few selected samples, an additional layer of SiO2 is deposited on top of the AlN or Alox layer by plasma enhanced chemical vapor deposition (PECVD). The interface traps at the AlN/SiC and Alox/SiC interfaces are investigated by capacitance voltage (CV) measurements on MIS capacitors. The dielectric breakdown properties are extracted from current voltage (IV) measurements. We find that both the AlN/SiC and the Alox/SiC interface contain very low density of interface traps and the use of SiO2/AlN or SiO2/Alox dielectric stack improves the breakdown voltage of the MIS devices.

2. Experimental methods

Two sets of n-type 4H-SiC MIS capacitors were made. One with single crystalline AlN and other with amorphous Alox as a dielectric. The 4H-SiC used in this study have 10 μm thick n-type epitaxial layers with a net doping concentration of ~ 1 × 10^{16} cm^{-3} grown on 4° off-axis (0001) highly doped ~ 1 × 10^{16} cm^{-3} 4H-SiC substrates. A single crystalline 10 nm thick Alox layer was grown on 4H-SiC in a hot-wall MOCVD reactor at 1100 °C. Ammonia and Al2(CH3)6 were used as a precursor for nitrogen and aluminum respectively. Prior to deposition of Alox, the SiC surface was exposed in H2 ambient at 1320 °C, in order to obtain a native oxide-free surface. The details of the Alox growth process and structural characterization of the crystalline AlN layers are given in Ref. [24]. The amorphous Alox is grown by depositing few monolayers of pure Al by electron beam evaporation at a rate of ~ 0.5 Å/s and then the sample is baked on a hot plate in room environment at a temperature of 200 °C for 5 min to form Alox layer. This process of deposition and subsequent low temperature oxidation was repeated twelve times resulting in a film thickness of 15 nm as determined by X-ray reflectivity (XRR) and Atomic Force Microscopy. Prior to growth of Alox, the SiC was cleaned with HF in order to remove the native oxide. Further details of the Alox growth process are given in Ref. [25]. An additional layer of SiO2 with thickness of 40 nm was deposited on selected samples from both sets by PECVD at 300 °C using source gases of nitrous oxide and silane. Reference MIS capacitors was deposited on selected samples from both sets by PECVD at 300 °C.

Circular MIS capacitors are made using Al as a gate metal and back contact as well. The interface quality is characterized by conventional CV analysis using Agilent E4980A LCR meter. The dielectric breakdown strength of the MIS samples is determined by IV measurements using a Keithley 617 electrometer. CV and IV measurements are performed in vacuum of 10^{-3} mbar in a cryostat.

3. Results and discussion

Fig. 1 shows CV spectra of MIS capacitors having AlN and Alox dielectrics measured at room temperature and at frequencies of 1 kHz and 1 MHz. The gate bias is swept from depletion (negative bias) to accumulation (positive bias) and the capacitance signal for both frequencies is recorded simultaneously at each gate bias point. Fig. 1a shows the CV curves for AlN sample. The dielectric constant deduced from the accumulation capacitance is about 8.7. Fig. 1b shows the CV spectra of the Alox. The dielectric constant for Alox is ~ 6.5. The flatband voltage in both AlN and Alox is ~ 0.7 V which is close to the theoretical flatband voltage (i.e. ~ 0.4 V) which shows that initially the AlN and Alox layers contain insignificant amount of fixed charge. A first estimate of the interface trap density is extracted from frequency dispersion of CV curves [27]. In the AlN and Alox case, such dispersion is hardly visible indicating a low interface state density.

The interface quality of AlN or Alox dielectric with 4H-SiC can be estimated by investigating the frequency dispersion of the CV spectra of an MIS capacitor. Electron capture into interface states is most often a fast process while electron emission from interface traps is normally much slower and is a thermal process which depends on the difference Ec-E (where E is the energy level of the interface trap and Ec denotes the SiC conduction band edge). If an electron is captured and not emitted again, this is detected as a shift of the CV curve to higher gate voltages. If the test frequency is high (1 MHz) then more traps will not emit their electrons and the curve is shifted as compared to the low frequency (1 kHz) curve. The extraction of Df follows the method of Berglund [27]. The interface trap density (Df) is determined by well-known High-Low-Capacitance method using an equation: $D_f = \frac{C_f C_p}{C_f - C_p} = \frac{C_{pq} q}{C_{pq} + C_q}$. Where $C_p$ is dielectric capacitance, $C_q$ and $C_{pq}$ are low and high frequency capacitance respectively.

Fig. 2 shows Df extracted from room temperature CV dispersion data for MIS samples with AlN or Alox as a dielectric as well as reference SiO2 samples. The single layer AlN and Alox samples contain the lowest Df. The detrimental interface states that exist within this energy range for thermally grown oxides are virtually absent at the AlN/SiC or the Alox/SiC interface. It is clear that the addition of a SiO2 dielectric layer on the top of AlN or Alox affects the AlN/SiC and Alox/SiC interfaces. However, the single AlN and the SiO2/AlN stack both have lower Df than reference samples. The Df of the SiO2/Alox stack is comparable to the reference N2O grown SiO2.

A sensitivity to electron injection is observed in both AlN and Alox samples. This is detected as a flatband shift in subsequent 100 kHz CV curves when the samples are repeatedly biased into accumulation. The magnitude of the shift depends on the maximum applied accumulation voltage. An example of such behavior is shown in Fig. 3 for single layer AlN and Alox MIS samples. Such behavior is also reported in literature for AlN and Alox MIS samples [14,19]. This flatband shift can be a result of trapping of electrons in defects located within the dielectric. Similar electron injection is also observed in the dielectric stacks (not shown here).

However, in this work the process is reversible since the trapped electrons can be released back to the SiC at room temperature by applying depletion bias stress and UV illumination for a certain time to the MIS capacitors [28–30]. An example of such an experiment is shown in Fig. 4 for AlN/SiO2 and Alox/300 kHz CV curves (not shown). The gate bias stress and UV illumination for a certain time to the MIS capacitors [28–30]. An example of such an experiment is shown in Fig. 4 for AlN/SiO2 and Alox/300 kHz CV curves. The gate bias is swept from depletion (negative bias) to accumulation (positive bias) and the capacitance signal for both frequencies is recorded simultaneously at each gate bias point. Fig. 1a shows the CV curves for AlN sample. The dielectric constant deduced from the accumulation capacitance is about 8.7. Fig. 1b shows the CV spectra of the Alox. The dielectric constant for Alox is ~ 6.5. The flatband voltage in both AlN and Alox is ~ 0.7 V which is close to the theoretical flatband voltage (i.e. ~ 0.4 V) which shows that initially the AlN and Alox layers contain insignificant amount of fixed charge. A first estimate of the interface trap density is extracted from frequency dispersion of CV curves [27]. In the AlN and Alox case, such dispersion is hardly visible indicating a low interface state density.

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$$D_f = \frac{C_f C_p}{C_f - C_p} = \frac{C_{pq} q}{C_{pq} + C_q}$$

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curve) or 5 MV/cm (dotted curve) is recorded for the single layer AlN or Al$_2$O$_3$ sample respectively. A sharp current leakage is observed for single layer AlN even at low dielectric electric fields. This suggests the AlN layers have higher density of bulk traps compared to Al$_2$O$_3$ that cause trap assisted leakage across dielectric. The breakdown field of the reference thermal SiO$_2$ sample is $\sim 9$ MV/cm (dash double dotted curve). The physical origin of the electron traps within the AlN and Al$_2$O$_3$ layers is unknown. Our postulate is that the AlN layer has either very high density of intrinsic point defects (e.g. silicon and oxygen point defects) or extended defects like dislocations [31]. The Al$_2$O$_3$ layer is expected to contain oxygen related intrinsic defects [32]. These defects are presumably the cause of the current leakage through the AlN and Al$_2$O$_3$ layers.

The SiO$_2$/AlN and SiO$_2$/Al$_2$O$_3$ stack samples have effective breakdown field, if we consider the dual dielectric as a single dielectric, of $\sim 8$ MV/cm (dashed curve for SiO$_2$/AlN and dash dotted curve for the SiO$_2$/Al$_2$O$_3$ sample). However, the breakdown electric field across the AlN or Al$_2$O$_3$ layer in the stack is $\sim 4$ MV/cm or $\sim 5.5$ MV/cm. Addition of SiO$_2$ on the top of AlN layer does not significantly improve the breakdown properties of the AlN or Al$_2$O$_3$ but allows the use of higher gate voltages for device operation.

4. Conclusions

CV analysis at room temperature shows that single crystalline AlN and amorphous Al$_2$O$_3$ layer have good interface quality in terms of low density of interface states in n-type 4H-SiC MIS capacitors. A significant electron trapping is observed within the AlN or Al$_2$O$_3$ when the MIS capacitors are biased into accumulation resulting in a large flatband voltage shift towards higher gate voltages. This can be connected to the relatively low breakdown field ($\sim 3$ MV/cm or $\sim 5$ MV/cm) of the AlN or Al$_2$O$_3$ layers. It is possible to slightly improve the breakdown field of the MIS devices by depositing a SiO$_2$ layer on top of the AlN or Al$_2$O$_3$. More work is needed in optimizing the growth conditions of the dielectrics and resolving the question of electron trapping within the AlN and Al$_2$O$_3$ layers. In summary, the AlN and Al$_2$O$_3$ MIS samples show very promising results in terms of interface state densities but electron injection into both layers is currently preventing their practical use.
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References


Fig. 4. Electron injection and emission in and out of traps located within (a) the AlN or (b) Al2O3 layer. The black solid 100 kHz CV curves are recorded after which electrons are intentionally injected into the AlN or Al2O3 by accumulation bias stress for certain period. The dotted 100 kHz CV curves are recorded after applying negative bias stress with UV illumination to the samples for 30 min.

Fig. 5. Comparison of leakage current density versus effective electric field (J–E) for differently prepared MIS samples.