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IGBT Power Stack Integrity Assessment Method for High-Power Magnet Supplies

Panagiotis Asimakopoulos, *Member, IEEE*, Konstantinos Papastergiou, *Member, IEEE*, Torbjörn Thiringer, *Senior Member, IEEE*, Massimo Bongiorno, *Senior Member, IEEE*, and Gilles Le Godec

***Abstract*—This paper proposes a method for assessing the integrity of a series of insulated-gate bipolar transistor (IGBT) power stacks during factory-acceptance tests and service stops. The key challenge that is addressed in this paper is detecting common assembly issues that affect the power stack thermal path as well as distinguishing the acute aging effects of bond-wire lift-off and solder delamination. The method combines offline V_{ce} measurements with current in the extended Zero Temperature Coefficient (ZTC) operating region as well as with sensing current without modifications to the power stack. It also employs on-the-stack V_{ce} calibration for both the measurements. Additionally, only a fixed duty cycle pattern is needed to control the switches. The paper also presents a sensitivity analysis of the method to various parameters such as the current level in the extended ZTC operating region, the precision of the V_{ce} measurement, as well as the ambient, the cooling-water, and the junction temperatures. The experimental results are obtained from a high-current IGBT power stack used in a magnet power supply for particle accelerators and are compared favorably to results from finite element method and lumped parameter network simulations confirming the applicability of the method.**

***Index Terms*—Aging detection, condition monitoring, insulated-gate bipolar transistor (IGBT), particle accelerators, thermal performance, V_{ce} method.**

I. Introduction

RELIABILITY in power electronics is one of the major concerns for the power electronics designers and the end users. It can be assured by proper dimensioning of components during the design phase and by verifying the manufacturing quality during factory-acceptance tests. While the equipment is in the operation phase, a major reliability issue is the aging of the power components and particularly the power semiconductors; insulated-gate bipolar transistors (IGBTs) are subject to thermal stressing related to their packaging technology. The field of online [1] and offline [2] health condition monitoring of such components has been broadly researched in the recent years. Extensive work has been conducted on accelerated testing and aging mechanisms due to thermal stressing [3]–[6]. The most common aging modes that are documented are bond-wire lift-offs and solder delamination at chip or baseplate level [4].

At CERN—European Organization for Nuclear Research, high-power electronic converters are widely used as dc, power magnet supplies for particle accelerators. Power stacks with a long lifetime (25 years) are specified at CERN and mass produced in industry. The power stack is the part of the power electronic converter that comprises the dc-link capacitors and the power semiconductor devices with their cooling system. This paper proposes a new method offering adequate precision and ease of implementation to verify the integrity, meaning the assembly and the initial thermal resistance value during factory-acceptance tests as well as the health condition of a series of IGBT power stacks during service stops.

Several methods exist in the literature that employ IGBT junction temperature estimation to detect aging issues. These methods are mainly used in accelerated lifetime tests or are presented as potential solutions for field application. A way to estimate the junction temperature and detect aging is the use of the saturation voltage drop $V_{\rm ce}$ of the IGBT with sensing current [7], [8]. The $V_{\rm ce}$ method with sensing current is accurate because it avoids the voltage drop of the cabling at high current and exhibits high linearity with a relation of about 2 mV/°C at the complete temperature operating region. On the other hand, the $V_{\rm ce}$ method with sensing current is not directly applicable for online condition monitoring because it requires the separation of the device under test (DUT) with auxiliary switches from the power circuit, in order to measure only with sensing current. Additionally, other methods are presented for online temperature estimation and aging detection but require relatively significant effort for the calibration of the IGBT modules [9], such as the $V_{\rm ce}$ method with load current [1], the internal gate resistance method [10], or the gate threshold voltage method [11]. As it has been shown in [7], the $V_{\rm ce}$ method with sensing current can be used in applications with predefined load profiles, such as the CERN application or traction, where the online monitoring is not required.

The method that is proposed in this paper uses the $V_{\rm ce}$ measurements with sensing and load current. Fig. 1 illustrates the phases where the method can be used along the lifecycle of a power stack. The required inputs are the $V_{\rm ce}$ measurements, the power losses, and the water and ambient temperatures.

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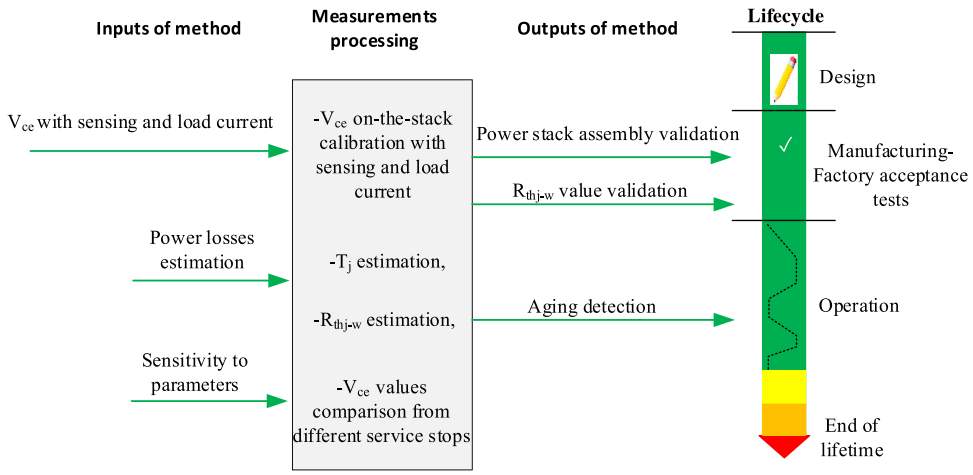

Fig. 1. Overview of the proposed method for integrity assessment of the IGBT-based power stack and lifecycle phases of power stack where the method is applied.

The following sections describe the way this information is combined in order to conclude about the integrity of a power stack. It is shown how manufacturing quality issues as well as thermal stressing can be detected by processing the $V_{\rm ce}$ measurements of a predetermined test cycle. This method can be directly applied to industrially finished power stacks without the need to add extra power components. The assessment of the assembly and of the thermal resistance of the power stack as well as the aging detection of the IGBT module is described as IGBT Power Stack Integrity Assessment (IPSIA).

Fig. 2 illustrates three recently presented power circuits that allow the $V_{\rm ce}$ measurements with load and sensing current to estimate the IGBT junction temperature for condition monitoring. All three propose the use of relays or switches for the temporary disconnection of the power converter load in order to perform measurements with sensing current. A circuit incorporating the $V_{\rm ce}$ measurements with both high and sensing current measurements [see Fig. 2(a)] has been proposed for bond-wire lift-off and solder delamination detection in [2] and [12]. The measurement with current around the nominal rating is followed by a measurement with sensing current, in order to measure the junction temperature indirectly, to make the necessary corrections for the high-current $V_{\rm ce}$ method and to detect bond-wire lift-offs. The high current is injected with the help of a current source connected in series with an IGBT. By using the $V_{\rm ce}$ measurements with sensing current and with the help of the same setup of Fig. 2(a), it is proposed that solder delamination can be detected based on the thermal resistance estimation.

Another contribution in the literature [13] proposes the circuit of Fig. 2(b), where the DUT disconnection is achieved by adding four switches. Using an elaborate switching sequence, the load current is redirected for a few switching periods in order to allow the $V_{\rm ce}$ measurement. Two of the switches isolate the load during the inverter current interruption and the two other switches allow the load current to freewheel during the interruption. Using the same principle as in [13], the method in [14] combines the $V_{\rm ce}$ methods with sensing and load current for aging detection due to bond-wire lift-off or solder delamination. In this case, the calculation of the thermal resistance for the aging evaluation requires measurements with sinusoidal current at level close to the nominal ratings, at the same temperature conditions, and an extra sensor at baseplate level.

The methods that are based on the power circuits of Fig. 2(a) and (b) require extra power components and calibration effort for $V_{\rm ce}$ with high current, both for temperature estimation and bond-wire lift-off detection. In particular, the need for extra power components makes these methods less suitable for already produced power stacks. For a high-current application such as the one at CERN, the current source of Fig. 2(a) would have several times higher ratings than for the low-power application in [2] and [12]. In terms of calibration, the $V_{\rm ce}$ measurement with high current for bond-wire lift-off detection is highly dependent on temperature and the influence of the interconnections resistance to the measurement has to be considered for the calibration. To conclude, the extra power components and their control for the load current redirection, as well as the calibration effort, add complexity to the methods.

The method in [15] that is illustrated in Fig. 2(c) is proposed for bond-wire lift-off detection in low-power devices. It is based on the $V_{\rm ce}$ measurement in the inflection point of the current operating region, where $V_{\rm ce}$ is independent of temperature (zero temperature coefficient (ZTC) operating region [16]), as shown in Fig. 3. Using the $V_{\rm ce}$ measurement in the ZTC operating region, the temperature calibration effort is avoided but calibration is needed to find the inflection point of the IGBT. The $V_{\rm ce}$ measurement is performed by injecting a controlled current through the reference reactors connected by dedicated relays, while at the same time disconnecting the load. This method cannot be used for solder delamination detection because the temperature estimation by the $V_{\rm ce}$ measurement at sensing current is not possible. The latter method can potentially be performed using the existing filter reactors.

To date, relevant literature mostly discusses methods for aging detection during operation in accelerated tests of the IGBT modules. The present paper proposes a method that targets series-produced high-power IGBT stacks. It can detect the aging and

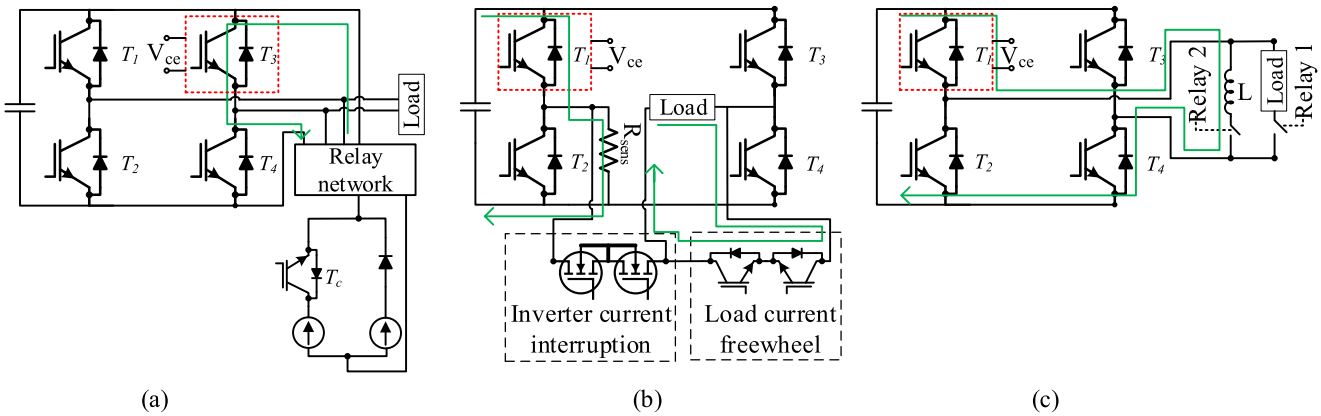

Fig. 2. Power circuits for aging detection of IGBT modules using the V_{ce} method with sensing or load current, the enclosed IGBT in the red-dashed square is the DUT. (a) Power circuit with additional high-current source and relays for the V_{ce} method with sensing and load current [2]. (b) Power circuit with current redirection for the V_{ce} method with sensing and load current [13]. (c) Power circuit with test inductor only for the V_{ce} method with load current in the ZTC operating region [15].

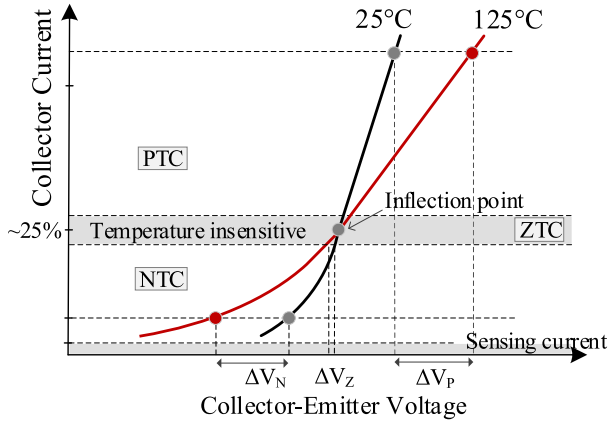

Fig. 3. Operating regions of IGBT in terms of collector current. The ability to detect and distinguish aging issues depends on the operating region: in NTC, an overlap of the effects caused by bond-wire lift-off and solder delamination can occur, whereas in PTC the two aging mechanisms are not distinguished because they cause the same effects. This work uses measurements in ZTC and low NTC (sensing current) to extract useful information for the aging detection.

distinguish between the two common IGBT aging mechanisms, namely bond-wire lift-off and solder delamination. The novelty of the proposed method stems from the following:

1) its ease of implementation by only switching two diagonal switches to create a testing current profile with only a fixed duty cycle pattern;
2) the DUT on-the-stack calibration both with sensing and high current;
3) the applicability on a power stack without disconnection of the DUT for the injection of a sensing current. The combination of the aforementioned features, as well as the measurement in the extended ZTC region for high-current modules avoiding the inflection point detection, makes this method a substantially improved sequence among the existing proposals for offline aging detection, especially for a series of power stacks.

The proposed test method for the integrity assessment is analyzed in Section II. Section III presents the test setup and the measuring tools that are utilized to, experimentally, demonstrate the proposed method. Section IV includes the experimental results and the comparison with the simulation results for the validation of the proposed method. Section V makes a general evaluation of the method compared to the existing methods and in terms of precision. The paper ends with the conclusions on the proposed method.

II. IGBT Power Stack Integrity Assessment (IPSIA)

A. Aim of the Method

This paper proposes a method in the form of a routine test to be performed during factory-acceptance testing of power stacks in order to validate the thermal performance and diagnose quality issues in manufacturing. The test can also be used in scheduled service stops to detect the aforementioned main aging modes of the IGBTs. The method focuses on the IGBTs, because they are the devices that are stressed the most in the application at CERN [17]. For applications with predefined load profiles and, as a result, predictable thermal stressing profiles, it is not needed to monitor the temperature online; the aging process typically affects the junction temperature profile during specific loading cycle and hence it can be detected by comparison of the V_{ce} measurements during the lifetime. The service stops for the power stack integrity assessment method have to be regularly executed, in order to avoid undetected extensive aging in the IGBT modules.

B. IGBT Collector-Emitter Voltage and Aging Detection

Fig. 3 illustrates a characteristic feature of IGBTs, such as the ones used in this paper, that is, the transition from a negative temperature coefficient (NTC) behavior with low collector current to a positive temperature coefficient (PTC) behavior when operating with higher current. Between the two operating regions, there is the ZTC operating region with the inflection point that is insensitive to temperature. In both PTC and NTC operating regions, the aging mechanisms are difficult to distinguish. More specifically for NTC, the aging mechanisms may

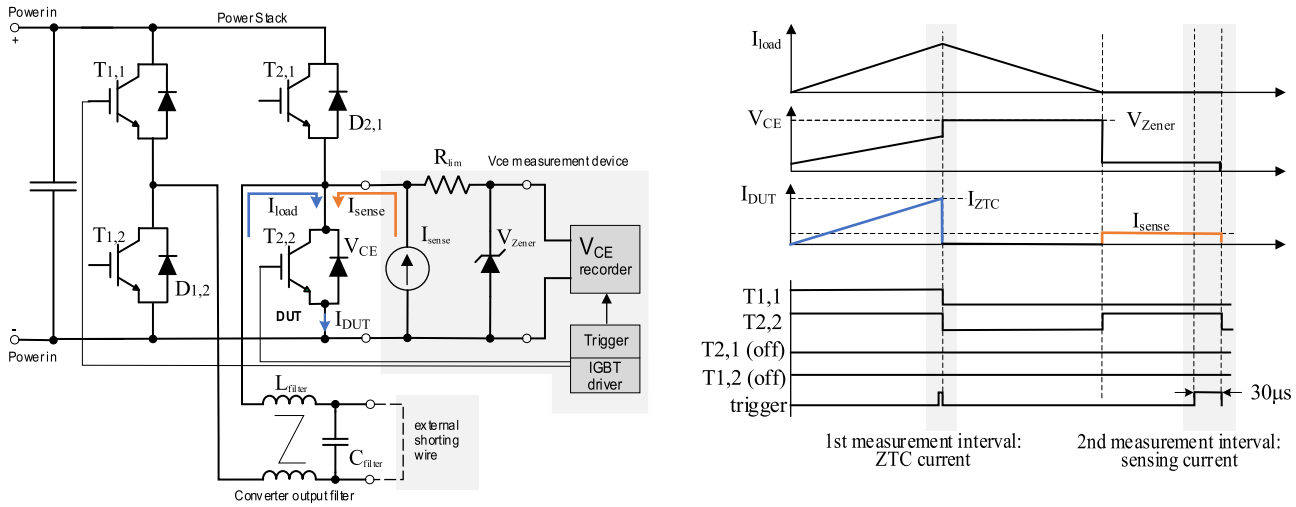

Fig. 4. Proposed method employs the elements in the shaded blocks: a $V_{\rm ce}$ sensing device (discussed in [7]) and a shorting wire connected across the power converter output. The key waveforms of measured $V_{\rm ce}$, load current $I_{\rm DUT}$, sensing current $I_{\rm sense}$, and gate pulses are generated with the fixed duty cycle pattern for the switches $T_{1,1}$ and $T_{2,2}$ during the proposed current cycle. A trigger is employed to time the measurements.

disguise each other until the next service stop because bond-wire lift-off increases $V_{\rm ce}$ whereas solder delamination results in lower $V_{\rm ce}$ [18] due to the increase of the thermal resistance in the heat propagation path. In the PTC operating region, both bond-wire lift-off and solder delamination increase $V_{\rm ce}$. This paper proposes two measurements, one in the ZTC operating region and one with a low sensing current. The combination of these two measurements gives the diagnostic information required to distinguish the IGBT aging.

According to the work presented in [19], the beginning of the aging and the degradation stage is detected via an increase of 3% and 10% in $V_{\rm ce}$, respectively, for a load current close to the nominal ratings of a high-power IGBT module. Moreover, an increase of 10% in junction-to-water thermal resistance is an indication of a forthcoming early failure. In a different work [6], the junction-to-baseplate thermal resistance increase of 5% indicates the beginning of aging, 10% is an indication of degradation, and 20% is an indication of failure. The thermal resistance estimation and its comparison with previous measurements are necessary, in order to detect solder delamination and prevent unscheduled stops.

C. Method Description

The proposed test requires an inductive load to be connected at the output of the power stack. An output-smoothing filter reactor that does not saturate with a unipolar current, like the one used for power electronic converters at CERN, is an example of such a load. By-passing any other components can be performed with a shorting wire as illustrated in Fig. 4. No additional power components are required other than the measurement devices. The test procedure for one of the IGBTs ($T_{2,2}$) is described with the help of Fig. 4.

In the first part of the procedure, the diagonal IGBTs $T_{1,1}$ and $T_{2,2}$ are operated with a constant duty cycle generated by the measuring setup (indicated in a shaded area in Fig. 4), in order to create a quasi-triangular current waveform. The peak current value is chosen to bring the IGBT in the ZTC operating region. The dc-link voltage, the switching frequency, and the duty cycle are selected as needed. In the second part of the test cycle, a time interval where only the DUT remains on is required for the sensing current of 1 A to be injected to it. The sensing current level is selected based on the work presented in [20]. The entire test cycle is repeated in every switching period. The $V_{\rm ce}$ measurement takes place twice in each switching cycle, once at the ZTC current level and once during the sensing current interval while the trigger signal is high, as shown in Fig. 4.

The $V_{\rm ce}$ measurement with sensing current is proposed in order to detect aging due to solder delamination in the cycling operation. A $V_{\rm ce}$ reduction that is detected during successive service stops would indicate a thermal resistance increase and an average temperature increase in the junction. On the other hand, the $V_{\rm ce}$ measurement with the rated IGBT current is known from literature [1] as an indicator of wire-bond lift-off as it causes a detectable $V_{\rm ce}$ increase. This paper contributes, also, by showing that with a $V_{\rm ce}$ measurement in the extended ZTC operating region the detection is possible for high-current modules under known ambient conditions, as elaborated in the following sections.

D. Sampling-Filtering Technique and Measurements Utilization

For the $V_{\rm ce}$ measurements with sensing current, a LabVIEW program is developed to acquire 30 $V_{\rm ce}$ samples with a sample rate of 1 MHz, once the sensing current flat-top is stabilized. In this paper, the time duration of the measuring window (30 μs) is limited by the switching frequency (3 KHz) for a given dc-link voltage (560 V) and a given inductive load. Additionally, the settling time of the $V_{\rm ce}$ measuring circuit, which is limited by the isolating amplifier, and the switching transients of the circuit set a minimum time length requirement. All the measurements

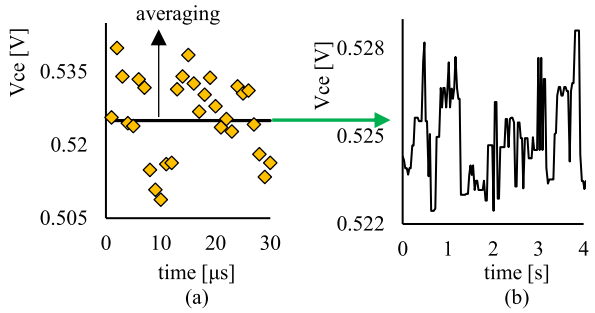

Fig. 5. Filtering technique example with measurements. (a) Samples per period and averaging. (b) Median filter output at steady state.

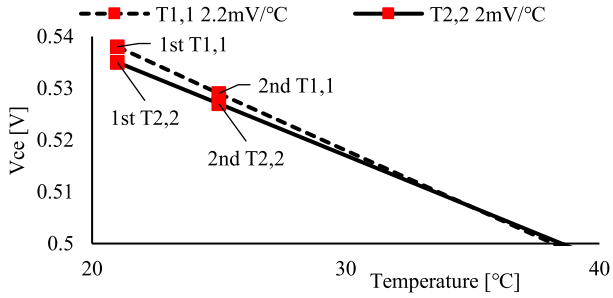

Fig. 6. Thermal characterization of IGBT modules at sensing current with and without water flow in the cooling plate.

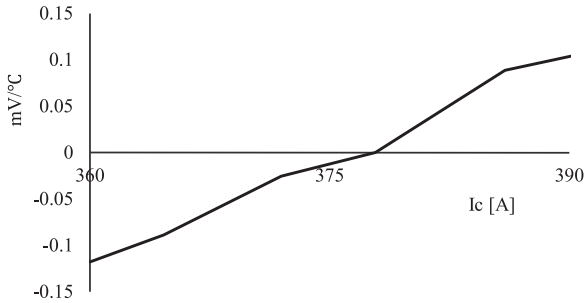

Fig. 7. Dependence of $V_{\rm ce}$ on temperature around the ZTC operating region.

are implemented in the industrial environment at CERN with high-power converters operating in the vicinity. By using the DUT of the specialized application, it was shown in [7] that the $V_{\rm ce}$ value with sensing current is independent of the gate-emitter voltage $V_{\rm ge}$ for the $V_{\rm ge}$ between 10 and 15 V. Every 30 ms, the last 30 samples are averaged and stored. The value of the averaging is the input to a median filter with a rank of 3, as illustrated in Fig. 5 [21].

For the measurement with ZTC current, the number of samples depends on the rate of the current rise. The rate of the current rise depends on the dc-link voltage and the inductive load. Again, the rise time of the current is sufficient for the $V_{\rm ge}$ stabilization [1]. For this paper, two samples corresponding to the last two values at the top of the ramp are taken and their average $V_{\rm ce}$ is calculated. Further analysis for the ZTC operating region follows in Section II-F.

E. On-Power Stack Calibration of IGBT Modules With Sensing Current

One of the challenges in this paper is to obtain the $V_{\rm ce}$ with sensing current calibration with temperature for already assembled power stacks. The calibration of a single IGBT module requires placing the device in a thermal chamber, injecting a sensing current to it, and measuring the voltage $V_{\rm ce}$ while the temperature in the thermal chamber is set to different levels. A few measurements are enough to define the linear relation between $V_{\rm ce}$ and temperature, usually it is around 2 mV/$^{\circ}C$.

This work makes use of the latter observation and effectively assumes only two temperature points to calibrate each IGBT while mounted on the power stack. This can be done by obtaining one point while the power stack is in ambient conditions (first measurement for $T_{1,1}$ and $T_{2,2}$) and a second point while cooling water flows through the cooling plate condition (second measurement for $T_{1,1}$ and $T_{2,2}$) allowing the structure to reach thermal equilibrium prior to a measurement. In the thermal steady state, the measured water temperature with the sensor of inlet water temperature is equal to the IGBT junction temperature.

The linear relation of temperature and $V_{\rm ce}$ at sensing current for the two switches is shown in Fig. 6 with the two measurements for each switch.

F. On-Power Stack ZTC Operating Region Verification of IGBT Modules

The IGBT current value at the inflection point can be defined with the help of the datasheet. A simple test performed with the complete power stack allows to fine tune the selection of the current level in the ZTC operating region, $I_{\rm ZTC}$, for the test current cycle in Fig. 4 for the purposes of the $V_{\rm ce}$ measurement. By applying the test current cycle and by adjusting the current at the top of the ramp, the $V_{\rm ce}$ values at the top of the ramp are compared before the cooling plate reaches a thermal steady state. The measured $V_{\rm ce}$ with $I_{\rm ZTC}$ does not vary from cycle to cycle while the cooling plate heats up, indicating that the measurement is independent of the temperature variation. Therefore, this is a method to verify that the IGBT module operates, indeed, in the ZTC operating region.

By using the datasheet values at 25 °C and 125 °C [22], Fig. 7 shows the dependence of $V_{\rm ce}$ on temperature in mV/°C. The inflection point where there is no temperature influence to $V_{\rm ce}$ is close to 375 A. The change in $V_{\rm ce}$ as a function of temperature for a constant current is considered to be linear, as observed from the measurements in [1] and [15]. It is observed that this relation is negative for current values lower than the inflection point, which can be noted when the $V_{\rm ce}$ value at 25 °C is subtracted from the value at 125 °C. In a band of 30 A around the inflection point, the maximum absolute value of this relation is approximately at the level of 0.1 mV/°C. With the help of Fig. 7, a conclusion is that it is not critical to measure $V_{\rm ce}$ exactly at the inflection point, because the sensitivity of $V_{\rm ce}$ for temperature values around this point is small. For specified operating conditions, the change in temperature can only be caused by a change in cooling-water temperature.

TABLE I
VOLTAGE DROP CHANGE IN THE LEADS FOR CURRENT LEVEL IN ZTC REGION

Temperature [°C]	Voltage change [mV]
25 (reference)	0
55	3
90	7
125	11

The variation of bond-wires and interconnections resistance with respect to temperature variation is considered in the graph of Fig. 7, according to the manufacturer [23]. On the other hand, the IGBT leads resistance $R_{CC'+EE'}$ is also influenced by the case temperature [22] and ambient air temperature. Based on the datasheet, the resistance difference for a temperature from $25/^{\circ}\mathrm{C}$ to $125/^{\circ}\mathrm{C}$ is 0.03 mΩ. The resistance change is calculated as

$$R_{\mathrm{actual}} = R_{\mathrm{ref}}\left[1 + \alpha\left(T_{\mathrm{actual}} - T_{\mathrm{ref}}\right)\right] \tag{1}$$

where R_{ref} is the reference resistance at the reference temperature T_{ref}, α is the temperature coefficient of resistance for the conducting material, and T_{actual} is the temperature during the measurement. Table I gives the voltage drop change across the copper leads as a function of temperature for a current at the level of the inflection point. As an example, the change at the power leads temperature of 30 °C would lead to a change of about 3 mV. Hence, the case and ambient temperature at different testing periods should be taken into account only for a significant temperature change and a correction factor can be applied to the V_{ce} measurements.

G. Power Losses Estimation and Thermal Resistance Calculation

The temperature estimation using the V_{ce} measurement at the selected sensing current can be used for the calculation of the thermal resistance of the IGBT module $R_{th,j-w}$ from junction to ambient, i.e., the water flow inlet. This calculation can be used as a verification, within a certain accuracy margin, for the thermal resistance that is provided by the supplier. Moreover, it is useful for comparisons with measurements in future service stops, in order to track the $R_{th,j-w}$ change with aging and detect solder delamination. The value of $R_{th,j-w}$ is calculated with the help of

$$R_{th,j-w} = \frac{\Delta T_{j-w}}{P_{\mathrm{loss}}} \tag{2}$$

where ΔT_{j-w} is the temperature difference between junction and water inlet used as a reference and P_{loss} is the sum of average switching and conduction losses of the IGBT module during the operation with the proposed current cycle at a thermal steady state.

An advantage of using this simplified current cycle is the ease of power losses estimation. Due to the discontinuous current mode of the cycle in Fig. 4, there is no turn-on switching energy loss. The measurement of turn-off losses at a current level at the top of the current ramp is only performed for the first power stack tested from a series of power stacks. For this work, the power stack supplier's measurements for the switching energy loss are used with the help of the equation for the calculation of turn-off energy loss provided in [24]. Regarding the two anti-parallel diodes that conduct during the current ramp-down in Fig. 4, their power losses are significantly lower than for the IGBTs. The diodes' switching losses are neglected because they turn-off at zero current in the end of the ramp-down. Therefore, the temperature measurements for the IGBTs are not, practically, influenced by the thermal coupling with the diodes.

Using (2), the accuracy of this method for the $R_{th,j-w}$ calculation can be compared with the accuracy of the method used for the thermal impedance estimation with sensing current in the IEC standard [25]. The temperature is measured both in the proposed method and in the IEC method with the V_{ce} method at sensing current; therefore, the precision in terms of temperature estimation is considered the same. The advantage of the IEC method is that it offers a precise value of the power losses since the IGBT conducts during a constant current and constant V_{ce} when it reaches a thermal steady state before the cooling down occurs. The proposed method requires measurements in dynamic conditions for the switching energy and linear approximations for the conduction energy that may lead to errors. The switching losses for the proposed cycle are significantly higher than the conduction losses, approximately five times more; therefore, the error by the conduction losses linear approximations has a negligible impact.

In this paper, $R_{th,j-w}$ includes the thermal resistance due to the thermal coupling of the two operating IGBTs, especially if they are placed closed to each other. The thermal coupling is further discussed in Section V. In this application, the criterion of 10% increase in thermal resistance can be adopted as an indication of degradation for the thermal resistance from junction to water assuming that no degradation will occur at the level of the thermal paste or of the cooling system due to accumulated particles in the cooling pipes. Considering the cooling, the monitoring of the water flow at the outlet and the particle filter at the inlet of the cooling plate protect the power stack from cooling degradation for the specialized application. A sensitivity analysis of $R_{th,j-w}$ in terms of junction temperature measurement is presented in Section V by using the results of this work.

III. EXPERIMENTAL SETUP

An industrially produced power stack is used for the experiments. The H-bridge comprises four single-switch IGBT modules mounted on a copper cooling plate [17]. For the validation tests, the DUT is connected in series to an external identical but open IGBT mounted on an identical cooling plate. The open module allows the performance of thermal imaging. The dc-link

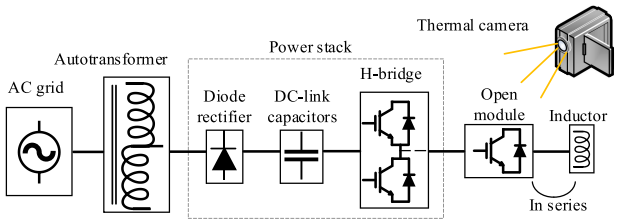

Fig. 8. Experimental setup used for the demonstration of the method. The open module and thermal imaging are used for the validation of IPSIA and are not used in the proposed routine test.

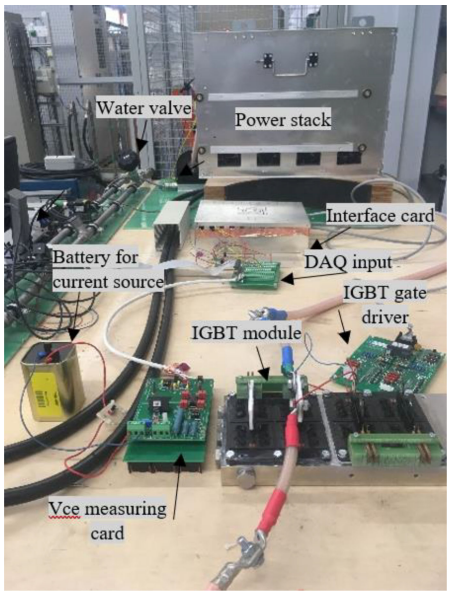

Fig. 9. Experimental setup with H-bridge output connected to open IGBT module.

TABLE II
RATINGS OF INTEREST FOR THE POWER STACK OF THE EXPERIMENTAL SETUP

Parameter	Value
DC-link voltage in experiment	560 V
Peak current value	365 A
IGBT switch nominal current/voltage	1600 A /1700 V
Nominal flow rate of water cooling system	12 l/ min
Inductive load value	Approximately 120 µH /1.1 mOhm

voltage is controlled using an autotransformer. Fig. 8 provides an overview of the experimental setup and Fig. 9 is a picture of the power circuit. The ratings of interest for the power circuit are provided in Table II. The cooling circuit has a central, manual valve for the flow rate regulation, a flow sensor, and two temperature sensors at the inlet and outlet. The cooling plates of the power stack and that of the open IGBT module are supplied in parallel by the cooling network.

TABLE III
COMPARISON BETWEEN THERMAL CAMERA AND THE $V_{\rm ce}$ MEASUREMENTS OF TEMPERATURE RISE FOR DIFFERENT THERMAL PASTE CONDITIONS

	No thermal paste	Reduced thermal paste	Manufacturer recommended thermal paste
Layer thickness	0 µm	50 µm	100 µm
Junction temperature rise with V_{ce} method [°C]	13	10	6
Junction temperature rise with thermal camera [°C]	11.5	8.5	5.5

The data acquisition (DAQ) and control system are built around a National Instruments USB-6251 card. The LabVIEW program produces the IGBT pulses required for the test routine; it provides the trigger for the measurements and finally collects and post processes the DAQ measurements. The circuit for the $V_{\rm ce}$ measurement with sensing and load current has been the subject of previous publications [7]. A Tektronix current probe TCP404XL with a bandwidth of 2 MHz and 1% precision is used for the load current measurements.

IV. RESULTS

A. Detection of Manufacturing Issues

Manufacturing issues such as the use of incorrect mounting torque or the incorrect application of a thermal paste layer can be detected by measuring the junction temperature or the junction-to-water thermal resistance of IGBTs and compare it with design calculations or with a reference power stack. To demonstrate the thermal effect of the use of insufficient thermal paste, an experiment is conducted where different thermal paste layer thicknesses are applied, according to the guidelines in [26]. The current cycle of the proposed method is applied with a peak current of 450 A to increase the semiconductor power losses and cause higher temperature variations across the thermal resistance. The open IGBT module is always turned on; therefore, it does not produce any switching losses. The current profile of the open IGBT is the same as the load's triangular current profile in Fig. 4. The temperature is estimated using the $V_{\rm ce}$ measurement with sensing current in the open IGBT module and it is compared with the surface average temperature among all chips measured using infrared imaging. Table III summarizes the junction temperature estimation with the sensing current method and the infrared camera measurements for the different thermal paste cases.

The absence of or insufficient thermal paste (thickness of 50 μm) due to wrong mounting or pump-out results in a significant increase in $R_{th,j-w}$ that is observed by measuring the

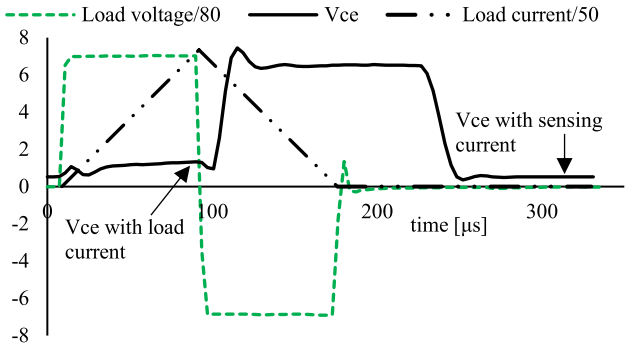

Fig. 10. Measurements within a switching period of the proposed cycle.

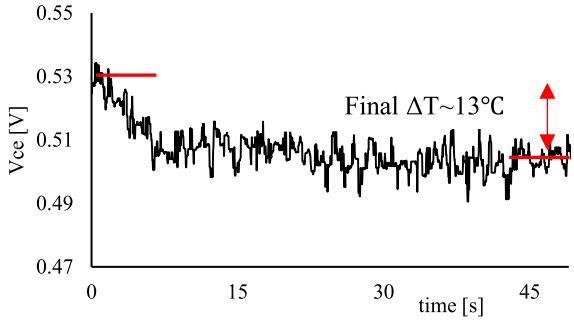

Fig. 11. Measurement of the $V_{\rm ce}$ voltage (with sensing current) evolution while the IGBT junction temperature increases for water flow rate of 12 L/min.

junction temperature rise. On the contrary, it was noticed that the application of excessive thermal paste with a thickness of approximately 200 μm did not cause a detectable thermal resistance difference for the thermal load of the experiment, if compared to the case with normal thermal paste. The correct mounting of the IGBT module forces the excessive thermal paste to the edges of the baseplate and out of the junction-ambient thermal path.

B. Solder Delamination Detection

The aim of this test is to detect any increase of the thermal resistance that can be linked to solder delamination during service stops. The junction temperature estimation is required for the thermal resistance calculation. First, the temperature estimation of the diagonal switches is implemented by using the current cycle that is proposed for the IPSIA method. The load current and load voltage along with the collector-emitter voltage $V_{\rm ce}$ of switch $T_{2,2}$ have been recorded. The test load current of 365 A keeps the semiconductor in the extended ZTC operating region below the inflection point in Fig. 3. A dc-link voltage of 560 V generates a current ramp rate of approximately of 4.6 A/μs with the 120 μH reactor load, while a switching frequency 3 kHz generates adequate switching losses in the power semiconductors.

As can be seen in Fig. 10 during the conduction of two diagonal IGBTs ($T_{1,1}$ and $T_{2,2}$) the current increases with a constant rate, and $V_{\rm ce}$ increases with the current increase. At the top of the ramp, $V_{\rm ce}$ is recorded under full load current set to ZTC level. At approximately 80 μs, the load current is directed to the antiparallel diodes of the other two diagonal IGBTs and the load current decreases until it becomes zero after approximately 160 μs from the beginning of the cycle. While the load current remains zero, the switch $T_{2,2}$ alone is turned on and a 1 A sensing current is injected to it. The voltage $V_{\rm ce}$ is recorded for a period of 30 μs until the end of the cycle, and after the $V_{\rm ce}$ value is settled. Fig. 11 illustrates, as an example, the $V_{\rm ce}$ reduction as the $T_{1,1}$ junction temperature increases for a water flow rate of 12 L/min.

Finite element method (FEM), [27], and lumped parameter network (LPN), [28], simulations are used to help with analysis of the method concerning the thermal coupling between the IGBT modules and the thermal time constant of the IGBT internal layers. First, for the accurate estimation of the junction

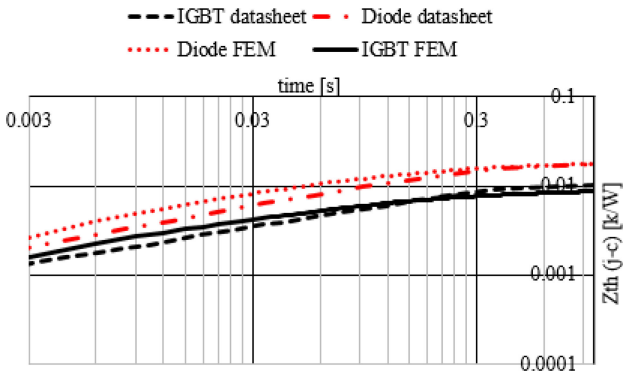

Fig. 12. Simulations results: thermal impedance comparison between FEM and datasheet for IGBT and anti-parallel diode.

temperature, the temperature reduction of the IGBT during the off-time of approximately 220 μs, from the peak of the ramp until the $V_{\rm ce}$ measurement with sensing current, is simulated using FEM with information for the IGBT module from [29] and [30] and with the modeling technique presented in [31]. FEM in the COMSOL environment is used to simulate both the heat conduction among the solid parts of the power stack as well as the heat convection to the water of the cooling system. As shown in Fig. 12, the FEM models of the thermal impedance characteristics of both IGBT-to-case and antiparallel diode-to-case match well to the datasheet characteristics.

The initial condition for the FEM model is the thermal steady state at the proposed cycle and no heating power is injected to the chips. The temperature decrease between the current peak and the measurement with sensing current is only 0.2 °C and can be neglected. It slightly affects the calculation of $R_{th,j-w}$, allowing the solder delamination detection. The FEM model is more accurate than the LPN model for such a short cooling-down time interval right after the heating power injection. The *RC* parts of the LPN dynamic model do not correspond to the physical layers of the IGBT module [28]. Moreover, no information is given below 1 ms about the thermal impedance in the IGBT datasheet [22]. The thermal time constant of the chip is calculated at the level of approximately 550 μs; therefore, the cool-down during 220 μs is limited to chip level. For a comparison, the thermal time constant of the DUT according to the work presented in [22] is approximately 100 ms, allowing a significant time

TABLE IV
COMPARISON OF MEASUREMENTS, FEM, AND LPN SIMULATIONS FOR TEMPERATURE ESTIMATION

Flow rate [l/min]	ΔT measurement [°C]	ΔT FEM [°C]	ΔT LPN [°C]	Power losses per IGBT [W]
12	12.7 ($T_{1,1}$) / 13 ($T_{2,2}$)	11.6	12.9	~330
18	11.8 ($T_{1,1}$) / 10.5 ($T_{2,2}$)	10.5	11.6	~330

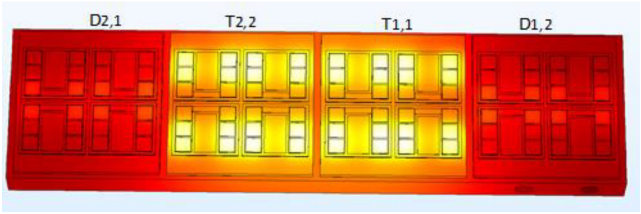

Fig. 13. FEM representation of the IGBT module placement and heat distribution among the chips inside each of the modules.

margin for the solder delamination detection. In the unlikely case that an output-smoothing inductor with a value of several mH is used as a load, the current ramp-down would have a long duration and the IGBT junction temperature variation until the $V_{\rm ce}$ measurement may not be negligible anymore.

Table IV provides the temperature rise at junction temperature for the two diagonal IGBT switches between the beginning of the cycling that corresponds to the ambient temperature and the thermal steady state. The proposed cycle is repeated for two cooling flow rate values, i.e., at 12 and 18 L/min and for the two diagonal switches $T_{1,1}$ and $T_{2,2}$, in order to compare the temperature rise with the FEM and LPN models. Additionally, the power losses injected to the simulation models are presented. For a more precise comparison, the FEM model is used to calculate the coupling between the two IGBTs mounted next to each other, as it is illustrated in Fig. 13.

The electro-thermal simulation model of the experimental setup is developed in PSIM using LPN. For the thermal resistance comparison between experiments, FEM and LPN at steady state, the sum of the thermal resistance of the IGBT module from the datasheet and of the thermal paste-cooling system from the supplier is used together with an added thermal resistance representing the thermal coupling between the IGBT modules.

The measurements match well with the results using the FEM model. The difference is justified by the precision of the $V_{\rm ce}$ measurement [7] and the small divergence of the FEM model's thermal resistance from the physical system. The thermal coupling between the two IGBTs is considered in the LPN model and is modeled as an additional series-connected thermal resistance of 0.003 K/W, as illustrated in Fig. 14.

After estimating the junction temperature using the $V_{\rm ce}$ measurement, the thermal resistance can be calculated with the help of the estimated power losses provided in Table IV. Table V

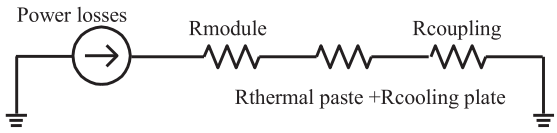

Fig. 14. LPN thermal model for static temperature calculations. The coupling effect among different IGBT modules is modeled as a series-connected thermal resistance.

TABLE V
COMPARISON OF MEASUREMENTS, FEM, AND LPN SIMULATIONS FOR THERMAL RESISTANCE ESTIMATION

Flow rate [l/min]	$R_{th,i-w}$ [K/W] measurement	$R_{th,j-w}$ [K/W] FEM	$R_{th,i-w}$ [K/W] LPN
12	0.039 ($T_{1,1}$) / 0.038 ($T_{2,2}$)	0.035	0.039 (0.036 without thermal coupling)
18	0.036 ($T_{1,1}$) / 0.032 ($T_{2,2}$)	0.032	0.035 (0.033 without thermal coupling)

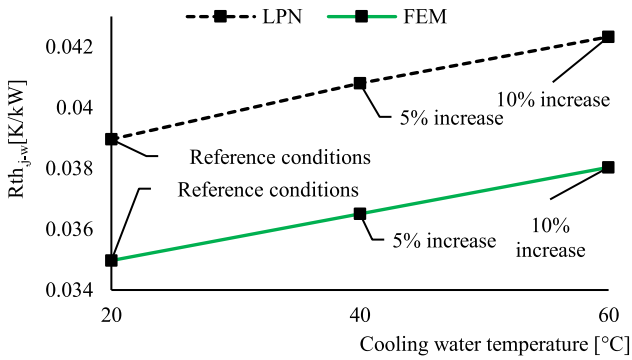

Fig. 15. Thermal resistance estimation error with cooling-water temperature increase by keeping the power losses of the reference conditions according to (2).

presents the thermal resistance estimation per switch for two different flow rate levels based on measurements and simulation with FEM and LPN.

It is observed that the $R_{th,j-w}$ difference between the measurement and the FEM model is approximately 0.004 K/W for 12 L/min, whereas the LPN simulation result matches with the measurements. The value of $R_{th,j-w}$ from the $V_{\rm ce}$ measurements can be used as a reference for the comparison of thermal resistance values between successive service stops during the equipment operating life. For the specialized application, the change of the inlet water temperature used as a reference is expected to be kept within a range of 1 °C, low enough, not to affect the measurement. The sensitivity analysis in Fig. 15 shows that a cooling-water temperature rise of 20 °C would result in an apparent thermal resistance value increment of 5%. The cooling-water temperature should therefore be taken into account each time the thermal resistance is recorded during the equipment service stops. The error in the estimated $R_{th,j-w}$ occurs under the assumption that the power loss increase due to the water temperature increase is not taken into account. In this

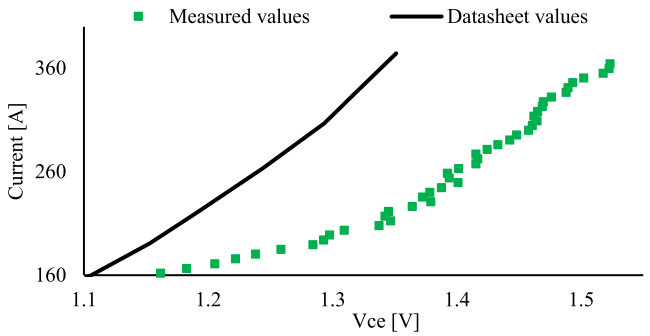

Fig. 16. $V_{\rm ce}$ values at chip level during current ramp-up according to datasheet and $V_{\rm ce}$ values close to power leads according to measurements.

case, the reference power losses would be used. The variable ΔT_{j-w} in (2) would increase due to the power losses increase, but $P_{\rm loss}$ would remain the same under the assumption of unvaried power losses. As shown by the FEM simulations, the impact of the power losses increase on the thermal resistance rise is greater than that of the thermal conductivity of Si. It is observed that a significant water temperature change should be taken into account in IPSIA and a recalculation or measurement of the power losses would be needed.

The precision of the measuring circuit, itself, also impacts the accuracy of the thermal resistance estimation and as a result it defines the ability to diagnose the IGBT module degradation such as the solder delamination. According to (2), with the assumption of a measurement accuracy of $+/-1$ °C, the minimum detectable deviation in $R_{th,j-w}$ is 7% with a nominal flow rate of 12 L/min.

A thermal resistance change of 10% is therefore considered a safe indication of solder degradation. It is observed that the impact of the temperature measurement on the estimated $R_{th,j-w}$ is smaller, if the temperature rise becomes higher, because the signal-to-noise ratio would be higher. This can occur, for example, as a result of higher switching losses due to higher operating voltage across the IGBTs (assuming the power stack ratings permit this). In this case, IPSIA would become more sensitive and would detect $R_{th,j-w}$ changes below 7%. The power losses increase could be achieved, for instance, if a double dc-link voltage and a double inductive load value are assumed, to significantly increase the switching losses and keep the same current rise time. The dc-link voltage increase should always be in respect to the power stack ratings.

C. Bond-Wire Lift-off Detection

The purpose is to verify if the proposed method can detect bond-wire lift-offs in the ZTC operating region. Fig. 16 shows the $V_{\rm ce}$ evolution during the current ramp-up measured with an open module. The difference between the datasheet values and the measurements is mainly due to the parasitic inductance and parasitic resistance of the terminal-chip leads. The difference between the datasheet and the measured values increases with the current increase because the parasitic resistance effect is amplified at high current values.

The bond-wires of a chip are intentionally cut one-by-one and the change in $V_{\rm ce}$ voltage is registered for each cut, according to Table VI. The measurements in the PTC region are not required for the implementation of IPSIA but are provided as a comparison for the capability to detect bond-wire lift-offs in the PTC and in the ZTC operating region. The measurement of $V_{\rm ce}$ is carried out at the top of the ramp-up by averaging the last two $V_{\rm ce}$ values. For these test series, only one substrate out of four is used. The bond-wire lift-off effect in both ZTC (92 A/substrate) and PTC (360 A/substrate) operation regions is evaluated.

TABLE VI
BOND-WIRE LIFT-OFF DETECTION WITH THE $V_{\rm ce}$ METHOD AT ZTC AND PTC OPERATING REGION

Number of disconnected bond-wires	Operating region	V_{ce} change [mV]
8/ 9/ 10 (chip failure)	ZTC	4/ 6/ 12
2/ 3	PTC	10/ 15

It is observed that for the PTC case the cut-off of two bond-wires provides clear evidence of aging. Concerning the ZTC case, the relatively low current does not allow the detection of loss of a few wire bonds, but it gives clear evidence when more than half of the connections to a chip are lost. According to Table I, an increase of around 30 °C in the power leads temperature could have approximately the same impact at $V_{\rm ce}$ as the eighth lift-off on the chip.

It is interesting to examine if a solder delamination effect can be distinguished from bond-wire lift-offs. Hence, the change of the average temperature among the healthy chips of the IGBT module with the chip failure is simulated with FEM for the proposed cycle. The increase in $R_{th,j-w}$ would be about 5% that is less than the 10% criterion that is set for solder delamination. Therefore, there would be no significant overlapping in the detection of the lift-off and solder delamination, even for a chip failure. Based on Fig. 7, the sensitivity of $V_{\rm ce}$ with temperature at this current level is approximately $0.1\ {\rm mV}/^{\circ}{\rm C}$. The proposed cycle keeps the junction temperature always at the same conditions. The water temperature is a parameter that can change. For a significant water temperature change of 20 °C, the $V_{\rm ce}$ change is about 2 mV and it can be considered for the aging detection. The impact of water temperature change at the thermal conductivity of silicon does not affect the measurement in ZTC.

V. EVALUATION OF THE INTEGRITY ASSESSMENT METHOD

In this section, the results of the sensitivity analysis on the main factors influencing the method are summarized. Table VII provides a summary of the parameters and their margin in the precision of the temperature estimation and of the aging detection according to the proposed method, as they previously were found.

Finally, Table VIII compares the existing methods using $V_{\rm ce}$ measurements for aging detection to the proposed method. The method in this paper does not require any power stack modifications. The prognostic procedure in [15] uses similar power

TABLE VII
SUMMARY OF SENSITIVITY ANALYSIS OF IPSIA METHOD WITH THE SPECIALIZED APPLICATION AS REFERENCE

Variable	Aging parameter	Margin of change of variable	Impact of precision within margin
V_{ce}	$R_{th,j-w}$	+/-1°C	7% (lower for higher power losses)
Water temperature	$R_{th,j-w}$ /solder delamination	+/-20°C	5%
Power leads temperature	Bond-wire lift-off	+/-30°C	3mV (close to minimum detected voltage increase at 8 bond-wires lift-off – Table VI)
Peak current value at ZTC	Bond-wire lift-off	+/-15A	Up to approximately 0.12mV/°C for 15A deviation from inflection point

TABLE VIII
OVERVIEW OF AGING DETECTION METHODS FOR ASSEMBLED POWER STACKS USING THE V_{ce} MEASUREMENTS

Method	Target	Power stack modifications-extra power components	On-the-stack V_{ce} calibration	Detection level	Temperature sensitivity	
					Lift-offs detection	Solder delam. detection
[2], [12], Fig. 2a	Lift-off (PTC) and solder delam.	IGBT, relay, high current source	No	Early detection for solder delam. and lift-offs	High to junction temperature change	Low, only for significant cooling medium temperature change between tests
[13], [14] Fig. 2b	Lift-off (PTC) and solder delam.	2 IGBTs, two MOSFETS	No	Early detection for solder delam. and lift-offs	High to junction temperature change	Low, only for significant cooling medium temperature change between tests
[15], Fig. 2c	Only lift-off (inflection point)	Inductive load and relays in case output filter inductor is not suitable	No	Early detection for lift-offs (only for low current devices)	Low to junction temperature change	Not detected
Proposed method (IPSIA), Fig. 4	IGBT assembly and $R_{th,j-w}$ validation, lift-off (extended ZTC) and solder delam.	None	Yes / suitable for assembled power stacks	Early detection for solder delam. / more than half chip failure for lift-offs	Low to junction temperature change	Low, only for significant cooling medium temperature change between tests

circuit by potentially using the output filter inductor and relays, but a different current profile and detects only bond-wire lift-off at the inflection point. The rest of the methods require significant power stack modifications. Additionally, the proposed method exhibits ease of calibration for already assembled power stacks and negligible impact of junction temperature on bond-wire lift-off detection due to the operation in the extended ZTC operating region, without the need to calibrate and measure at the inflection point. Among the methods, it is distinguished for its ease of implementation for a series of power stacks. However, the bond-wire lift-off detection in ZTC for the high-current modules in the experiment is feasible when more than half of the chip's bond-wires are detached. On the other hand, the high-power IGBT modules may offer redundancy due to their high number of bond-wires in parallel compared to the discrete devices. Regarding the reference temperature measurement, a temperature sensor can be attached to the water inlet to measure steady state temperature, if not already available in the power stack as water temperature sensor or as integrated sensor on the module's baseplate.

VI. CONCLUSION

This paper presented a method for the integrity assessment of industrially produced, water-cooled IGBT power stacks. This method exhibits advantages, such as V_{ce} fast calibration without the need for IGBT unmounting; it requires no power stack modifications and is applied with only a fixed duty cycle pattern. The method can be employed not only for aging monitoring during service stops but also for the validation of the power stack in terms of manufacturing quality and thermal performance in the factory-acceptance phase. The experimental results demonstrated that the insufficient application of thermal paste can cause up to two times higher junction temperature rise

that can be easily detected. Furthermore, the sensitivity analysis has shown that a cooling-water temperature variation of 20 °C causes a considerable deviation of 5% on the estimation of the thermal resistance value and, hence, affects the detection of solder delamination. With the sensitivity analysis of $V_{\rm ce}$ in ZTC for high-current modules, it is demonstrated that the $V_{\rm ce}$ measurement does not have to be carried out exactly at the inflection point. The effect of junction and ambient temperature on $V_{\rm ce}$ is not significant in the extended ZTC operating region. However, in ZTC for high-current modules, the detection of bond-wire lift-off is possible when more than half of a chip's bond-wires have failed. Finally, in case of power leads temperature variations of over 30 °C during testing, a correction is required in the $V_{\rm ce}$ measurement in ZTC to compensate for the change in the power leads voltage drop.

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