Deep Integration Antenna Array: Design Philosophy and Principles

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Abstract—An active integrated antenna array is designed through a new design flow called Deep Integration. Amplifier output currents are combined to synthesize the optimal antenna current distribution to produce the desired radiation characteristics. The electromagnetic field from a cluster of amplifiers is power-combined in low-loss (air) dielectrics inside a single antenna element to increase the total radiated output power. These elements can be combined in an array to further increase radiated power. Such solutions are highly compact in size and capable of delivering high Effective Radiated Power (ERP), which is particularly important in the area of mm-wave integrated circuit design for wireless applications. A simulation example is provided of a Deep Integration antenna array, demonstrating the design philosophy and principles.

Index Terms—deep integration, active integrated antennas.

I. Introduction

A standard link budget analysis of a wireless communication system reveals that higher data rates can be reached if either or both the frequency bandwidth and signal to noise ratio are increased. Increasing the bandwidth is trivial at higher millimeter-wave frequencies, as abundant unlicensed spectrum is available. However, generating a high output power at these frequencies using inexpensive circuit technology is challenging. Resistive losses increase with frequency and those generated in active devices may require active cooling, increasing operational costs. Therefore high-efficiency transmitters are highly desirable. Additionally, the free space path loss increases with frequency, which severely limits the achievable communication distance. One must therefore use high gain antennas or array antennas as used in e.g. Massive MIMO.

The challenge is to design active antennas generating high Effective Radiated Power (ERP) at mm-wave frequencies that can operate in an energy-efficient manner. Furthermore, a highly integrated wireless system solution is necessary that is compact in size (small foot print), potentially inexpensive and compatible with mainstream integrated circuit (IC) technologies.

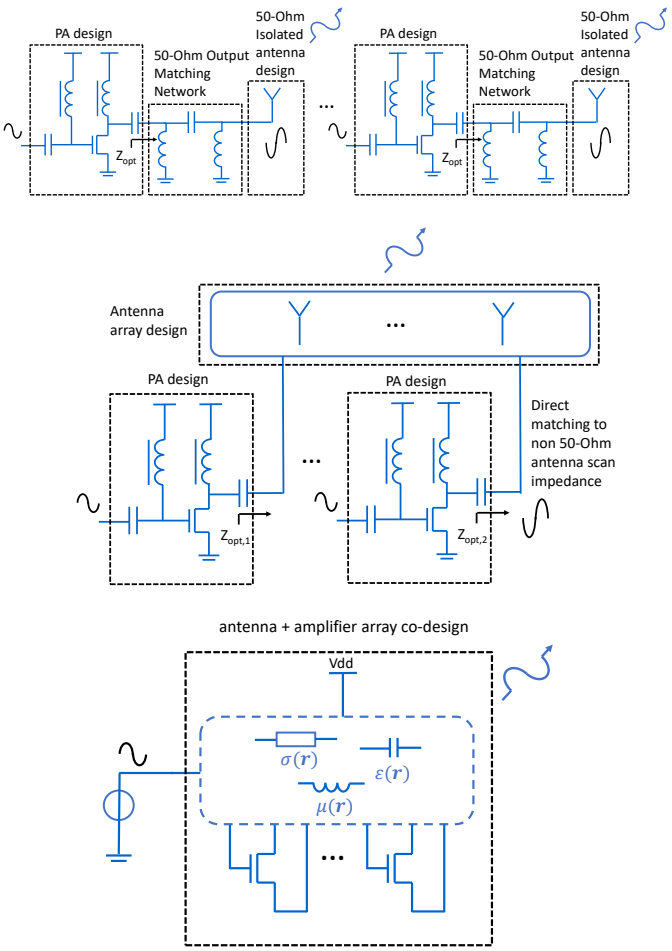


Fig. 1. (top) Textbook example: isolated antennas matched to PAs through impedance matching networks; (middle) Active integrated antennas: direct impedance match of amplifiers to the scan impedance of mutually-coupled antenna array elements, and; (bottom) Deep integration – a new material synthesis concept: joint antenna-circuit design by merging nonlinear semiconductor devices with linear passives.

II. Deep Integration and Related Work

It may be possible to solve the above challenges through a new design flow which is called Deep Integration. The concept has been introduced for the first time in [1]. The evolution of the idea is illustrated in Fig. 1(a)–(c). The array antennas in Fig. 1(a) are designed in isolation of each other for a standard reference impedance (e.g. 50-Ohm) and each antenna is matched to the optimal load impedance Z_{opt} of a single-stage power amplifier (PA).

This is a classical textbook example.

Fig. 1(b) represents a strongly integrated solution [2]. The antenna mutual coupling must be taken into account while the PAs are impedance-matched – in this case directly – to the so-called scan impedance of each antenna array element. Since each scan impedance depends on the array excitation coefficients, the load as seen by the corresponding PA will change (load modulation). The change in load affects the gain, output power and efficiency of each nonlinear PA. The co-design challenge becomes much harder but is likely more compact and potentially more optimal overall than the standard solution in Fig. 1(a).

Finally, in Fig. 1(c), the antenna array and the PAs are merged into a single medium. This represents the case of Deep Integration. The passive part of the medium provides the DC biasing, the passives, the transistor extrinsic parasitics, and the antenna functionality, generally modeled through an in inhomogeneous material distribution (e.g. realized in the Back-End-of-Line of an IC). The nonlinear part of the medium consists in this case only of semiconductor transistors (FETs) along with their possible intrinsic nonlinear parasitics. The material distribution must be synthesized such that the PA and antenna performance are jointly optimal. A possible design flow is discussed in [3]. It is evident that, if the passive medium is removed the antenna functionality is severely affected. Also, the external transistor parasitics making up the PAs get affected, so that the PA performance changes drastically as well. Likewise, if the transistors are removed, the currents through the radiating medium will affect the antenna currents and thereby the antenna radiation characteristics.

Deep Integration is arguably the most ultimate form of integration but constitutes also the most challenging problem. If solved, it may provide extremely compact and potentially inexpensive integrated antenna-circuit solutions.

Similar solutions have been considered in the literature. Starting from the early 2000s, so-called 'integrated circuit-antenna modules' where discussed in [4] as an umbrella term for a large class of circuit-antenna realizations. Arrays of amplifiers located in a spatially distributed EM field to directly amplify the field mode and power-split and -combine it quasi-optically through lenses was discussed in [5] and referred to as grid amplifiers. More recently, a technique very similar to Deep Integration has been presented in [6]. The inverse design approach as presented in [6] is similar to the one in [1]. The authors of [6] propose to synthesize fundamental and harmonic surface currents in silicon and also showcase a 282 GHz beam-scanning array in 45-nm SOI CMOS.

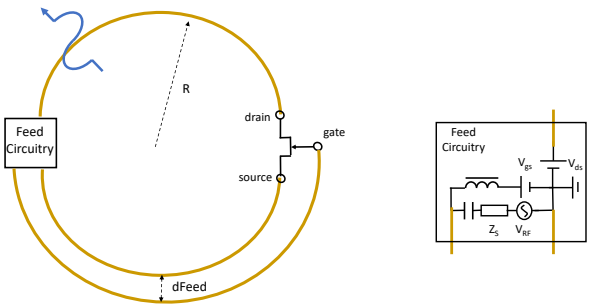
Another strongly related branch of implementations are the in- or on-antenna power-combining methods [7], [8]. Each antenna is then fed by multiple amplifiers that are strongly coupled at their outputs through the multiport single antenna. One specific realization exploiting the resulting load modulation effects is the so-termed Doherty transmitter reaching 53% power-added-efficiency from 1.95–2.10 GHz at the peak output power level [9].

The next section describes a simulation example of a Deeply Integrated antenna array. It is based on an example shown in [10], but with an improved feeding network at the gate of the FET. Conclusions and future work are discussed thereafter.

III. Deeply Integrated Antenna Array Example

A. Single active loop antenna

Consider the loop antenna in Fig. 2 with an integrated semiconductor device.

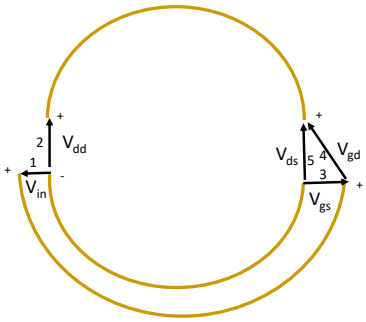


(a) (b)

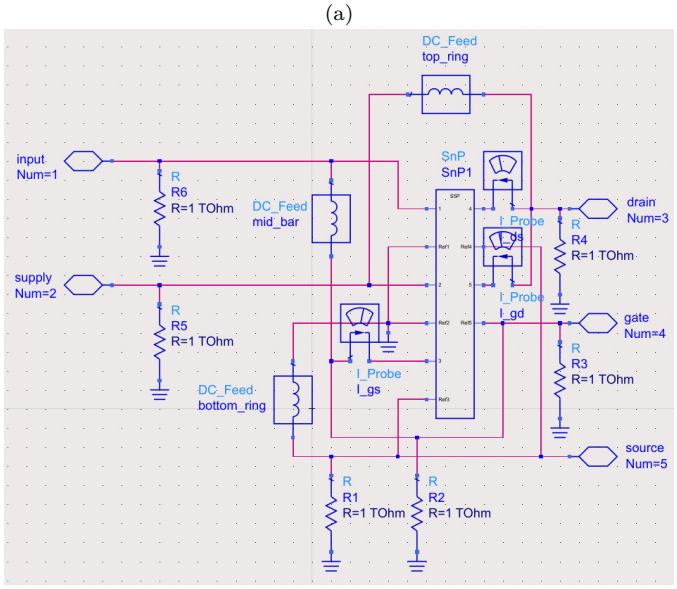
Fig. 2. (a) Perfect Electrically Conducting (PEC) loop antenna spaced $\lambda/4$ above an infinitely large PEC ground plane, and; (b) The DC and RF feeding circuit (bias-T)

For this experiment we considered the Qorvo TGF2942 GaN FET of which nonlinear models from Modelithics [11] are available in Keysights' ADS software. Note that the transistor is floating, as there is no need for a local ground connection. Nevertheless, it is properly DC-biased for Class-AB operation via the antenna and feed conductors. A 3 GHz RF signal is injected into the system using a bias-T network as shown in Fig. 2(b). The passive medium (i.e. metal conductor with wire diameter 1 mm) has the merged functions of the antenna, DC-biasing network and matching network for the PA transistor at RF frequencies. No lumped matching network is required during the joint antenna-PA optimization; instead, the passive medium will be modified to simultaneously affect the RF performance of both the antenna and the PA. In our case, we have used an of-the-shelve commercial transistor. We cannot modify this transistor so we cannot benefit from the extra degree-of-freedom we ideally would have had.

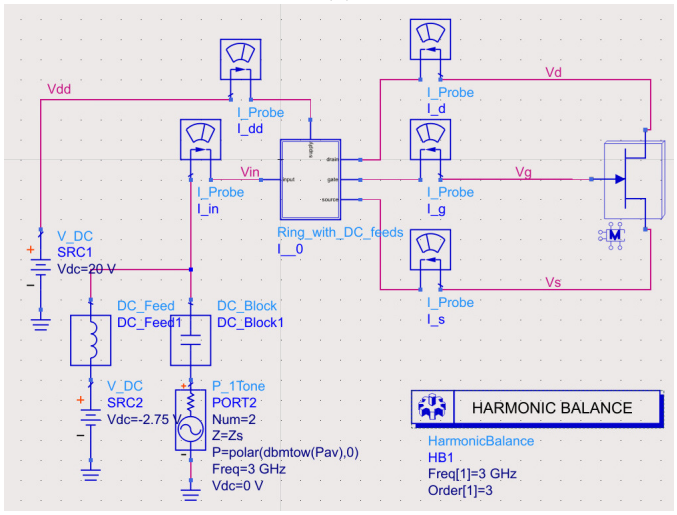
Figure 3(a) shows the enumeration and the lumped port definitions in CST. The S-parameter matrix is exported at DC (0 Hz), the fundamental frequency (3 GHz), and at the second and third harmonics. The 5-port S-parameter matrix at these frequencies has been imported in ADS



(a)



(b)

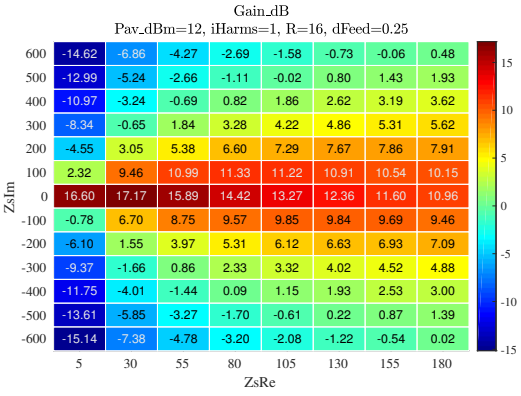


(c)

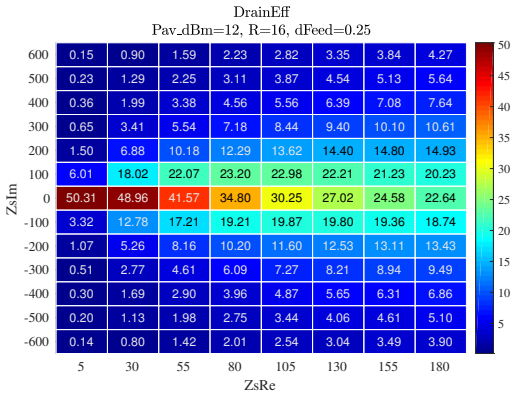
Fig. 3. (a) CST lumped port definitions; (b) ADS-imported 5-port S-parameter block with added wiring and loading for DC stabilization, and; (c) ADS model (top-level) showing the DC-biasing and RF-feeding circuits and commercial GaN transistor.

where the pin-out in Fig. 3(b) has been re-defined. Note how the pin numbers 1–5 indicate the + polarities of the lumped ports in Fig. 3(a) while the - polarities are the corresponding reference pins. Some of these polarities are shared and must therefore be interconnected in accordance with Fig. 3(a). The circuit includes additional DC-feeds and loads to assist DC-convergence for the ADS Harmonic Balance simulations. The pin-out is changed to have a 'clean' top-level design in ADS as shown in Fig. 3(c) which now has a clear resemblance with the system in Fig. 2.

Following the Qorvo data sheet, we have set the DC gate voltage to -2.75 V to obtain a quiescent DC drain current of around 20 mA (Class-AB). We have swept the antenna radius R in CST, as well as the source impedance $Z_S = \mathrm{ZsRe} + j\mathrm{ZsIm}$ and input power level in ADS. These results are shown in Fig. 4 for $R = 16$ mm (circumference is then 1λ, which gave the best results). The system transducer



(a)



(b)

Fig. 4. Parameter sweep of complex-valued source impedance Z_S (at fundamental frequency only). Gain and drain efficiency are plotted for $P_{av} = 12$ dBm.

gain of the antenna is defined as the ratio of the sum of conducted powers over radiated power.

$$G = \frac{P_{out}}{P_{av}} = \frac{P_{rad}}{P_{av}} = \frac{\frac{1}{2}\sum_{n=1}^{5} \mathrm{Re}\{V_n I_n^*\}}{P_{av}} \qquad (1)$$

where the output power P_{out} equals the radiated power

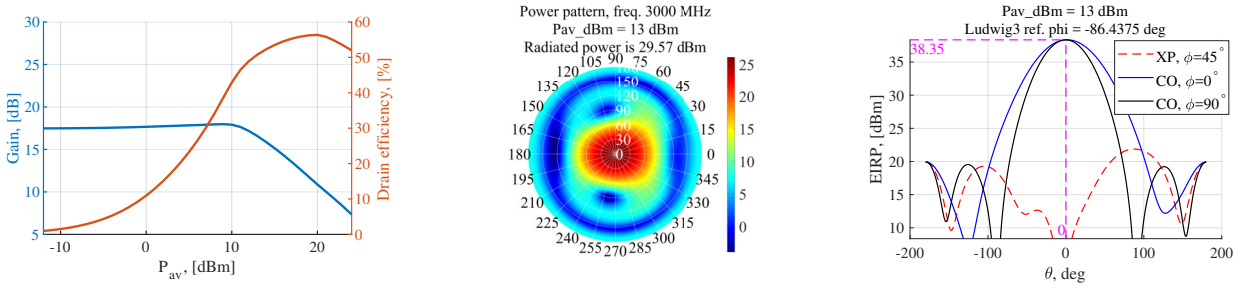


Fig. 5. (a) Drain efficiency and gain compression of the GaN PA inside the loop antenna; (b) 2-D power pattern of the active antenna; (c) E- and H-plane EIRP pattern cuts.

P_{rad} owing to the lossless passive medium (PEC conductors). This power is the total power entering the 5-port at the fundamental frequency only. Upon defining the total DC power consumption as $P_{\text{DC}} = V_{\text{dd}}I_{\text{dd}} + V_{\text{in}}I_{\text{in}}$, the system (drain) efficiency is written as

$$\eta = \frac{P_{\text{out}}}{P_{\text{DC}}}. \tag{2}$$

From the results in Fig. 4 it is concluded that high simultaneous gain and efficiency is obtained for $Z_{\text{S}} = 30\ \Omega$ (@$P_{\text{av}} = +12$ dBm), i.e., $\eta = 49\%$ and $G = 17$ dB.

Accordingly, the source impedance $Z_{\text{S}} = 30\ \Omega$ is fixed and the input power is swept. The corresponding gain and efficiency curves are shown in Fig. 5(a). The -1 dB compression point is at $+13$ dBm, for which a contour plot of the radiated power is shown in Fig. 5(b) and the EIRP pattern cuts in Fig. 5(c). The E- and H-plane beamwidths differ slightly because the radiation of a one wavelength loop antenna resembles that of an electric (folded) dipole. The EIRP is $+38$ dBm, of which $+13$ dBm is the available input power, $+30$ dBm gets radiated (because transducer gain is about 17 dB) and the antenna gain of a one wavelength loop antenna placed $\lambda/4$ above a PEC gnd-plane is indeed about 8 dBi [12].

The load-pull data in the Qorvo datasheet reports a maximum power-added-efficiency of 62.8% and a maximum gain of 22.6 dB at the 3 dB compression level and at 3 GHz. Although our drain efficiency of 49% and transducer gain of 17 dB are lower, they are reached simultaneously and are still high enough to argue that the impedance environment to the transistor inside the antenna is close to optimal, even without additional impedance matching networks.

B. Stacking active loop antennas

To be capable of handling more power one can stack the rings vertically, as indicated in the inset of Fig. 6(a). The inter-loop distance d can be kept as small as $\lambda/20$ and be excited in-phase. This two-loop system will handle twice more power, potentially. However, the strong mutual coupling de-tunes the impedance environment from the optimal one, so that the performance degrades as can be seen in Fig. 6(a) and (c). Additional impedance matching is needed to improve the performance. We have used lumped components to do so which must later on be realized in a distributed manner by an antenna re-design; a 846 pH and 1.23 pF parallel LC-resonator at the gate was used, as well as a 11.7 nH series drain inductor. After impedance matching, the performance is as good as in Fig. 6(b) and (c), which surpasses that of the single loop. Apparently the active impedance environment for both loops simultaneously excited in-phase and equi-amplitude is closer to the optimal one. It is difficult to break down why, which is a disadvantage of the Deep Integration paradigm, because the subsystems get merged and a global optimization is performed numerically.

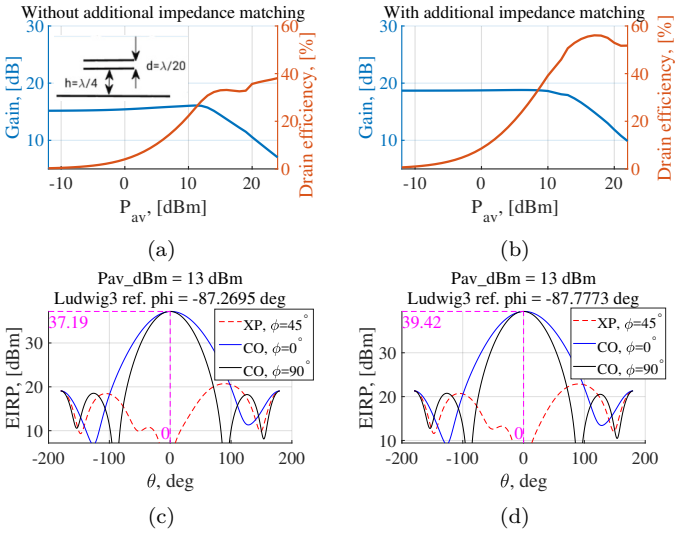
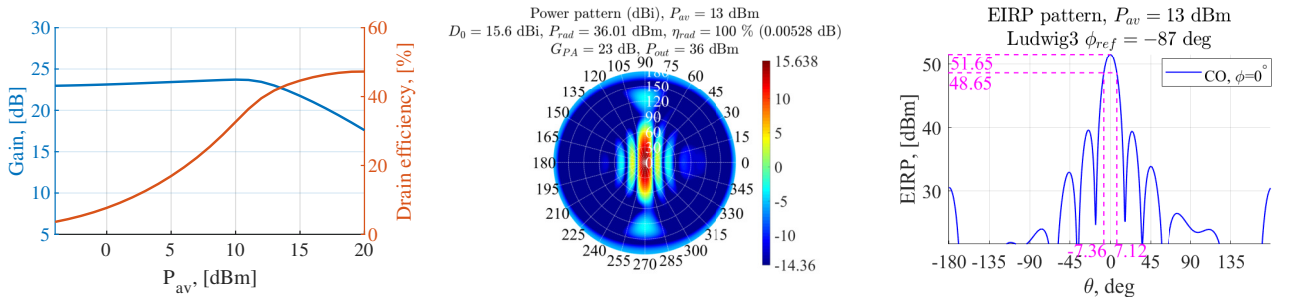


Fig. 6. Gain, drain efficiency, and E- and H-plane EIRP pattern cuts. Without and with lumped matching components (left- and right-hand-side column, respectively).

C. 5×1 array of active loop antennas

An array of five loop antennas in the xy-plane, aligned along the x-axis (H-plane), with a pitch of 0.7λ has been simulated in CST. The simulation results are shown in Fig. 7. In in Fig. 7(a), one observes that the drain efficiency



(a) (b) (c)

Fig. 7. 5×1 active antenna array, on-axis scan: (a) Drain efficiency and gain compression of a single PA connected to an array element; (b) 2D Power pattern of array; (c) On-axis radiated power of array (H-plane cut).

is barely compromised relative to Fig. 5(a). In Fig. 7(b) the 2-D power pattern is shown in a contour plot. The total radiated power is +36 dBm for $P_{\text{av}} = +13$ dBm per PA-antenna combination. The array gain/directivity is 15.6 dBi and the total gain of the combined PAs is 23 dB. Finally, the EIRP for the co-component in the on-axis direction is +52 dBm and is shown in Fig. 7(c) for the H-plane cut. The major axis of the polarization vector is aligned along $\phi = 87$ degrees (90 degrees is ideal).

IV. Conclusion & Future Work

GaN PA transistors have been integrated inside a loop antenna array. The geometry of a single loop antenna is optimized to closely match the optimal load and source impedances of the transistor — no additional lumped matching circuit is necessary. The RF excitation and DC bias are supplied elsewhere in the loop to excite the antenna-PA combination. Compared to the single active loop antenna, the performance of a 5×1 array of active loops is as expected. We achieved a +52 dBm EIRP in the on-axis direction with a total PA drain efficiency of 42% at 3 GHz.

Deep Integration is arguably the ultimate integration but constitutes also the most challenging problems. If solved, it may provide extremely compact and potentially inexpensive integrated antenna-circuit solutions. A challenge with Deep Integration is with the troubleshooting of these highly integrated optimized antenna-circuit modules.

Future work could be to prototype this Deep Integration structure in PCB technology, and to confirm the performance by measurements for a specific wireless application.

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