Effects of self-heating on high-frequency performance of graphene field-effect transistors

Marlene Bonmann[1], Marijana Krivic[1], Muhammad Asad[1], Xinxin Yang[1], Andrei Vorobiev[1], Jan Stake[1], Luca Banszerus[2], Christoph Stampfer[2], Martin Otto[3], Daniel Neumaier[3]

[1]*Terahertz and Millimetre Wave Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Gothenburg, Sweden,*
[2]*2nd Institute of Physics, RWTH Aachen University, 52074 Aachen, Germany,*
[3]*Advanced Microelectronic Center Aachen, AMO GmbH, 52074, Aachen, Germany*

In this work, we study the effects of self-heating (Joule heating) on the performance of graphene field-effect transistors (GFETs) with high extrinsic transit frequency (f_t) and maximum frequency of oscillation (f_{max}) [1]. It has been shown, that self-heating in the GFETs might be significant and lead to degradation of the output characteristics with potential effects on the f_t and f_{max} [2,3,4]. Due to relatively short gate length of 0.5 µm in the GFETs, used in this work, the local channel temperature cannot be accurately estimated by means of the infrared microscopy. Therefore, we applied the method of thermosensitive electrical parameters [5]. In particular, we analysed the gate and drain currents in response to variations of the external heater temperature and dc power (Fig. 1). The analysis allows for estimation of the thermal resistance, which is, for GFETs on SiO_2/Si substrates, approx. $2 \cdot 10^4$ K/W, and in good agreement with that calculated by the model based on the solution of Laplace's equation [6]. In turn, the known thermal resistance allows for evaluation of the GFET channel self-heating temperature. Fig. 2 shows the f_{max} versus dc power (P_{diss}) at different external heater temperatures. The self-heating temperature at P_{diss} =10 mW is approx. 130 °C. The drop in the f_{max} at higher P_{diss} can be fully explained by self-heating. Apparently, one can expect reduced self-heating effects in the GFETs on higher thermal conductive substrates as hBN or SiC.

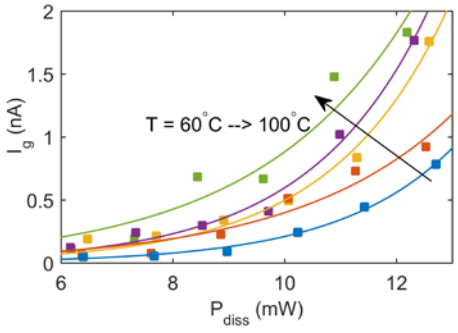

Fig. 1. The gate current, I_g, vs dc power, P_{diss}, of GFETs on SiO_2/Si substrates at different external heater temperatures in the range 60-100 °C and gate voltage V_g = 0.5 V.

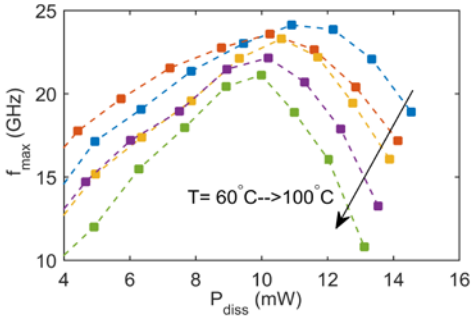

Fig. 2. The measured (extrinsic) maximum frequency of oscillation, f_{max}, vs dc power, P_{diss}, of GFETs on SiO_2/Si substrates at different external heater temperatures in the range 60-100 °C and gate voltage V_g = -1 V.

References

[1] M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, and J. Stake, IEEE Electron Device Lett., 40, 131 (2019).
[2] M.-H. Bae, S. Islam, V. E. Dorgan, and E. Pop, ACSNano, 5 (10), (2011).
[3] S. Islam, Z. Li, V. E. Dorgan, M.-H. Bae, and E. Pop, IEEE Electron Device Lett., 34 (2), (2013).
[4] F. Schwierz, Proceedings of the IEEE, 101 (7), 1567 (2013).
[5] L. Dupont, Y. Avenas, and P.-O. Jeannin, IEEE T. Ind. Appl., 40 (4), (2013).
[6] A. Darwish, A. J. Bayba, and H. A. Hung, IEEE T Electron Dev., 62 (3), (2015).