Thesis for the Degree of Licentiate of Engineering

Graphene field-effect transistors for high frequency applications

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Gothenburg, Sweden 2019

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ISSN 1652-0769
Technical report MC2-423

Printed by Chalmers Reproservice
Gothenburg, Sweden October 2019

Abstract

Rapid development of wireless and internet communications requires development of new generation high frequency electronics based on new device concepts and new materials. The very high intrinsic velocity of charge carriers in graphene makes it promising new channel material for high frequency electronics.

In this thesis, the graphene field-effect transistors (GFETs) are fabricated using chemical vapor deposition (CVD) graphene and investigated for high frequency electronics applications. The characterization and simulation of high frequency performance of the state-of-the-art GFETs devices are given. A modified fabrication process is used. This allows for preserving intrinsic graphene properties in the GFET channel and, simultaneously, achieving extremely low graphene/metal contact resistance. As a result, GFETs with state-of-the-art high frequency performance were fabricated and used in further analysis for development of GFETs with continuously improved performance.

In particular, the dependencies between the material quality and the high-field high-frequency performance of GFETs fabricated on Si chip have been studied. It was shown, that the low-field carrier mobility can be selected as the material quality parameter. The high-frequency performance of GFETs is characterized by f_{T} and f_{max}. The surface distribution of the graphene/dielectric material quality across the chip has been exploited as a tool to study the dependencies of GFET high-frequency performance on the material quality. The f_{T} and f_{max} increase in the range of 20-40 GHz with low-field mobility in the range of 600-2000 cm^2/Vs. The dependencies are analyzed by combining the models of the drain resistance, carrier velocity, saturation velocity and small-signal equivalent circuit. Additionally, this allows for clarifying the effects of the equivalent-circuit parameters, such as contact resistance (R_{c}), transconductance (g_{m}) and differential drain conductance (g_{ds}), on the f_{T} and f_{max}. The observed variations of f_{T} and f_{max} are mainly governed by corresponding variations of g_{m} and g_{ds}. Analysis allows for identifying a most promising approach for improving the GFET high-frequency performance, which is selection of adjacent dielectric materials with optical phonon energy higher than that of SiO_2, resulting in higher saturation velocity and, hence, higher f_{T} and f_{max}.

Keywords: Graphene, field-effect transistors, high frequency, transit frequency, maximum frequency of oscillation, microwave electronics, contact resistance, transconductance

List of publications

Appended papers

This thesis is based on the following papers:

[A] M. Asad, M. Bonmann, X. Yang, A. Vorobiev, K. Jeppson, L. Banszerus, M. Otto, C. Stampfer, D. Neumaier and J. Stake, "The dependence of the high-frequency performance of graphene field-effect transistors on material quality", Submitted to *2D Materials*, October 2019.

[B] M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier and J. Stake, "Graphene field-effect transistors with high extrinsic f_{T} and f_{max}", *IEEE Electron Device Letters*, Vol. 40, no. 1, pp. 131-134, January 2019.

[C] M. Asad, M. Bonmann, X. Yang, A. Vorobiev, J. Stake, L. Banszerus, C. Stampfer, M. Otto and D. Neumaier, "Correlation between material quality and high frequency performance of graphene field-effect transistors", *Graphene Week* 2019, Helsinki, Finland.

Other papers and publications

The content of the following publications partially overlaps with the appended papers or is out of the scope of this thesis.

[a] M. Asad, M. Bonmann, X. Yang, A. Vorobiev, J. Stake, L. Banszerus, C. Stampfer, M. Otto and D. Neumaier, "Graphene field-effect transistors for high frequency applications", in Swedish Microwave Days, Lund, Sweden, 2018.

[b] M. Asad, M. Bonmann, X. Yang, A. Vorobiev, J. Stake, L. Banszerus, C. Stampfer, M. Otto and D. Neumaier, "Graphene field-effect transistors for high frequency applications", in Graphene Week 2018, San Sebastian, Spain, 2019.

[c] A. Vorobiev, M. Bonmann, M. Asad, X. Yang, J. Stake, L. Banszerus, C. Stampfer, M. Otto and D. Neumaier, "Graphene Field-Effect Transistors for Millimeter Wave Amplifiers", *in IRMMW-THz 2019*, Paris, France, 2019, to be published in *Proceedings of the IEEE*.

[d] M. Asad, G. Badawy, H. Zhao Ternehall, M. Sadeghi and S. Wang, "Effect of nano-apertures pattern on InAs nanowires evolution process grown by selective area molecular beam epitaxy", in Compound Semiconductor Week2017, Germany, 2016.

[e] M. Asad, G. Badawy, H. Zhao Ternehall, M. Sadeghi and S. Wang, "Probing the growth mechanism of InAs nanowires grown by using selective area molecular beam epitaxy", in China national MBE conference 2017, China, 2017.

Notation and abbreviations

Notation

C_g	Gate capacitance
C_{ds}	Drain-source capacitance
C_{gd}	Gate-drain capacitance
C_{ox}	Gate oxide capacitance per unit area
E	Energy
E_F	Fermi energy
E_g	Band gap energy
E_{int}	Intrinsic field
E	Applied electric field
f_{max}	Extrinsic maximum frequency of oscillation
f_T	Extrinsic transit frequency
$f_{max-int}$	Intrinsic maximum frequency of oscillation
f_{T-int}	Intrinsic transit frequency
h	Planck's constant
h_{21}	Current gain
$\hbar$	Reduced Planck's constant
j_{ds}	Drain to source current density
k_B	Boltzmann's constant
L_d	Drain conductance
L_g	Gate length
L_{acc}	Access length
m^*	Carrier effective mass
μ_0	Low field mobility
n	Electron carrier concentration
n_0	Residual carrier concentration
$n_{m,doping}$	Metal induced doping concentration
n_{mg}	Carrier concentration in graphene under the metal
p	Hole concentration
q	Elementary charge
R	Resistance
R_c	Contact resistance
R_{mg}	Metal/graphene junction resistance

R_{ung}	Ungated contact resistance
R_D	Drain parasitic resistance
R_{ds}	Drain to source channel resistance
R_G	Gate resistance
R_i	Intrinsic gate source resistance
R_{pd}	Drain pad resistance
R_{pg}	Gate pad resistance
R_S	Source parasitic resistance
R_{sh}	Sheet resistance
R^g_{sh}	Graphene sheet resistance
ρ_c	Specific width contact resistivity
σ_c	Conductivity
σ_{min}	Minimum conductivity
τ	Scattering time
U	Mason's unilateral gain
V_{Dirac}	Dirac voltage
V_{ds}	Drain to source voltage
V_{gs}	Top gate source voltage
v_{drift}	Drift carrier velocity
v_F	Fermi velocity
V_g	Gate voltage
v_{sat}	Saturation velocity
W_g	Gate width

Abbreviations

Al_2O_3	Aluminum oxide
Al	Aluminum
Au	Gold
Cu	Copper
CVD	Chemical vapor deposition
FET	Field-effect transistor
FWHM	Full width at half maximum
GaAs	Gallium arsenide
GFET	Graphene field-effect transistor
hBN	Hexagonal boron nitride
HEMT	High electron mobility transistor
HBT	Heterojunction bipolar transistor
InP	Indium phosphide
LNA	Low noise amplifier
MESFET	Metal-semiconductor field-effect transistor
Ni	Nickel
Pd	Palladium
Pt	Platinum
RF	Radio frequency
SEM	Scanning electron microscope

SiO_2	Silicon dioxide
$SrTiO_3$	Strontium titanate
TLM	Transfer length method
Si	Silicon

Contents

Chapter 1

Introduction

Ever since the very first field-effect transistor was fabricated by Shockley and Morgan in the Bell Labs [1], it brought revolution in semiconductor electronic technology. Transistors are the basis of all electronic equipment that is the part of our routine life, including computers, radios, mobile phones, displays, sensors and even more. Continuous effort on scaling down the transistors to miniaturize the electronic equipment for the ease of consumers, resulted in new device concepts like laptops, tablets, smart phones and other handheld devices. The number of users of wireless devices increases over the years. According to recent statistics, the number of mobile users worldwide at the end of 2020 will reach 5 billion, which means billion of devices connected through internet and exchanging vast amounts of information in the form of text messages, pictures and videos with very high data rates [2]. With the current 4G technology, today's wireless networks operate at hundreds to thousands of Mbit/sec. In the coming 5G-6G revolution, it is expected to connect billions of more devices through internet and wireless connections which operate at multi-Gbit/sec [3, 4]. All these advancements in wireless communications put pressure on analog/radio frequency (RF) components to increase their efficiency and the bandwidth. To cope with increasingly high data rates, it is necessary to develop analog frontends of communication systems with high speed transistors operating in millimeter wave bands and allowing for multi-gigabit data rates.

Up till now, the RF electronics industry demands have been fulfilled by Si-based transistors such as Si metal–oxide–semiconductor field-effect transistors (MOSFETs), SiGe heterojunction bipolar transistors (HBTs) and III-V compound metal-semiconductor field-effect transistors (MESFETs) and high electron mobility transistors (HEMTs) [5, 6]. A general problem with current Si MOSFET and III-V HEMT technology is the continuous scaling down to meet the industrial demands, where field-effect transistors (FETs) have already reached the best performance and no further significant improvement in performance can be expected in future. For instance, InP HEMT showed its best performance a decade ago for sub 50 nm gate length with transit frequency (f_{T}) up to 680 GHz and maximum frequency of oscillation (f_{max}) upto 1 THz. Since then, no significant improvements have been demonstrated [7, 8]. The reason is that the continuous downscaling leads to extremely short gates,

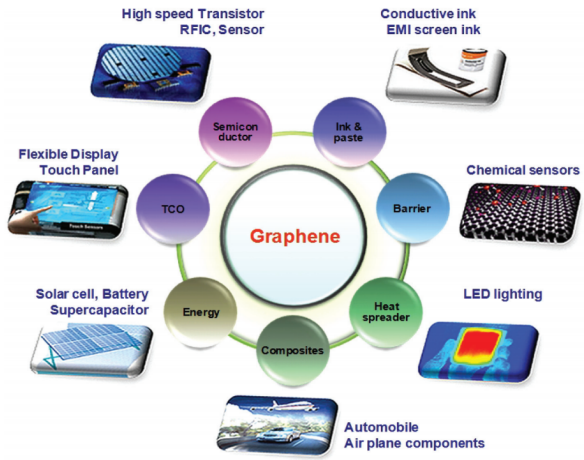

Figure 1.1: Scope of graphene in different research sectors [17].

very thin gate dielectric, extremely thin channel thickness with corresponding problems, such as short channel effects, low breakdown voltage, low operating voltage, large surface scattering and threshold voltage variations [5, 6, 9, 10]. In addition to that, the HEMT technology is not very cost effective and limited to a few expensive applications, and the same is true for SiGe HBT [11, 12].

To continue progress in RF electronics, it requires extremely small dimensions and new material concepts. To begin with, the 2D material graphene is considered as a very promising new channel material for the next generation of FETs for advanced high frequency applications. Graphene was first demonstrated by Andre Geim and Konstantin Novoselov in 2004 via separation from graphite by mechanical exfoliation [13, 14]. The interesting feature of graphene is that, by applying the gate field, one can tune the carriers density and therefore, the current density. Transistors for high speed/high frequency applications require fast charge carriers in the channel, which can react quickly to an applied electric field. Graphene has exceptional charge carriers properties with mobility over $1 \times 10^5 \mathrm{cm}^2/Vs$ at room temperature, which is 100 times higher than that of Si, and charge carrier saturation velocity $6 \times 10^5 \mathrm{cm}/s$, which is 6 times higher than that of Si [15, 16]. With these exciting features, graphene is a strong candidate for future RF electronics. Over the years, scientists explore many graphene applications in different areas as shown in figure 1.1 [17].

Examples of potential applications of graphene field-effect transistors (GFETs) in high frequency electronics include amplifiers, subharmonic mixers, detectors, frequency multipliers and oscillators [18–21]. For these applications, graphene can be obtained by different technologies including peeling off from graphite, CVD and epitaxialy grown graphene. To fabricate devices, it requires transferring the graphene onto a dielectric substrate, which usually deteriorates the graphene transport properties and, hence, the GFET's performance. The high frequency performance of the FETs is usually characterized by the transit frequency f_{T} and maximum frequency of oscillation f_{max}, defined as the frequencies at which current gain and unilateral power gain drop to unity,

respectively. It has been predicted that both f_{T} and f_{max} depends on the material quality of the graphene and adjacent dielectrics. The extrinsic f_{T} and f_{max} state-of-art of GFETs in comparison with those of conventional Si-MOSFETs are shown in paper [B]. It can be seen that, now, the high frequency performance of the GFETs is comparable or even better than that of the best published Si MOSFETs and also shows promising scaling down behavior. However, extrinsic f_{T} and f_{max} of the GFETs are still limited by a number of extrinsic factors associated, in particular, with the presence of impurities and defects originating from the fabrication processes and the use of unfavorable substrate dielectric materials. The limitations prevent taking full advantage of the graphene intrinsic properties and realizing highly competitive high frequency GFETs.

Approaches for minimizing the extrinsic limitations and, hence, improving the high frequency GFET performance have been proposed, in particular, preserving the intrinsic graphene properties by sandwiching/encapsulating it between dielectric layers, e.g. hexagonal boron nitride (hBN) or aluminum oxide (Al_2O_3) [22]. Also, reducing the parasitic contact resistance by using clean metal/graphene interfaces and edge contacts has been considered. Furthermore, the contact resistance of the ungated regions can be eliminated by using the fabrication concept of self-aligned T-shape gates [23]. In this thesis, we used a modified fabrication process to address all the issues/challenges mentioned above and improve the high frequency GFET performance. Encapsulation of graphene by the gate dielectric layer at the first stages of the fabrication flow allows protecting the graphene from the further processing steps, and, hence, allows high quality graphene. It also allows for reducing the source drain contact resistance. As a result, we obtained record high extrinsic f_{T} and f_{max} performance values, which are discussed in details in paper [B].

A crucial issue, associated with effect of the graphene/dielectric material imperfections, is the spatial inhomogeneity of the graphene properties over the substrate surface. It is critical not only with regard to GFET performance, but also reliability and reproducibility of the parameters during wafer scale production. In paper [A], we present the results of a study of the dependence between the material quality and the high-field high-frequency performance of GFETs fabricated on a silicon chip. By combining the models of the drain resistance, carrier velocity, saturation velocity and small-signal equivalent circuit, we were able to analyse the dependence between material quality and high-frequency performance. Additionally, this allows for clarifying the effects of the equivalent-circuit parameters, such as contact resistance (R_{c}), transconductance (g_{m}) and differential drain conductance (g_{ds}), on the high-frequency performance of GFETs.

The thesis outline is, in chapter 2, graphene's electronic properties relevant for applications in high frequency field-effect electronics. Chapter 3 describes the basic principle of GFETs operations, fabrication, DC and RF characterization and performance analysis. Chapter 4 presents the results of the study of dependencies between the high-frequency performance of GFETs and the graphene/dielectric material quality. Chapter 5 contains the conclusion, summary, and description of future work.

Chapter 2

Properties of graphene for high frequency electronics

The analog front-ends of advanced communication systems require high speed transistors operating at high frequency and providing large bandwidth. Materials with high mobility and large charge carrier saturation velocity are required to realize such devices. In this context, monolayer graphene is a promising candidate. This chapter describes the basic properties of graphene which makes it qualified for high frequency applications. The unique graphene properties such as V-shaped band structure, charge carrier density and charge carrier transport under low and high electric field will be discussed. It begins with the quote of Nobel laureate Andre Geim: "*Graphene opened up a material world we didn't even know existed.*"

2.1 Crystal structure and electronic band structure

The existence of a single layer of atoms was not consider possible due to the atoms' thermodynamic instability [24], until very recently, when scientists managed to peel off a 2D monolayer of carbon atoms from bulk graphite [13,14]. Sheet of a single layer of carbon atoms as shown in figure 2.1 (a) that are tightly bond into honeycomb-like hexagonal structure was named 'graphene' [25]. Carbon is a material in Group-IV of the periodic table and has four valence electrons in its outermost shell. Carbon atoms have the tendency to form three symmetrical covalent bonds because the $2s$, $2p_x$ and $2p_y$ orbitals can be transformed into three symmetric sp^2 hybrid orbitals with planar symmetry as shown in figure 2.1 (b). Notice that the p_z orbital remains unhybridized. These sp^2-hybridized carbon atoms with triangular planar structure form σ-bonding with neighbour carbon atoms and replicate the process to form a 2D crystal structure earlier defined as graphene sheet. The distance to the nearest neighbor carbon atom is 0.142 nm. The graphene sheet shows strong mechanical strength and very high electrical conductivity. Now the question is: where does this mechanical strength and electrical conductivity come from? The strong σ-bonding's in the planar structure provide the mechanical strength

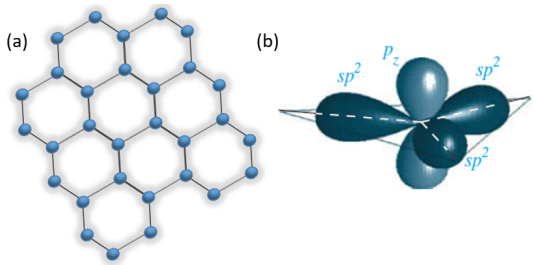

Figure 2.1: (a) The crystal structure of graphite (b) the symmetrical covalent bonding of carbon atoms and the tetrahedral symmetry of sp^3 hybrid orbital [26].

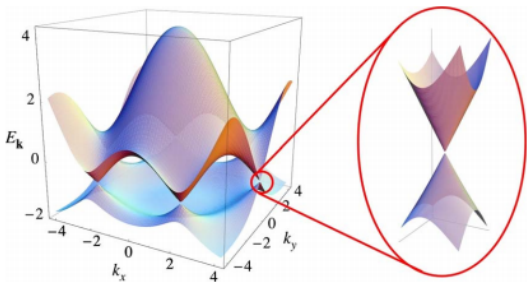

Figure 2.2: Electronic dispersion in the honeycomb graphene lattice mapped using tight-binding approximation. The conductance band touches the valence band at a point named as Dirac points [27].

to the material and the excellent electrical conductivity originates from the remaining unhybridized p_z orbital, which forms much weaker π-bonding with its neighbour atoms. Below, only the electrical properties of graphene will be considered.

2.1.1 Graphene electronic band structure

To understand the electrical properties of graphene, it is important to understand its electronic band structure. Theoretically, the concept of graphene electronic band structure was studied a long time ago in order to explain the properties of graphite. A simplified energy-momentum relation using theoretical argument, the tight-binding approximation for graphene lattice is described by assuming the electrons can jump to the three nearest neighbour atoms as [27]:

$$E(k)^{\pm} = \pm\alpha\sqrt{1 + 4\cos\frac{\sqrt{3}a}{2}k_x\cos\frac{a}{2}k_y + 4\cos^2\frac{a}{2}k_y}, \tag{2.1}$$

Here, α is a fitting parameter and k is the wave vector. The $(+)$ and the $(-)$ signs correspond to conduction and valence bands, respectively. The band structure mapped using (2.1) is shown in figure 2.2. The conduction and valence bands touch at the conjugate K-points called the Dirac points. The Dirac points, also known as charge neutrality points, express a key feature of graphene i.e. zero bandgap nature of monolayer graphene. In conventional semiconductors, the energy and momentum relation involves reduced mass of

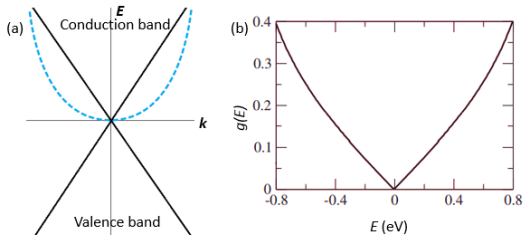

Figure 2.3: (a) Electronic dispersion in convention semiconductor (dashed line) and in graphene (solid line) close to the Dirac point. (b) The graphene density of state close to the Dirac point [27].

the free carriers and can be expressed as:

$$E(k) = \frac{\hbar^2 k^2}{2m^*}$$

Here, $\hbar$ is the Planck's constant, k is a wave vector and m^* is the effective mass of the charge carrier. Both electrons and holes experience different effective mass in a semiconductor, which result in different total energy, thus, holes and electrons behave differently. Zooming in close to the Dirac point in figure 2.2 reveals the highly symmetric nature of the dispersion relation in the vicinity of the Dirac point. Due to the tight-binding approximation, the graphene qausi particles exhibit linear energy dispersion relation. A linear conical dispersion relation in the vicinity of the Dirac point is described in terms of the Fermi velocity (v_F) as:

$$E(k) = \pm\hbar v_F \sqrt{k_x^2 + k_y^2} \tag{2.2}$$

Figure 2.3 shows parabolic relation of E versus k for common semiconductors in comparison with graphene shown by the linear curve. The linear dispersion relation indicates a massless nature of graphene charge carriers. Normally, massless particles like fermions governed by the Dirac equation are described by the Fermi velocity instead of the velocity of light. This means both electrons and holes in graphene exhibit a constant Fermi velocity $v_F = 10^6 m/s$, irrespective in momentum, which indicates the origin of superior carrier mobility in graphene. It further shows that the transport properties of electrons and holes are same in graphene.

2.1.2 Graphene density of states

The density of states is another important aspect of the electronic band structure since it defines the carrier concentration. The density of states (number of states per unit energy interval) in graphene close to the Dirac point is derived from the momentum energy relation as:

$$g(E) = \frac{2|E|}{\pi(\hbar v_f^2)} \tag{2.3}$$

The density of states is zero at zero Fermi energy. Zero density of states make it a semiconductor-like material, while zero bandgap gives graphene a semi-metal

like resemblance. The density of states drived from Eq.(2.3) is shown in figure 2.3 (b). It can be seen that the density of states increases as the Fermi energy level moves away from the charge neutrality point.

2.1.3 Carrier concentration

The charge carrier concentration is defined by the carrier distribution in the valence or conduction band and is given by the density of state times the probability that a state is occupied or empty:

$$n = g(E) \cdot f_f(E) \tag{2.4}$$

Here $f_f(E)$ is the Fermi-Dirac probability function. The carrier concentration for the volume of a given system is obtained by taking the integral of (2.4). Solving the integral of the above equation gives a simple analytical expression relating the charge carrier concentration in graphene directly to the Fermi level:

$$n = \frac{1}{\pi}\left(\frac{E_f}{\hbar v_f}\right) \tag{2.5}$$

2.1.4 Intrinsic and extrinsic carrier concentration

At this stage, it is important to distinguish between intrinsic and extrinsic graphene properties. Graphene can be defined as of an intrinsic nature, when the Fermi energy level lies exactly at the Dirac point, which means no external doping and charge carrier presence in graphene. In such system, at T = 0 K the conduction band is complete empty and the valence band is completely filled, the Fermi level lies at the Dirac point [28]. With this definition in mind, the graphene used in all practical applications is extrinsic in nature. At temperature T > 0, there are thermally generated carriers present at all times in the system. The temperature dependent thermally generated carrier density is given by:

$$n_{th} = \frac{\pi}{6}\left(\frac{k_B T}{\hbar v_f}\right) \tag{2.6}$$

where k_B is the Boltzman constant and v_{F} is the Fermi velocity. In the absence of external doping, one can say that n_{th} is the intrinsic carrier concentration of graphene at a given temperature. When the graphene is transferred onto foreign substrate, usually the charged impurities at the interface surface or in the substrate oxide induce so-called residual charge carrier concentration (n_0) in the graphene channel. One can also make graphene extrinsic via doping by applying positive or negative gate voltage, which makes the graphene channel n-type or p-type, respectively. The net charge carrier concentration in the extrinsic graphene is given as:

$$n = n_0 + n_{th} + \frac{C(V_g - V_{Dir})}{q} \tag{2.7}$$

Here, C is gate capacitance per unit area, V_g is the gate voltage and q is the elementry charge.

2.2 Charge carrier transport

2.2.1 Low field mobility and scattering mechanisms

Mobility is one of the important parameter in the carrier transport mechanisms in materials. Mobility influence the device performance through the charge carrier response to the applied electric field. Charge carrier mobility in any material is fundamental to describe the electrical conductivity, the resistivity and velocity of the charge carrier in that material. As mentioned above, graphene possess extremely high intrinsic mobility of charge carriers. However, due to its 2D nature, graphene is very sensitive to its vicinity and the charge carrier mobility is often limited by different scattering mechanisms associated with substrate and impurities around the graphene sheet. For instance, the very first paper published on graphene to demonstrate field-effect phenomenon in graphene sheet by Novoselov [13], reported the mobility upto $10^4 \mathrm{cm}^2/Vs$ at room temperature. A few years later, it was reported that carrier mobility in graphene can be as high as $1 \times 10^5 \mathrm{cm}^2/Vs$ at room temperature [15] and over $2 \times 10^5 \mathrm{cm}^2/Vs$ at 5 K. The origin of this is effect of the substrate. Novoselov et al. prepared sample on SiO_2 substrate while the mobility over $1 \times 10^5 \mathrm{cm}^2/Vs$ was demonstrated by using suspended single layer graphene. Free standing graphene offers very high quality, where, the mobility is either limited by lattice acoustic phonons scattering at high temperature or by the impurity scattering i.e. the impurities laying at the graphene surface [29–31]. However, the free standing graphene is not viable from the device fabrication point of view. Therefore, graphene is inevitably in contact with foreign material substrate for real electronic applications. As the graphene is transferred to dielectric substrates, its properties drops dramatically. For example, on the SiO_2 substrate, the graphene mobility is an order of magnitude less than that of the suspended graphene [31, 32]. This is because of additional scattering mechanisms such as remote interfacial phonon scattering, charged impurity scattering, scattering by ripples, neutral defect scattering and resonant scattering [33]. Various possible scattering mechanism and their relative contributions to the net mobility can be counted by Matthiessen's rule as [34]:

$$\tau^{-1} = \tau_{cl}^{-1} + \tau_{sr}^{-1} + \tau_{op}^{-1} + \tau_{LA}^{-1} + \tau_{corr}^{-1} \tag{2.8}$$

Here, τ is the scattering time between two scattering events, and the subscript (cl) represents Coulomb scattering i.e. charged impurities, (sr) represents short range scattering i.e. neutral defect, (op) indicates remote optical phonon scattering, (LA) longitudinal acoustic phonons, and (corr) is for corrugations or graphene ripple scattering. All these scattering mechanisms contribute to mobility through the expression [35, 36]

$$\mu = \frac{e v_f^2 \tau}{E} \tag{2.9}$$

where E is electric field. Coulomb scattering is the long range scattering mechanism due to the charged impurities at the interface and in the oxide. Long range scattering is considered to be the main scattering mechanism controlling the carrier transport in graphene FET devices at low carrier density and relatively high concentration of impurities [28]. Short range scattering

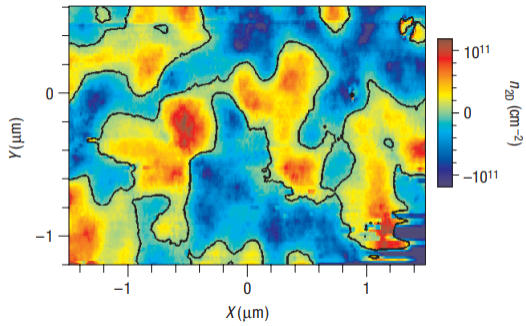

Figure 2.4: Charge carrier density profile measured at the Dirac point [40].

is also present in graphene mainly due to lattice defects. It dominates at high carrier densities and in cleaner samples. Another extrinsic scattering mechanism is the remote optical phonons at low temperature and is inversely proportional to the carrier density simply because higher carriers densities lead to a higher scattering rate [29]. The significant scattering effects can be due to the ripples in graphene and are partially related to the substrate roughness [37]. To bring graphene based technology to a higher level, it is necessary to overcome the limitations of extrinsic scattering mechanisms.

In this context, an endeavor to reach the intrinsic graphene transport properties comes with the valuable addition of the alternate substrate material hexagonal boron nitride (hBN). hBN is a wide bad bandgap material. It has hexagonal lattice symmetry with graphene crystal and has a lattice mismatch of 2 %. With clean hBN encapsulated graphene heterostructure FET devices, room temperature mobility over $1 \times 10^5 \mathrm{cm}^2/Vs$ has been demonstrated [38,39].

2.2.2 Spatial inhomogeneity of graphene quality

Spatial inhomogeneity of graphene quality is responsible for variations in electronic properties and thus the device performance over the wafer surface. One of the main reasons for spatial inhomogeneity in 2D graphene sheet is the randomly distributed charged impurities located in the oxide and at the interfaces. The charged impurities are typically associated with the oxygen vacancies in the adjacent dielectrics and/or water molecules trapped at the graphene/dielectric interfaces [41]. This causes a spatially inhomogeneous random network of two dimensional electron and hole puddles in the graphene as shown in figure 2.4. These laterally inhomogeneous densities of charged impurities have been reported in many studies [30,31,33,35,42]. The inhomogeneous electron and hole puddles define the minimum conductivity, which can be measured at the Dirac point. The spatial inhomogeneity of carrier concentration in the graphene sheet affects the device performance all over the chip. As mentioned earlier, the long range scattering in graphene originates from charged impurities.

Figure 2.5 shows the map of the mean free path of electrons in 2D graphene on SiO_2 in correlation with the surface distribution of charged impurities [35]. The maxima and minima in the mean free path (circled) correspond maxima

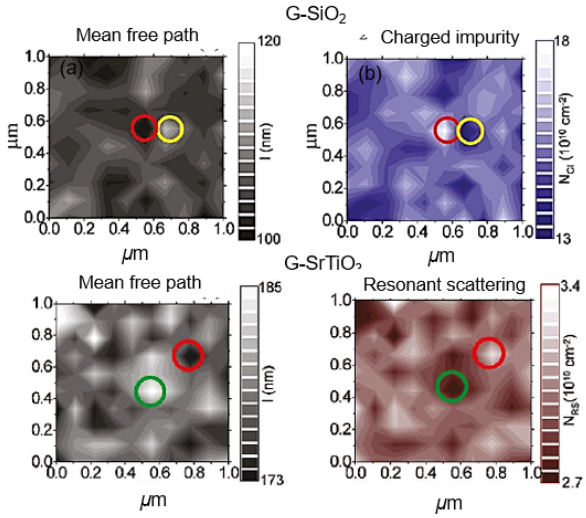

Figure 2.5: (a) Map of mean free path of electrons in graphene on SiO_2 (b) in relation with 2D spatial distributed charged impurities map (c) map of mean free path of electrons in graphene on $SrTiO_3$ and (d) corresponding map of the density of resonant scattering centers [35].

and minima in the charged impurities density map. This suggests that the mean free path depends on charged impurities, which act as scattering centers and effectly reduce the mean free path.

Another possible candidate responsible for surface distribution of material quality is is resonant scattering [43]. Resonant scattering in graphene is usually associated with vacancies and adsorbates like H, OH, and CH_3, C_2H_5, CH_2OH [35, 44]. Figure 2.5 shows the map of the mean free path of electrons in graphene on $SrTiO_3$, in correlation with resonant scattering density map. The relationship between the maxima and minima of mean free path and the minima and maxima of resonant scattering density suggests that resonant scattering source limits the mean free path in addition to charged impurities. In this thesis, the spatial inhomogeneity of material quality is used for study of dependencies between the material quality and high frequency performance of GFETs, which is presented in paper [A].

2.2.3 Transport under high electric field

Up to now, we have discussed low field mobility which can be used as a material quality parameter. At relatively high fields, the charge carrier velocity is a more appropriate parameter. The velocity increases with electric field and at high field the charge carrier velocity becomes insensitive to further increase in applied field, and thus saturates due to inelastic scattering. The saturation of charge carrier velocity causes the current to saturate in the channel, a phenomenon often observed in short channel field-effect devices. Charge carrier

velocity under high electric field is defined as [45, 46]

$$v = \frac{\mu_0 E_{int}}{\sqrt{1 + \left(\frac{\mu_0 E_{int}}{v_{sat}}\right)^2}} \tag{2.10}$$

Here, μ_0 is the low field mobility, v_{sat} is the saturation velocity and E_{int} is the intrinsic electric field along the channel. Saturation velocity can be evaluated using an analytical model which assumes that the saturation velocity is limited by inelastic emission of optical phonons (OPs), and it includes the influence of charge carrier concentration n, temperature and optical phonon energy $\hbar w_{\mathrm{OP}}$ [47, 48]:

$$v_{sat} = \frac{2}{\pi}\frac{w_{OP}}{\sqrt{\pi n}}\sqrt{1 - \frac{w_{OP}^2}{4\pi n v_f^2}}\frac{1}{N_{OP}+1} \tag{2.11}$$

Here, $N_{OP} = 1/[exp(\hbar w_{OP}/kT) + 1]$ is the phonon occupation and n is the charge carrier concentration. High saturation velocity is a critical parameter for high speed devices. For instance, the intrinsic transit frequency of a FET device is defined by the saturation velocity: $f_{\mathrm{T}} \approx v_{sat}/(2\pi L_g)$, where L_g is the channel length. Saturation velocity in graphene is defined by the optical phonon energy $\hbar w_{\mathrm{OP}}$ of graphene and the substrate. The record high saturation velocity measured with graphene devices using hBN substrate is $6 \times 10^5 \mathrm{cm}/s$ [16], which is much higher in comparison with other semiconductors or 2D materials. The saturation velocity for graphene on SiO_2 substrate deteriorates due to its low surface optical phonon energy $\hbar w_{\mathrm{OP}} = 55\ meV$ [47] which in the case of hBN is over 100 meV.

Chapter 3

Graphene field-effect transistors for high frequency electronics

Field-effect transistors transistors are the basic building blocks of all integrated circuits and modern microelectronic devices. This chapter discusses the basic operation of GFETs, design, fabrication, modeling and measurement techniques. The high frequency performance of GFETs will be discussed using analysis of small signal equivalent circuit.

3.1 Basic operation principles of FETs and GFETs

Different types of field-effect transistors have been developed and studied over the years, including insulated-gate FET, heterojunction FET, junction FET, meta/semiconductor FET and the metal insulated/oxide FET [46]. Among the FETs, MOSFETs are widely used in high frequency electronics applications, serving in high frequency circuits as amplifiers, mixers, detectors and modulators etc. They are three-terminal devices, basically consisting of three electrodes-gate, source and drain-as shown in figure 3.1. The charge carriers flow from the source to drain electrode through a conducting channel. The carrier flow is controlled by applying voltage at the gate terminal. The gate is fabricated so as the gate electrode is separated from the channel using dielectric oxide (insulating layer). MOSFETs can be of different categories, for example, depending upon the types of the carriers in the channel, named as n-channel and p-channel MOSFETs. In an n-channel MOSFET, the majority carriers are electrons, while in p-channel MOSFET, the majority carriers in the channel are holes. The type of the carriers in the channel can be modulated by applying a positive or negative bias at the gate terminal.

A relatively new member of the FETs family is the graphene field-effect transistor (GFET) [49]. General operating principles of GFET are similar to that of MOSFET but there are some distinguishing features associated, for example, with zero bandgap in monolayer graphene, which is addressed in more detail below. Graphene is used as a channel material in GFET replacing the

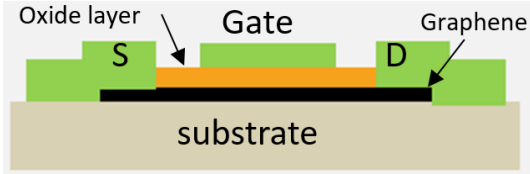

Figure 3.1: Schematic cross-section view of the GFET.

conventional semiconductor. GFETs have been demonstrated in both bottom gate and top gate configurations [13, 49]. In this thesis, we developed and studied GFETs in top gate configuration similar to that shown in the figure 3.1. As mentioned above, employing graphene as a channel material is motivated by its superior intrinsic properties such as extremely high carrier mobility and high saturation velocity. Combination of these properties is a prerequisite for development of a new generation of advanced high frequency electronics circuits. The GFETs can be employed in advanced amplifiers, fundamental/subharmonic frequency mixers, detectors, frequency multipliers and oscillators [20, 50–53]. Recently, we demonstrated GFETs with record high extrinsic transit frequency (f_{T}) 34 GHz and extrinsic maximum frequency of oscillation (f_{max}) 37 GHz, see [paper B].

3.2 Fabrication and material characterization

3.2.1 Graphene synthesis and Raman spectroscopy

Realization of high performance high frequency transistors depends generally on the channel material quality. Graphene for GFET channels can be fabricated by different technologies. Graphene used in earlier graphene devices was obtained by mechanical exfoliation from bulk graphite using scotch tape. Later on, the technique of graphene synthesis on catalyst Cu substrate by chemical vapor deposition (CVD) was demonstrated. Another method is graphene epitaxial growth through sublimation of silicon carbide (SiC) substrate surface.

Mechanical exfoliation

Peeling the graphene from graphite slab with scotch tape was the earliest method of fabrication of graphene for field-effect device experiments [13]. Exfoliated graphene obtained from graphite by far offers the best quality with room temperature mobility over $1 \times 10^5 \mathrm{cm}^2/Vs$ and saturation velocity up to $6 \times 10^5 \mathrm{cm}/s$ [16, 38, 39]. The exfoliated graphene based devices are very useful for fundamental research but wafer scale fabrication using exfoliated graphene is not possible yet.

Epitaxial graphene

Wafer scale graphene synthesis is extremely important for industrial scale fabrication. Epitaxial graphene can be grown via thermal decomposition of SiC by sublimation of Si atoms and the segregation of the carbon atoms at high

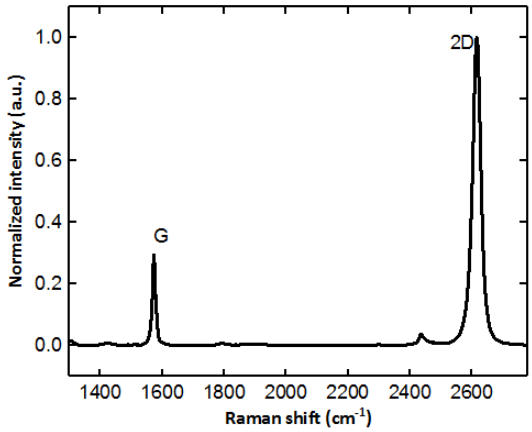

Figure 3.2: A typical Raman spectrum of a monolayer CVD graphene.

temperature in inert environment [54]. Epitaxial graphene has successfully been grown on both Si-face and C-face SiC wafer. The graphene grown on C-face reveals higher charge carrier mobility. This method is more promising for wafer scale fabrication because the graphene is grown directly on the substrate and does not require transfer process, which typically causes a lot of additional imperfections. A drawback of this method is that it is not very cost effective.

CVD graphene

CVD grown graphene is, currently, well developed and widely used, in particular because it is compatible with large scale devices fabrication. In this method, the graphene is grown on a Cu foil using precursors and gas flows. Graphene grown on Cu foil is further transferred onto a substrate for subsequent device processing [55]. Devices reported in this thesis are based on high quality CVD graphene grown and transferred in AMO and Aachen University in Germany. The Hall effect mobility measured in this CVD graphene on SiO_2 substrate is upto 7000 cm^2/Vs. The same group of researchers in Aachen demonstrated that the mobility of hBN encapsulated CVD graphene can be as high as $1 \times 10^5 cm^2/Vs$ [56].

Raman spectroscopy

It was demonstrated that the monolayer and bilayer graphene shows considerably different electron transport properties [25,57]. Additionally, impurities, such as chemical and organic residues, structural defects and other imperfections also modify/degrade the graphene electron transport properties. Therefore, to control the performance of GFET devices, it is important to determine the quality of graphene and identify the number of layers. Raman spectroscopy is a most frequently used method for non-destructive analysis of the graphene quality and number of layers [58, 59]. The basic principle of Raman spectroscopy is as follows. The monochromatic light irradiates the material under test, resulting in inelastic scattering. The scattered light is detected and analyzed. In the

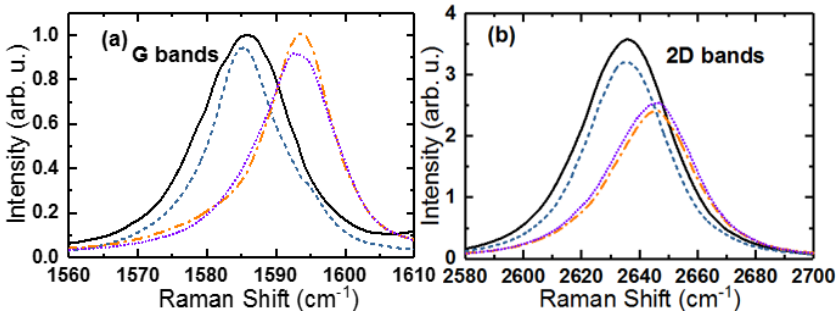

Figure 3.3: Raman spectra of the G bands (a) and 2D bands (b) of graphene as transferred (solid line) and after patterning with Al_2O_3 using MMA-EL6 (dashed line), without Al_2O_3 using PMMA (dashed dotted line), and without Al_2O_3 using MMA-EL6 (dotted line).

measured Raman spectrum, the difference of the wave vector of the incident radiation k_{in} to outgoing wave vector k_{out} is plotted versus intensity. Figure 3.2 shows the Raman spectrum of the monolayer CVD graphene, indicating G and 2D peaks at around 1570 cm^{-1} and 2600 cm^{-1}, respectively. The G peak is associated with the high-frequency E_{2g} phonons and the 2D peak is the result of the process of momentum conservation by two phonons with opposite wave vectors [59]. An additional D peak can also be detected at 1350 cm^{-1} and is associated with structural defects in the graphene (not visible in figure 3.2). The shape, intensity and position of these peaks provide information about the graphene structure and imperfections. For example, the intensity ratio of I_{2D}/I_G along with FWHM and positions of the G and 2D peaks give information about the doping, strain and number of graphene layers present in the sample [58–61]. In this thesis, Raman spectroscopy was used for study of the graphene quality improvement in response to development/modification of fabrication technology (see details below). In particular, analysis of the Raman spectra in figure 3.3 allows for evaluation of the doping effect caused by resist residues and verifying the effective removal of polymer residues in the modified fabrication technique.

To verify the effectiveness of removing the e-beam resist residues in modified fabrication method, the following test samples were prepared on Si/SiO_2 substrates and analyzed using Raman spectroscopy:
i) graphene with Al_2O_3 layer after developing the MMA-EL6 e-beam resist followed by patterning the Al_2O_3 layer, which represents the modified technology;
ii) graphene without Al_2O_3 layer after developing MMA-EL6 and PMMA e-beam resists, which represents the previously developed technology [20, 62];
iii) as-transferred graphene used as a reference.

As can be seen in figure 3.3, the positions and intensities of the G and 2D peaks corresponding to patterning with Al_2O_3 using MMA-EL6 match closely to those of the as-transferred graphene. The positions of the peaks corresponding to patterning without Al_2O_3 using both MMA-EL6 and PMMA are upshifted and intensities of the 2D peaks are reduced. It was shown that the positions of the G and 2D peaks are defined by concentration of charge carriers and strain [60, 61]. The 2D to G peak intensity ratio, I(2D)/I(G),

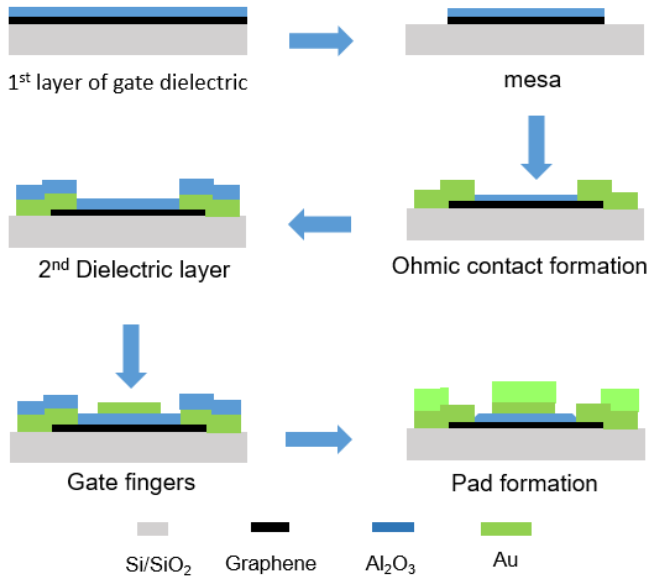

Figure 3.4: Schematic of the fabrication steps of two fingers top gate GFET.

is a strong function of the charge carrier concentration and does not depend on the strain [58, 60, 61]. The downshifts of the G and 2D bands positions, reported in [63] for PMMA-covered graphene, are not accompanied by remarkable I(2D)/I(G) changes and, hence, are explained by the tensile strain produced by PMMA. The upshifts and decrease in the I(2D)/I(G) caused by removing polymer residues via post-annealing, reported in [64,65] are explained by formation of charged defects resulting in hole doping. Our analysis indicates that the upshifts and the I(2D)/I(G) eduction observed in our experiments correspond to patterning without Al_2O_3 using both MMA-EL6 and PMMA (see figure 3.3) can only be explained by hole doping [60], apparently caused by residues of polymers. The matching of positions and intensities of the G and 2D peaks corresponding to patterning with Al_2O_3 using MMA-EL6 confirms that, in the case of the modified technique, the polymer residues are effectively removed.

3.2.2 Fabrication of GFETs and test structures

In this work, the GFETs and test structures were fabricated using high quality CVD graphene transferred onto high resistive Si substrate covered by 1 μm thick SiO_2 layer grown by wet oxidation. The relatively thick SiO_2 is used with the aim to reduce the parasitic pad capacitances in the GFETs. The measured Hall mobility of the charge carriers is up to 7000 cm^2/Vs. The following main fabrication steps of the modified process are carried out as shown in figure 3.4. As a first step the graphene sheet is covered by a dielectric layer (Al_2O_3). This modification, in comparison with previously used process, serves two important purposes [48]:

- It provides a cleaner metal/graphene interface under the contact electrode.
- It provides a cleaner interface between the top gate dielectric and graphene

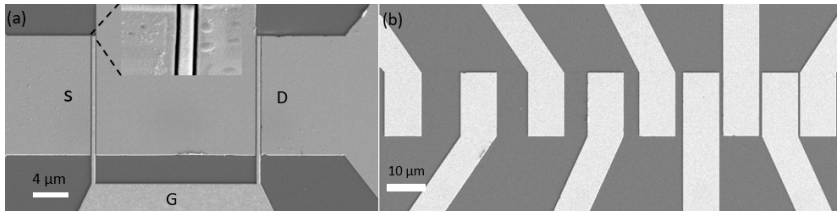

Figure 3.5: SEM micrographs of (a) two finger top gate GFET (b) TLM test structure.

channel.

The previously used GFET fabrication process starts with the formation of source and drain contacts and thus does not protect the graphene channel from contamination by residues of e-beam resists and other processing chemicals [48]. After mesa patterning, ohmic contacts are formed by patterning the contact area using e-beam lithography, followed by etching the protective oxide layer by buffer oxide etchant (BOE) and finally depositing Ti/Pd/Au (1 nm/15 nm/250 nm) metal layers, see figure3.4. It has been found via Raman spectra analysis that etching the oxide layer by BOE allows for effective removal of polymer residues from the graphene surface. More details are given in the next sections. The next processing step is deposition of a second layer of Al_2O_3 gate dielectric using atomic layer deposition technique, where the first Al_2O_3 layer serves as a seed layer. Next, gate fingers are patterned and a metal stack of Ti/Au (10 nm/300 nm) is deposited. The final processing step is the formation of contact pads for microprobes. All processing steps are carried out using e-beam lithography and e-beam evaporation. Typical SEM micrographs of top gated double gate finger GFET and transfer length method (TLM) test structures are shown in figure 3.5.

3.3 Graphene-metal contacts

Development of high performance GFETs requires development of low resistive and stable metal/graphene contacts. In this work, metal/graphene contacts with extremely low specific width contact resistivity have been developed. The contact resistance has been evaluated via analysis of the GFET transfer characteristics and, also, specially prepared TLM test structures. In the next sections, types of the metal/graphene contacts and origin and limits of contact resistance are reviewed.

3.3.1 Planar and edge type contacts

The metal/graphene contact configurations, reported to date, can be divided into two main categories: planar or top contacts and the 1D edge or side contacts. The schematic of the top and edge type contacts is shown in figure 3.6. Planar contacts are the most commonly employed in conventional semiconductor device technology and is shown in figure 3.6 (a). With planar contacts, the charge carriers are injected through the top metal/graphene interface. In this study, planar contacts with very low specific width contact resistivity ρ_c down to 90

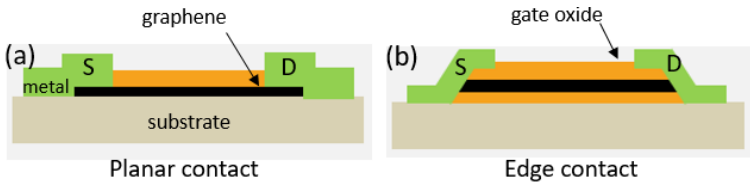

Figure 3.6: (a) Schematic cross section view of the planar contact and (b) the edge contacts.

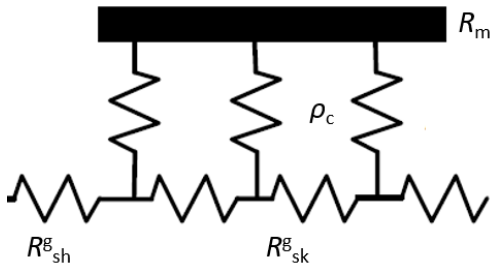

Figure 3.7: Equivalent circuit representation of the graphen/metal junction [70].

$\Omega \times \mu m$ have been demonstrated. Very recently, side contact technology was introduced by making 1D edge type contacts to 2D graphene layer as shown in figure 3.6(b) [66]. With edge type contacts, current carriers are injected through 1D side edges of the graphene sheet. The reported lowest specific width contact resistivity of the edge type contacts is approx 150 $\Omega \times \mu m$ [66]. The edge type contact is a distinguishing feature of the encapsulated graphene configuration approach.

3.3.2 Origin and limits of contact resistance

Ideally in FETs, the source and drain contacts should be ohmic with metal/graphene junction resistance as low as possible. It was demonstrated that in GFETs, the relatively high metal/graphene junction resistance may degrade significantly the device performance [67–69]. The contact resistance in FETs is characterized by the specific contact resistivity $\rho_c = R_{mg} \times W_g$, where R_{mg} is the metal/graphene contact resistance. An equivalent circuit representation of the planar metal/graphene junction in GFET is shown in figure 3.7. As the current flows from the graphene channel to the metal, it encounters the four resistive interfaces [70].

As it can be seen from figure 3.7, R_{mg} is the combination of four series resistances, for example, the resistance of the metal layers (R_m), metal/graphene junction resistance ρ_c, the sheet resistance of the graphene underneath the metal contact (R^g_{sk}) and the sheet resistance of the graphene channel (R^g_{sh}). The metal resistance is very small and the graphene sheet resistances depends upon the doping density. In general, ρ_c which is defined by the R_{mg} is used to describe the real resistance [71]. In the case of a clean metal/graphene interface, the quantum limit of the intrinsic contact resistance is given by $R_{mg} = h(\sqrt{\pi/n_{mg}})/4q^2$ [72], where h is Planck's constant. The intrinsic

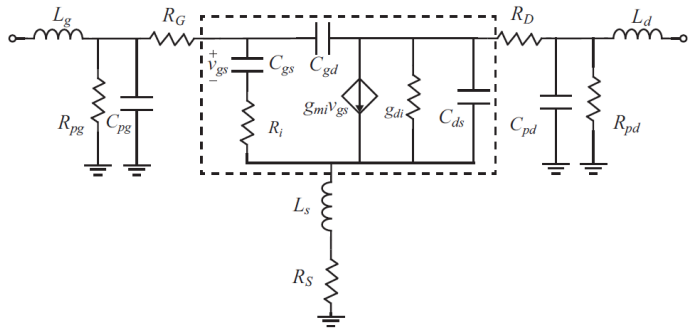

Figure 3.8: The small signal equivalent circuit of GFET with dashed line box separating the intrinsic transistor circuit.

resistance limit depends on the n_{mg}, which can be evaluated as

$$n_{mg} = \sqrt{n_0^2 + n_{m,doping}^2} \tag{3.1}$$

Here, n_0 is the residual carrier concentration and $n_{\mathrm{m,doping}}$ is the doping concentration induced by the metal in the graphene sheet, which depends on the metal work function.

3.4 Characterization and modeling of GFETs

In this section, small signal equivalent circuit models, DC, high frequency S-parameter measurements and high frequency performance benchmarking of GFETs are considered. The details of measurments and evaluation of high frequency performance of GFETs including those with record high f_{T} and f_{max} of 34 GHz and 37 GHz , respectively, are published in paper [B].

3.4.1 Small signal equivalent circuit

The equivalent circuit is used for device modeling, optimization and predicting the GFET performance and limits. It consists of two parts: the dashed line box represents the intrinsic transistor, while the outer part shows the extrinsic one which includes the parasitic elements. The intrinsic circuit includes the gate to source capacitance C_{gs}, the gate to drain capacitance C_{gd} and the charging resistance R_{i} of the gate to source capacitors. Further, it includes the current source $g_{\mathrm{mi}}V_{\mathrm{gs}}$, in which g_{mi} is the transconductance, g_{di} is the differential drain conductance and C_{ds} is the source to drain capacitance. The subscript (i) is for intrinsic circuit elements. The intrinsic circuit elements can be extracted from the measured scattering parameters (S-parameters) of the device [73].

The extrinsic elements of the small signal equivalent circuit include the parasitic elements i.e. gate, source and drain resistances and inductances R_{G}, L_{g}, R_{S}, L_{s}, R_{D}, and L_{d}. They also include the parasitic pad capacitances and resistances C_{pg}, C_{pd}, R_{pd} and R_{pg}. The pad capacitances, inductances and resistances can be extracted from the S-parameter measurements of the open and short test structures. The small signal equivalent circuit model is used

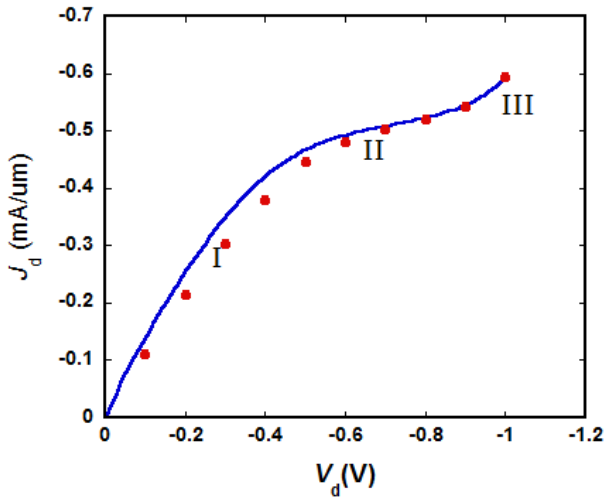

Figure 3.9: Output characteristic of the GFET with model fitting.

for the analysis of device scalability, design and performance prediction. In this thesis, the equivalent circuit has been used to interpret the high frequency performance of GFETs in paper [B]. As the next step, a method to correlate the material quality and high frequency performance of GFETs is presented.

3.4.2 DC-characterization

The high frequency field-effect transistor with top gate configuration studied here is shown in figure 3.5 and schematically in figure 3.4. Under the very realistic assumption that the gate capacitance C_G is much higher than the quantum capacitance C_q, the drain current density j_d expression is [74]:

$$j_d = q \int n(x) v_{drift} dx \tag{3.2}$$

where q is elementary charge, $n(x)$ is the carrier concentration along the channel and v_{drift} is the charge carrier drift velocity. The charge carrier drift velocity and the saturation velocity can be derived from equations (2.10) and (2.11). The net charge carrier concentration along the channel is given by (2.7). Since potential varies along the graphene channel and under the assumption of uniform doping concentration, the net voltage along the channel can be described by

$$V_{g,net} = V_g - (x/L)V_d \tag{3.3}$$

where L is the channel length. The channel carrier concentration is given by [75]:

$$n = n_0 + (q(V_g - (x/L)Vd))^2/(\pi\hbar^2 v_f^2) \tag{3.4}$$

by putting the (3.3) and (3.4) into (3.2) and solving the integral, an analytical expression for the drain current as function of V_g and V_d is:

$$j_d = q\mu V_d(n_0 + \Lambda(V_g^2 + V_d^2/3 - V_d V_g)) \tag{3.5}$$

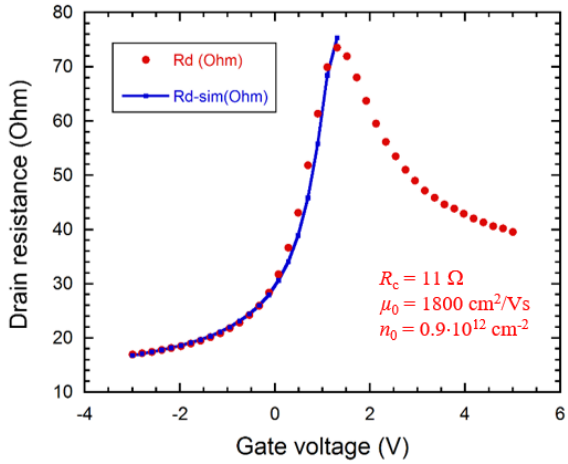

Figure 3.10: Typical dependence of the drain resistance on gate voltage of the GFET fitted with drain resistance model fitting.

Here μ is effective mobility given in (2.10) and $\Lambda = e^2/\pi\hbar^2 v_f^2$ is a constant. The output characteristic of the GFET along with fitting using equation (3.5) is shown in figure 3.9. Three different regions can be identified: the region I where $V_g > V_d$ and the channel is unipolar, the region II when $V_d \geqslant V_g$ and charge neutrality region is formed at the drain end, and the region III where the charge neutrality region shifts to the source and the channel is becoming unipolar [76]. From the output characteristic, one can extract the differential drain conductivity, which is one of the main limiting factor of the high frequency performance of the GFET as discussed in paper [A].

A typical dependence of the drain resistance of a GFET on gate voltage is shown in figure 3.10. The dependence reveals two distinguishing features. First is the minimum conductivity point (highest resistivity) at which the gate voltage is designated as the Dirac voltage, and the second is the bipolar nature of graphene. The minimum conductivity region is defined mainly by the impurities in the system. The density of charged impurities defines the Dirac voltage - for instance, in a clean graphene sample $V_{Dir} = 0V$. From the Dirac voltage one can estimate the added carrier density as [31, 42]:

$$\bar{n} = -\frac{C_{ox} V_{Dir}}{q} \tag{3.6}$$

Then n_0 can be found using the random phase approximation formalism [42]. Alternatively, the n_0 can be found via the drain resistance model, the method which we use in the below analysis. In our samples, the n_0 is, typically, widely distributed over the Si chip in the range of $1 - 2 \times 10^{12}\ cm^{-2}$. Since the Dirac voltage indicates the switching of the charge carrier type, in the region where $V_g < V_{Dir}$ the carriers are p-type and in the region where $V_g > V_{Dir}$ the carriers are n-type. One can extract the R_c, n_0, μ_0 and V_{Dir} via fitting the

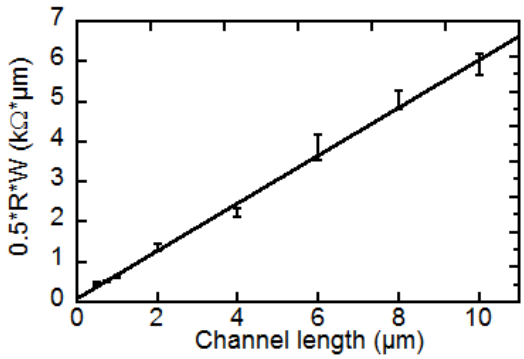

Figure 3.11: The $0.5 \times R \times W$ of a TLM tests structure versus channel length.

R_{ds} vs V_g dependence by the drain resistance model [77]:

$$R_{ds} = R_c + \frac{L_g}{qW\mu_0\sqrt{n_0^2 + (C_{ox}(V_g - V_{Dir})/q)^2}} \tag{3.7}$$

$$n = \sqrt{n_0^2 + (C_{ox}(V_g - V_{Dir})/q)^2} \tag{3.8}$$

where R_c is the source drain contact resistance, L_g is the gate length, W_g is the gate width and n is the total carrier concentrations.

Contact resistance measurements

Realization of low resistive metal/graphene junctions is a challenging task for researchers working with graphene device technology. There are basically two configurations of the junctions developed (i) the top or planar type contacts and (ii) the side or edge type contacts. The parameter characterizing the metal/graphene contact is the specific width contact resistivity $\rho_c = R_c \times W$ [78]. For contact resistance measurements, different types of test structures have been used such as two terminal technique, three terminal cross-bridge Kelvin resistance, four terminals Kelvin probe technique and multi-terminals technique e.g. transfer length method (TLM) or circular TLM method [79–83]. The TLM method is the most commonly applied method to extract the contact resistance, in particular because it takes into account the edge effect and current crowding [70, 84]. In addition to measuring the contact resistance, one can also extract the sheet resistance of the graphene between the contacts. In this thesis, the TLM method is applied to extract the contact resistance of the metal/graphene contacts along with the analysis of the R_{ds} vs V_g dependence of the GFETs. A TLM test structure is shown in figure 3.5(b). In TLM methods, a chain of identical contacts are fabricate with different channel lengths between them. The total resistance R between the contacts is measured using DC IV characterization. The R measured between the two contacts is a combination of metal resistance (R_m), contact resistance R_c, and the graphene sheet resistance R_{sh} and can be expressed as:

$$R = R_m + 2R_c + \frac{R_{sh}L}{W} \tag{3.9}$$

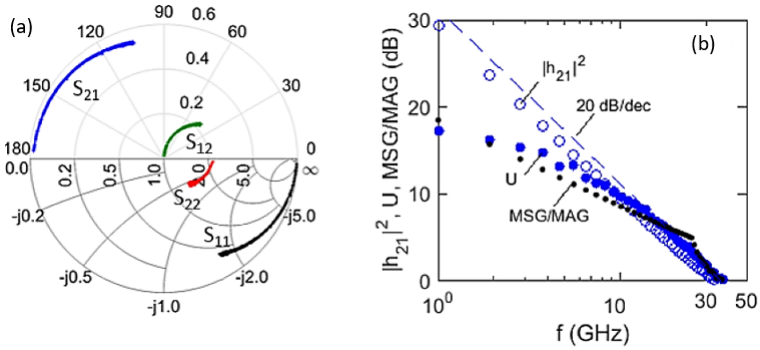

Figure 3.12: (a) The S-parameters of a GFET measured in the range of 1 to 50 GHz shown on the Smith chart. (b) The current gain (| h_{21} |^2) and unilateral power gain (U) versus frequency.

Here L is the graphene channel length and W is the channel width. The total measured R multiplied by $0.5W$ for different channel spacings are then plotted versus L as shown in figure 3.11. The slope gives the sheet resistance of the graphene while R_c is obtained from y-intercept at $L = 0$. The experimentally measured ρ_c in this way is 90 $\Omega \times \mu$m, which is lower than the edge type contacts and is close to the theoretical limit of 88 $\Omega \times \mu$m [66, 85].

3.4.3 High frequency performance

The figures of merits of high frequency transistors are the transit frequency f_{T} and the maximum frequency of oscillation $f_{\max}$ which are commonly considered for benchmarking the high frequency performance. The f_{T} is the frequency at which current gain h_{21} drops to unity, and the $f_{\max}$ is the frequency at which unilateral power gain (Mason's gain) U is equal to unity [86]. Both f_{T} and $f_{\max}$ can be directly extracted from the S-parameter measurements at optimized bias range. The expressions for f_{T} and $f_{\max}$ in terms of parameters (S-parameters) are:

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{3.10}$$

$$U = \frac{| S_{12} - S_{21} |^2}{det(1 - SS^*)} \tag{3.11}$$

The presentation of measured S-parameter data from GFET on the Smith chart is shown in figure 3.12 (a). The small signal current gain and unilateral power gain extracted from S-parameter plotted versus frequency are shown in figure 3.12 (b). Both the h_{21} and U are sensitive to drain bias, therefore, f_{T} and $f_{\max}$ also depend upon the drain and gate bias as show in figure 3.13. It can be seen that the f_{T} and the $f_{\max}$ increase with the drain bias and finally saturate reaching the peak values of 34 GHz and 37 GHz at $V_g = 0.5$V. Saturation of drain current as well as f_{T} and $f_{\max}$ can be attributed to saturation of the charge carrier velocity in the channel.

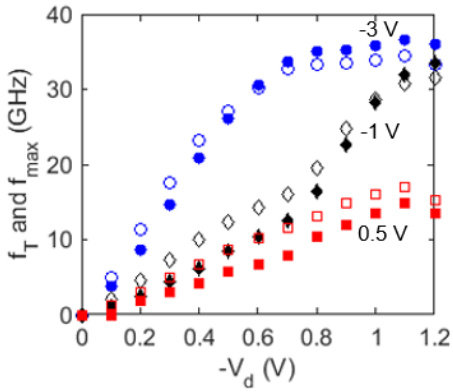

Figure 3.13: The transit frequency and maximum frequency of oscillation versus drain voltage as a function of V_g = 0.5, -1 and -3 V.

For further analyses and modeling of the high frequency performance, it is convenient to use the small signal equivalent circuit model of the FET. The model shall provide assistance for designing, scalability and performance analysis. The expression for f_{T} and f_{max} derived from the small-signal equivalent circuit are given as [73, 87]:

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \frac{1}{1+g_{ds}R_c+\frac{C_{gd}\cdot g_m\cdot R_c}{C_{gs}+C_{gd}}+C_{gp}}, \tag{3.12}$$

$$f_{\mathrm{max}} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}\left(\frac{1}{2\cdot g_m}+\frac{R_c}{2}+R_g\right)+g_m R_g \frac{C_{gd}}{C_{gs}}}}, \tag{3.13}$$

In equations (3.12) and (3.13), two main parameters g_{m} and g_{ds} are directly associated with the carrier transport mechanism in the channel and are called the transconductance and differential drain conductance, respectively. The R_{c} is also critical for high frequency performance of the GFET. The R_{c} is considered as the main parasitic parameter hindering the development of the high performing GFET [20, 50, 87, 88]. For an ideal GFETs, g_{m} must be as large as possible whereas g_{ds} and R_{c} should be as small as possible.

In the [paper A], a methodology for extraction of the parameters g_m, g_{ds} and R_c from the DC characteristics of the GFET is proposed and considered. The g_{m} is defined as:

$$g_m = v\cdot\left(C_{\mathrm{gs}}+C_{\mathrm{gd}}\right)/L \tag{3.14}$$

The high field mobility model is applied to calculate the velocity defined in (2.10).

Next, g_{ds} can be extracted directly from the output characteristic of the GFET by simply taking the derivative of drain current density. In figure 3.14, both current density and differential drain conductance are shown versus intrinsic electric field (E_{int}). The E_{int} in the channel is given as:

$$E_{int} = -\frac{V_d - I_d R_c}{L} \tag{3.15}$$

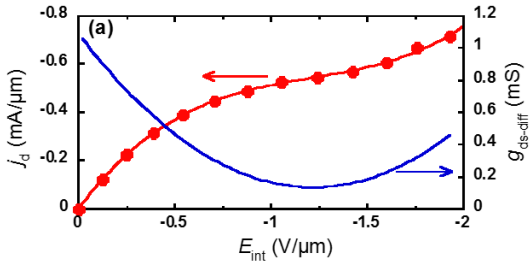

Figure 3.14: Drain current density and differential drain conductance versus intrinsic electric field.

With drain current density j_{d} revealing a kink in the dependence, the drain conductivity reaches its minimum. Since high g_{ds} has a negative impact on the high frequency performance of FETs, minimum g_{ds} apparently corresponding to highest values of f_{T} and f_{max} in figure 3.13.

The contact resistance R_{c} is extracted from the transfer characteristics by using (3.7). The R_{c} obtained using the drain resistance model is the sum of the access resistance (ungated area in the channel) R_{ung} and the metal-graphene junction resistance R_{mg}. Here we develop a method which allows classifying the R_{ung} and R_{mg}. For instance, R_{mg} is given as:

$$R_{mg} = R_c - R_{ung} \tag{3.16}$$

$$R_{ung} = \frac{R^g_{sh} \cdot L_{ung}}{W} \tag{3.17}$$

$$R^g_{sh} = \frac{W}{L_g}(R_{ds0}(V_g = 0) - R_c) \tag{3.18}$$

Where R^g_{sh} is the graphene sheet resistance, W is the channel width and R_{ds0} is the channel resistance at zero gate bias. The parasitic elements C_{gs}, C_{gd} and R_g in (3.12) and (3.13) can be extracted as follows: the C_{gs} and C_{gd} are estimated using the gate oxide capacitance (C_{ox}) as $C_{gs} = 0.5 C_{ox} L_g W_g$ and $C_{gd} = k_1 C_{ox} L_g W_g$, respectively. The oxide capacitance ($C_{ox} \propto 1/t_{ox}$) in these devices is $3.319 \times 10^{-3} F/m^2$. k_1 is the fitting parameter introduced to take into account the decrease in charge carrier concentration at the drain end. The gate resistance is determined by $R_g = 3 R_{sh,g} W_g L_g$ where $R_{sh,g}$ is the gate electrode sheet resistance [46].

3.4.4 State-of-the-art GFETs

By using all the extracted parameters in (3.12) and (3.13), simulated extrinsic f_{T} and f_{max} values can be generated and plotted in figure 3.15. First of all the simulated curve and the measurement show good agreement, proving the concept and the validity of the model. The extrinsic f_{T} and f_{max} values obtained in this work are 34 GHz and 37 GHz for 500 nm gate length, which are the highest among the results reported so far for similar gate length. This improvement in results is attributed to high g_m due to high v_{sat}, low g_{ds} and low contact resistance. Furthermore, the performance is comparable with

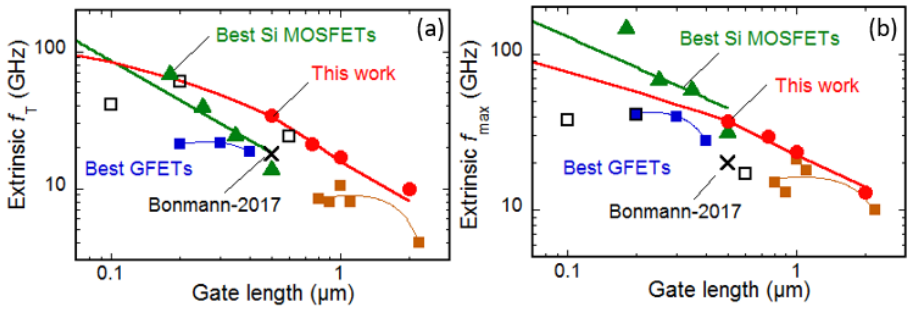

Figure 3.15: Extrinsic f_T and f_{max} (red solid circle) versus gate length along with simulated line in comparison with our previous published results (cross) and other published GFETs (squares) [88–92] and the state of the art Si MOSFETs (Triangles) [93–96] with the same channel length ranges.

the well established Si MOSFET technology. Additionally, the dependences on channel length reveal much better scaling behavior resembling that of Si MOSFET. Using the simulation, one can predict extrinsic f_T and f_{max} up to 100 GHz for 50 nm channel length.

Chapter 4

The dependence of the high frequency performance of GFETs on material quality

This chapter considers intrinsic and extrinsic factors limiting the high frequency performance of GFETs, focusing on the graphene zero bandgap issue and effects of graphene/dielectric material quality. A new method developed for the study of the relationships between the material quality and the GFET high frequency performance is presented. Conclusions drawn from the published papers are summarized. A most promising approach for further development of GFETs for high frequency applications is proposed.

4.1 Factors limiting the high frequency performance of GFETs

Owing to a very high carrier velocity up to 6×10^7 cm/s, graphene possesses great potential for high frequency applications [16, 97]. However, the high frequency performance of the state-of-the-art GFETs is significantly reduced. The published state-of-the-art extrinsic f_{T} and $f_{\max}$ of the GFETs are, typically, below 100 GHz [see Paper B]. For comparison, the HEMTs based on the III–V compounds, with low-field mobility above $10^4 \mathrm{cm}^2/Vs$ and carrier velocity of the order of $10^6 \mathrm{cm}/s$, reveal the f_{T} and $f_{\max}$ up to 1 THz at deep-sub-μm gate lengths [7]. The high frequency performance of GFETs is, currently, limited by a number of intrinsic and extrinsic factors.

4.1.1 Intrinsic limitations

The main intrinsic limitation of the GFET high frequency performance is associated with the zero bandgap phenomenon in monolayer garphene resulting in relatively high drain conductance [57]. The large drain conductance in GFETs degrades the extrinsic f_{T} and $f_{\max}$ of GFETs, see (3.12)-(3.13). The intrinsic transit frequency ($f_{\mathrm{T-int}}$) and maximum frequency of oscillation

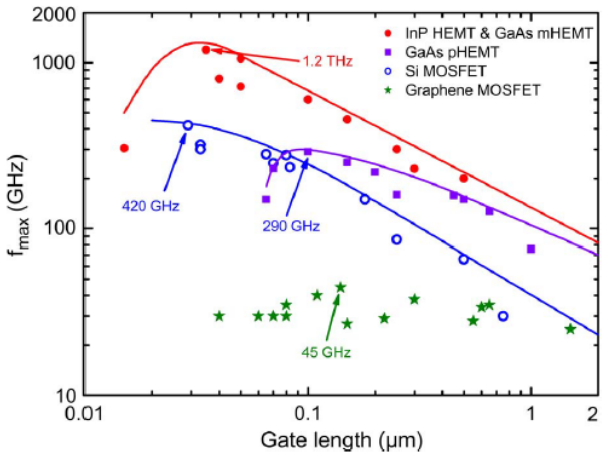

Figure 4.1: The maximum frequency of oscillation of GFETs in comparison with other high frequency semiconductor devices versus gate length [57].

($f_{\max-\text{int}}$), i.e associated with the intrinsic part of the equivalent circuit, see figure 3.8, can be expressed as [57]

$$f_{T-int} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{4.1}$$

$$f_{max-int} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds} R_i}} \tag{4.2}$$

It can be seen that only $f_{\max-\text{int}}$ is affected by g_{ds}. Therefore one can expect more pronounced degradation of the $f_{\max-\text{int}}$, caused by the relatively high g_{ds}, than of the f_{T}. Figure 4.1 shows the state-of-the-art $f_{\max-\text{int}}$ of the GFETs versus gate length in comparison with that of the Si MOSFETs and III-V compound HEMTs. As it can be seen, $f_{\max-\text{int}}$ reveals reduced values and absence of scaling-down behavior. It is assumed that the main reason for this is the relatively high g_{ds} in GFETs [57].

The origin of high g_{ds} in GFETs is due to the weak saturation of the drain current, as shown in figure 3.9. The semiconductor FETs typically reveal pronounced current saturation at high drain fields. The drain current saturation in semiconductor FETs is due to the formation of a pinch-off mode region in the channel and corresponding drift velocity saturation of the charge carriers in this region, because of higher drain field. The principle of pinch-off is that the charge carrier density decreases continuously towards the drain end with increasing the drain bias, until the carriers are completely depleted from the drain end and the resistance of the channel becomes infinite. In this situation drain current becomes insensitive to drain field and the current saturates. However, the physics of drian current saturation in GFETs is different than in conventional MOSFETs. Because of the zero bandgap, GFETs reveal ambipolar behavior, which results of a region with a residual concentration of the charge carriers, instead of a pinch-off region, and subsequent change of the type of the charge carriers with further increase of the drain voltage. This results only a corresponding kink in the output characteristic, i.e. not sufficient drain current

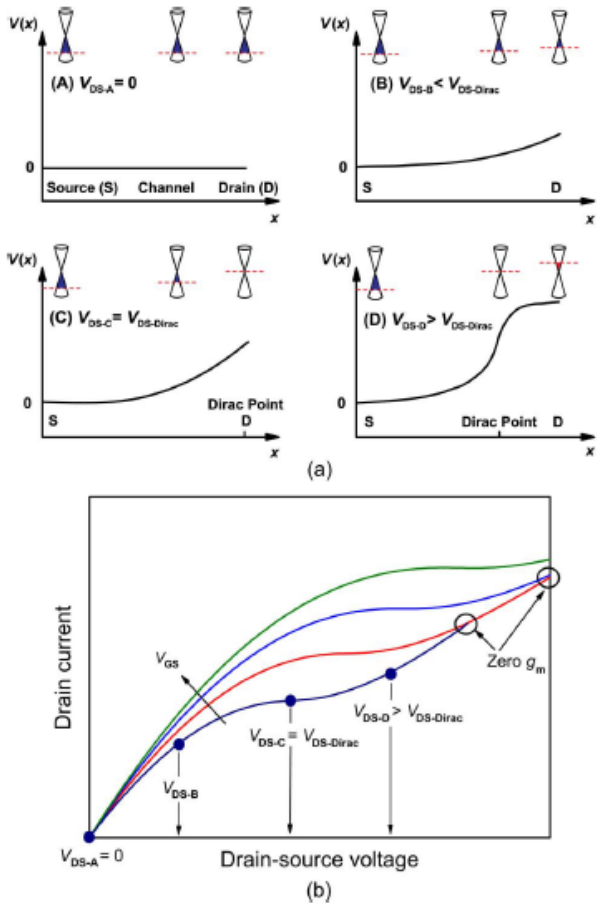

Figure 4.2: (a) shows the potential profile along the channel in GFET for four different drain-to-source biases (V_{ds}) (b) output characteristic shows the behaviour of drain current corresponding to four different V_{ds} biases and similar behaviour of drain current for different gate-source (V_{GS}) voltage [6, 57].

saturation. Figure 4.2 demonstrates schematically evaluation of potential profile in the GFETs with increasing the drain field and corresponding drain current dependence on the drain voltage.

For comparison, the g_{ds} in a typical Si MOSFET is of the order of 0.01 mS, which is approx. 30 times less than that of the GFET's $g_{\mathrm{ds}} = 0.3$ mS measured, in particular, at bias conditions corresponding to the highest $f_{\max} = 37$ GHz [94].

Apparently, the g_{ds} in GFETs can be reduced by the drain current saturation. For this purpose, the approach of the bandgap engineering in bilayer graphene and graphene nanoribbons was applied [98, 99]. However, this approach turned out to be not promising because of reduction of the carrier mobility with increasing bandgap even faster than that in the semiconductor counterparts, as shown in figure 4.3 [57].

An alternative approach has been proposed to realise the drain current

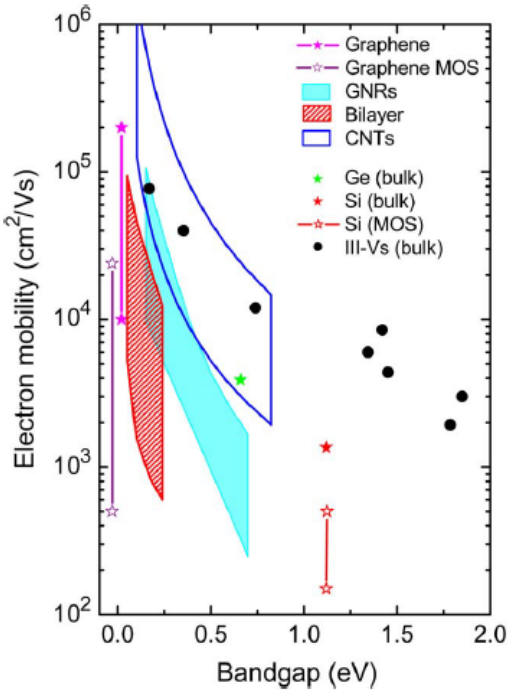

Figure 4.3: Mobility versus bandgap of Si, Ge, III–V compounds, carbon nanotubes, mono and bi-layer graphene and graphene nanoribbons [57].

saturation in GFETs without bandgap formation, but via velocity saturation of the charge carriers at high fields [100]. It was shown experimentally and by applying the carrier velocity and velocity saturation models that the effective carrier velocity in graphene tends to saturate at the fields above approx. 1 V/μm [45, 47]. This is further confirmed in a recent study of charge carrier velocity in GFETs using delay time analysis [48]. Figure 4.4(a) shows the intrinsic transit frequency of the GFETs found via delay time analysis. Figure 4.4 (b) shows the corresponding effective velocity of the charge carriers versus intrinsic drain field. It can be seen that in fact the charge carrier velocity in the GFET's channel saturates at drain field above approx. 1 V/μm and agrees well with the previous observations [47]. Similarly, the drain current saturation at above approx. 1 V/μm has been predicted using Monte Carlo simulations, which support the proposed approach of drain current saturation via velocity saturation in graphene [101]. Figure 4.4(c) shows the drain current versus electric field in graphene for three different saturation velocities corresponding to different substrate materials. Additionally, it can be seen that the saturation velocity is defined by the optical phonon energy of the substrate, see (2.11). It can be seen from figure 4.4(c) that an increase in saturation velocity results in a corresponding increase in drain current, since the saturated drain current density is defined as $j_{\mathrm{d}} = qnv_{\mathrm{sat}}$. The approach of drain current saturation via velocity saturation is used in development of the GFETs with state-of-the-art high frequency performance, operating in the velocity saturation mode [paper B].

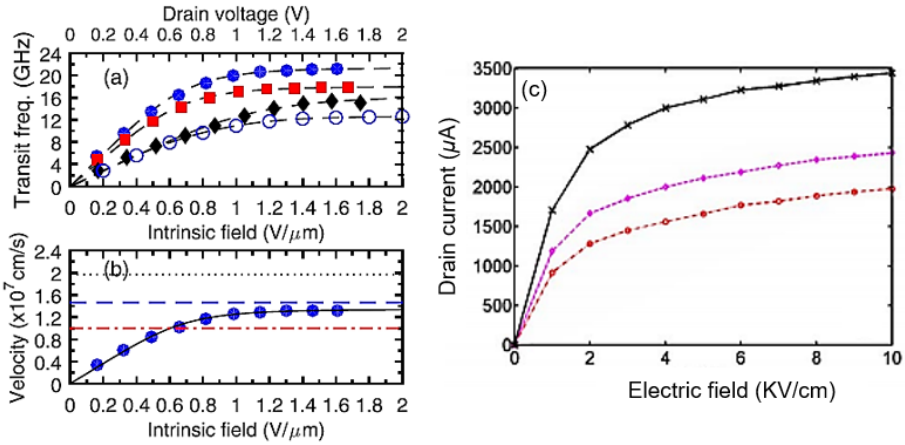

Figure 4.4: (a) Intrinsic transit frequency vs electric field in the channel for devices with different residual carrier concentration (circles, squares, and diamonds). The extrinsic transit frequency vs drain voltage is indicated in the same graph with open circles. Dashed lines are polynomial fitting curves and serve as a visual guide to the eye. (b) The drift velocity of the carriers in the channel extracted from the extrinsic f_T using delay time analysis and fitted by the empirical expression of Eq. (2.10) (solid line) vs the electric field in the channel. The effective saturation velocities calculated using (2.11) for graphene with Al_2O_3 optical phonons (OPs) (dotted), graphene with SiO_2 OPs (dashed), and graphene with SiO_2 and Al_2O_3 OPs are also shown (dashed-dotted) [48].(c) The drain current vs the applied electric field for three different OP energies, $\hbar\omega_{OP}$= 55 meV of SiO_2, (the dash-dot line with circles), 87 meV of Al_2O_3, (the dashed line with diamonds) and 200 meV for the OPs of graphene (the solid line with crosses) [101].

Apparently, drain current saturation via velocity saturation is a promosing approach for further increase of the f_{max}. Figure 4.5 shows the highest f_{max} measured and analysed in this work versus gate length together with that of the best previously published GFETs and Si MOSFETs at similar gate lengths. To demonstrate the effect of saturation velocity, the f_{max} is simulated [see details in paper C] for different $v_{sat} = 3 \times 10^7$ and $5 \times 10^7 cm/s$ correponding to the graphene encapsulated by Al_2O_3 and hBN layers, respectively. The simulation results, assuming $g_{ds} = 0.3$ mS, are shown by the dashed and dash-dotted lines in figure 4.5. To demonstrate the effect of drain conductance on the f_{max} the solid line represents simulation results assuming $g_{ds} = 0.01$ mS, which is typical for the Si MOSFETs, and $v_{sat} = 5 \times 10^7$ m/s.

Thus drain current saturation via drift velocity saturation is promosing approach for reduction of the g_{ds} and corresponding increasing of the GFET high frequency performance. However, as indicated above, there are also extrinsic limiting factors associated with the graphene/adjacent dielectric material quality. They will be discussed in the next sections.

4.1.2 Extrinsic limitations

In this work, the extrinsic limitations of the f_T and f_{max} are associated with the imperfections in the graphene, adjacent dielectrics and interfaces. Additionally, the f_T and f_{max} are limited by parasitic capacitances and resistances, in particular by metal/graphene junction resistance. The metal/graphene junction

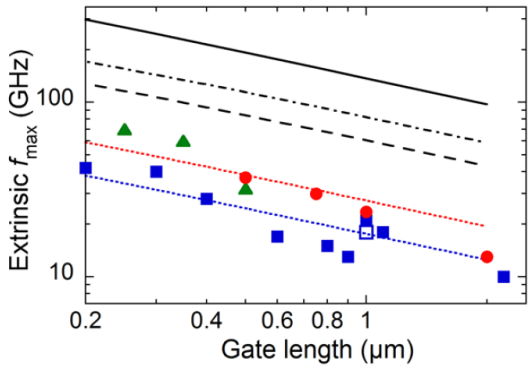

Figure 4.5: Extrinsic maximum frequency of oscillation ($f_{\max}$) versus gate length of GFETs analyzed in this work (circles) shown together with the highest published extrinsic $f_{\max}$ of GFETs (squares) and Si MOSFETs (triangles) [paper B]. The lines are simulations using models described in [paper C]. The upper and lower dotted lines correspond to parameters of the GFETs with the highest measured $f_{\max}$ (circle) and our previously published GFET (open square), respectively [48]. The solid line represents $f_{\max}$ of the GFETs similar to those analyzed in this work, but assuming g_{ds}=0.01 mS, typical for the Si MOSFETs [94]. The dashed and dash-dotted lines represent $f_{\max}$ of the GFETs similar to those analyzed in this work, but assuming graphene encapsulated by Al_2O_3 and hBN layers, respectively.

resistance in GFETs is partly related to the graphene/interface material quality. For instance, the polymer residues remaining after the graphene transfer and contact patterning modify the graphene/metal interface in the contact area, which also increases the source/drain contact resistances [102, 103].

Low field mobility and material imperfections

In this section, the effects of the grapene/dielectric material quality on the low-field mobility are briefly considered. It is shown that the low-field carrier mobility can be selected as the most appropriate material quality parameter because of its combined response to different types of imperfections. The effects of the imperfections on the low-field DC graphene properties have been thoroughly studied over the past years both theoretically and experimentally.

The commonly observed experimental low-field DC characteristics of graphene devices can be fully described by one or a combination of a few mechanisms of the charge carrier scattering, including scattering by the charged impurities (also known as Coulomb or long-range scattering [104]), the resonant scattering and scattering by the substrate surface polar phonons [35, 43, 105]. The charged impurities are typically associated with the oxygen vacancies in the adjacent dielectrics and/or water molecules trapped at the graphene/dielectric interfaces [41]. The resonant scattering in graphene is usually associated with vacancies and adsorbates like H, OH, and CH_3, C_2H_5, CH_2OH [35, 44]. The scattering by the substrate surface polar phonons is associated with the electrostatic coupling of the carriers in graphene to the long-range polarization field created at the graphene/substrate interface by the substrate phonons [35, 105]. The short-range scattering caused by defects or dislocations in the graphene lattice and scattering from graphene ripples is also considered [104]. Apparently, at the current level of the graphene/substrate material quality, i.e. concen-

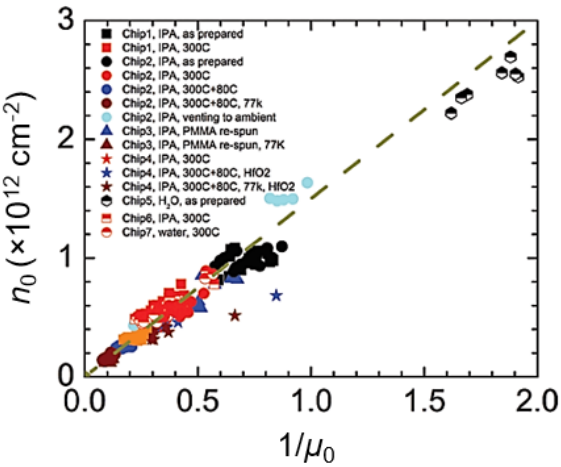

Figure 4.6: Residual charge carrier concentration versus inverse low-field mobility in GFETs located at different positions on the Si chip. The line corresponds to the product $\mu_0 \cdot n_0 = 1.5 \times 10^{15}$ 1/Vs [109].

tration of impurities, the scattering by the charged impurities is usually the dominating mechanism [35, 106]. According to the self-consistent theory of charge carrier transport in the graphene, the charged impurities in the substrate and/or graphene/substrate interface create a spatially inhomogeneous screened Coulomb potential [42].

At low carrier density, the system breaks up into puddles of electrons and holes with added concentration compensating the average charge impurity potential. Therefore, besides the corresponding carrier scattering the charged impurities are responsible for formation of the electron-hole puddles at the neutrality (Dirac) point [31, 40, 107]. The existence of the lateral inhomogeneities in the graphene DC low-field electronic properties associated with the charged impurities is confirmed experimentally by means of high resolution two-dimensional mapping using THz and near-field spectroscopy [35, 108]. A distinguishing feature of the scattering by the charged impurities is that the low-field mobility is defined only by the concentration of impurities and the dielectic constants of the adjacent dielectrics, but does not depend on the carrier concentration [42]. The latter allows for applying the semi-empirical drain resistance model of the GFET and evaluation of the contact resistance, low-field mobility and residual carrier concentration as fitting parameters [77].

The concentration of impurities plainly defines the residual concentration of the charge carriers, i.e. the concentration at the Dirac point [42]. Therefore, the n_0 found via the drain resistance model can be used as a material quality parameter. The product of the low-field mobility and the residual carrier concentration is constant and, for graphene on the SiO_2 substrate, for example, is $\mu_0 \cdot n_0 = 1.5 \times 10^{15} 1/Vs$ [42]. This relationship is confirmed experimentally for mobilities in the wide range of approx. $10^2 - 10^4 \mathrm{cm}^2/Vs$ [109, 110].

Figure 4.6 shows the residual charge carrier concentration versus inverse low-field mobility in the GFETs. The line corresponds to the product of $\mu_0 \cdot n_0 = 1.5 \times 10^{15} 1/Vs$. The general agreement between the experimental dependence

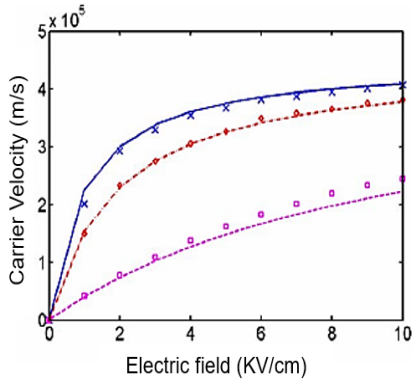

Figure 4.7: The charge carrier velocity vs the applied electric field as a function of different impurity concentration decreases from top to bottom. The crosses (×) correspond to no impurity and the squares (□) represents highest impurities [101].

and the line confirms that the μ_0 and n_0 distributions are associated mainly with spatially inhomogeneous screened Coulomb potential [104]. However, as can be seen from figure 4.6, some mobilities are mobilities deviate by the product of $\mu_0 \cdot n_0 = 1.5 \times 10^{15} 1/Vs$. This indicates additional contributions of the other charge carrier scattering mechanisms, such as "short-range" or "resonant" scattering, associated with different scattering mechanisms as discussed above. The mobility addressing all the scattering mechanisms can be combined using the Matthiessen rule as discussed in section 2.2 [46]. Therefore, we assume that the more appropriate parameter for characterization of the graphene/dielectric material quality is the combined low-field mobility, found, for example, using the drain resistance model. The surface distribution of the graphene/dielectric material quality over the Si chip surface allows us to study the dependencies between the material quality, DC and high frequency performance of the GFETs via comparative analysis of the performance of transistors located at different positions on the Si chip, as shown below in section 4.2..

High field charge carrier velocity and material imperfections

So far, the effects of material quality on low-field graphene properties have been considered. In contrast to the DC low-field properties, the effects of the graphene/dielectric material quality on the high-field high-frequency performance of the GFETs are not addressed. The high drain field is required for higher carrier velocity and, hence, higher f_{T} and f_{max}. In the previous sections, the effects of residual charge carrier concentration on the low field mobility have been described, which forms the basis for further investigation of the effects of charged impurities on the high field charge carrier velocity. Analysis of (2.10) indicates that the high-field carrier drift velocity depends on μ_0 and, hence, on the charged impurity concentration. Figure 4.7 shows the results of Monte Carlo simulations of the average carrier velocity in graphene versus the electric fields. It can be seen that the charge carrier velocity decreases with the impurity concentration due to the increase in elastic scattering rate, i.e. indirectly due to the decrease in the low-field mobility [101].

Further Monte Carlo simulations demonstrate the graphene quality effect

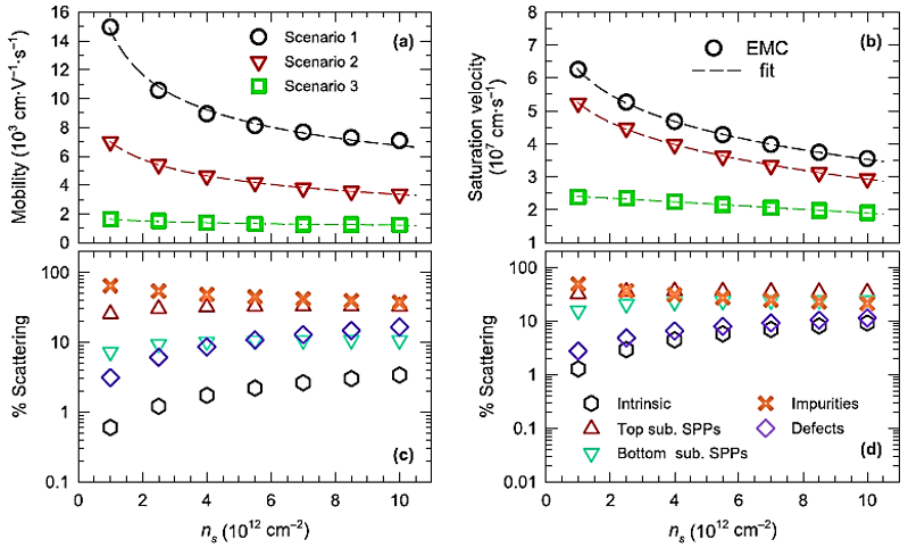

Figure 4.8: (a) the low-field mobility (b) the saturation velocity versus charge carrier density as a function of different impurities and defect densities in graphene. Three case scenarios: scenario 1 corresponds to no impurities and no defects; scenario 2 to $n_{imp} = 0.95 \times 10^{12} cm^{-2}$ and $\alpha = 0.07 eV nm$; and scenario 3 to $n_{imp} = 8 \times 10^{12} cm^{-2}$ and $\alpha = 0.1 eV nm$. Symbols represent the Monte Carlo data while lines are fits to the analytical expression. For scenario 2, the percentage of each scattering type as a function of the carrier concentration is presented for the case of low-field (c) and high-field (d) [111].

on the low field mobility and saturation velocity [111]. Figure 4.8 show the low-field mobility and the saturation velocity versus charge carrier density as a function of graphene quality by assuming different impurities and defect concentrations in graphene. There are three diffent case scenarios (1) perfect graphene without imperfections; (2) $n_{imp} = 0.95 \times 10^{12} cm^{-2}$ and defect-related potential $\alpha = 0.07 eV$ nm (3) $n_{imp} = 8 \times 10^{12} cm^{-2}$ and $\alpha = 0.1 eV$ nm. A clear message is that both the low-field mobility and the saturation velocity decrease with the impurity and defect concentration [111]. For the case of clean graphene without imperfections, the low field mobility and saturation velocity are mainly suppressed by the surface polar phonon originating from top and bottom dielectric interfaces [111]. For scenario (3), the long range scattering mainly due the charged impurities degrades the low field mobility and saturation velocity throughout the carrier density range [111]. Figure 4.8 (c) and (d) shows the percentage of scattering rate in the graphene channel for intermediate impurities and defect concentration, both at low and high electric field. In the case of low field mobility, the surface polar phonon scattering from the top dielectric interface as well as the impurity scattering are the dominant scattering mechanisms. At high field, charged impurity scattering in addition to scattering scattering from the surface phonons and scattering from the top and bottom dielectric contribute to deterioration of the charge carrier velocity. In a recent study using the delay time analysis of the GFETs, see figure 4.4, it was shown that within the considered range, the charged impurities do not limit the saturation velocity directly by the phonon mechanism, but act as traps emitting charge carriers at high fields, which prevents the current

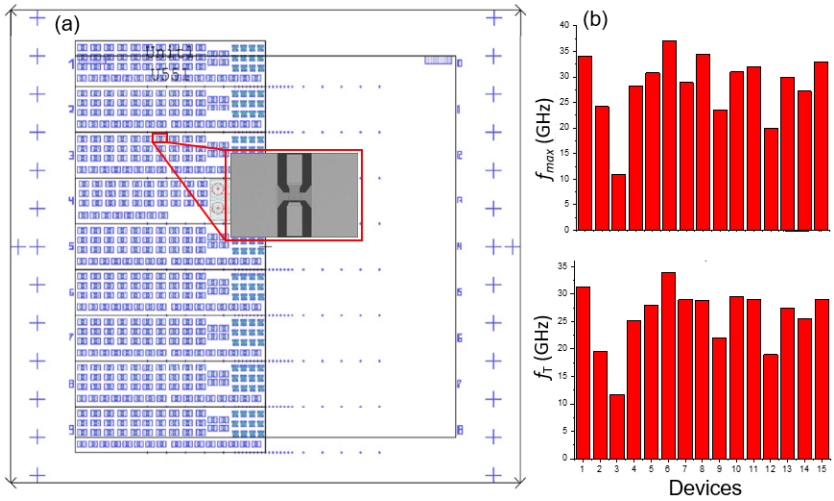

Figure 4.9: (a) The schematic layout of the array of GFETs on the Si chip and zoomed in SEM image of a GFET in the array (b) Histograms of measured f_{T} and f_{max} from the GFETs located at different positions on the chip.

from saturating and, thus, potentially limiting the extrinsic f_{T} and f_{max} [48]. Nevertheless, to the best of the author's knowledge up to date, there are no published systematic analyses of the effects of graphene quality directly on the high frequency performance of the GFETs.

4.2 Method of study

For systematic analysis of the effect of material quality on the high frequency performance of GFETs, we exploited the surface distribution of the graphene/dielectric material quality across the Si chip surface, caused by lateral inhomogeneities. Figure 4.9(a) shows schematically the array of the fabricated similar GFETs located at different positions across the chip within the area of approximately $10 \times 5\ cm^2$. The GFETs located at the different position on the chip have been characterized and used in the comparative analysis.

Figure 4.9(a) also shows a typical SEM image of two-finger gate GFETs. The gate length and total gate width of the GFETs are 0.5 μm and 30 μm, respectively. Extrinsic high frequency performance of GFETs located at different positions on the Si-chip were measured at the drain fields above 1 V/μm, and the histogram shown in figure 4.9(b) depicts distributions of the f_{T} and f_{max}. It can be seen that the extrinsic f_{T} and f_{max} deviate between 20 to 40 GHz, which is attributed to the surface distribution of the graphene/dielectric material quality caused by the lateral inhomogeneities and variations across the Si chip surface. The spatially distributed material quality over the chip is exploited as tool to study the relationships between the material quality, DC and high frequency performance of GFETs. The low-field mobility is used as a parameter representing the material quality as discussed earlier to establish relationships. The relationships between high frequency performance of GFETs and low field mobility are analyzed by using the proposed new

method combing semi-emperical models of the drain resistance, carrier velocity, saturation velocity and small-signal equivalent circuit. This approach allows us to simulate the high frequency performance of GFETs as a function of mobility. Furthermore, it allows to clarify the relative effects of the graphene quality on the specific equivalent circuit parameters and their corresponding effects on the high frequency performance of the GFETs.

4.2.1 Relationships between mobility, equivalent circuit parameters and high frequency performance

Figure 4.10 shows the experimentally measured extrinsic f_T and f_{max} of GFETs located at different positions on the Si chip versus corresponding values of μ_0. As can be seen, there are dependencies between the graphene quality and the high-frequency performance of the GFETs. In general, f_T and f_{max} increase in the range of approx. 20-40 GHz with μ_0 varying in the range of approx. 600-2000 cm^2/Vs, which is larger than the deviations from the corresponding simulated dependencies. The solid lines in figure 4.10 represent the f_T and f_{max} versus μ_0 simulated using (3.12)-(3.13) and corresponding polynomial dependences of g_m, g_{ds} and R_c on μ_0 found as fits to experimental data. Good agreement between the experimental trends and simulated dependences of the f_T and f_{max} verify the analytical expressions of f_T and f_{max}, as well as the models used for calculations of the g_m, g_{ds} and R_c. The dotted lines in figure 4.10 are linear fits to the simulations. The simulated f_T and f_{max} dependences on μ_0, in the studied mobility range, can be well approximated by linear functions of $f_T(\mu_0) = A_1 + B_1\mu_0$ and $f_{max}(\mu_0) = A_2 + B_2\mu_0$ with coefficients A_1=10 GHz, A_2=16 GHz, $B_1 = 1.3 \cdot 10^{-11} V/cm^2$ and $B_2 = 9.5 \cdot 10^{-12} V/cm^2$. The approximations can be used for the evaluations and predictions of the f_T and f_{max}, in the studied mobility range and in the vicinity, using the low field mobility only found from the GFET DC transfer characteristics, i.e. without measuring the S-parameters. For instance, extrapolations to μ_0=5000 V/cm^2 give f_T=75 GHz and f_{max}=64 GHz for the GFETs of similar design. Thus, the established correlations clarify the ways of further development and improvement of GFET high frequency performance.

The established correlations between the f_T, f_{max}, g_m, g_{ds}, R_c and the low-field mobility allow for analysis of the relative effects of the equivalent circuit parameters on the high frequency performance of the GFETs. For demonstration, figure 4.10 shows the experimentally measured f_T and f_{max} versus μ_0 together with the simulation curves calculated using (3.12)-(3.13) and corresponding polynomial functions of the g_m, g_{ds} and R_c, while keeping one of the parameters constant at its highest and lowest values in the studied ranges. The colored areas between the upper and lower curves correspond to the areas of hypothetical variations of specific parameters. In particular, the upper and lower curves of the g_{ds} and R_c variation areas correspond to their lowest and highest values, while the upper and lower curves of the g_m variation area correspond to its highest and lowest values, respectively. As can be seen, the variations of the R_c in the studied range have relatively weak effects on the f_T and, especially, f_{max}. This can be explained by the extremely low contact resistance in our GFETs. As shown above, the lowest R_s and R_d, are less than 10 percent of the R_{ds} at the gate voltage of the highest measured f_T

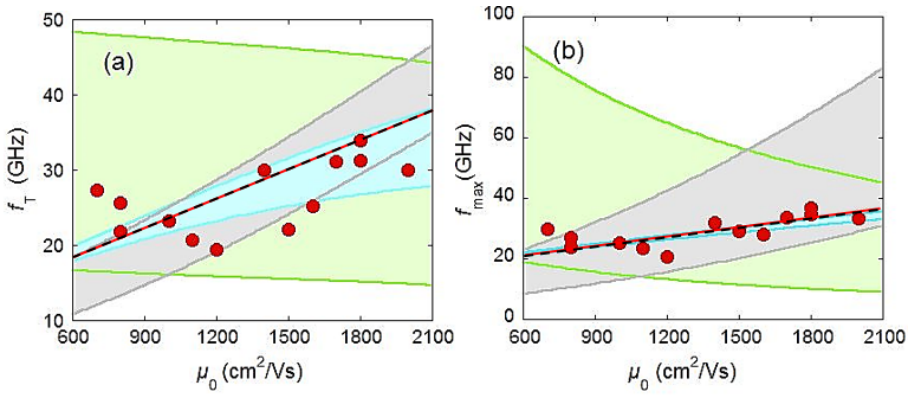

Figure 4.10: Extrinsic transit frequency (a) and maximum frequency of oscillation (b) of the GFETs, located at different positions on the Si chip, versus corresponding values of the low filed mobility. The solid lines are simulations using (3.12)-(3.13), corresponding polynomial dependences of the g_{m}, g_{ds} and R_{c} on μ_0 and keeping one of the parameters constant at its highest and lowest values in the studied ranges. The coloured areas between the upper and lower curves correspond to the areas of hypothetical variations of the g_{m} (grey), g_{ds} (green) and R_{c} (blue).

and f_{max}. One can see from figure 4.10 that variations in the f_{T} and f_{max} are mainly governed by corresponding variations in the g_{ds} and g_{m}. Apparently, for the higher f_{T} and f_{max} the lower g_{ds} and higher g_{m} are required. It is commonly accepted that the relatively high g_{ds} in the single layer GFETs, due to the zero energy bandgap, is the main factor limiting the high frequency performance [57]. It was shown that bandgap engineering in graphene is not promising because of simultaneous reduction in the carrier mobility and, hence, high-field velocity [57]. Our analysis indicates that a more favorable way is increasing the g_{m} via selection of the adjacent dielectric materials with optical phonon energy higher than that of the SiO_2. This will increase the saturation velocity limited by the remote phonon scattering [45]. For example, the Al_2O_3 and hBN optical phonon energies are 87 and 100 meV, respectively, resulting in corresponding saturation velocity of approx. $3 \cdot 10^7$ and $5 \cdot 10^7$ cm/s [45]. It can be shown that the f_{max} of the Al_2O_3 and hBN encapsulated GFETs can be approx. 120 and 180 GHz, respectively, at L_g=200 nm.

Chapter 5

Conclusions and future outlook

In this thesis, the high frequency performance of GFETs has been explored. This involves fabrication, characterization of the DC and RF performance and the performance analysis. A fabrication technique was optimized, which allowed for remarkable improvement in the GFET performance.

In particular, the dependence between graphene/dielectric material quality, equivalent circuit and high-frequency parameters of GFETs have been studied. This includes analysis of the mobility, contact resistivity, carrier velocity, drain conductivity, transit frequency and maximum frequency of oscillation via applying drain resistance, velocity and saturation velocity models. The established correlations allow for understanding dominant limitations of the high-frequency performance of transistors, which clarifies the paths for their further development. It was found that, the relatively high-drain conductivity is currently the main limiting factor, which, however, can be counterbalanced with high transconductance by increasing the carrier velocity via operating transistors at higher fields in the velocity-saturation mode. Contrary to previous reports, we found that contact resistance has a minor influence on the GFET high-frequency performance. Furthermore, a promising approach for improving the GFET high-frequency performance is applying gate and substrate-dielectric materials with reduced charged-impurity density and optical-phonon energy higher than that of SiO_2, resulting in higher saturation velocity and, hence, higher f_T and f_{max}.

Chapter 6

Summary of appended papers

In this chapter appended papers, on which basis the thesis is composed, are summarized as follows:

Paper A

The dependence of the high-frequency performance of graphene field-effect transistors on material quality

In this paper, a noval approach characterizing the high frequency performance of GFETS in relation with material quality defined by low field mobility is demonstrated. The relationship between high frequency figures of merit f_{T}, f_{max} and the high freqeuency limiting factors such as transconductance g_{m}, drain conductance g_{ds} and contact resistance R_{c} is established. My contribution includs measurements, data analysis with co-authors and paper writing.

Paper B

Graphene field-effect transistors with high extrinsic f_{T} and f_{max}

In this paper, the state-of-the-art GFETs high frequency performance with record higt extrinsic f_{T} and f_{max} up to 34 GHz and 37 GHz, respectively, is presented for 500 nm gate length. My contributions include significant efforts on optimizing and performing the measurements, the data arrangement and analysis.

Paper C

Correlation between material quality and high frequency performance of graphene field-effect transistors

In this study, the analysis of high frequency performance of graphene field-effect transistors (GFETs) in relation with material quality by applying models of drain resistance, carrier velocity and saturation velocity is presented. Main results to identify the limitations and propose an approach most promising for further development of the GFETs suitable for advanced mm-wave amplifiers. My contribution includs measurements, data analysis with co-authors and paper writing.

Acknowledgements

The author would like to thank all those people who helped me and continue their support for making this work possible. In particular, Professor Jan Stake for his encouragement, support, guidance and for giving me the opportunity to perform this work. My sincere appreciation to Dr. Andrei Vorobiev for his openhanded support, fruitful discussions and valuable opinions which were important for the progress of this work. Thanks to Professor Kjell Jeppson for reading my manuscript, discussion and giving me his valuable advice. I am thankful to Dr. Michael Andersson for sharing his knowledge in processing and fabrication. Thanks to Xinxin Yang for teaching me GFET fabrication process. Thanks to Marlene Bonmann for his valuable support and discussion on the design and measurements of GFETs and in general. A special thanks to Dr. Josip Vukusic for his valuable comments.

Thanks to everyone in the clean room who helped me with the processing and in particular, to Bengt Nilsson and Mahdad Sadeghi for their availability and valuable hints on fabrication processes. Thanks to all the Terahertz and Millimetre wave lab members for friendly environment at work and in particular, to Professor Serguei Cherednichenko and Vladimir Drakinsky for enjoyable discussions.

Thanks to Dr. Daniel Neumaier and Professor Christoph Stampfer from AMO and Aachen University for providing CVD graphene.

My acknowledgements to the financing institutions EU Graphene Flagship Project, Swedish Foundation for Strategic Research (SSF) and Swedish Research Council for the supporting this work.

Finally, I would like to thanks my mother and my wife for their encouragement and support during this work.

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Paper A

The dependence of the high-frequency performance of graphene field-effect transistors on material quality

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Submitted to *2D Materials*.

Paper B

Graphene field-effect transistors with high extrinsic f_{T} and f_{max}

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***IEEE Electron Device Letter*, Vol: 40, no. 1, pp. 131-134 January 2019.**

Paper C

Correlation between material quality and high frequency performance of graphene field-effect transistors

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***Graphene Week 2019*, Helsinki, Finland.**