Thesis for the degree of Licentiate of Engineering

Broadband Receiver Electronic Circuits for Fiber-Optical Communication Systems

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Abstract

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The exponential growth of internet traffic drives datacenters to constantly improve their capacity. As the copper based network infrastructure is being replaced by fiber-optical interconnects, new industrial standards for higher datarates are required. Several research and industrial organizations are aiming towards 400 Gb Ethernet and beyond, which brings new challenges to the field of high-speed broadband electronic circuit design. Replacing OOK with higher M-ary modulation formats and using higher datarates increases network capacity but at the cost of power. With datacenters rapidly becoming significant energy consumers on the global scale, the energy efficiency of the optical interconnect transceivers takes a primary role in the development of novel systems.

There are several additional challenges unique in the design of a broadband short-reach fiber-optical receiver system. The sensitivity of the receiver depends on the noise performance of the PD and the electronics. The overall system noise must be optimized for the specific application, modulation scheme, PD and VCSEL characteristics. The topology of the transimpedance amplifier affects the noise and frequency response of the PD, so the system must be optimized as a whole. Most state-of-the-art receivers are built on high-end semiconductor SiGe and InP technologies. However, there are still several design decisions to be made in order to get low noise, high energy efficiency and adequate bandwidth. In order to overcome the frequency limitations of the optoelectronic components, bandwidth enhancement and channel equalization techniques are used.

In this work several different blocks of a receiver system are designed and characterized. A broadband, 50 GHz bandwidth CB-based TIA and a tunable gain equalizer are designed in a 130 nm SiGe BiCMOS process. An ultra-broadband traveling wave amplifier is presented, based on a 250 nm InP DHBT technology demonstrating a 207 GHz bandwidth. Two TIA front-end topologies with 133 GHz bandwidth, a CB and a CE with shunt-shunt feedback, based on a 130 nm InP DHBT technology are designed and compared.

Keywords: TIA, data communication, VCSEL, photodetector, short-haul interconnects, receiver front-end, SiGe HBT, InP DHBT, broadband amplifiers, distributed amplifiers.

Acknowledgment

I am striving to express my appreciation towards colleagues, friends and family readily. Since I might have had varying levels of success in doing that, I believe it helps having it on paper. If nothing else, then at least to serve as a testament of how much their support meant to me during my studies. This part of the thesis is where I feel I can hang my scientist coat by the door and be my own true literary self; so please dear reader, bear with me while I express my due gratitude.

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Stavros Giannakopoulos
Göteborg, November 2019

List of Publications

This thesis is based on the following appended papers:

Paper A. Stavros Giannakopoulos, Klas Eriksson, Izzat Darwazeh, Zhongxia Simon He, and Herbert Zirath. *Ultra-Broadband Common Collector-Cascode 4-Cell Distributed Amplifier in 250nm InP HBT technology with over 200 GHz bandwidth.* In 2017 12th European Microwave Integrated Circuits Conference (EuMIC), pp. 142-145. IEEE, 2017.

Paper B. Stavros Giannakopoulos, Zhongxia Simon He, Izzat Darwazeh, and Herbert Zirath. *Differential common base TIA with 56 dB Ohm gain and 45 GHz bandwidth in 130 nm SiGe.* In 2017 IEEE Asia Pacific Microwave Conference (APMC), pp. 1107-1110. IEEE, 2017.

Paper C. Stavros Giannakopoulos, Zhongxia Simon He, and Herbert Zirath. *Tunable Equalizer for 64 Gbps Data Communication Systems in 130nm SiGe.* In 2018 Asia-Pacific Microwave Conference (APMC), pp. 627-629. IEEE, 2018.

Paper D. Stavros Giannakopoulos, Zhongxia Simon He, Izzat Darwazeh, and Herbert Zirath. *Transimpedance Amplifiers with 133 GHz bandwidth on 130 nm InP DHBT.* Electronics Letters 55, no. 9 (2019): p.521 – 523. IET, 2019.

List of Acronyms

APD	–	Avalance Photodetector
BER	–	Bit Error Rate
BW	–	Bandwidth
BiCMOS	–	Bipolar Junction Transistor - Complementary Metal Oxide Semiconductor
CB	–	Common Base
CC	–	Common Collector
CE	–	Common Emitter
CMOS	–	Complementary Metal Oxide Semiconductor
DA	–	Distributed Amplifier
DFE	–	Decision-Feedback Equalization
DHBT	–	Double Heterojunction Bipolar Transistor
EQ	–	Equalizer
FEC	–	Forward Error Correction
FET	–	Field Effect Transistor
HBT	–	Heterojunction Bipolar Transistor
MMF	–	Multi-Mode Fiber
MMIC	–	Monolithic Microwave Integrated Circuit
MZM	–	Mach Zehnder Modulator
NRZ	–	Non-Return Zero
OOK	–	On-Off Keying
OI	–	Optical Interconnect(s)
PAM	–	Pulse Amplitude Modulation
PD	–	Photodetector/Photodiode
RT	–	Room Temperature
SNR	–	Signal-to-Noise Ratio
SOI	–	Silicon on Insulator
TIA	–	Transimpedance Amplifier
VCSEL	–	Vertical Cavity Surface Emitting Laser

Contents

Part I

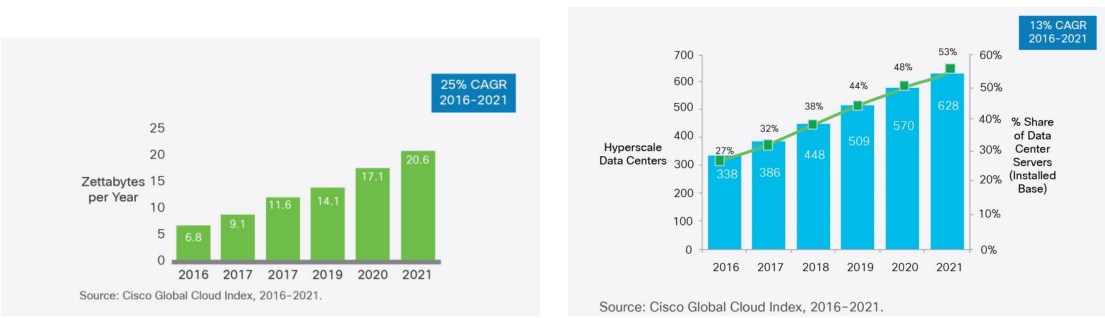
Introductory chapters

Chapter 1

Introduction

The global internet traffic has been steadily increasing, with current predictions calculating that the global traffic per year will reach 3.3 Zettabytes by 2021, as Fig. 1.1a indicates. The exponential increase on internet traffic, computing and network capacity is translated into higher demands on the interconnect infrastructure. Those demands impose requirements for increased interconnect bandwidth, bandwidth capacity, and higher energy efficiency on the existing networks. The Cisco Global Cloud index report states that approximately 71.5% of that traffic is restricted on interconnects within data centers [1]. With the continuous increase on the number of hyperscale data centers (Fig. 1.1b), in order to cover the traffic demands, the total energy consumption becomes significant.

The energy consumption of the data centers was 330 billion kWH in 2007 according to Greenpeace's Make IT green report [2]. The projected energy demand is expected to increase to 1000 billion kWh in 2020 [3]. The short-haul optical interconnects (OI) are an important contributor to the total energy demands of data-centers, with the networking amounting up to 23% of the total power consumption [3]. However, by replacing copper interconnects with short range OIs the energy consumed per Gbps of transmission can drop from 25 mW per Gbps to 1 mW per Gbps as seen in Fig. 1.2 [4].



(a) Global data traffic statistics.

(b) Hyperscale data center numbers.

Figure 1.1: Global traffic and hyperscale data center number statistics and future predictions [1].

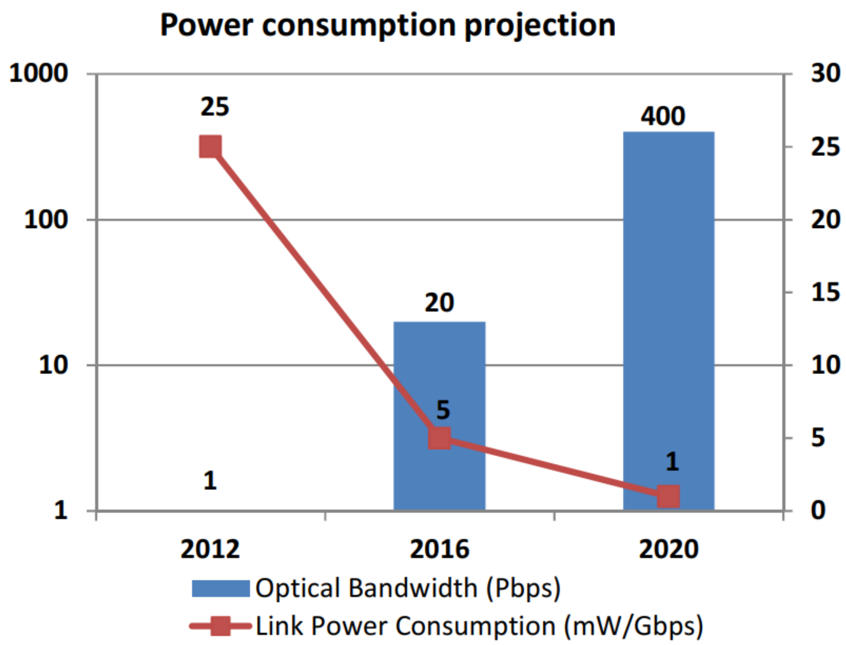


Figure 1.2: Optical power consumption and bandwidth required by Internet data centers by 2020 [4].

1.1 Applications

The field of short haul fiber-optical interconnects is quite mature with several commercially available interconnect solutions such as Thunderbolt [5], Infiniband [6] and the further development of the existing Ethernet standards [7]. Those technologies utilize optical interconnects over fiber to deliver gigabit datarates over hundreds of meters (Fig. 1.3). The transition from copper-based communications to OI brings multiple improvements [8], and is made possible thanks to state-of-the-art light emitters and detectors that can operate beyond 50 Gbps [9, 10]. Vertical Cavity Surface Emitting Lasers (VCSELs) have been on the forefront of research allowing the miniaturization of fiber-optical interconnect transcievers.

In addition to data center networks, energy efficient optical interconnects are utilized in a variety of fields. In automotive industry, they are used as intra-vehicle network buses using polymer fibers [11, 12]. In a similar fashion, free space optical communications are used in intra-aircraft and intra-satelite communication networks [13].

1.2 Thesis outline

This thesis is aimed towards exploring the field of high speed electronics for short-range optical interconnects suitable for data communication applications. The goals of such an task were to achieve datarates of 50 Gbps and 100 Gbps with as low energy consumption as possible. This thesis consists of two parts. Part I is a general

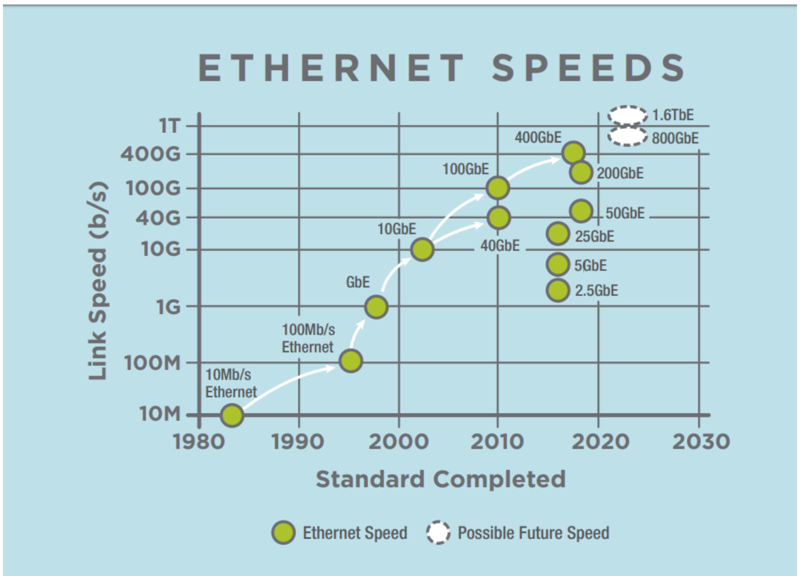


Figure 1.3: Existing and upcoming Ethernet standards [7].

introduction to the field and puts the appended papers in context. In Chapter 2, I provide the background of short-haul optical interconnect systems as well as the limitation imposed by the optoelectronic components. In Chapter 3, I review the relevant literature in receiver circuits, summarize some notable circuit topologies and present our contribution to the field. Then in Chapter 4, I conclude Part I of this thesis.

Part II contains the appended papers. The contributed papers attempt to cover most of the components found in a short range fiber optic receiver system. In Paper A, we demonstrate a 250 nm InP Double Heterojunction Bipolar Transistor (DHBT) ultra-broadband distributed amplifier. In Paper B, we demonstrate a 130 nm SiGe Heterojunction Bipolar Transistor (HBT) receiver front-end consisting of a Common Base, broadband transimpedance amplifier optimized for low input impedance. In Paper C, we demonstrate a 130 nm SiGe HBT tunable gain feed forward equalizer optimized for VCSEL-based short-range communications. In Paper D, we propose two transimpedance amplifier topologies designed on a 130 nm InP DHBT process, achieving bandwidth higher than 133 GHz.

Chapter 2

Short range fiber-optical data communication system

This work is part of the Multi-Terabit Optical Interconnects (MuTOI) project. The project focuses on the demonstration of a fiber-optical data communication system suitable for short-range interconnects commonly used within internet data-centers and hyper-computing clusters.

2.1 System overview

A fiber-optical data communication system follows the main design principles of typical communication systems: there is a transmitter, a transport medium, and a receiver. The transport medium is an optical fiber instead of a copper wire (as in typical wired communications); therefore, the signal changes from electrical to optical and then from optical back to electrical. In the transmitter, the electrical signals are converted to optical via a laser diode; then in the receiver they are captured by a photodector and converted to electrical form.

2.1.1 Top view

The top view of a typical fiber-optical system is presented in Fig. 2.1. In such a system, the transmitter and receiver subsystems are hybrid opto-electronic systems. More in-depth discussion on these hybrid systems is presented in Section 2.2. The figure assumes that a synchronous clock is provided both at the transmitter and at the receiver. In a real system, the receiver typically has to extract the clock and digital data from the received asynchronous analog signal. The subsystem that performs this function is called Clock and Data Recovery block (CDR) [14]. A further break-down of the system into its components is presented in Fig. 2.2, including the common blocks of the transmitter and receiver subsystems. The figure also indicates whether the data is represented as voltages, optical signals, or currents as well as whether the data is in analog or digital format. The system in Fig. 2.2 is broken down into two subsystems in addition to the optical transport medium: the

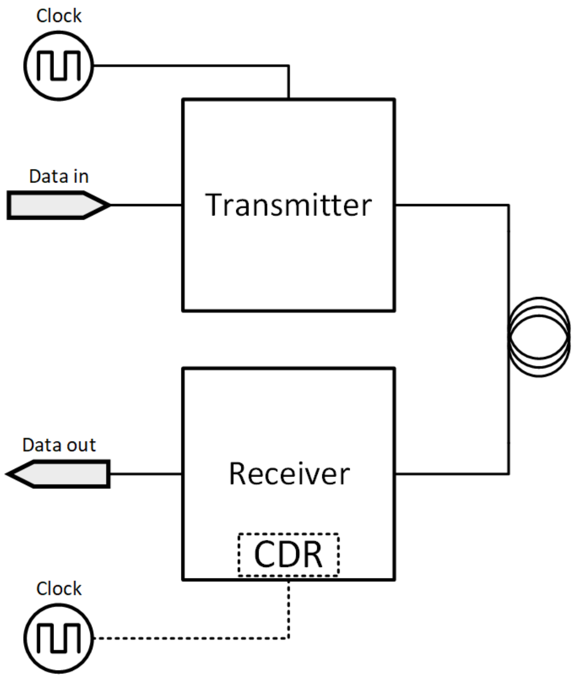


Figure 2.1: Fiber-optical system top view.

transmitter subsystem (TX) and the receiver subsystem (RX). The optical transport medium includes the optical fiber, the electrical-to-optical conversion block, and the optical-to-electrical conversion block. In this work, we assume a vertical cavity surface emitting Laser (VCSEL) as the electrical-to-optical conversion block and a P-i-N photodiode as the optical-to-electrical conversion block. Those components are then integrated with the electronics at a system level (heterogeneous integration).

2.1.2 Transmitter subsystem

A complete TX subsystem consists of one or multiple data inputs and a clock input if the clock is not generated in the transmitter. An encoding block after the data inputs might be used applying error redundancy algorithms such as forward error correction (FEC) which has been shown to improve performance of VCSEL based links [15]. Additionally, a variety of data encoding or modulation schemes (further discussed in Section 2.3) can be used in order to achieve trade-offs between the bandwidth utilisation, data throughput, and signal to noise ratio (SNR). Most state of the art TX subsystems also include a form of pre-emphasis or pre-distortion of the signal in order to compensate for the characteristics of the output amplifier and the transmission channel, which in this case is dominated by the laser-photodiode performance. An analog or digital-to-analog front-end amplification block is used last in the chain in order to amplify the data in the correct voltage-current swing required for the optimal operation of the laser.

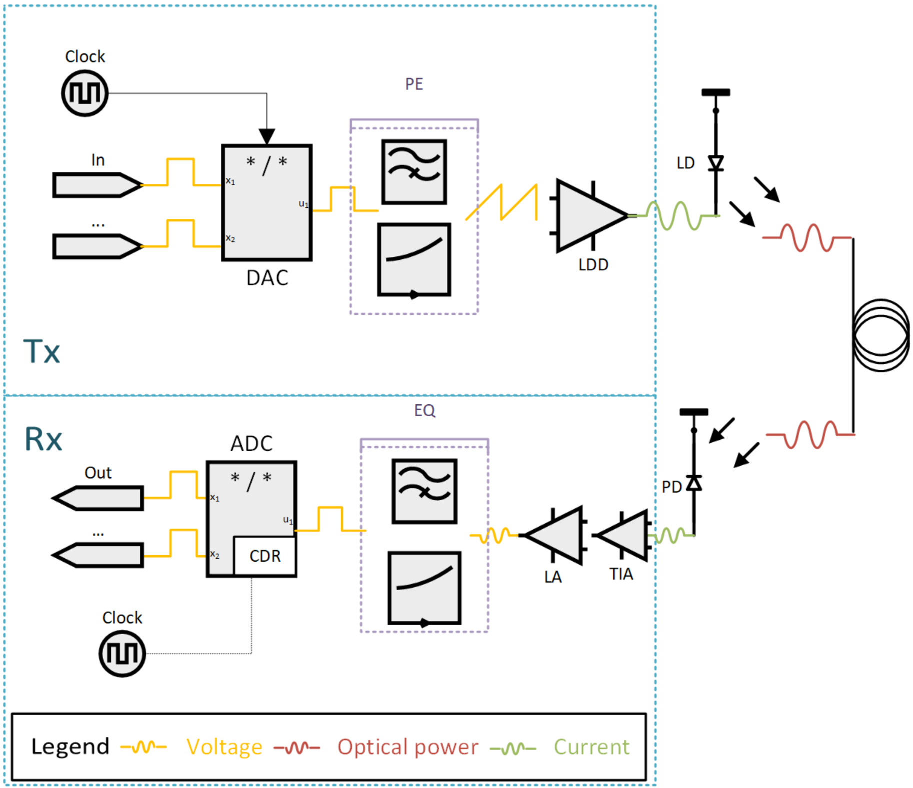


Figure 2.2: Optical link breakdown with the receiver (RX) and transmitter (TX) subsystems.

2.1.3 Receiver subsystem

The RX subsystem with a front-end transimpedance amplifier (TIA) interfacing with the photodiode converting the photo-current generated into voltage signals. The TIA is usually followed by either a limiting amplifier or a linear amplifier depending on the complexity of the modulation scheme. Then an equalization block is used to further compensate for the channel and TIA bandwidth limitations. Additional blocks for correcting jitter and amplitude variations are also used in order to allow proper decoding and clock retrieval.

2.2 Optoelectronics

While several varieties of directly modulated lasers are used in short-haul optical data communication systems, the field is dominated by VCSELs and multi-mode fiber (MMF) links [16]. Continuous wave lasers modulated by Mach Zehnder modulators (MZM) are also utilized on long-haul high-capacity interconnect systems. For the receiver, p–i–n photodiodes are the most common photodetectors for such links due to their lower junction capacitance and higher bandwidth and lower bias voltage compared to avalance photodiodes (APD) [17].

2.2.1 VCSELs

VCSELs are one of the primary light sources used in datacom applications. The main structure of a laser diode is still present in a VCSEL; it consists of a light amplification medium between two mirrors with very high reflectivity. By increasing the bias current through the diode, as illustrated in Fig. 2.3, the rate of electrons passing through the gain medium increases. When the current increases past a minimum value called threshold current, the device starts lasing and further current increase causes an increase on the rate of photons generated and emitted. VCSELs, as opposed to typical light emitting diodes, uses mirror structures called distributed Bragg reflectors (DBR) instead of simple mirrors. These structures are formed by alternating thin sheets of high and low refractive index to achieve near perfect reflectivity. A second significant difference is that VCSELs emit light vertically, as opposed to edge-emitting lasers, which allows multiple VCSELs to be fabricated and measured on a wafer without the need of dicing [17].

In terms of operation, the VCSEL is a nonlinear load whose frequency and transient behavior change based on a number of factors such as the biasing conditions, temperature, and parasitics. The physical aspects of the VCSEL define most of its behavioral traits: the wavelength of emission, the jitter, the conversion efficiency, the linearity, the power consumption, the bandwidth and any oscillations on high frequency modulation, and the threshold current. VCSELs are typically biased and modulated by currents in the order of a few mA - typically 1-18 mA. The VCSEL must always be operating above threshold to avoid the turn on delay, in order to cope with high modulation frequencies, so typically a margin of about 1–2 mA above threshold is used [17].

In Fig. 2.4a, the I-V curve of a high speed VCSEL is shown for room temperature (RT) and at 85°C along with its corresponding I-P curve. The former can provide information about the device's dynamic resistance. The latter gives information regarding the threshold current, the thermal rollover, as well as the slope of the I-P curve. The slope efficiency given as $\frac{\Delta P}{\Delta I}$ is a measure of the VCSELs slope of output optical power to input current. The curve is an indication of the VCSEL's operating

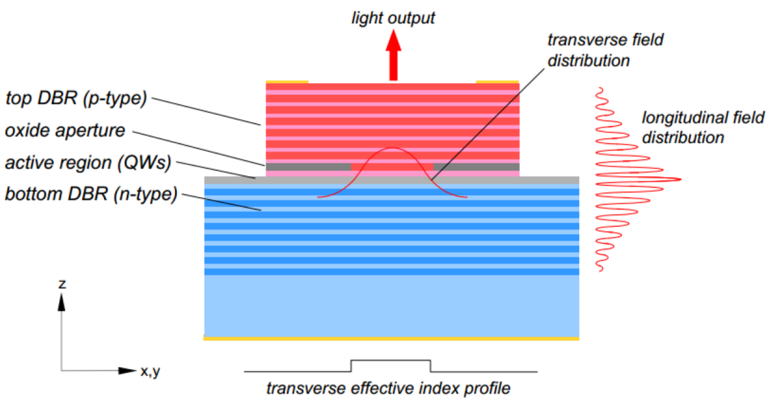
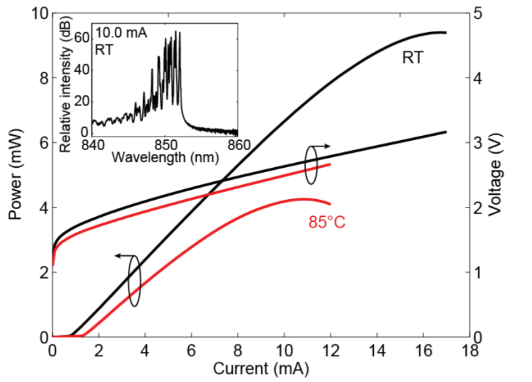
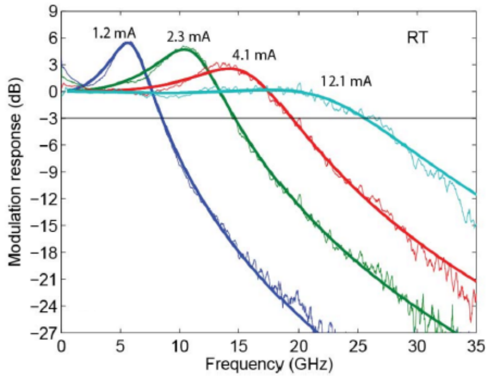


Figure 2.3: Cross-section of a typical VCSEL [17].



(a) VCSEL IPV curves at room temperature (RT) and 85°. Inlay: wavelength of emission.



(b) Modulation response of a VCSEL at room temperature (RT) for various bias currents.

Figure 2.4: IPV and modulation response of a state-of-the-art 850nm VCSEL [9].

current range as well as the output power. The difference between the maximum optical power generated and the minimum optical power above threshold gives the optical power extinction ratio (ER) which is specified in dB. As shown in Fig. 2.4a, the optical power becomes non-linear at high operation currents (thermal rollover) and close to the threshold. Therefore, for large signal modulation suitable for high extinction ratio, the optimal bias point would be at the middle of the linear curve.

In Fig. 2.4b, the modulation response of a state-of-the-art 850nm VCSEL is given for various bias currents. The modulation bandwidth of the VCSEL evidently depends on the bias current. Therefore, the optimal bias point and optical modulation amplitude are dependent on the type of modulation used [18].

2.2.2 Photodiodes

A photodiode is a diode that, under zero bias or reverse bias, generates a current proportional to the incident optical power. Two main varieties of photodiodes are used in fiber-optical communications, P-i-N or PIN photodetectors and avalance photodetectors (APD). PIN photodetectors are based on a P-i-N doped structure with an intrinsic region between the p and n doped regions. While this PD can be used in the so called photovoltaic mode (without any bias), generally a reverse bias is applied (photoconductive mode) in order to ensure that the intrinsic region is fully depleted. APD photodetectors are similar in design but typically larger and while they provide amplification of the incident light via avalance multiplication they have increased noise and larger capacitance. Additionally, they require higher reverse bias voltages to operate [19].

PIN PD performance

Photodiodes used in short-haul high-speed optical interconnects have three main characteristics of interest: the responsivity, the bandwidth, and the noise. The

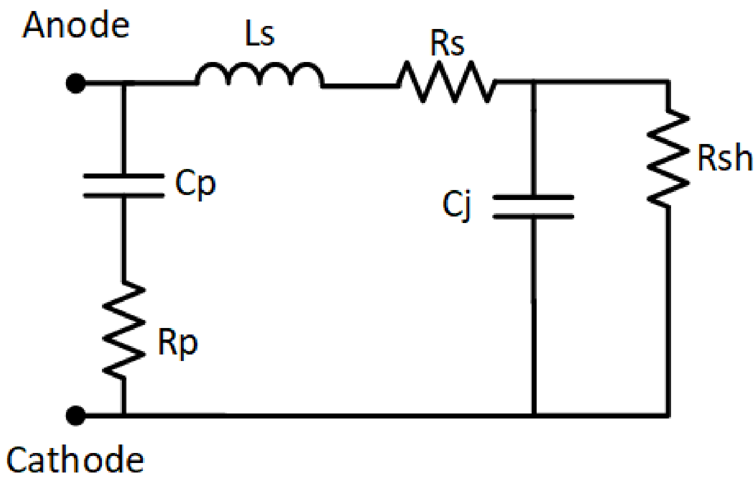


Figure 2.5: PD parasitics model.

responsivity (R), measured in amperes per watt ($\frac{A}{W}$), gives the photocurrent generated as a response to optical power incident on the photodiode's aperture at a given wavelength. The current generated by the photodiode is called photocurrent (I_{ph}) and is given as:

$$I_{ph} = R \cdot P \tag{2.1}$$

R is the responsivity of the PD and P the received optical power.

The modulation bandwidth of operation (3-dB bandwidth) is dependent on the physical limitations of the photodiode. The parasitic components of a PIN photodiode are shown in Fig. 2.5. The parasitics include the bond-pad of the PD in the form of the pad capacitance C_p and resistance to ground R_p. A series inductance L_s and resistance R_s represent the traces from the pads to the junction as well as the junction series resistance. The main components are represented by the junction capacitance C_j and the shunt resistance R_{sh}. In photovoltaic mode, there is another term in addition to the junction capacitance, the diffusion capacitance, but when reverse bias is applied it becomes negligible.

When the PD is operated in photoconductive mode and is connected to an amplifier it becomes loaded by the amplifier's input impedance (R_L). While an ideal TIA should have zero input impedance, real systems have an impedance of typically up to 50 Ω. In that case, the overall frequency response of the PD-TIA system is that of an RC low-pass filter. The shunt resistance is generally very large compared to R_L so it can be neglected. The pad capacitance C_p can be combined with C_j, making it C_{PD}. The response of the PD-TIA system is therefore limited by R_L and C_{PD} [20].

Photodiode noise

The noise of the photodiode is a combination of shot noise, thermal noise, and $1/f$ noise [20]. In addition, a leakage current called dark current (I_{dark}) appears even in the absence of optical signal. This is a reverse current across the junction and stems from thermal generation of free carriers [17].

The $1/f$ or flicker noise becomes significant at lower frequencies, however in this work we assume a lowest frequency in the order of a few kHz; therefore, we can neglect that term. The dark current contribution is dependent on the reverse bias of the PD (V_A).

$$I_{dark} = I_{SAT}(e^{\frac{qV_A}{Nk_BT}} - 1) \tag{2.2}$$

Where q is the electron charge, K_B is the Boltzmann constant, N is the diode ideality factor, T the absolute temperature, and I_{SAT} the reverse saturation current. For the PIN diodes considered in this work, the optimal bias for high speed operation is -5 V [10]. Under that condition the dark current is in the order of a few nA [19]; therefore, it becomes negligible compared to the other noise terms discussed below.

The thermal noise is given as:

$$\overline{i^2_{n,Th}} = \frac{4k_BT\Delta f}{R_{sh}} \tag{2.3}$$

Where q is the electron charge, Δ_f is the bandwidth over which the noise power is integrated, T the absolute temperature, and R_{sh} is the shunt resistance of the PD. For 30 Gbps+ PIN photodetectors this is in the order of 250 $k\Omega$ [10].

The diode shot noise is the most significant factor and is given as:

$$\overline{i^2_{n,sh}} = 2q \cdot (I_{ph} + I_{dark}) \cdot \Delta f \tag{2.4}$$

Where q is the electron charge, Δ_f is the bandwidth over which the noise power is integrated, and I_{ph} is the photocurrent given in equation 2.1. As shown in equations 2.4 and 2.3, the noise is dependent on the bandwidth of the receiver. For 50 GHz bandwidth, I_{ph} of 0.4 mA, R_{sh} of 250 $k\Omega$, and neglecting the dark current, equations 2.4 and 2.3 indicate that the shot noise contribution is ≈ 2000 times larger than that of the thermal noise. However, that does not take into consideration the noise contribution of the TIA, which will be discussed in the next chapter.

In Fig. 2.6 we can see the simplified equivalent model of the photodiode when used in combination with an amplifier. The model includes the photocurrent I_{ph}, the PD parasitics, the TIA's input impedance loading the PD R_L, the equivalent noise source of the PD $I_{n,pd}$, and the dark current of the PD I_{dark}.

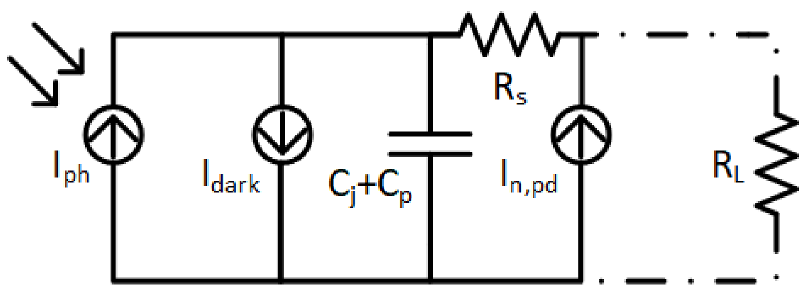


Figure 2.6: PD equivalent model.

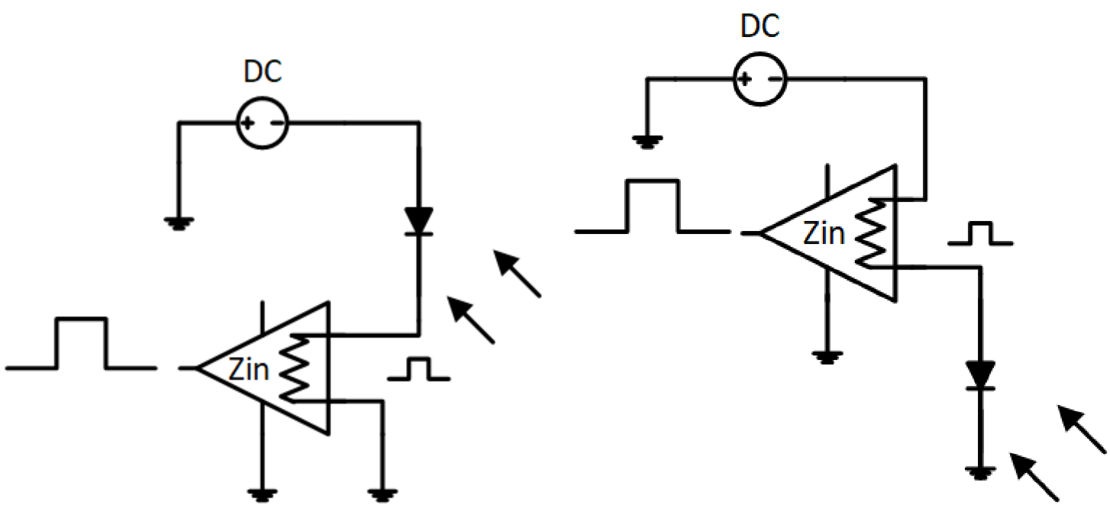
Biasing and coupling

The biasing of the photodiode and the coupling with the amplifier can take two forms: AC and DC coupling. On DC coupling we can also further distinguish into: common anode, when the anode terminal is grounded for the AC signal, and common cathode, when the cathode is grounded. The two alternative coupling modes can be seen in Fig. 2.7. The ideal TIA has zero input impedance (Z_{in}), however in practice the input impedance is typically 50 Ω.

The common-anode architecture is preferred when the voltage at the input of the transimpedance amplifier (V_{in}) can be kept stable by other circuit components despite the variations of the photo-current. The reverse bias of the photodiode must be typically at or above 2 V so the V_{in} of the circuit should provide that exact voltage while the photodiode anode would be grounded. This can be a challenge since it requires the design to be shifted +2 volts, which also calls for more careful design to not surpass the breakdown voltage limits of the transistors; as an example the fast HBT devices in 130 nm SiGe BiCMOS process have a $V_{B,CE}$ of approximately 1.5 V [21, 22]. Alternatively, if a negative voltage supply is available it should replace the ground in the anode, thus alleviating the aforementioned issues, in the expense of symmetric supply, which will increase the number of DC-pads required, thus increasing the chip size.

The common cathode is less challenging to realise with an additional external bias on the photodiode, thus eliminating the need for biasing through the input of the TIA. In this method the voltage across the diode will be $V_{bias} - V_{diode}$ where the later is the voltage drop across the diode junction. This voltage will be "seen" at the input of the TIA and should be taken into account when designing the input stage.

Even though in literature AC coupling of the input source is used in narrow-bandwidth tuned low noise amplifier design, it cannot be applied in the context of



(a) Common Anode. (b) Common cathode.

Figure 2.7: Different PD-TIA coupling topologies used in literature.

this project. NRZ data have a broadband spectrum that can span from kHz to GHz. Therefore, an AC coupled connection between the PD and the TIA would eliminate the low frequency components of the signal, and consequently introduce errors.

2.3 Modulation formats

Short-haul fiber-optical data communication systems are dominated by NRZ amplitude modulation formats. The simplest and most commonly used is the binary On-Off Keying (OOK) modulation. It is straightforward to realise and measure transceivers based on this modulation. Additionally, binary OOK modulation imposes less strict SNR-requirements than higher modulations, and therefore less strict noise requirements. Essentially it is simply a binary method of signaling, with '0' typically mapped to no signal or low optical power, and '1' to a signal pulse or high signal power. However, that means that the bit-rate is the same as the baud-rate. Therefore, for 100 Gbps data-rates a bandwidth of approximately 100 GHz is required, which can prove very challenging to realize due to the bandwidth limitations of the optoelectronic components mentioned above. The state-of-the-art performance for VCSEL-based OOK optical link achieved is 71+ Gbps at the time of this report [23, 24].

In order to transmit more data in a bandwidth-restricted channel, M-ary digital modulation schemes are utilized. The most common is 4-level Pulse Amplitude Modulation (PAM-4). In comparison with OOK, which can be considered PAM-2 modulation, PAM-4 transmits double amount of information for the same bandwidth. Alternatively the bandwidth can be reduced to 50 GHz, which will allow a baudrate of 100 Gbps. The trade-offs in this case are: the SNR penalty imposed, which is at least -6 dB; the increased complexity of encoding and decoding blocks on the transceivers; and the increased complexity of characterization and measurement. The state-of-the-art in binary PAM-4 modulation VCSEL based links are 90+ Gbps [25, 26] and 110+ Gbps in duo-binary PAM-4 [27].

As mentioned earlier, an important metric in short haul fiber-optical interconnects is power consumption. However, the main goal of the field is to increase the datarate. Therefore, the energy consumed per bit of information sent is used as a means to measure the efficiency of datacom systems. This figure of merit is called energy efficiency (η_e) and is measured in $\frac{\text{pJ}}{\text{bit}}$ or $\frac{\text{mW}}{\text{Gbps}}$.

2.4 Transceiver electronics

As discussed above, the communication channel is heavily limited by the optoelectronic devices. However, even the simple modulation formats mentioned impose high requirements to the integrated electronic circuit design. Thankfully, due to the continuation of Moore's law on silicon devices and with the increasing maturity of III-V integrated devices, there are several processes suitable for the task.

Advanced deep sub-micron CMOS processes dominate on low-baud-rate high-energy-efficiency transceivers, especially with advanced silicon on insulator (SOI) and Fin-FET processes [28]. Additionally, they provide millimeter-wave components such as high frequency inductors and capacitors, and characterization tools suitable for RF applications driven by the 5G mobile network, datacom, and automotive industries. On the other end of the spectrum, Indium Phosphide (InP) double heterjunction bipolar transistors (DHBTs) and other III-V-material-based technologies that have traditionally been used for high-power or THz RF applications are becoming more common in the field. By reaching higher scales of integration and providing more interconnect layers, they enable transceiver circuit designs with unprecedented baud-rates. Lastly, the continuous advancement of Silicon Germanium heterostructure bipolar transistor (SiGe-HBT) and Bi-CMOS processes come to bridge the gap between the aforementioned processes both in performance and in production volume. In the core of this progress lies the added benefit of monolithically integrated photonic components; silicon photonics in CMOS processes, germanium photodetectors on SiGe, and lasers and photodetectors grown directly on InP transceivers.

In the next chapter, I will discuss the specific merits of each process in receiver electronic circuit design.

Chapter 3

Broadband Receiver Electronic Components

In this chapter, I discuss the basic building blocks of a broadband electronic fiber-optical receiver system. I begin with a review of the most prominent receiver front-ends and complete receiver systems in literature, broken down the semiconductor technology used and rated in regards of power consumption and bitrate. Then I analyze the basics for the transimpedance amplifier, broadband amplifier, and equalizer circuits and present our contribution to the field for each respective sub-module.

3.1 Literature review on receiver systems

In order to establish the current state of the field, a thorough but not exhaustive literature review was performed; the results are presented in Fig. 3.1. The focus of the review was on fiber-optical interconnect receiver systems and receiver system blocks, and they were evaluated in terms of two important performance metrics: power consumption and bitrate. The combination of those two values provides the figure of merit for such systems: the energy efficiency, as defined in the previous chapters. The reviewed works were classified based on the technology used in order to further illustrated the pros and cons of each technology.

Several trends are clearly visible in Fig. 3.1. Silicon-based CMOS systems offer the lowest power consumption but fall behind in terms of bitrate. The highest-performing CMOS-based receiver is designed and fabricated in deep sub-micron state-of-the-art FinFET technology [28], in order to benefit from high unity-gain frequency. However, some of the most prominent designs are achieved with more conventional 65 nm CMOS [42, 48], 90 nm CMOS [34] and even 180 nm CMOS [33]. The main benefit of CMOS-based processes, aside from their compatibility with the contemporary switching and network equipment, is the high degree of integration and digital logic that can be implemented monolithically. Therefore, most CMOS-based systems also include a variety of additional subsystems: bias-generation

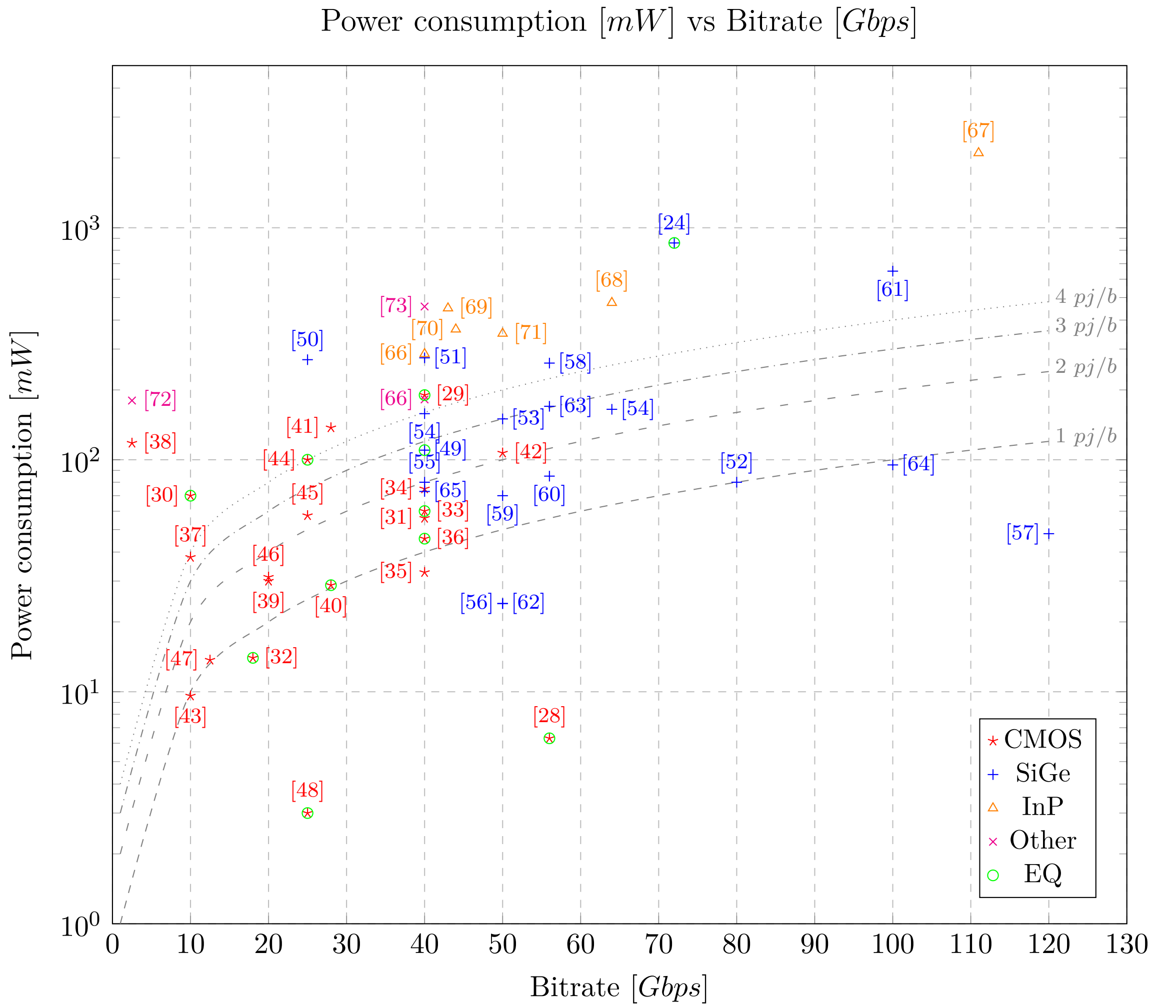


Figure 3.1: Prominent receiver system publications based on reported measured bitrate and power consumption.

blocks, DC-offset cancellation, automatic feedback/gain control, digital equalization etc. Those subsystems are non-trivial to realise in HBT-only technologies.

Systems designed in InP processes typically are the most power-consuming, but also provide some of the highest bit- and baud-rate receivers. Due to their high gain and very high f_t and f_{max}, InP based systems have demonstrated the highest performing TIA-Demultiplexer system [67]. It is evident however, that the power consumption, and consequently the energy efficiency of such systems is relatively high.

SiGe-based systems fall in the middle between the two aforementioned technologies. This is partly due to the increased frequency of operation compared to Si-CMOS. Additionally, most SiGe technologies offer high-performing HBTs built on top of an existing and mature CMOS process with high-density metal system. In that way, the SiGe BiCMOS processes get the best of both worlds: high CMOS integration for digital control blocks, and higher f_t and f_{max} due to the high-speed

HBTs provided. The limiting factor is that the processes available in SiGe have not achieved the maturity and miniaturization that silicon-based CMOS have. During the later half of this decade, several state-of-the-art receivers have been published [24, 54, 60, 64, 65], demonstrating the growing maturity of SiGe-based processes.

State-of-the-art systems until 2015 used OOK to achieve competitive results [24, 65], with the exception of CMOS based designs. After that point in time however, higher modulation schemes became more prominent (PAM-4, duo-binary, PAM-8) even on the faster SiGe and InP based processes [54, 61].

As discussed in the previous chapters, the optoelectronic components have typically modulation bandwidths in around 25 GHz - 30 GHz. Therefore the electronic circuits must employ an array of bandwidth extension or equalization methods in order to receive 50 Gbps+ datarates. The most common bandwidth extension methods used are: inductive peaking [64], staggered gain peaking [65], continuous-time linear equalization (CTLE) [74], and decision-feedback equalization (DFE) [75].

3.2 TIA

The transimpedance amplifier (TIA) is a core component to any system that amplifies current with low input impedance. This is important for fiber-optical communications in the receiver design, where a photodetector converts incident light into a small photocurrent. That photocurrent (in the order of a few hundred μA) is in turn converted into a voltage by the TIA. The voltage output of the TIA is in the order of a few mV and requires further amplification to be quantized and converted into digital-logic values.

3.2.1 TIA figures of merit

The main figure of merit for a current-to-voltage amplifier is the transimpedance gain which is typically given as V_{out}/I_{in} or Ω of transimpedance, or $dB\Omega$ through equation 3.1.

$$A_{TI}[dB\Omega] = 20 \times log(\frac{V_{out}}{I_{in}}) \tag{3.1}$$

Noise is a very important measure of TIA performance. Since TIAs are used as the first stage of the receiver system, they are the main contributors of the system's entire noise performance. The noise of the TIA is given as a noise spectrum, which by integrating over the bandwidth and dividing by the TIA gain at the mid-band point R_{TIA}, gives us the input-referred rms noise current ($i^{rms}_{n,TIA}$) as seen in equation 3.2 [76].

$$i^{rms}_{n,TIA} = \frac{1}{|R_{TIA}|}\sqrt{\int_0^\infty |Z_{TIA}(f)|^2 \times I^2_{n,TIA}(f)df} \tag{3.2}$$

Where $Z_{TIA}(f)$ is the frequency response of the TIA, and $i^2_{n,TIA}(f)$ is the output-referred noise spectrum of the TIA.

While gain and noise are important for receiver circuits, power consumption is always relevant in any circuit design. As mentioned in Chapter 2.3, there is an evident need to maintain as high energy efficiency as possible.

An additional limitation in TIA design is the maximum optical current that can be tolerated (I_{MAX}). This is the maximum current that the TIA input stage can tolerate before going into compression, which would affect the jitter and bit error rate (BER). In order to optimize the design for I_{MAX} we can find the maximum photocurrent that the given PD can generate. This is limited by the maximum optical power that the PD can receive multiplied by its responsivity as shown in equation 2.1. Additionally, the receiver's sensitivity is defined by the ability to detect very small currents, which is in turn limited by noise. The smallest detectable current typically is orders of magnitude smaller than the I_{MAX}, therefore the receiver needs to have a very large dynamic range.

Bandwidth is the frequency range at which the amplifier provides adequate amplification and is defined up to the frequency where the gain of the receiver drops by 3 dB. In TIA and receiver design, there are several bandwidth-limiting factors. The photodetector capacitance seems to be an important limitation in state of the art technology. The intrinsic junction capacitance is on the order of 20–100 fF for the 30 GHz bandwidth photodetectors [10]. That parasitic capacitance is also approaching the value of the bond-pad capacitance which is typically $\approx$ 10–60 fF on either side of the wire-bond. Additionally, depending on the topology of the first amplification stage, the TIA input capacitance must also be taken into account. The total capacitance of the PD (including the parasitic and pad capacitances), the TIA input impedance, and the feedback resistor (if any) define the frequency performance of the system in terms of an R-C response as shown in equation 3.3.

$$BW_{PD-TIA} = \frac{1}{2\pi R_{in}(C_{PD} + C_{TIA})} \tag{3.3}$$

By reducing the input resistance of the TIA (R_{in}), we can improve the receiver bandwidth [77, 78]. However, the noise of the system would increase proportionally. Therefore, while designing for very low input impedance is beneficial for bandwidth-limited systems, it will affect the noise performance. Additionally, any stage after the input stage affects the total Gain-Bandwidth product of the system and typically extra measures are taken in order to keep a large bandwidth together with adequate gain. It is natural that the performance is also limited by the maximum oscillation or transition frequency (f_t), and the maximum unit current gain frequency (f_{max}) of the transistors in any given process.

A figure of merit seen in equation 3.4, as given by Voinigescu [76], combines most of the aforementioned design goals of a broadband transimpedance amplifier:

$$FoM = \frac{Z_{TIA} \times I_{MAX} \times BW_{3dB}}{i_{n,TIA}^{rms} \times P_{DC}} \tag{3.4}$$

Another consideration in addition to the bandwidth and gain of the amplifier is its linearity. In this context, linearity refers to the transient behavior of the TIA in respect to gain compression; sufficient linearity can be achieved by biasing the amplifier within its linear region of operation. If a TIA-PD receiver is meant to be used not only for OOK, but also PAM-4 modulation, a linear response is required in order for all three levels in an eye-diagram to be sufficiently open. In order to maintain linearity on the receiver system level, a typical design practice is to include a variable gain amplifier after the TIA stage in order to tune the overall TI-gain of the receiver. Additionally, the input stage of the TIA must have sufficiently high I_{MAX} as mentioned earlier. Alternatively, tunable feedback can be used on the TIA to adjust the transimpedance gain. Most TIAs in literature are linear and use gain tuning in order to adjust to different input signal amplitude scenarios. However OOK-optimized designs use limiting amplifiers, cascaded after the TIA stage in order to improve the eye opening and reduce the requirements on the analog-to-digital conversion and clock retrieval blocks [14].

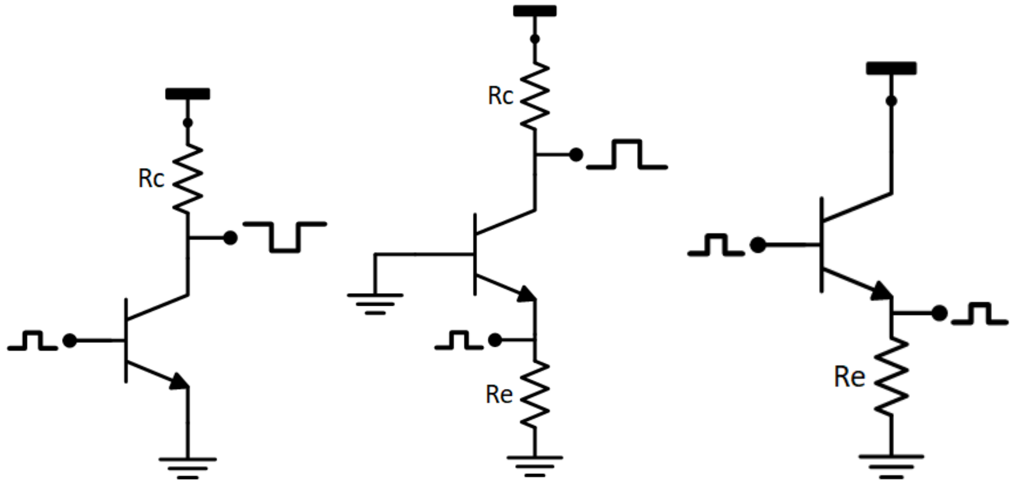
3.3 Broadband Amplifiers

As described in the beginning of this chapter, in order to achieve 100 Gbps communication while maintaining low energy per bit, we need to utilize high-end semiconductor processes and clever design implementations. In order to do that, we choose to design in SiGe- and InP-based technologies since they represent the majority of the published work beyond 40 Gbps. By making this decision, we commit to HBT- and DHBT-based topologies and a relatively low degree of integration when compared with what is possible in CMOS processes. The most prominent broadband amplifier topologies in literature are briefly presented in this section.

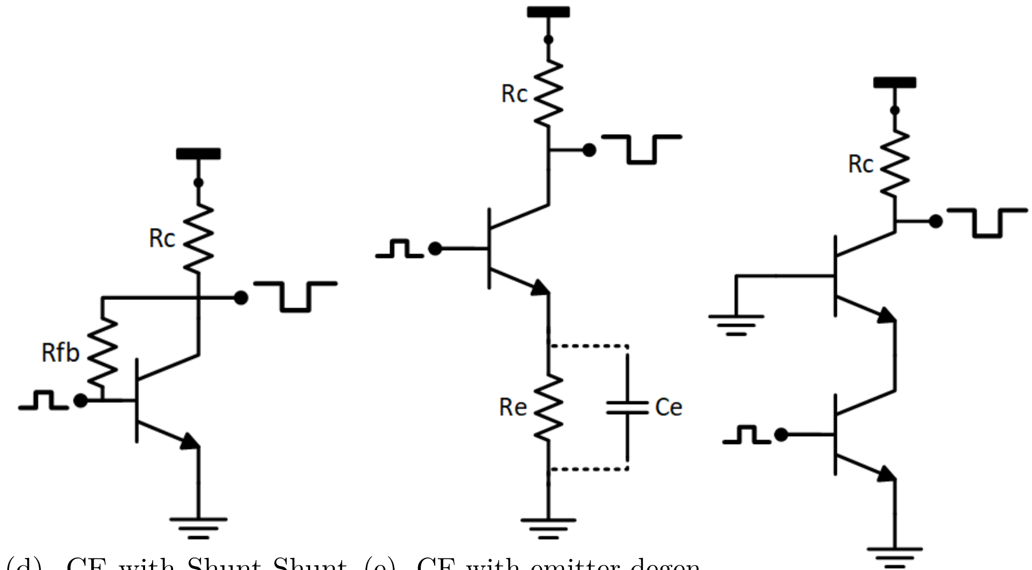
3.3.1 Single stage amplifiers

An abundance of different amplifier topologies are used in TIA designs. In this section, the most prominent topologies in HBT and DHBT technologies will be presented and evaluated based in the amplifier criteria presented in the previous paragraph.

The common emitter amplifier is the most commonly used amplifier in literature (Fig. 3.2a). It has high current and voltage gain, adequate bandwidth (mainly limited by the Miller effect if not counteracted), and can be very stable in variation and temperature with proper bias networks and emitter degeneration (Fig. 3.2e). The relatively high input impedance provided by CE can be very beneficial in OP-amp design where an ideally infinite input impedance is wanted. However, in TIA design, where a low input impedance is optimal, this is typically addressed with shunt-shunt feedback in order to lower the input impedance seen by the photodiode (Fig. 3.2d). One additional downside, as mentioned, is the Miller effect which can degrade the bandwidth of the CE stage. It should be noted that the most successful CE architectures depend on emitter degeneration, as seen in Fig. 3.2e, in order to achieve the aforementioned merits (stability, etc) by sacrificing gain.



(a) Common Emitter. (b) Common Base. (c) Common Collector.



(d) CE with Shunt-Shunt feedback. (e) CE with emitter degeneration. (f) Cascode amplifier.

Figure 3.2: Single ended amplifiers.

The common base (CB) amplifier seen in Fig. 3.2b is prevalent in TIA literature due to its innately low input impedance and its immunity to the Miller effect which is commonly one of the main bandwidth limitations in amplifier design. In addition to those merits, it also provides high voltage gain and high output impedance, all of which are preferred in TIA design. However, CB input stages tend to be more noisy than other single-transistor architectures since the noise of the transistor contributes directly to the input noise. CB stages can be used with or without feedback. Careful design is required to maintain the base ”ground” connection for all frequencies and in biasing the stage since the input AC current can destabilize the quiescent point. The common base due to the very low input impedance, in combination with high gain, was used extensively in optical communication systems since the 1980s [77].

Common collector amplifier stages shown in Fig. 3.2c are a versatile tool in broadband amplifier design. With high input impedance, low output impedance, and near-unity voltage gain, they serve as buffers and DC-level shifters between other amplification stages. Due to their very high current gain, they are often used as output stages to drive the standard loads of 50 Ω. Alternatively, they can easily be used as input buffers with broadband matching to 50 Ω with appropriate resistors used.

3.3.2 Multiple-transistor amplifiers

The cascode circuit shown in Fig. 3.2f is a very common circuit topology originating from vacuum tube amplifier design [79]. It consists of the cascade of a common emitter stage feeding into a common base stage. The CB stage serves as a current buffer to the CE stage; therefore, the overall gain of the two stages is similar to that of the CE amplifier. The very low input impedance of the CB stage serves as the load impedance for the CE stage which diminishes the effects of the Miller capacitance. The cascode is a very stable amplifier due to its very high isolation. The cascade of these two stages provides a higher bandwidth than the CE stage due to the Miller effect being diminished, but it also requires higher voltage headroom and an additional bias supply for the CB stage. The main downside of the cascode for TIA design is, similarly to CE, the high input impedance, which needs to be reduced through feedback, reducing the gain.

Differential amplifiers also originate from the era of vacuum tube designs [80]. They are amplifier stage pairs sensitive to differences between their two inputs. The main benefit of such circuits is the common mode rejection. They amplify differences between the inputs and dampen signals or noise which are common in both inputs [81]. There are a few varieties of differential amplifiers, but the majority are based on the CE differential pair which is discussed in the following section.

The differential CE amplifier is a combination of two CE stages as shown in Fig. 3.3a. The stages are connected to a shared current source and their input signal is out of phase. This topology amplifies the differences between the inputs and the main benefit of such a design is that the total output swing doubles. In addition to that, signals that are common between the two inputs are canceled out (common mode rejection). However, the design becomes more complex due to the doubling of load resistors, transmission lines etc. and the voltage headroom has to be increased to accommodate the current source.

The cascode differential pair seen in Fig. 3.3b is a variation of the CE differential pair, with the addition of a common base stage to each of the CE devices. It combines the benefits and drawbacks of the cascode stage mentioned in section 3.3.2 and the CE differential pair discussed above.

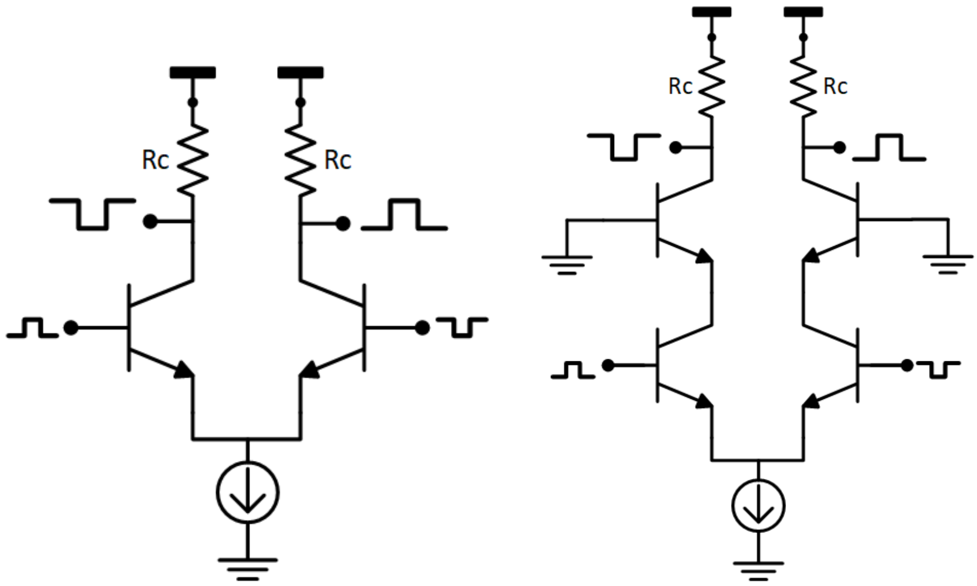
3.3.3 Distributed Amplifiers

The distributed amplifier consists of several amplifier cells connected in parallel with matched transmission lines at the input and output as shown in Fig. 3.4. The transmission lines are designed so that the signal that travels down the line of the amplifiers and interferes constructively at each stage. This is accomplished by carefully designing the transmission lines for the appropriate phase delay, including the input and output parasitics of each cell in the design. The benefits of this architecture are the large gain, but most importantly the ultra-wide bandwidth. While distributed amplifiers have been used for instrumentation and long-haul optical communication links, they are typically too power consuming for the energy efficiency driven approach of short-haul communications.

3.4 Bandwidth Enhancement and Equalization

There are several techniques to increase the bandwidth of a TIA, however each one has a trade-off. The most common way to extend the bandwidth of a TIA, and maintain a low input impedance is to use feedback. The most common type of feedback used is negative shunt-shunt feedback, comprising of a simple resistor between the output and the input of the TIA. Inductive feedback is also used to achieve peaking and improve the total bandwidth [57]. However, large inductors (in the order of a few nH) are bulky and do not work for very high frequencies, due to their self-resonance, thus are avoided in monolithic microwave integrated circuit (MMIC) design.

Inductive peaking and capacitive degeneration are two very common ways to extend the bandwidth of an amplifier stage. In the former case the inductor connected in series with the load of the amplifier increases the load impedance at a certain frequency based on the inductance, subsequently increasing the overall gain of the amplifier (peaking) around that frequency [36]. Capacitive degeneration is most



(a) Differential CE. (b) Differential Cascode.

Figure 3.3: Differential amplifier topologies.

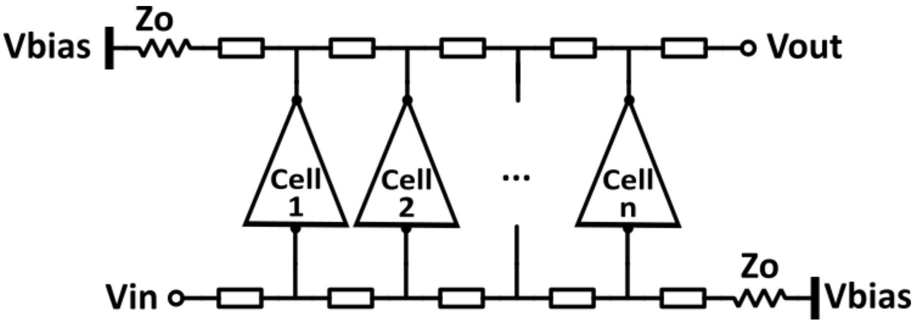


Figure 3.4: Typical topology of a distributed amplifier.

commonly used with CE and differential CE amplifiers in combination with resistive degeneration. The resistive degeneration reduces the amplifier gain, thus expanding the bandwidth; while the capacitive feedback peaks the gain (bypassing the resistor) at a certain frequency close to the 3 dB cut-off region. Additionally, series inductors at the input and sometimes at the output of the receiver are used to improve the matching [82].

Another method of improving bandwidth is by cascading many small-gain, high-bandwidth amplification stages after the TIA but at the expense of energy efficiency and chip area. Those amplification stages can utilize peaking at higher frequencies in order to compensate for the drop of gain in the main TIA stage. An additional benefit becomes apparent if those stages have tunable gain or tunable frequency of peaking, in which case the overall bandwidth response of the receiver can be controlled and adapted on demand.

Lastly, dedicated equalization circuitry can be used after the TIA stage similar to what is typically used in cable and backplane equalization systems [83].

3.5 Contributions to the field

In this section we will discuss the appended papers and their main contribution to the field.

3.5.1 Ultra broadband Traveling wave amplifier in 250 nm InP

In Paper A, we present the measurement and characterization of an ultra-broadband distributed amplifier designed in a 250 nm InP DHBT process provided by Teledyne Scientific Company (TSC) [84]. The author's contributions on this work are the measurement, characterization, and the publication of the results based a previously fabricated broadband amplifier MMIC. There were significant challenges in order to properly measure a system with DC-200+ GHz bandwidth. The design was composed of four CC-Cascode amplification cells cascaded, connected to the output transmission line. Ultra-Broadband distributed amplifiers such as the one measured are typically used in instrumentation as well as in MZM driver front-ends [85]. At the time of the publication, it was the widest bandwidth DA that could operate from DC frequencies.

3.5.2 130 nm SiGe Differential TIA

In Paper B, we present the design, measurement and characterization of a fully differential TIA for high speed short haul fiber-optical communication receivers fabricated in Infineon's B11hfc 130 nm SiGe process [21, 22]. The TIA is based on a common base transimpedance stage, followed by a common collector stage for signal buffering and DC-level adjustment, one linear amplification cascode stage, and another CC output stage for driving the 50 Ω load. Both the CB and the cascode stages utilize inductive peaking to extend the bandwidth. The TIA demonstrated a bandwidth of 45 GHz, a transimpedance gain of 56 $dB\Omega$ and a power consumption of 82 mW. Eye diagram measurements up to 32 Gbps OOK give it an energy efficiency of 2.6 pJ/bit. The main contribution of this work is the use of the less often used CB input stage which provides a low input impedance of approximately 20 Ω which helps increase the bandwidth of any PD connected at the input. Furthermore, the input impedance can be tuned by controlling the current of the CB stage providing a measure of versatility. The downside of CB amplifiers is the input referred noise current density of 30.6 pA/$\sqrt{Hz}$ which is higher when compared with other input stages in literature. That makes this TIA more suitable for larger, bandwidth-limited PD with OOK modulated signals.

3.5.3 130 nm SiGe Equalizer

In Paper C, we report the design and measurement of a fully differential continuous-time linear tunable equalizer, aimed for integration in short-haul fiber-optical communication receivers. The author's contribution was on the measurement, characterization and publication of the results. The equalizer included a 50 Ω matched input CC stage, followed by two CE differential pairs connected in parallel. One of the pairs used capacitive and resistive degeneration to peak at the frequency of interest. The exact frequency was tunable by a varactor diode operating as the capacitive degeneration. The two parallel amplifiers' gain was controlled by their tail current source allowing separate tuning of base-band and peaked gain. The MMIC was fabricated in Infineon's B11hfc 130 nm SiGe process [21, 22] and achieved equalization of 29 dB up to 50 GHz with a power consumption of 130 mW. Eye diagrams with up to 64 Gbps were measured with a bandwidth limited coaxial cable as the lossy medium. The energy efficiency of the equalizer including the input buffer was 2.03 pJ/bit based on the measured eye diagrams.

3.5.4 130 nm InP TIAs

In Paper D, we present the design and fabrication of two receiver frontend circuits using TSC 130 nm InP DHBT process [86]. The first of the two circuits composed of a CB-CC feedback-less TIA input stage optimized for high gain, high bandwidth and low input impedance ($\approx 20\ \Omega$). The second circuit was a CE shunt-shunt feedback TIA design optimized for similar high gain and bandwidth and input impedance of 50 Ω. Due to the very high f_t and f_{max} of the process of 520 GHz and 1.15 THz respectively, the TIA circuits were able to achieve transimpedance bandwidth of 133 GHz and a TI gain of 42 $dB\Omega$. The two circuits were further characterized with eye diagrams up to 64 Gbps, and the input referred noise current was measured to be 30.2 $pA/\sqrt{Hz}$ for the CB and 13.9 $pA/\sqrt{Hz}$ for the CE. The energy efficiency of the two circuits was 0.5 pJ/bit for the CB and 0.4 pJ/bit for the CE. At the time of publication, the two TIA front-ends had the highest reported bandwidth for TIAs in literature.

3.5.5 Comparison with state-of-the-art

After discussing each paper and their contributions, we proceed to place the results into perspective in Fig. 3.5.

As seen in the figure, Paper D with the respective designs 1 and 2 provides quite high bitrate and low power. It is worth mentioning that most other publications in literature include at least a linear amplifier and sometimes power consuming output buffers in their MMICs, so the very low power in that case only includes the TIA stage. However, due to equipment limitations, the TIAs in that work were not tested at bitrates higher than 64 Gbps. Simulated results indicate higher than 100 Gbps operation so the bitrate and energy efficiency values can be improved with further measurements. The same holds for the TIA MMIC in Paper B where the limitation of the bitrate was 32 Gbps while the simulated results indicated operation up to 56 Gbps. The design in Paper C corresponds to an equalizer so it should not be taken out of context in the comparisons. However, we can see in the figure that most works below 50 Gbps use some form of equalization.

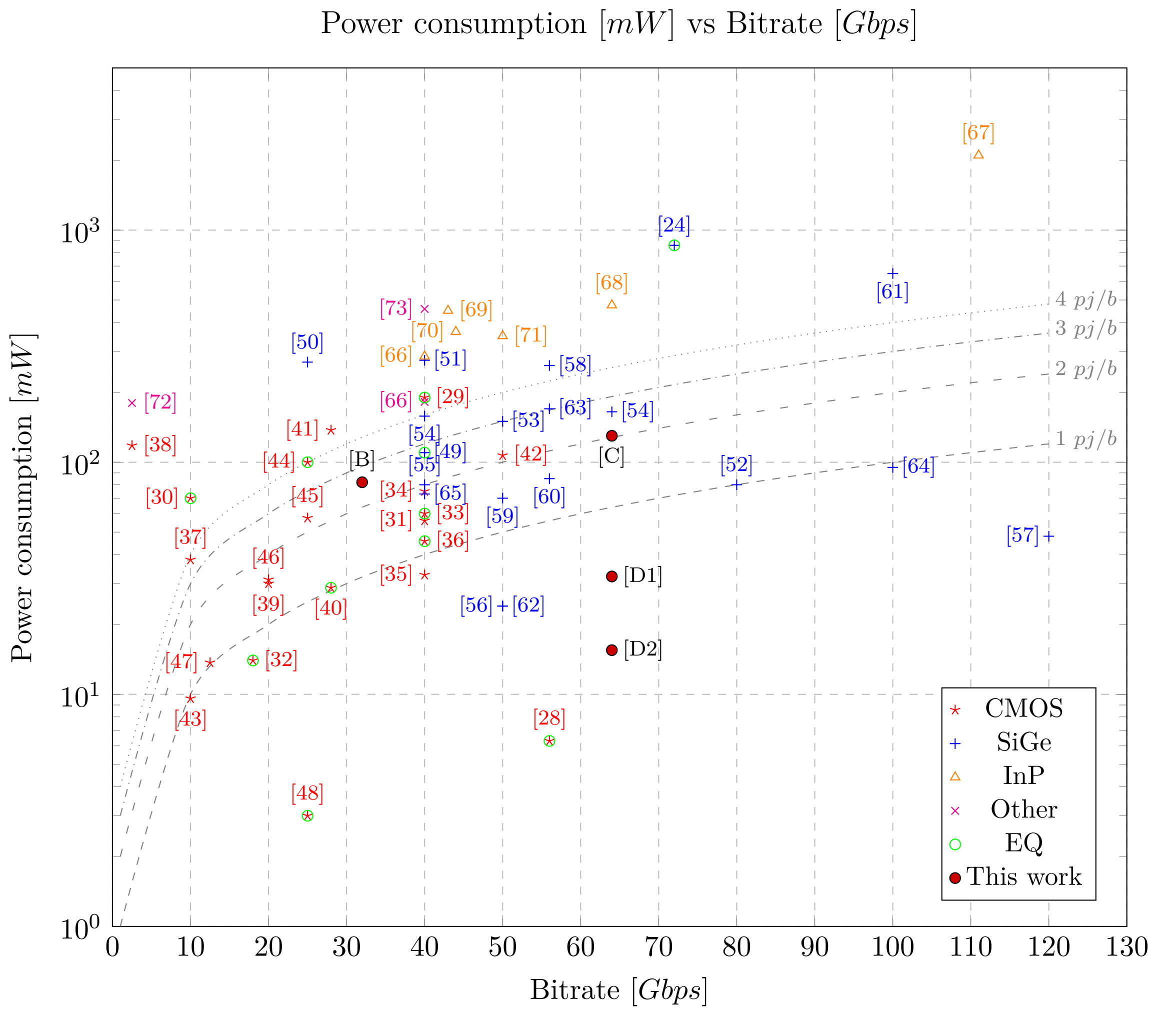


Figure 3.5: Prominent receiver system publications based on reported measured bitrate and power consumption. Results from papers appended in this thesis are included.

Chapter 4

Conclusion

Optical interconnects are becoming a staple of data center networks by offering high datarates at decreasing cost and energy. In this thesis, the field of short reach fiber-optical interconnect receivers is introduced. High-speed, broadband electronic circuits were designed in state-of-the-art semiconductor technologies with the goal to overcome the unique challenges posed by the optoelectronic channel. In addition to the specific field, there is a plethora of other applications for such systems: intra- and inter-vehicle optical communication, intra- and inter-satellite optical communication, radio-over-fiber. While those fields are in various datarates and stages of maturity, they call for original topologies and interdisciplinary application of existing circuits.

4.1 Future work

In this work I presented some of the building blocks of a receiver; therefore, a natural following work is to fully integrate TIA, equalizer and broadband (variable gain) amplifier monolithically. An additional engineering challenge would be the packaging board to allow coupling and alignment of the optical fiber.

The demonstrated circuits focused on OOK modulated data; however, in order to achieve 100 Gbps within the given bandwidth we need higher modulation schemes. PAM-4 is the most popular in literature, but requires circuits with optimized noise performance due to the SNR penalty imposed. Therefore, new circuits optimized for multi-level modulation should be designed.

As discussed in the previous chapters, the final output of a receiver system is in the form of digital data; therefore, clock and data recovery circuits need to also be designed and integrated to the receiver. Additionally, several secondary circuit blocks are required in order to satisfy the long term stability and quality requirements of the industry. Typical examples are: on chip bias generation networks (with band-gap references, noise rejection etc), DC offset cancellation, feedback control circuits, additional tunability on equalizers and variable gain amplifiers, serial to parallel interface (SPI) and memory blocks to allow programming of tunable circuits without the need for additional bias connections, voltage control oscillator (VCO) for on-chip clock generation and phase-locked loop (PLL) to align the local clock with the incoming high speed data-stream.

Lastly, while the designed receiver electronics presented on this work were aimed at OOK and PAM-4 broadband communication, that does not mean that they cannot be used with other higher modulations. That opens up the potential to use existing circuits for transmission of Phase Shift Keying (PSK), or quadrature PSK (QPSK) which are popular in radio-over-fiber applications.

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