THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Towards an on-chip power supply

Integration of micro energy harvesting and storage techniques for wireless sensor networks

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one step closer...

Abstract

The lifetime of a power supply in a sensor node of a wireless sensor network is the decisive factor in the longevity of the system. Traditional Li-ion batteries cannot fulfill the demands of sensor networks that require a long operational duration. Thus, we require a solution that produces its own electricity from its surrounding and stores it for future utility. Moreover, as the sensor node architecture is developed on complimentary metal-oxide-semiconductor technology (CMOS), the manufacture of the power supply must be compatible with it. In this thesis, we shall describe the components of an on-chip lifetime power supply that can harvest the vibrational mechanical energy through piezoelectric microcantilevers and store it in a reduced graphene oxide (rGO) based microsupercapacitor, and that is fabricated through CMOS compatible techniques. Our piezoelectric microcantilevers confirm the feasibility of fabricating micro electro-mechanical-systems (MEMS) size two-degree-of-freedom systems which can solve the major issue of small bandwidth of piezoelectric micro-energy harvesters. These devices use a cut-out trapezoidal cantilever beam to enhance the stress on the cantilever's free end while reducing the gap remarkably between its first two eigenfrequencies in 400 - 500 Hz and 1 - 2 kHz range. The energy from the M-shaped harvesters will be stored in rGO based microsupercapacitors. These microsupercapacitors are manufactured through a fully CMOS compatible, reproducible, and reliable micromachining processes. Furthermore, we have also demonstrated an improvement in their electrochemical performance and yield of fabrication through surface roughening from iron nanoparticles. We have also examined the possibility of integrating these devices into a power management unit to fully realize a lifetime power supply for wireless sensor networks.

Keywords: MEMS, CMOS compatible, Piezoelectric energy harvester, Microsupercapacitor, On-chip power supply.

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List of Publications

This thesis is based on the following appended papers:

Paper 1. **Agin Vyas**, H. Staaf, C. Rusu, T. Ebefors, J. Liljeholm, A. D. Smith, P. Lundgren and P. Enoksson. *A Micromachined Coupled Cantilever for Piezoelectric Energy Harvesters.* Micromachines (ISSN 2072-6669), no. 5 (2018): 252.

Paper 2. **Agin Vyas**, Q. Li, F. Cornaglia, K. Wang, A. Anderson, M. Haque, V. Kuzmenko, A. D. Smith, P. Lundgren, P. Enoksson. *Surface Roughening with Iron Nanoparticles for Promoted Adhesion of Spin Coated Microsupercapacitor Electrodes.* MRS Advances 4, no. 23 (2019): 1335-1340.

Paper 3. **Agin Vyas**, K. Wang, A. Anderson, A. Velasco, R. Van den Eeckhoudt, M. Haque, Q. Li, A. D. Smith, P. Lundgren, P. Enoksson. *Enhanced electrode deposition for on-chip integrated micro-supercapacitors by controlled surface roughening.* Submitted

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A. D. Smith, Q. Li, A Anderson, **Agin Vyas**, V Kuzmenko, M Haque, L. G. H. Staaf, P. Lundgren, P. Enoksson, *Toward CMOS compatible wafer-scale fabrication of carbon based microsupercapacitors for IoT*, IOP Conference Series: Journal of Physics: Conference Series 1052 (2018) 012143.

Agin Vyas, F. Cornaglia, T. Rattanasawatesun, Q. Li, M. Haque, J. Sun, V. Kuzmenko, A. D. Smith, P. Lundgren, P. Enoksson. *Investigation of Palladium Current Collectors for Vertical Graphene-based Microsupercapacitors*, Journal of Physics: Conference Series. Vol. 1319. No. 1. IOP Publishing, 2019.

Q. Li, A. D. Smith, M. Haque, **Agin Vyas**, V. Kuzmenko, P. Lundgren, P. Enoksson. *Graphite paper/carbon nanotube composite: A potential supercapacitor electrode for powering microsystem technology*, Journal of Physics: Conference Series, 922 (2017) 012014

Q. Li, A. D. Smith, **Agin Vyas**, F. Cornaglia, A. Anderson, M. Haque, V. Kuzmenko, E. Kohler, P. Enoksson. *Giving micro-supercapacitor fingers?*, 29th Micromechanics and Microsystems Europe workshop 2018, August 26-29, Bratislava, Slovakia.

A. Velasco, **Agin Vyas**, K. Wang, Q. Li, A. D. Smith, P. Lundgren, P. Enoksson. *Investigation of vertical carbon nanosheet growth and its potential for microsupercapacitors*, 30th Micromechanics and Microsystems Europe workshop 2018, August 18-21, Oxford, United Kingdom.

R. Van den Eeckhoudt, **Agin Vyas**, E. Karabulut, G. Gereb, P. Gatenholm, P. Lundgren, C. Rusu and P. Enoksson. *Flexible and robust design for acoustic and vibrational energy harvesting*, 30th Micromechanics and Microsystems Europe workshop 2018, August 18-21, Oxford, United Kingdom.

Agin Vyas, R. van den Eeckhoudt, Q. Li, G. Geréb, A. Smith, C. Rusu, P. Lundgren, P. Enoksson. *Integrated Flexible Energy Harvester and Supercapacitor for Self-powered Textile Sensors*, PowerMEMS 2019, December 2-6, 2019, Kraków, Poland.

List of Acronyms

IoT	–	Internet-of-Things
WSN	–	wireless sensor network
CMOS	–	Complimentary metal-oxide-semiconductor
PEH	–	Piezoelectric energy harvester
MEMS	–	Micro electro-mechanical-systems
VLSI	–	Very large scale integration
MOSFET	–	Metal oxide semiconductor field effect transistor
MKS	–	Mass spring damper
MSC	–	Microsupercapacitor
IC	–	Integrated circuit
LDV	–	Laser doppler vibrometer
SOI	–	Silicon-on-Insulator
DRIE	–	Deep reactive ion etching
PZT	–	Lead Zironate Titanate
GO	–	Graphene oxide
rGO	–	reduced graphene oxide
CAD	–	Computer Aided Design
CNF	–	Carbon nanofiber
CNT	–	Carbon nanotube
VACNS	–	Vertically aligned carbon nanosheets
CV	–	Cyclic voltammetry
GCD	–	Galvanic charge discharge
PMU	–	Power management unit
D2W	–	Die to wafer
W2W	–	Wafer to wafer

Contents

Chapter 1

Introduction

A new era of computing technology is developing called the Internet of Things (IoT). It envisions a technology where there is an interaction between machines and infrastructure. Smart devices connected devices over a cloud computing-based infrastructure will encompass several aspects of our lives [1]. The groundwork of this platform is laid by the interaction of microsystems in machines, objects, environments, and infrastructure to collect and analyze data accrued by such systems. With the collection and processing of this data, we can command and control things to make our lives much more comfortable and safer. These devices would make the simple household technologies more energy efficient [2]. Integration of such a lifetime power supply into an IoT platform would lead to some efficiency in the overall sustainable development [3].

When these microsystems combine to interact with each other, they form a wireless sensor network (WSN) with them acting as nodes of an information circuit. The research on these microsystems has blown up since the advancement in micro-electromechanical systems (MEMS) technology [4, 5, 6, 7]. MEMS technology has enabled the development of microsystems at a low cost with an even lower power requirement than before. WSNs can influence all sectors of life with application areas ranging from health, military and security to agriculture, mining, and deep-sea exploration. For example, a doctor can monitor a patient's information remotely through sensing his physiological data while allowing a better understanding of the patient's condition. Sensor networks can detect chemical agents in air and water, which can lead to the identification of their types, concentration, and location that can lead to an early alarm. WSNs on rail tracks with strong vibrations can detect faults in the tracks, wheels, or the surroundings. Essentially, these sensor networks will provide a user with better information and intelligence of the surrounding [8].

A sensor node is a composition of four units, as shown in Figure 1.1. They are - transceiver, processing unit, sensor unit, and the power unit. Sensor nodes interact and communicate with each other wirelessly through a unit called transceiver. A transceiver is a combination of a transmitter that sends the signal and a receiver that accepts the signal. The transceiver is connected to a processing unit that comprises a processor and storage. A processor performs the basic arithmetic, I/O operations, and logic operations alongside allocating commands for the different components running in the system. The storage saves the information in the form of bits for future use. The processing

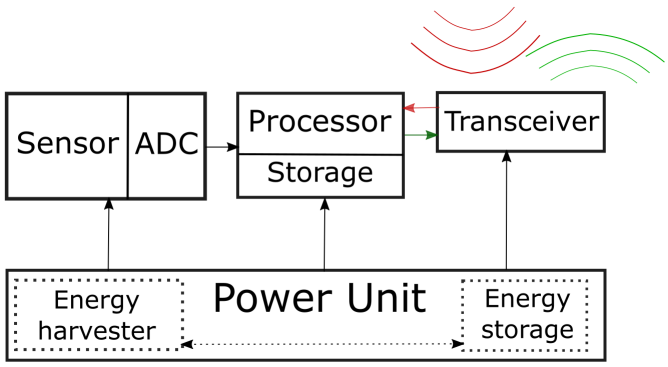

Figure 1.1: Components of a wireless sensor node.

unit is also connected to the sensing unit. The sensing unit is made up of a sensor and a unit that converts analog signals into digital called the analog-digital-converter (ADC). The sensor senses the physical information of its surrounding like temperature, vibrations, chemical concentration, light, humidity in the form of an electric current or a potential (ΔV) in most cases. The ADC's function is a translator of the sensor's information to the processor from analog to digital. The acquired digital information is stored and processed in the processing unit. The power unit powers all three subunits of the microsystem. There can be other subunits, too depending on the type of application.

There are several restrictions on the sensor node in order to be fully compatible with a WSN deployment. First, they must be small, sometimes as small as a cubic centimeter [9] (and be light enough at the same time). Secondly, they need to be consuming low power. Thirdly, they require low production costs, and finally, as these sensor nodes are to be used in often inaccessible places, the lifetime of these devices must be long. Having a large power unit and being small are two conditions that contradict each other. The wireless sensor node, being a microelectronic device, can only be equipped with a limited power source (< 0.5 Ah, 1.2 V) [8]. In some application scenarios, replenishment of power resources might be impossible. Sensor node lifetime, therefore, shows a strong dependence on battery lifetime. Currently, these sensors are powered by typical Li coin cells that we use in analog watches. These batteries are traditionally created of an electrode from earth metal and an electrolyte of an acidic solution and have a maximum lifetime of 3-5 years. Once they stop functioning, they need to be dumped somewhere in the environment as these batteries as not recyclable. Disposal of these systems has an immensely negative impact on the environment. The toxic acidic nature of the electrolyte, when dumped, poses a significant threat to our ecological dimension of soil, water, and air. The acidic batteries disposed on the ground can reduce the agricultural output [10]. Moreover, usage of earth metals deplete the finite resources of the ecosystem's economic capital [11]. Burning them would lead to a release of toxic waste gases[12]. With growing concerns with climate change, it is imperative to devise solutions that not only extend the lifetime of these sensors but are also environmental friendly.

It is possible to extend the lifetime of these devices using units of energy harvesting and energy storage. Energy harvesting is the process of extracting energy present in the environment in the form of solar, wind, thermal, or vibrational energy and convert it into

usable electrical energy [13]. These sources of energy will never deplete as long as the earth is rotating and revolving around the sun. Energy storage units are devices that can store this electrical energy in the form of charge and then supply it to the system when needed [14]. The power consumption of these devices is based on the microelectronics for data processing, sensing, and communication. Since the microelectronic devices are fabricated through complimentary metal-oxide-semiconductor (CMOS) technology, the power unit's fabrication process must be compatible with it.

1.1 Energy harvesting

The first component of the on-chip power supply comprises an energy harvesting unit. This unit converts forms of energies that are present in their environment into useable electrical energy through various physical mechanisms. These energies can be of the form of solar, wind, hydrothermal, mechanical, thermoelectric, or acoustic [13]. These energies are harvested and used to power miniaturized sensors in WSNs and wearable electronics. Among these energy sources, mechanical energy is the most distributed as some vibrations are present in all surroundings, be it a person in motion, a jet engine, a railway track or a mining or underwater location [15].

Mechanical energy can be extracted by the vibrations, noise, rotation, and most recently, hydraulic pressure induced in the device through three different mechanisms - electrostatic, electromagnetic and piezoelectric harvesting [16]. If a harvester device is fabricated with its characteristic frequency similar to the surroundings' one, it can utilize these vibrations and convert the mechanical energy into electrical energy. This form of energy harvesting is called kinetic energy harvesting. Out of the three, piezoelectric energy harvesters (PEH) has the maximum energy density and a high energy conversion efficiency. [17]. They have a simple configuration that can utilize MEMS technology for their fabrication. PEHs also do not require any input voltage for starting up compared to the electrostatic and electromagnetic harvester [3-5][18, 19]. Thus, they can be considered as potential candidates for powering miniature devices and wireless sensors.

Vibrational energy harvesters (VEH) in PEHs use the concept of converting stress induced by mechanical vibrations into electrical energy by expansion and contraction of the piezoelectric material which is layered on top of a vibrating surface, usually a cantilever. The cantilever is designed in such a way that it has its natural frequency within a targeted range. They, however, suffer from two significant drawbacks - 1) their range of output producing frequencies is quite low, 2) being MEMS, their power cannot easily reach the desired levels [20].

1.2 Energy storage

The second main component of an on-chip power supply is the energy storage unit. The energy harvesters gather the energy from ambient sources in the surroundings and deliver it to the power conditioning unit. The energy storage unit is then connected to the output of the power conditioning circuit, which provides a steady stream of DC output whenever the harvester extracts energy. First chosen as primary energy

storage systems were rechargeable batteries such as NiMH [21] and Li-ion [22]. While rechargeable batteries show high capacity and low leakage, wireless sensor life is limited by the cycle life of rechargeable batteries [23]. Cycle life of a battery is the number of charge-discharge cycles it can go through before its capacity drops below 80 % of its maximum capacity. The residues from the electrode-electrolyte reaction ages the device by increasing the internal resistance over a period of time. However in reality, by the time it has completed its cycle life, the capacity of the battery can reach up to 50 % or even 20 % in some cases. Due to this, a WSN would require replacement after not even 1-2 years. Supercapacitors, in recent years, have emerged to be successful technological tools in storing charge. They have a higher cycle life than batteries, and in recent years, their performance has been demonstrated to be equivalent to the low-end commercial batteries [24]. Therefore, they can be, again as PEHs, considered as a truly viable option for a lifetime on-chip power supply.

1.3 Manufacturing

1.3.1 IC-compatibility

The standard process technology for integrated circuits (ICs) and very large scale integrated (VLSI) circuits is shown in Figure 1.2. The fabrication of these components starts on a wafer which is a polished semiconductor substrate. The next step usually involves deposition or growth of thin films such as SiO_2, Si_3N_4, polySi or dielectric films, and even metalized oxides. After the growth of thin films, the substrate undergoes doping through diffusion or ion implantation. This process is used in IC technology to fabricate pn junction diodes which can later be used in MOSFET (metal oxide semiconductor field effect transistor) fabrication. Then, the substrate is subjected to photolithography where a polymeric photoresist is spin-coated on it and then exposed in UV light through a special mask with a specific design. The photoresist is sensitive to UV light depending on its chemical structure. It is generally of two types - positive and negative. In the case of the positive photoresist, the UV light breaks the linkages of the polymer exposed, while in the negative, the exposure strengthens the bonds of the polymer. During the development of the photoresist step, the weaker linkage polymers are etched out of the substrate while leaving the photoresist in the desired pattern. The exposed surface is then used for further doping, film formation, or etching, depending on the process' requirement. The process is then repeated in several cycles depending on the total number of photolithographic masks [25].

However, there are several constraints in the IC fabrication process regarding the choice of material and equipment. The first major constraint is the material for the wafer. An IC wafer should be mechanically robust with necessary hardness required to survive indentations, laser marking, stains, streaks, and scratches. The second constraint comes in the form of radiation required for photolithography which is restricted to the users of optical and UV light, X-ray, and e-beam, a short for electron beam. The third constraint is in the form of metals used in IC fabrication. This list is restricted to Al, Au, Ag, Cr, Mo, W, Pt, Pd, Ta, and Ti [25]. Furthermore, the process is also dependent on the melting point of these metals. Among the used metal, Al has the lowest melting point at

660 °C. So, the fabrication of energy harvesters, supercapacitors, and their subsequent integration should be conducted with the techniques within these constraints.

Fabrication of VEHs requires photolithography, etching, metallization, doping, and deposition techniques. These processes are standard in micromachining techniques too. Furthermore, with improving MEMS technology, these processes have become highly developed in improved reliability, mass production, and cost reduction while achieving a high wafer yield. Therefore, energy harvesters that are fabricated through MEMS techniques can be easily integrated into a CMOS compatible fabrication process.

However, for the energy storage element, supercapacitors generally require a large volume and specialized manufacturing techniques that make them hard to be integrable in microsystem electronics technology that requires semiconductor micromachining. Therefore, developing CMOS compatible fabrication processes has attracted much attention over the past few years [26, 27, 28, 29, 30]. Microsupercapacitors are miniaturized supercapacitors that are small enough to be integrated into electronic devices. They can be integrated either as self-powering systems with charging through energy harvesters, or enhanced micro battery systems where they act as hybrid devices with batteries to improve the lifetime of a device.

Successful integration of MSCs in a fully IC compatible process scheme can lead to an on-chip power supply that improve their lifetime. Compared to other techniques to manufacture MSCs such as screen printing[31], ink-jet printing[30], laser scribing[29], electrostatic spray deposition[28], electrophoretic deposition[32], chemical exfoliation[33] and doctor blade coating[34], the use of spin coating has the advantage of already being an established conventional part of standard CMOS processing, implying that it is as such inherently CMOS/MEMS compatible. These techniques are not compatible with semiconductor device processing, with it moving towards a completely automatic factory. Processes like ink-jet printing and screen printing do not have an

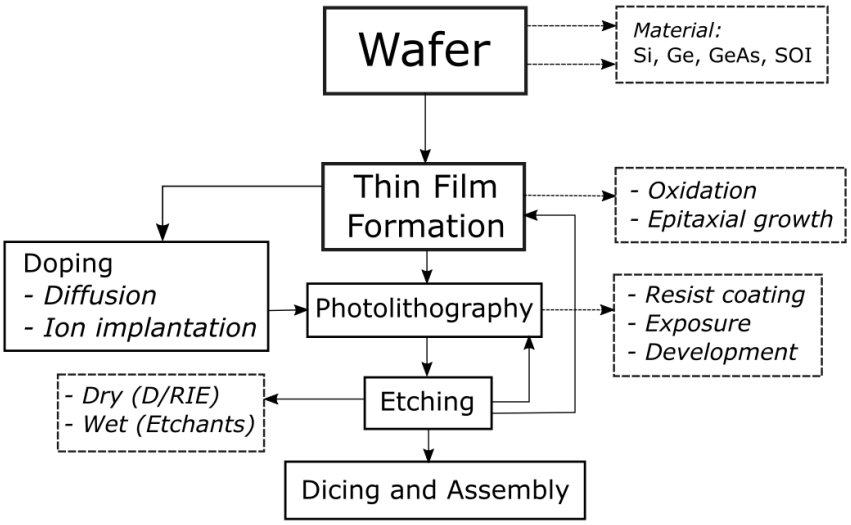

Figure 1.2: Main fabrication steps for a IC fabrication process. The dotted square boxes show the constrained variety of processes possible in a CMOS compatible fabrication facility.

effective scaling down technique, while its raster-scanning process inhibits laser scribing. Thus, in view of the expected further automation in IC manufacturing [35], its compatibility advantage makes spin coating a strong candidate for being the preferred MSC manufacturing technique, provided it can demonstrate that it can fabricate devices of sufficient quality and yield.

1.4 Scope of the thesis

In this thesis, we are going to discuss different components of an on-chip power supply in the following chapters: Chapter 2 deals with discussion of VEHs. First, we will examine the theoretical principles of single degree of freedom structures, followed by the restrictions on its performance. Then we shall review the solutions used in macro energy harvesting for improvement in bandwidth and power efficiency. We have also described the fabrication process for energy harvesters, issues related to it, and ensuing mechanical characterization. In Chapter 3, we shall take up supercapacitors and more specifically MSCs. We will argue for the potential fabrication methods for these devices that can demonstrate integration into an on-chip platform in CMOS compatible process scheme. The fabrication methods that we followed for their manufacturing are described with a special section for the issues that we encountered while performing the process. We shall then examine some of the results for the designs fabricated and optimizations for performance improvement. Finally, in Chapter 4, we shall discuss the feasibility of on-chip integration of the fabricated VEHs and MSCs through a describing the circuit design and performance requirements for each device. Finally, we will conclude with a discussion on the best possible method for their packaging and integration.

Chapter 2

Piezoelectric Micro-energy Harvester

Piezoelectric energy harvesters are devices that convert the energy in the surroundings through actuation of a piezoelectric material. Piezoelectricity is the property of materials that develop voltage upon application of stress onto their surface. It is a reversible process as the material can develop strain when an electric field is applied to it[36]. This effect was demonstrated by Pierre Curie and Jacques Curie in 1880 [37]. VEHs convert the vibrations in the surrounding into electrical energy through stress on their cantilever beams.

2.1 Introduction

In order to understand the working mechanism of VEHs, the device must be visualized as an analogous to a mass-spring-damper (MKS) system, as seen in Figure 2.1. The mass of the device is m, y is the amplitude of displacement, k is stiffness of the beam, $y(t)$ is the displacement of the beam, $z(t)$ is the relative position of the center of mass of the beam with respect to its displacement and b_m and b_e are the damping coefficients and $b = b_m + b_e$, where m and e are the mechanical and electrical indices respectively.

Let the displacement of the system $y(t) = Y sin(\omega t)$. With that we get the transfer function as a second order differential equation

$$mz"(t) + bz'(t) + kz(t) = -my"(t) \tag{2.1}$$

Now in a standard form,

$$z"(t) + \frac{b}{m}z'(t) + \frac{k}{m}z(t) = y"(t) \tag{2.2}$$

From the solutions of the second order differential equation, we know that

$$\frac{b}{m} = 2\zeta\omega_n \qquad\qquad \frac{k}{m} = \omega_n^2$$

where ω_n is the natural frequency of the system, and ζ is the damping ratio. So, from this, we get

$$\omega_n = \sqrt{\frac{k}{m}} \qquad\qquad \zeta = \frac{b}{2\sqrt{km}}$$

We can also write ζ in terms of a derived notation called the quality factor (Q) as

$$Q = \frac{\sqrt{km}}{b}$$

which can also written in terms of ω_n as

$$Q \approx \frac{\omega_n}{\Delta\omega} \tag{2.3}$$

where $\Delta\omega$ is the bandwidth of frequencies that have an output of at least half the amplitude at the resonant frequency ω_n. It is also denoted as the 3 dB bandwidth of any harvesting system. Considering our input signal $y(t)$ the solution to equation 2.1 is

$$z(t) = \frac{m\omega^2 Y}{k - m\omega^2 + j\omega b} sin\omega t \tag{2.4}$$

After calculating the solution for $z(t)$, we get

$$z(t) = \frac{\omega^2}{\sqrt{(\omega_r^2 - \omega^2) + (\frac{b\omega}{m})^2}} Y sin(\omega t + \phi) \tag{2.5}$$

where ϕ is the phase angle

$$\phi = tan^{-1} \frac{b\omega}{k - \omega^2 m}. \tag{2.6}$$

Now that we have a solution for $z(t)$, we can calculate the average power, mechanical parasitic and electrical output as

$$P = b(z'(t))^2 \tag{2.7}$$

which gives us

$$P(\omega) = \frac{m(\zeta_m + \zeta_e) Y^2 (\frac{\omega}{\omega_r})^3 \omega^3}{[1 - (\frac{\omega}{\omega_r})^2] + (2(\zeta_m + \zeta_e)\frac{\omega}{\omega_r})^2} \tag{2.8}$$

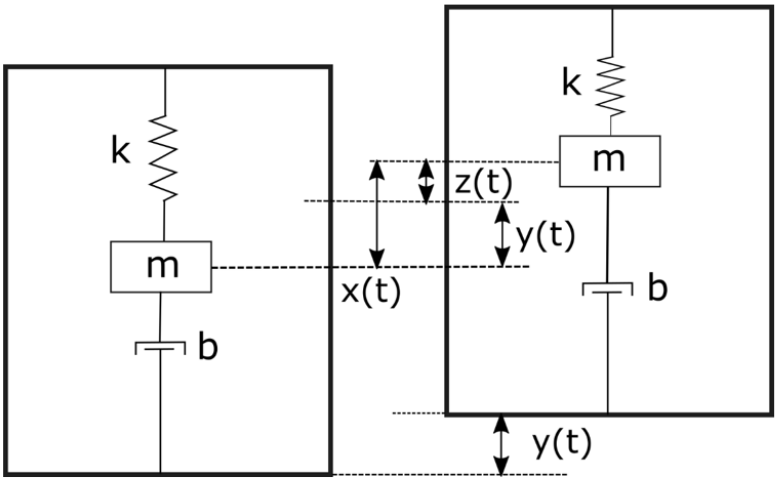

Figure 2.1: Typical schematic of the MKS 1DOF system.

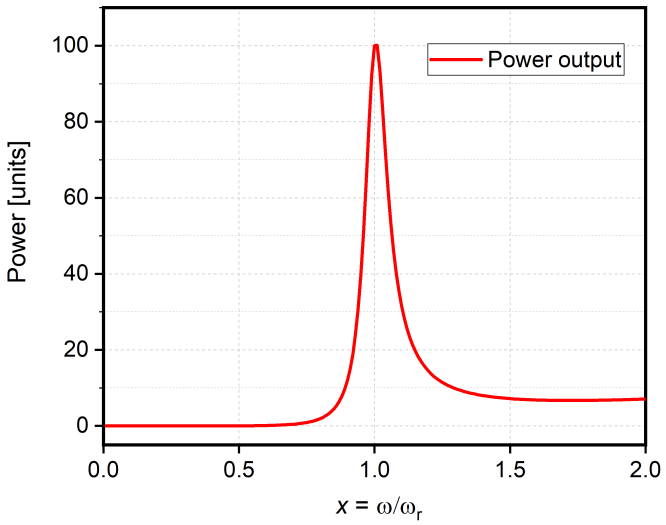

Figure 2.2: Simulated power output of a generic single cantilever based energy harvester with respect to $x = \frac{\omega}{\omega_r}$

When the frequency of the system ω is equal to the resonant freqency ω_r, the power reaches its maximum which is

$$P = \frac{mY^2\omega_r^3}{4(\zeta_m + \zeta_e)} \tag{2.9}$$

On analysis of equation 2.8 further, we figure out the main issue that needs to be optimized with the utilization of VEHs in on-chip power units, i.e., narrow bandwidth of operational frequencies.

Considering $\frac{\omega}{\omega_r} = x$ and keeping m, Y and ζ_m, ω_r, and ζ_e as constants C_n, we get the equation 2.8 as

$$P = \frac{C_1 x^6}{(1-x^2)^2 + C_2 x^2} \tag{2.10}$$

When we plot this equation in Figure 2.2, we see the dramatic reduction of output power at either side of ω_r. Therefore, we need to find solutions for improving its bandwidth of frequencies by reviewing some of the pre-existing solutions in macro-energy harvesters. These solutions must also be feasible for realization in a MEMS structure which can then further be integrated with an on-chip power supply.

One of the potential solutions to the bandwidth and power problem is a nonlinear generator with bistable structures. A bistable structure provides the cantilever design with multiple stable equilibrium positions that allows it to have multiple frequencies where the stress distribution on the beams is optimal. Stanton et al. [38] incorporated a magnetic nonlinearity with the help of two magnets strategically placed in a linear system. Wu et al. [39] and Erturk et al. [40] also arrived at the same conclusion of obtaining a broad bandwidth. Having a bistable structure with magnetic attachments is a novel idea; however, it is usually large and requires an auxiliary support structure that cannot be currently placed in a MEMS design.

Similarly, studies by Blystad [41] and Liu [42] suggest amplitude limiters as another way to increase the bandwidth. A metal plate is used as a mechanical stopper to limit the displacement of the cantilevers. Soliman et al. [43] experimented on such a structure with a single stopper and showed an improvement in the power output bandwidth of the device. Even with the improved bandwidth, in practicality, lower maximum output power and fatigue-induced failures in such designs make their incorporation harder in microstructural harvesters.

Another idea of improving bandwidth is to create a generator array consisting of cantilever beams of different lengths and proof masses operating at different frequencies. Studies conducted by Shahruz et al. [44], Ferrari [45], Xue [46], and Liu [47], Qi et al. [48] expounded upon this concept with more cantilevers in a single array. Although favorable results are obtained, the requirement of integrating particular coupling mechanisms for each cantilever and the device's volume efficiency, make multifrequency generator array more complicated to design and fabricate as a MEMS design.

Currently, known solutions use two-degree-of-freedom (2DOF) structures to improve the bandwidth in micro-cantilever designs. Roundy et al. (2005) [49] initially proposed the idea of incorporating multiple proof masses to create a multiple-DOF with at least one structure resonating in the desired frequency range. Ou et al. (2010) [50], then, derived a theoretical model of a dual-mass beam structure for bandwidth broadening. Aldraihem and Baz (2011) [51] and Arafa et al. [52] (2011) studied a 2DOF acting as a dynamic magnifier. Although close resonances could be achieved, the magnifier required a huge weight, which proved counterproductive to miniature harvesters. Later, Erturk et al. [53] and Xu et al. [54] considered innovative L-shaped designs for cantilevers to bridge the gap of natural frequencies.

To devise natural frequencies closer, Jang et al. [55] (2011) developed a 2DOF piezoelectric energy harvesting device which exploited the structure's translation and rotation vibration modes. The device showed two-peak power output and displayed bandwidth improvement at high power levels compared to the conventional single-degree-of-freedom (SDOF) device. Kim et al. [56] (2011) demonstrated the performance comparison between a 2DOF and conventional SDOF device. Wu et al.[57] proposed a "cut-out" 2DOF harvester with a secondary beam enclosed within the main beam, which achieves two close resonances with significantly large amplitudes. Although, even with close resonance peaks, the bandwidth of the system included an anti-resonance frequency which led to a significant drop of the output voltage.

While several studies show significant improvement of bandwidth through 2DOF structures, much research on it does not focus on the distribution of stress on the cantilever beams. Studies by Staaf et al. [58, 59] provide an assessment of using parallel cantilevers coupled to one another at one end. This improves the stress distribution patterns and the bandwidth through coupled resonance at frequencies near the natural excitation. The details of the VEHs can be found in Table 2.1.

Macro-energy harvesters are a potential source for energy; however, their manufacturing is not equipped to produce hundreds of devices at the same time. Surface micro-machining fabrication techniques have been used in manufacturing CMOS devices, sensors, actuators, and also energy harvesters at a large scale [60]. They presented a single cantilever with a hanging proof mass. A single cantilever based piezoelectric

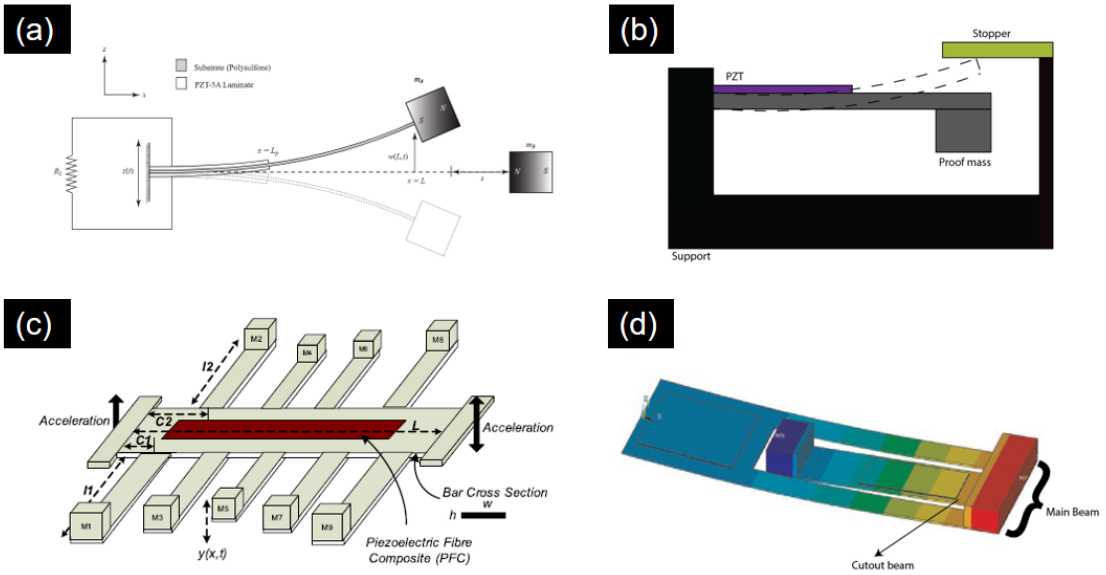

Figure 2.3: Techniques in macro-energy harvesting that are used for improving the device's bandwidth of frequencies: (a) a bistable structure [41], (b) amplitude limiter, (c) array configuration [46], (d) 2DOF freedom structure [42]. Images are reproduced after permission from the publishers.

energy harvester is one of the efficient designs. In principle, the micro-structure consists of a rectangular beam with a hanging proof mass. The proof mass is usually quite thick compared to the cantilever beam. The large proof mass acts as a hanging mass to the spring system, thereby reducing its natural frequency. The proof mass can be made during the micromachining process, or it can be added onto the fabricated structure. One of the first micro-energy harvesters were fabricated by Marzenski et al. [61]. Later, Jeon and Choi [62], [63] fabricated a d_{33}, PZT-based vibrational harvester. The cantilever beam was composed of a thin SiO_2/SiN_x layer with a diffusion barrier of ZrO_2 separating PZT from the structure. The proof mass was made up of SU-8 thick resist. Fang et al. [64] similarly created microcantilevers through micromachining techniques and added a Ni proof mass post-processing. Due to Ni's higher density over Si (8.9 g/cm^3 vs. 2.3 g/cm^3), it reduces the resonance frequency of the device. We have examined several micro-energy harvesters in a more concise format in Paper 1. Also, the list of device performances can be found in Table 2.1.

With the above energy harvesters, most of the designs comprise of a beam that has an active piezoelectric area along the fixed ends while the free end is left unused as it experiences minimal stress, which can be considered as a "dead area". The piezoelectric material is essentially a capacitor. When the material is stressed, its molecular orientation starts exhibiting a dipole moment. This dipole moment gives rise to an electric field that leads to the redistribution of charge in the crystal lattice. If there is no stress on the piezoelectric material, the total dipole moment of the piezoelectric material reduces, thus giving less charge. This is an issue when we discuss the performance of MEMS vibrational harvesters as these devices require the utilization of all the piezoelectric material area on the cantilevers for efficient performance. Therefore, we require novel

solutions from the macroscopic VEHs to test them on a MEMS scale.

In recent years, the focus of the vibrational micro-energy harvester research has shifted to the fabrication of specialized designs to improve the bandwidth of the energy-providing frequencies. Park et al. [65] designed an intrinsically stress-induced bent Si cantilever of 3 mm × 2 mm × 18 μm. The harvester had two directions of oscillation, vertical and radial. When the cantilever is released, it undergoes bending deformation through the presence of a low temperature oxide (SiO_2) and a low stress nitride (SiN_x) on top of the Si substrate. They designed the study on the principle of proportional dependence of the output power on the bending moment. They also shaped the cantilevers in a trapezoidal form to improve the distribution of stress on the beam. The device gave 1 μW power output at a resonance frequency of 115 Hz with a Q-factor of 51. Leuke et al. [67] fabricated a set of folded spring structures for reduction of operating frequency of the microstructures. The folded beam shape reduces the overall stiffness of the design and thus bring the natural frequency of the system unto 30 - 300 Hz. Also, the next natural frequencies of the structure are brought closer to one another. They achieved a power output of 690.5 nW at 226 Hz in one of the designs which had four

Table 2.1: List of macro- and micro-VEHs ordered according to year of publication from oldest to newest.

Ref.	**Volume (mm^3)**	**Res. Freq. (Hz)**	**V_{pp}** (V)	**Power** (W)	**Geometry**
[64]	0.6	608	0.89	2.16 μ	Single cantilever
[63]	0.05304	13900	2.4	1 μ	Cantilever
[47]	0.045	610	3.9	3.98 μ	Array
[45]	13.5	113	-	89 μ	Array
[40]	620	46.4	-	-	Dynamic magnifier
[54]	480	39.8	-	13.54 m	Right angle
[50]	3640	26	-	-	2DOF no cutout
[48]	6800	14-30	18	-	Array
[56]	800	11	60 V/g		2DOF two cantilevers
[52]	1650	21	4.7	5.68 μ	2DOF no cutout
[39]	2640	18	22 V	1.25 m	2DOF "cut-out" rectangular
[42]	0.075	30-48	100 m	100 n	Dynamic magnifier
[65]	3	115	16 m	1 n	Quasi bendable cantilever
[66]	0.36	234.5	1.62 - 5	66.75 μ	Rectangular
[67]		45 - 3667	-	690 n	Folded Spring
[59]	48	330-410	11.7 V		S-shaped coupled cantilever
[36]	0.05	1258	-	-	M-shaped

folded Si springs attached to a central hanging proof mass. Yu et al. [66] designed a five cantilever system with a single large proof mass. The fabricated generator had plates of size 3 mm × 2.4 mm × 50 μm and a Si proof mass of 8 mm × 12.4 mm × 0.5 mm. The power output at its resonant frequency of 234 Hz was 66.75 μW. A similar concept was also employed by Zhang et al. [68] where instead of rectangular folded springs, they used circular annular rings, each attached to the central proof mass. The device die is 6 mm × 6 mm in size and demonstrated resonance frequencies less than 11 Hz with a voltage output 7.5 mV at less than $0.2g$ acceleration.

2.1.1 Two-degree of freedom (2DOF) design

A piezoelectric energy harvester is normally designed as a spring-mass-damper (MKS) system for analytical modeling. The schematic in Figure 2.4(a) is a conventional 2DOF lumped parameter model which is used for the analysis of the M-shaped designs. In this model, m_1 and m_2 are the masses of the primary and secondary structures respectively, k_1, k_2, and b_m, b_e are their respective spring constants and dampings. When the system is in an excited base configuration, the initial displacements of the base, primary, and secondary proof masses are y_0, y_1 and y_2. $-V\theta$ is the force induced by mechanical coupling, where V is the potential formed in the piezoelectric film and θ is electromechanical coupling coefficient.

Two equations of motions and two Kirchoff's voltage equation are derived from the free-body-diagram shown in Figure 2.4(b). They are as follows:

$$m_2 y_2" = -k_2(y_2 - y_1) - b_e(y_2' - y_1') \tag{2.11}$$

$$m_1 y_1" + m_2 y_2" = -k_1(y_1 - y_0) - b_m(y_1' - y_0') \tag{2.12}$$

$$C_s V' + \frac{1}{R} V = \theta(y_1' - y_0') \tag{2.13}$$

Taking a Laplace transform of equations 2.11, 2.12, and 2.13, where $s = j\omega$ we get,

$$m_1 s^2 \hat{U}_1 + m_2 s^2 \hat{U}_2 = -k_1(\hat{U}_1 - \hat{U}_0) + s b_m(\hat{U}_1 - \hat{U}_0) - \theta \hat{V} \tag{2.14}$$

$$s^2 m_2 \hat{U}_2 = -k_2(\hat{U}_2 - \hat{U}_1) + b_e s(\hat{U}_2 - \hat{U}_1) \tag{2.15}$$

$$\hat{V}(C + \frac{1}{R}) = s\theta(\hat{U}_1 - \hat{U}_0) \tag{2.16}$$

Now, a standard 2^{nd} order ordinary differential equation can be written in terms of ω, frequency and ζ, damping coefficient.

$$x" + \frac{b}{m} x' + \frac{k}{m} x = 0 \tag{2.17}$$

where $\frac{b}{m} = 2\zeta\omega_n$ and $\frac{k}{m} = \omega^2$. Therefore, after using the annotations, we have

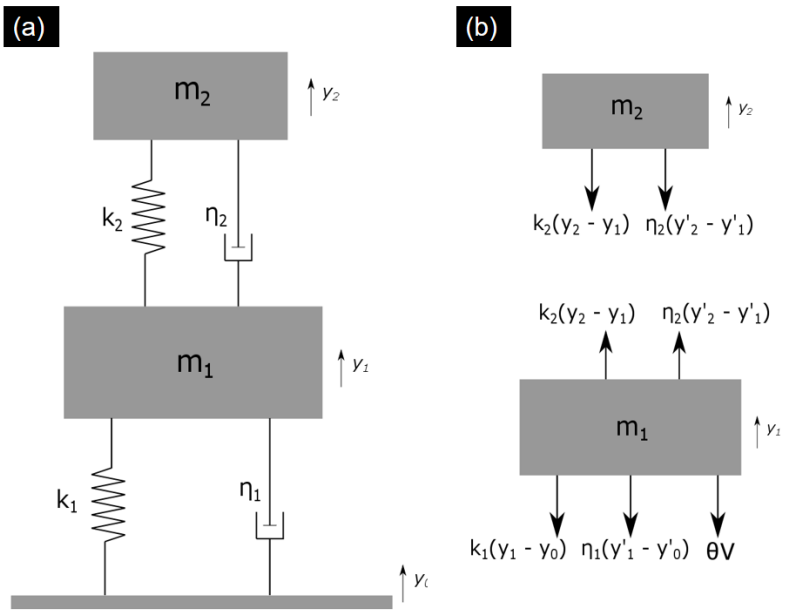

Figure 2.4: (a) Typical MKS system for 2DOF cantilever design (b) Free body diagram of each mass.

$$\omega_1 = \sqrt{\frac{k_1}{m_1}} \qquad \omega_2 = \sqrt{\frac{k_2}{m_2}} \qquad \zeta_1 = \frac{b_m}{2\sqrt{k_1 m_1}}$$
$$\zeta_2 = \frac{b_e}{2\sqrt{k_2 m_2}} \qquad \mu = \frac{m_2}{m_1} \qquad \lambda = \frac{\omega_2}{\omega_1}$$
$$\Omega = \frac{\omega}{\omega_1} \qquad r = \omega_1 CR \qquad k_e^2 = \frac{\theta^2}{Ck_1}.$$

Solving equations 2.14, 2.15, and 2.16, we get the equation for the two dimensionless natural frequencies as [69]

$$\Omega_{1,2} = \sqrt{\frac{(1+\mu)\lambda^2 + (1+k_e^2)}{2} \pm \frac{\sqrt{((1+\mu)\lambda^2 + (1+k_e^2))^2 - 4\lambda^2(1+k_e^2)}}{2}} \tag{2.18}$$

It can be seen from equation 2.18, that the closening of the first two natural frequencies depends on the parameters μ and λ. Figure 2.5 shows the contour plot of $\Delta\Omega$ vs μ and λ. The next section describes the simulation results in COMSOL for three designs that provided different values of and μ and extends the hypothesis generated by equation 2.18.

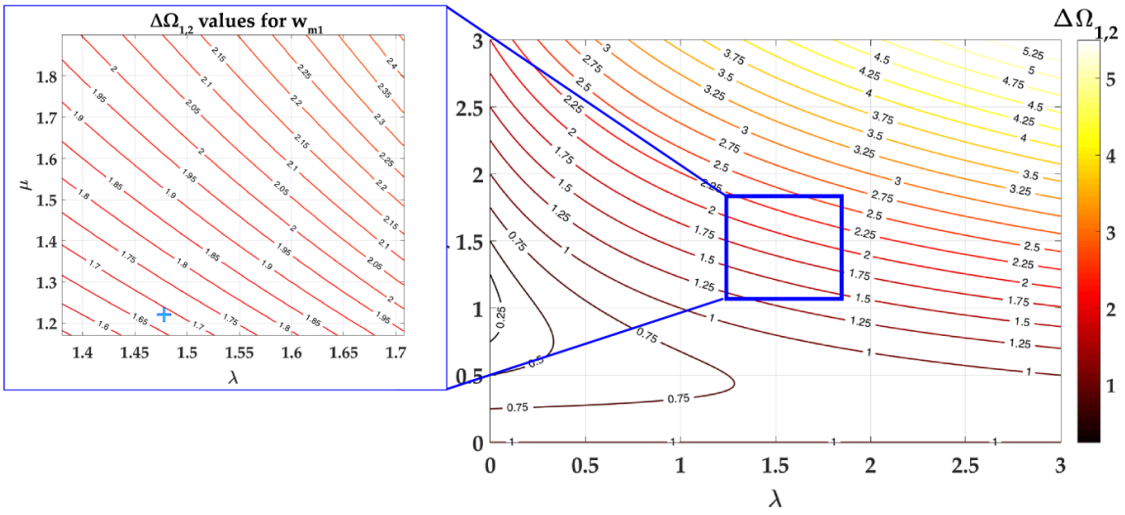

Figure 2.5: Contour plot of difference in the first two dimensionless eigenfrequencies ($\Delta\Omega$) with respect to ratio of beam masses (μ) and their respective first eigenfrequencies (λ)

2.2 Simulations

2.2.1 Design

The 2DOF micro-energy harvester is numerically simulated in COMSOL to acquire the optimal dimensions for the realization of enhanced stress distribution and narrowing of natural frequencies. Three different topologies of designs were investigated, namely, M-shape, M-long, and M-big. Figure 2.6 shows the schematic of the generalized harvester in COMSOL. The big-block is taken as the fixed support in the simulation. For modeling a MEMS piezoelectric energy harvester, the design structure consists of Si and the piezoelectric material is chosen to be PZT-5A, the one with the closest elasticity matrix with the PZT that we could accrue from Silex Microsystems on our wafers. The five main dimensional parameters that play an important role in determining natural frequencies are the length and width of the side beams, l_s and w respectively; length of middle beam, l_m, and widths of the middle beam at the attached and free ends, w_{m1} and w_{m2} respectively. The thickness of the device is decided by the SOI wafer used, i.e., 20 μm. The thickness of the proof mass is 100 μm for each design so that they could be fabricated within a single fabrication process plan.

Dimensions l_s and w govern the natural frequency of the system. They were chosen such that the device is in 1.2 - 1.5 kHz. If M-shape is taken as a reference, then M-long has a longer and narrower middle beam, while M-big is approximately double the size of M-shape to test the scaling of characteristics. Table 2.2 provides the detailed differentiation of dimensions on each design. The designs employed for the M-shape, M-long, and M-big were chosen to bring the first two natural frequencies as close to each other as possible. Therefore, each of these designs is an ideal representation of its particular features. Further description of the dimensional analysis relating to μ and λ is given in Paper 1.

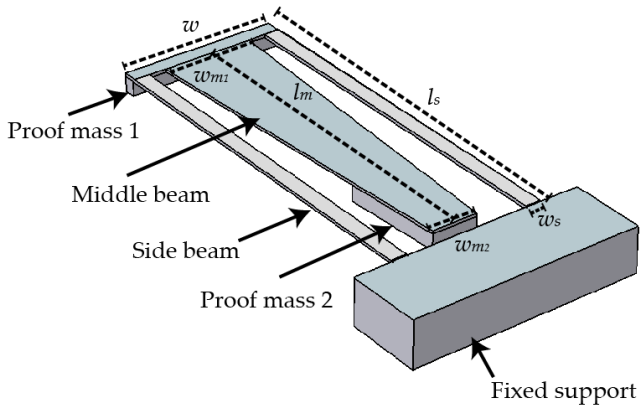

Figure 2.6: Schematic image of the M-design harvester setup in COMSOL. Table 2.2 outlines the dimensions of each design.

Table 2.2: Dimensions of M-shape, M-long, and M-big used in COMSOL simulations, in μm.

Dimensions	**M-shape**	**M-long**	**M-big**
l_s	2500	2900	5000
w	1000	1000	2000
l_m	2288	2700	4576
w_{m1}	560	500	1000
w_{m2}	300	100	400
w_s	100	100	200

2.2.2 Results

The results for the eigenfrequency simulations are shown in Figure 2.7. For the M-shape, the first and second eigenfrequencies are observed at 1473 Hz and 1763 Hz. The M-long design has its first two resonating frequencies at 1232 Hz and 1456 Hz. The M-big design, which is twice the dimension of the M-shape, gives its mode shapes at 408 Hz and 476 Hz. To the best of the author's knowledge, when the frequencies are in kHz, such closening of the first two natural frequencies has not been published anywhere else.

The von-mises stress gradient suggests that the vibration of the middle beam enhances the distribution of stress on the cantilever beams on each of the three designs. The middle beam does not act as a dormant proof mass; it has its own characteristic vibrational mode. The presence of stress on the middle beam is coupled with the side beam's stress, which leads to a larger area acting under stress. Figure 2.8 displays the distribution of stress on the outer edge of the cantilever side beams. The free end of the beam is at $x = 0$. The boundary conditions for each design were kept constant. Gravity and body load are the only forces acting on the whole device. There is no external acceleration provided to the system. The single cantilever has the maximum stress at its fixed end. About 20% of the beam experiences no stress near the free end. In contrast, the M-shape has the highest stress at its fixed end, half of it at approximately 75% from

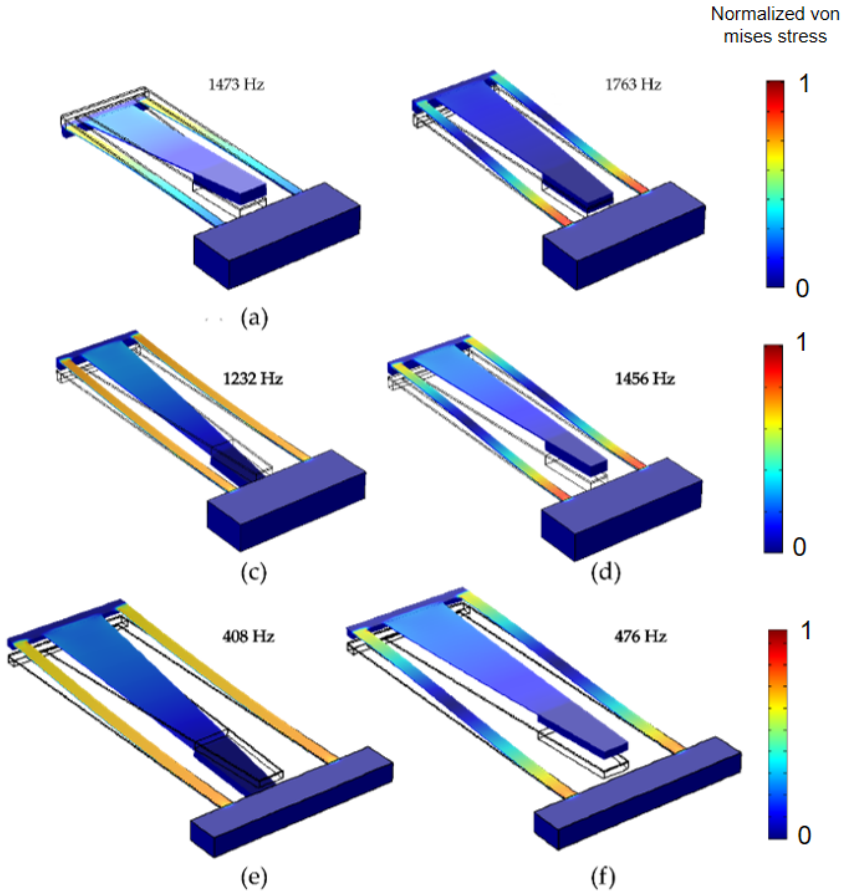

Figure 2.7: Mode shapes of **(a)**, **(b)** M-shape, **(c)**, **(d)** M-long and **(e)**, **(f)** M-big at the first and second natural frequencies. The gradient on the side displays the von-mises Stress (N/m^2) on the cantilever beams without the PZT piezoelectric layer.

the fixed at, and around 40 % at the fixed end. M-long and M-big devices display a different characteristic curve where the stress at their free and fixed ends are nearly constant. M-shape shows a constant stress at both ends, while M-big demonstrates an increased stress at its free end. Furthermore, on analyzing Figure 2.8, M-shape and M-long have a more than double the stress average than of Single cantilever. Although M-big has a lower value, the near-constant characteristic curve compensates for it.

The simulation output of the voltage of the designs suggest that M-shape has a peak voltage of 16.1 V at its first resonance frequency of 1538 Hz. It demonstrates a characteristic coupled curve from its 1538 Hz to 1820 Hz (2^{nd} eigenfrequency). This demonstrates that even at frequencies far off from the resonant frequencies, there is enough stress on the beams to generate an output. The Q-factor for the M-shape is 34.9. In M-long, a peak voltage of 4.7 V is obtained at 1257 Hz with a Q-factor of 36.9. At 1320 Hz, the output voltage reduces to 0 V, and it starts rising again until the second natural frequency at 1477 Hz. Figure 2.7(d) suggests the formation of an S-shape at 1456 Hz. Although the beam experiences high stress, the piezoelectric material on the same beam is stressed in opposite directions, thereby negating their respective outputs. Anti-resonance is featured at the second eigenfrequency in all designs. Similarly, M-big

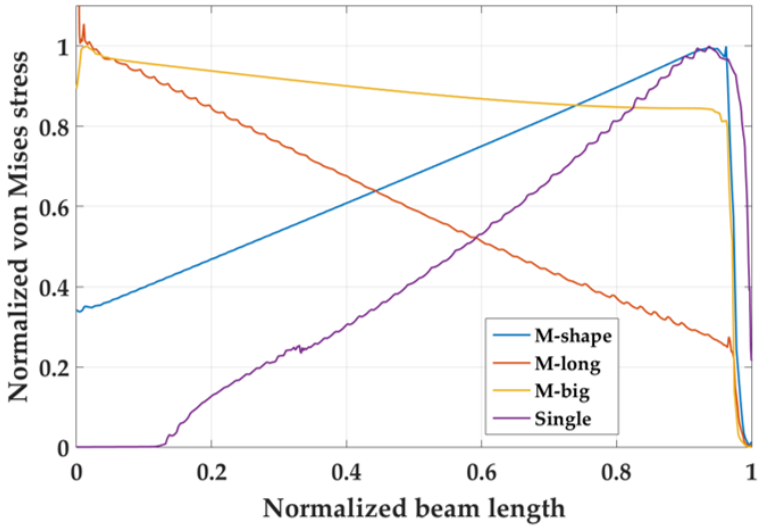

Figure 2.8: Normalized von mises stress on the sidebeams of the M-shaped energy harvesters compared to the single cantilever.

shows anti-resonance in between the two characteristic frequencies. It has the highest voltage output of the three design due to a larger piezoelectric area. Its peak voltage of 30.5 V is demonstrated at 426 Hz with a Q-factor of 35.5. Among these three designs, M-shape fares the best by having a lower Q-factor and a strongly-coupled model that induces a broader bandwidth of utilizable frequencies.

2.3 Fabrication

2.3.1 Process plan

After modeling and simulations for various cantilever designs, the fabrication of all three energy harvesters is performed through the following process scheme on a 6" Si-on-Insulator (SOI) wafer. Figure 2.9 shows the fabrication scheme.

- A 6" SOI wafer is cleaned (Figure 2.9(a)). The deposition processes of the bottom electrodes, lead zirconate titanate (PZT), and top electrodes were performed by Silex Microsystems AB, Sweden. A 20 nm layer of TiO_2 is sputtered onto the substrate. TiO_2 acts as an adhesion layer for Pt and also provides epitaxial uniformity to the buffer oxide. The Pt layer of 100 nm is sputtered, keeping the texture template uniform for the subsequent PZT deposition. A buffer layer of LaNiO (20 nm) is added on top of the surface. Then, a PZT layer of 1.1 μm is deposited by a sol-gel process on the buffer layer. The PZT layer has previously demonstrated an electromechanical coupling coefficient, e_{31} = -18 C/m^2 . Finally, the top electrode Pt/Ti layer is evaporated.

- The layers are etched one-by-one through separately patterned resist masks. For each layer, an AZ4562 thick resist pattern is spin-coated at 3000 rpm/s for 30

sec, and then soft-baked at 100 °C for 3 min. The resist is exposed through an Ultra Violet (UV) enabled mask aligner for 50 sec. The exposed pattern is then developed in MF319. The resist deposited on top of the surface protects the required layouts on the wafer. Thereafter, the top Pt/Ti layers are etched under Argon plasma at 400 W for 10 mins. The resist mask is removed, and another is patterned for the PZT layer. The 1.1 μm PZT layer is etched through a solution of HF:HNO_3:H_2O in 1 min 20 sec. Finally, the buffer oxide and the bottom Pt/Ti layers are etched by the same Argon plasma. (Figure 2.9(b)).

- A resist mask is deposited over the electrodes, and the device Si layer of the SOI wafer is etched until the buried oxide through SF_6 and C_4F_8 deep reactive ion etching (DRIE) process in Centura II (DPS & MxP). The etch process is performed by the tool in three steps, 1.2 sec of C_4F_8 passivation layer deposition, followed by the passivation breakthrough step of 1.3 sec and Si etching step of 1.5 sec. More information on the recipe is provided in Paper 1. The DRIE process lasted for 21 min for a 20 μm Si etch. (Figure 2.9(c))

- The wafer is then processed from the backside. The SOI wafer is bonded onto a carrier wafer by a thermal tape (120 °C release temperature), and an Al hard mask is etched; firstly a 500 nm Al layer is sputtered at the back; it is then patterned via ma-N1410 negative resist – wafer is heated at 100 °C for 5 min, the resist is spin-coated at 4000 rpm and then patterned through backside enabled UV mask aligner; finally an 85 % H_3PO_4 solution is used for etching Al in 3 min and 30 sec. (Figure 2.9(d))

- An AZ4562 resist mask is deposited and patterned to protect the proof mass structures. Since the etch rates for AZ resist:Si is 1:66, the 7 μm resist mask is thick enough to sustain the 100 μm Si etching. Si is then DRIE etched using SF_6 and C_4F_8 in STS-ICP plasma etcher in two cycles – etching for 12 sec and passivation for 7 sec. (Figure 2.9(e))

- The resist mask is then removed, and the bare wafer is etched from the backside for 280 μm until the buried oxide layer. (Figure 2.9(f))

Once the required structures are obtained, the wafer is diced into smaller chips.

2.3.2 Issues in fabrication

During the fabrication process, the challenges in frontside etching and the final thermal tape release led to the failure of nearly 90 % of the devices on the wafer. The frontside etching is to be performed on a resist patterned, 20 μm thick device layer. Centura II (DPS & MxP) is used for this process step. There were several bubbles trapped at the adhesive during the bonding of SOI wafer to the 8" carrier. This led to an uneven distribution of cooling on the wafer backside and eventually, the resist evaporated due to high temperature. This led to an uneven etching of Si in the device layer. Moreover, some of the electrodes were also etched during the process. Figure 2.10(a) shows the partially released *M-shape* device. The unetched Si is visible in the red circle. During

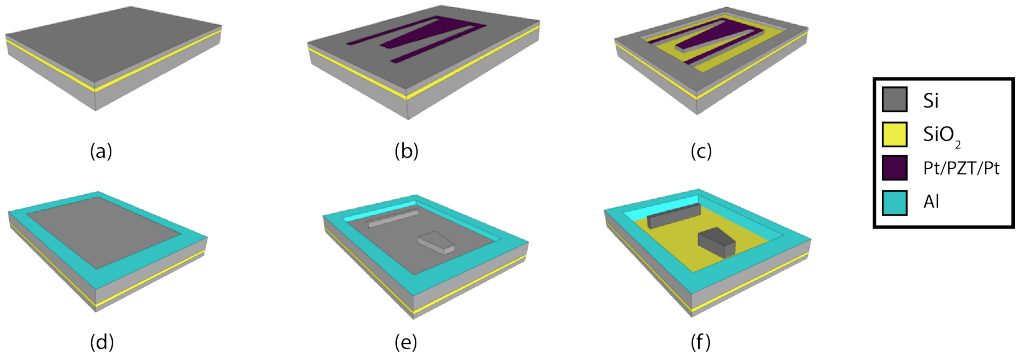

Figure 2.9: Process scheme for the microenergy harvester fabrication.

the release of thermal tape at 120 °C, there were several devices snapped near the edges of the secondary proof mass. Figure 2.10 demonstrates one such *M-big* device, which does not has a secondary proof mass, indicated at the blue circle.

2.4 Results and discussion

A setup of instruments is designed to record the vibrational characteristics of the device, shown in Figure 2.11. It consisted of a laser interferometer (Figure 2.11(1)) and reference, shaker table (Figure 2.11(2)), photodetector, and a vibrometer. The object is placed at the excitation table (Figure 2.11(3)). The laser beam from the scanning head is positioned to a scan point on the object through mirrors fitted into the system. The scattered light

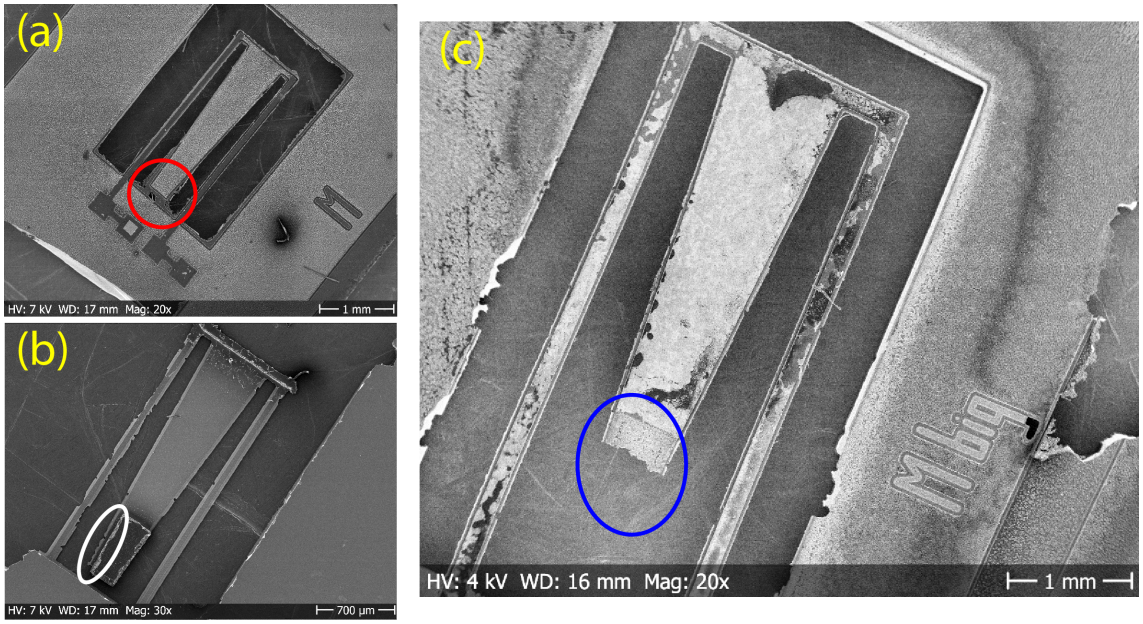

Figure 2.10: SEM micrographs of the fabricated energy harvesters. (a) *M-shape*. The red circle shows the partially etched Si device layer. (b) *M-long* after complete fabrication process. (c) *M-big*. The secondary proof mass is snapped off during thermal release, its intended place denoted through the blue circle.

from the device is received correspondingly. The backscattered light interferes with the reference beam at the scanning head and the photodetector records this interference. The decoder in the vibrometer provides a voltage which is proportional to the velocity of the vibration parallel to the measurement beam. This voltage output is digitized and processed as a vibrometer signal. There are various kinds of excitations possible in the measurement setup. They can be periodic with rectangular or sinusoidal vibrations, transient, i.e., with a pulse or an impact blow, and random noise generated signals.

Figure 2.12 shows velocity response in the measured frequency domain for the free end of the *M-shape* and *M-long* devices when investigated under an electrical signal. In the first graph, Figure 2.12(a), the response is recorded under a Gaussian white of amplitude 0.1 V across a frequency spectrum of 3.5 kHz. The first eigenfrequency of the design is measured at around 5000 Hz. It can be assumed that this is the eigenfrequency of the unreleased structure.

The second graph in Figure 2.12(b) shows the *M-long* device under a periodic chirp signal of 0.1 V across 3.5 kHz. The first two eigenfrequencies are measured at 1294 Hz and 1781 Hz. The shift in resonance peaks can possibly be due to over-etching of the proof masses; it still remains to be investigated. An interesting phenomenon in the graph is the presence of bandwidth of frequencies that oscillate at a measurable velocity between the two natural frequencies. This is the effect of using a 2DOF design that the device is stressed even at frequencies away from its eigenfrequencies due to its coupling mechanism. However, the coupling is not the only possible explanation for the shape of the response - and a simulation or model calculation of the shape of the frequency response is needed to draw further conclusions.

Figure 2.11: LDV setup for the vibration measurement experiments

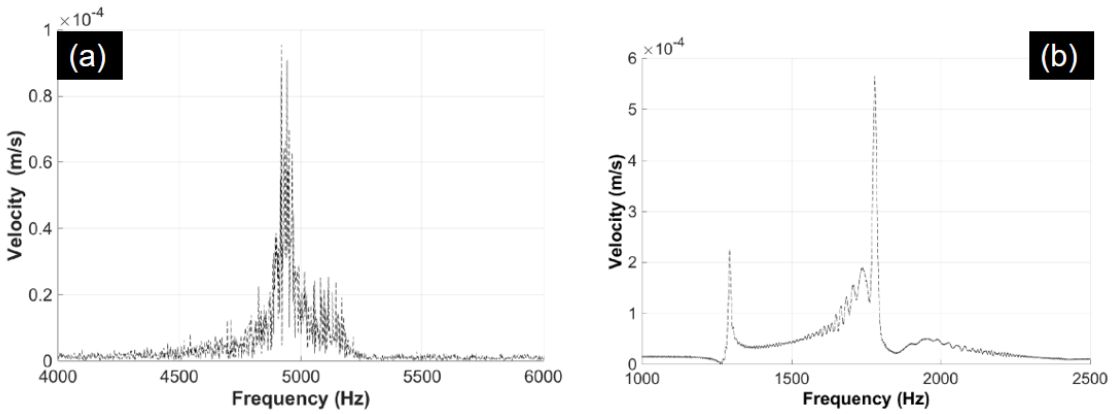

Figure 2.12: Characterization of *M-shape* and *M-long* in a LDV setup in different excitation signals. (a) *M-shape* under a gaussian white noise signal of 0.1 V amplitude. (b) *M-long* under a periodic chirp voltage signal of 0.1 V.

Chapter 3

Microsupercapacitors (MSCs)

As discussed in chapter 1, supercapacitors are energy storage devices that are essential for realizing an on-chip power supply. Supercapacitors generally utilize formation of capacitors at the electrode-electrolyte interface in the presence of a potential difference. The electrode material is a conductive film, sheet, or group of particles that have a large surface area for the interaction with the electrolyte. The electrolyte is a solution that can form ionic charges when a potential difference gives rise to an electric field in them. In the presence of a potential difference, the electrode atoms interact with the electrolyte atoms. This electrostatic interaction between the atoms leads to the formation of nano-capacitors with $d \approx nA$ [70]. These capacitors in parallel configuration lead to a substantial capacitance at the electrode-electrolyte interface. It is generally considered in the literature that these interacting molecules form an electric double layer (EDL) at the electrode-electrolyte interface. Helmholtz discovered this phenomenon for the first time in 1853 [71]. The studies by Guoy-Chapman in 1910 and 1913 [72] and later on Stern in 1924 [73], improved the theory of EDL charge storage further. The stored charge is then used to power the sensor node or the electronic unit connected to the output of the on-chip power storage unit. A supercapacitor has three main principles of storing charge - the electric double layer (EDL), pseudocapacitive, or a hybrid of the two. Figure 3.1 shows the schematic representation of the two mechanisms.

In EDLCs, charge storage takes place electrostatically (non-Faradaic) i.e., no shifting of charge takes place between electrode and electrolyte (which makes them highly reversible along with high cycling stability). Pseudocapacitance is another form of charge delivery in supercapacitors. In this case, the electrode stores charge through electrosorption, intercalation, and oxidation/reduction reactions between the electrode and electrolyte. Both these forms require a high surface area of interaction between the electrode and electrolyte. Thus, we can say that the choice of electrode material is mainly dependent on its specific surface area. Also, for a better capacitor formation at the interface, the electrolyte ion size should be equivalent to the pore size in the electrodes [70].

Supercapacitors are generally manufactured in the form of coin cells or box-like configuration. Coin cells are circular coin-shaped current collectors that also form the casing of the electrodes and electrolytes in the form of a cylindrical shell. The electrodes are cut out in the form of circular films to fit into each end of the coin cell. The electrolyte

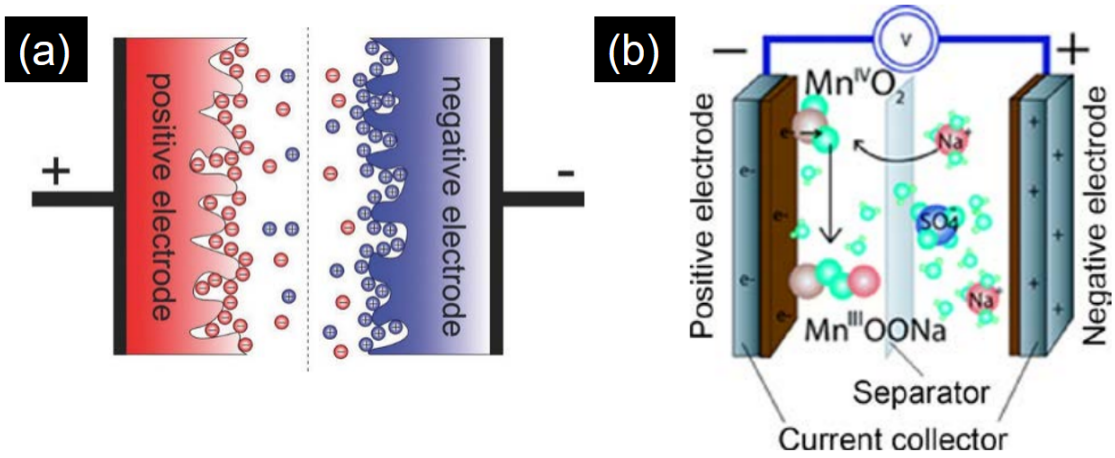

Figure 3.1: Schematics of (a) EDL and (b) Pseudocapacitive mechanisms for charge storage in supercapacitors [74]. Images are reproduced after permission from the publishers.

is then introduced in the system through a separator, a porous non-conducting film that allows transportation of ionic charges across its interface. The coin cell is sealed using a packing glue. These coin cells can be connected either in series or parallel depending on the requirements of the device that needs to be powered. The second configuration is the box-type assembly, where a rectangular box is used instead of the circular shaped current collector[75]. Both these designs have been commercially manufactured and are being used in high power applications in conjunction with batteries [76].

However, these supercapacitors generally require a large volume and specialized manufacturing techniques that make them hard to be integrable in microsystem electronics technology. Therefore, developing CMOS compatible fabrication processes has attracted much attention over the past few years [26, 27, 28, 29, 30]. Miniaturized supercapacitors, also referred to as microsupercapacitors (MSCs), are small enough to be integrated into electronic devices. Kim et al. [77] first conceptualized an MSC using a thin film capacitor with W-RuO_2 electrodes . Further, Yang [78] fabricated wire-like MSCs in 2007 . These studies have now expanded quite much since the integration of micromachining techniques in fabricating these devices. These devices can be integrated either as self-powering systems with charging through energy harvesters, or enhanced micro battery systems where they act as hybrid devices with batteries to improve the lifetime of a device. MSCs are devices that are generally fabricated on a substrate using MEMS technology. These devices are emerging as strong candidates for energy storage units in conjunction with micro-batteries due to various reasons. Firstly, they can be easily integrated into on-chip integrated circuits and secondly, they are cheap to manufacture as MEMS technology can be used to fabricate several devices on a single substrate while using a standardized process. However, we require optimization of such advantages for MSC integration into pre-existing MEMS and CMOS processes. In the next few sections, we are going to discuss the MSCs in more detail. We will first discuss a brief literature survey of the field and describe the advantages/disadvantages of different MSC fabrication techniques. Next, we shall talk about the electrodes materi-

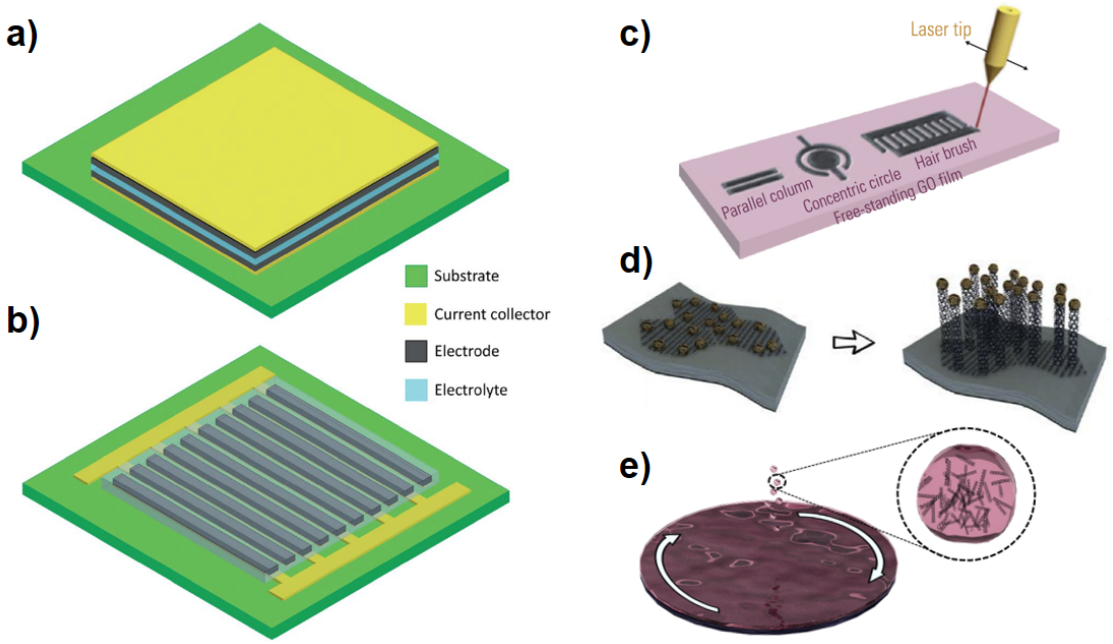

Figure 3.2: Types of MSC designs (a) stacked and (b) planar [79]. Methods for electrode deposition (c) laser scribing [79], (d) chemical vapor deposition for CNFs and VACNS [80], (e) spin coating of carbon based solutions (Paper 3. Images are reproduced after permission from the publishers.

als that can be utilized in a CMOS-compatible fabrication process. In section 3.1, we shall discuss the fabrication methods of CMOS-compatible processes, and subsequent issues in fabrication. Then we shall discuss the results from these fabrication processes. Finally, we shall talk about the optimization process performed and its effect on the electrochemical performance of the devices.

3.1 Device design

There are two main configurations for MSC fabrication – stacked and planar (Figure 3.2(a,b)). Stacked MSCs are sandwich-type structures with an electrolyte between two electrodes, while planar MSCs are devices with two in-plane electrodes separated by a specific distance. A planar MSC design holds several advantages over the stacked structure. Firstly, since the planar electrodes are on the same substrate, the side-by-side interactions of the electrolyte with electrodes results in an improved rate performance. Secondly, fabrication of the planar structure through microfabrication can allow us to accurately control the spacing between the two electrodes, leading to high ion transport across the two terminals. Moreover, the stack of electrodes, electrolytes, and current collectors would require specific masking techniques in the fabrication process, leading to a challenging list of process steps. Thus, for high-performance planar MSCs, it is imperative to have an electrode deposition technique that results in thicker electrodes and ensures that the deposited film can sustain and withstand post-processing lithography and device integration steps. A variety of methods can be used to fabricate thin films of

these materials [81].

Figure 3.2(c-e) show the different fabrication processes that are generally used to deposit, etch, or grow the electrode structures onto planar substrates. Among these, we will mainly discuss the possible techniques utilized for CMOS compatible integration, namely - laser scribing, ink-jet printing, photolithography, and chemical vapor deposition.

3.1.1 Laser scribing

Laser scribing, as shown in Figure 3.2(c), is a method to develop MSCs in a simple, cost-effective, and scalable way. Its concept is to irradiate graphite oxide with a laser beam to convert it into graphene through a photothermal effect. This ability of reduction makes it feasible for direct patterning of electrodes on any form of substrates. It is also possible to fabricate both planar and stacked MSCs through this process.

In some cases, direct laser reduction of GO to graphene sheets can be performed by a LightScribe DVD optical drive [82, 83, 84]. The films that were produced were mecahnically robust. They also showed a high electrical conductivity. The authors claimed that these films can be used directly on a substrate without requiring binders or current collectors. These electrodes were fabricated on flexible substrates such as nitrocellulose membrane, photocopy paper, or conductive Al foil. The devices demonstrated a high power density and excellent cyclic stability. Later, Wen et al. [85] improved the performance of LSG by combining it with a coated layers of GO/carbon nanotubes (CNTs) hybrid powders on flexible polyethylene terephthalate (PET) sheets. In the presence of CNTs with a smaller diameter, the laser-scribed CNT combination of electrodes is yeilds a better electrochemical performance. These devices were integrated with solar cells to demonstrate the feasibility of using MSCs as energy storage units for an on-chip power supply [86].

Laser scribing is a process that can be integrated into CMOS compatible machinery but has not been yet. Despite its excellent electrochemical performance, this process is severely restricted to materials that can be reduced by laser irradiation. Another issue with this process is the speed of performance. It is stated that about a 100 MSCs can be fabricated in 30 min using a LightScribe DVD burner [87], which is not enough when it comes to the fabrication of semiconductor devices. CMOS devices are currently fabricated on 200 mm wafers which can incorporate more than 300 energy harvesters, or at least a 1000 ICs based on their areal statistics [88]. Using a laser scriber will be a massive bottleneck in the pipeline fabrication process. Moreover, if this technology needs to be integrated with CMOS processing with the same feed through, then select laser lamps that can expose entire wafers through a photomask must be used. To the best knowledge of the author, such practices still have not been introduced in a research facility, so it is safe to say that they are far from being utilized in an IC manufacturing facility conventional CMOS processing equipment is more prevalent. Despite the disadvantages, the simplicity, reproducibility and substrate independence of laser scribing makes it a perfect candidate for flexible and wearable electronics where the throughput and use of equipment are not severally constrained by pre-existing irreplaceable technologies.

3.1.2 Ink-jet printing

Ink-jet printing is another promising electrode fabrication technique that can be easily explored in CMOS integration strategies. It is a typical technique used to deposit electrode films at precise places defined by a computer automated design (CAD). With ink-jet printing, a variety of electrode films can be deposited which are not limited to carbon materials. In this process, a liquid ink of an electrode is prepared and deposited on a substrate with a jet nozzle similar to 3D-printing equipment. The process is as scalable as the size of the jet nozzle allows, i.e., it can go up to 2 μm of resolution [89]. The main advantage of ink-jet printing is similar to laser scribing as it requires only one fabrication step for electrode deposition. Another significant advantage of ink-jet printing over laser scribing and photolithography relates to the minimum use of ink while fabrication takes place. With laser scribing and photolithography, there is a substantial waste of electrode material, which is either not utilized in the former and wasted during a spin coating or doctor blading process as in the latter. Moreover, the direct phase transformation of the liquid ink into a solid-state active electrode nanomaterial adds to its merits.

This process has been used to fabricate flexible MSCs using CNT/Ag and poly(3,4-ethylenedioxythiophene): poly(styrene sulfonate) (PEDOT:PSS) as the electrode material [90]. At that time it had delivered the best rate capability among all reported paper-based MSCs. Ink-jet printing is also used to deposit graphene inks [30], reduced graphene oxide (rGO) with polyaniline (PANI) composites [91], and lamellar $K_2Co_3(P_2O_7)_2.2H_2O$ nanocrystal whiskers on graphene sheets [92] with tunable geometry and thickness. These devices have demonstrated high flexibility, excellent rate/mechanical stability and high cycling stability with a good electrochemical performance demonstrating great promise for applications in flexible all-solid-state microsupercapacitors.

The main issue with ink-jet printing as with laser scribing is the introduction of new equipment in a CMOS processing framework. Clogging of inks in the nozzles and slow throughput are a few disadvantage that ink-jet printing faces. This is a recurring issue in 3D printing as the nozzle either needs to clean out entirely or replaced after a certain number of cycles. Thus, only after such challenges are addressed, this process will be fully capable of introduced in an automated IC fabrication process.

3.1.3 Photolithography

Among the list of different fabrication process described, photolithography is the only IC-compatible process that is currently used in MEMS and CMOS processes. MSCs can be fabricated easily and cheaply with an extremely high resolution that is only dependent on the lithography tool available.

Several strategies can be used to fabricate MSCs using photolithography. One of them is spray coating, where an electrode material is spray-coated on a substrate. Then either a metal can be evaporated on the substrate and then etched using reactive ion etching, or a resist can be deposited on the electrode layer, followed by developing trenches for electrode evaporation and lift-off [81]. Another variation of the technique

can be a double lift off of the electrode and the current collector using a single photoresist mask on the substrate. [93]. This process can be called as the inverted current collector process as the current collector is on top, instead of being on the bottom as conventional MEMS processes. The main advantage of this technique is that it requires only one photomask, and thus its easier to fabricate. However, there are more disadvantages that inhibit the utilization of this process in integration with CMOS circuitry. Inaccessibility of the electrolyte on the top and bottom ends of the electrodes would severely restrict its performance. Secondly, during the development process for electrode or current collector lift-off, the tendency of the electrode material to dissociate from the substrate is quite high. Known measures to improve the adhesion to surface involve deposition of a metallic nanoparticle layer desscribed in Paper 2. This nanoparticle layer would then need to be etched out using a second photomask. Therefore, use of a single photo masking technique is good to research the device structure and electrode properties in an easily fabricated device, but, its reduced electrode surface area and dissociation of electrode material from the substrate during aqueous development of resist restricts it to be fully CMOS compatible. Using a two-mask lithography process, however, is an extremely employable process in CMOS processing. Techniques such as spray coating, doctor blade layering, and spin coating of electrodes on prepatterned electrolytes can be supported feasibly by using a second masking process for etching the electrodes from unwanted areas. The fabrication process for a two-mask MSC process is described in section 3.3.

Pech et al. [94] fabricated a pair of interdigitated electrodes from onion-like carbon that operated as a single microsupercapacitor . That microsupercapacitor showed a discharge rate three-orders higher than conventional supercapacitors because of the ease with which ions could diffuse between the electrodes. After that, the research of interdigitated electrodes has expanded to include other materials, such as CNTs, graphene, rGO, and hydrated GO. Laszcyzk et al. [95] demonstrated an MSC fabrication technique where they deposited CNT as an electrode material through a doctor blade technique. Pan et al. [96] followed a new protocol mimicking the spider's spinning process are developed to create highly oriented microfibers from graphene-based composites via a purpose-designed microfluidic chip. Similarly, Kim [29] fabricated an electrode based on a boron-doped 3D porous carbon pattern by lithographic processes is demonstrated. The electrode layer is obtained by carbonization and doping of a polymer pattern fabricated by interference lithography. Lithography can also be performed on flexible substrates such as PET. Hu et al. [97] fabricated Au/PANI electrodes involving laser printing technology and in situ anodic electropolymerization while exhibiting remarkably high mechanical flexibility and show an excellent cycling stability .

Considering the needs of an automated CMOS process, out of the three deposition techniques, spray coating, doctor blade layering, and spin coating. Spray coating is a process in which a solution is designed to be used in a jet that sprays the ink across the whole substrate. It is different from ink-jet printing in terms of the manner of the coating. In a doctor blading process, an electrode solution is poured on the substrate. Then, a blade with a specific distance from the substrate is swiped over the electrode film. In the spin coating process, the electrode solution is used analogous to a photoresist, following the same fabrication process as currently being used for polymeric resists such

as AZ4562, or S1813. Among these, only spin coating emerges out to be a viable option. Other alternate techniques are limited by several obstacles which are less relevant to the current discussion. It suffices to stress that spin-coating and photolithography is a route to use existing standard tools in IC manufacturing, hence it is advantageous, regardless of the various difficulties other techniques need to face before possibly being implemented in manufacturing.

3.1.4 Chemical vapor deposition

Chemical vapor deposition is an attractive electrode fabrication process as it is pre-existing in the semiconductor industry for thin film deposition. Several carbon-based materials have found a way among MSC electrodes through this growth process. Among these, graphitic petals or graphene nanosheets directly synthesized on Ni foil and carbon cloth using microwave plasma chemical vapor deposition (MPCVD) exhibit promising potential for MSC applications [98]. Xiong et al. fabricated high-power MSCs based on micrometers-thick graphitic petal electrodes [99]. The electrodes were prepared by using microwave plasma CVD and patterned by optical lithography and reactive ion etching. Similarly, multilayer graphene and monolithic 3D graphene have also been fabricated by Ye [100] and Zhang [101], respectively. A wide variety of material such as diamond-coated Si nanowires has also been grown through the CVD technique. These were used to fabricate asymmetric MSCs [102]. Similarly, Zhang et al. [103] developed a facile vapor deposition and sewing sequence to create rugged textile MSCs.

So, among these different techniques, only spin-coating and CVD emerge as fabrication processes that are utilizable in near-immediate future for the fabrication of on-chip MSCs for integration wit ICs and MEMS energy harvesting devices. In the next section, we will describe the different materials that we have used for fabricating MSCs that can be considered CMOS compatible.

3.2 Material selection

MSC electrode design is based on the same considerations as supercapacitors – electrodes with large specific surface area and their pore size. Carbon-based electrodes fulfill both of these requirements owing to their excellent electrical conductivity and high specific surface area [104]. Graphene, rGO, CNTs, and ACs are some such materials with ultrahigh specific surface areas and impressive mechanical and chemical stability. Moreover, their pore sizes are greatly beneficial in improving the charge/discharge performance, and their electrical conductivity is high too. They promote rapid diffusion of ions due to their excellent meso, micro, and nanopore distribution across their surface. Carbon-based nanomaterials can be obtained in solution through vendors that sell products through the internet.

For the spin coating process, we require solutions that can act as photoresists, i.e., like polymers with a specific density and viscosity, uniform coverage across a substrate during spinning, and good adhesive properties. We used several solutions based on graphene. First, we started with using rGO dispersed in water. However, since rGO does not form any H-bonds with water, the solution is constituted of macro colloidal spheres

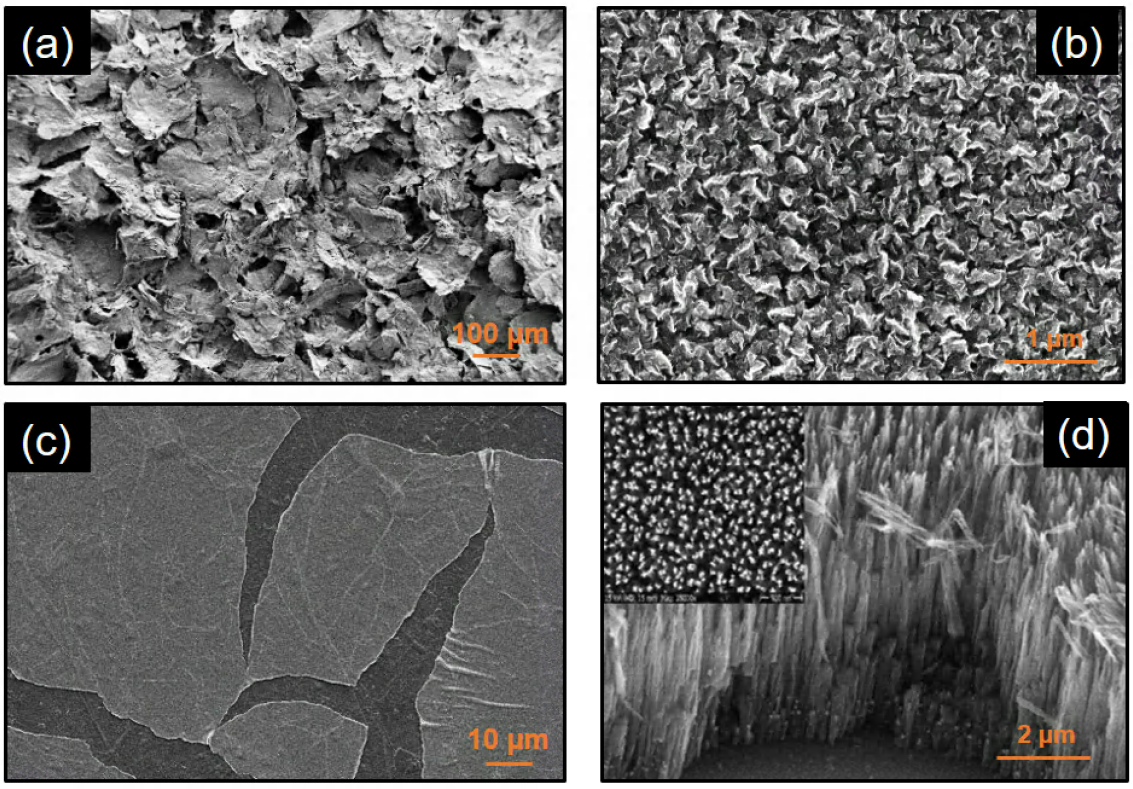

Figure 3.3: Scanning electron micrographs of different materials that can be used for MSC fabrication (a) CNTs, (b) VACNS, (c) rGO, (d) CNFs [105]. Images are reproduced after permission from the publishers.

of rGO separated from each other in the solution at large distances. Spin coating this solution proved extremely ineffective as the coverage of these particles on the substrate was barely visible. The coating process added two considerations for the solvent for the electrode material. Firstly, the electrode must dissolve into the solvent. Secondly, the density of the solution must be high enough for uniform coverage across the substrate surface. When we used a solution of GO with water, it led to quite positive results. In the end, we fabricated the MSCs using three inks - GO and water, CNT and water, and AC in water. Figure 3.3(a, c) shows the SEM of the CNTs and rGO on the fabricated substrate. Among the three, GO, and CNT MSCs were fully fabricated, while the AC solution was deemed to be ineffectual in the spin coating process. The CNT fabrication process, however, was not reproducible as the spin coating process for CNT solutions could not be fully optimized. Besides, the retention of CNTs after several fabrication steps was not uniform on the wafer, which led to non-uniform etching in the subsequent fabrication process. In this work, we are going to discuss rGO MSCs in the spin coating process more specifically as their fabrication process has proved to be the most reproducible process. On top of that, rGO's ability to form bonds with metal oxides makes them a viable candidate for hybrid MSCs. Use of metal oxides such as RuO_2, MnO_2, V_2O_5, IrO_2, Fe_3O_4, NiO, Co_3O_4 etc. transition metal sulphides with rGO films during MSC fabrication can lead to even higher performances for MSCs based on the spin coating process [106].

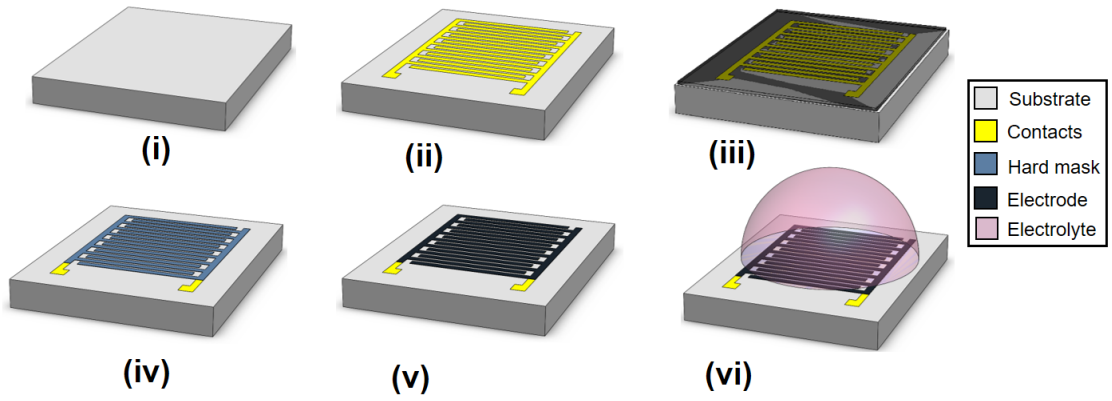

Figure 3.4: Fabrication process for MSCs: (i)standard cleaning of the substrate followed by oxidation, (ii)lift-off or reactive ion etching of the current collectors, (iii) electrode deposition, (iv) Al hard masking, (v) Electrode etching in O_2 plasma, (vi) Electrolyte and electrochemical analysis.

We used CNFs and VACNS as electrodes for the spin coating process. Figure 3.3(b, d) show the SEMs of these materials. CNFs are carbon materials that have the potential to be grown using a moderate CMOS compatible temperature of 390 °C. The strategy for their growth is optimized by Smoltek AB, a carbon growth company based in Gothenburg, Sweden. Their studies [105] suggest that use of CNFs as electrode materials is adaptable in the CMOS compatible MSC fabrication process. VACNS are carbon material that demonstrates extremely high electrical conductivities. We realized that the electrochemical performance of spin-coated MSCs is limited due to high contact resistance between the current collectors and the spin-coated electrode. So, if an interface between electrode and collector that minimizes the contact resistance - i.e. not just a highly conducting interlayer is used as an interconnect between the current collectors and spin-coated material, which is also carbon, the MSC performance can be improved significantly. Plus, the growth of VACNS is substrate independent, which implies that it can easily be integrated into the reproducible fabrication process scheme. However, we will limit our discussion to rGO based MSCs and their performance with respect to on-chip integration.

3.3 Fabrication

The wafer-scale fabrication procedure for MSCs is shown in Figure 3.4.

3.3.1 Oxidation and current collector fabrication

Oxidation

A 2” Si wafer is used as a substrate. Its surface is oxidized to SiO_2 in the oxidation furnace Centrotherm at 1050 °C for 45 min. (Figure 3.4a).

Lift-off

Gold and titanium (Au/Ti) current collectors are deposited using the lift-off technique. Lift-off process is a clean process that does not involve a substrate being subjected to highly reactive chemical etchants. Generally, a resist should have a higher process thickness than desired metal thickness. This allows for the metal layer to break off the resist wall during an evaporation procedure. The resist is then developed, and the freestanding metal layer on top is lifted off. Thus, S1813 lift-off resist with a thickness of 1.3 μm is spin-coated for 60 s at 4000 pm with 2000 rpm/s acceleration. After soft baking for 5 min at 180 °C, the resist is exposed in the mask aligner using a contact layer photomask. When the wafer is in hard contact with the photomask with a helium cushioning of 20 μm, UV light is radiated on the setup. The light breaks the polymer linkages of the exposed positive resist, which is then developed in MF319 developer for 60 s and transferred to the water. A post bake for 1 min at 120 °C is essential for resist hardening. Once the pattern is ready, Au/Ti (100 nm/10 nm) metal layers are evaporated onto the substrate in Lesker PVD. Physical vapor deposition (PVD) is a process in which the bombardment of electrons heats a metal in condensed form in an ultra vacuum chamber. The vapor phase produced by the e-gun travels in a vertical electric field toward the target wafer where it reverts to a condensed phase as a thin film. After the deposition of Au/Ti layers, the lift-off process is completed by submerging the wafer into mrREM 400 bath while being ultrasonically treated for 55 min. Figure 3.5(a) shows the optical micrograph of the patterned interdigitated Au/Ti electrodes on Si/SiO_2 substrate. Although gold is used for proof of concept, it can be replaced with CMOS compatible metals such as Pt, Pd, or Mo.

3.3.2 Electrode deposition

Graphene oxide

The GO solution used for spin coating was purchased from Graphene Supermarket. The solution was diluted in DI-water to 3g/l and then sonicated for 15 min at 80 °C in 35 kHz sonication. The sonication before spin-coating dissociated the graphene platelets from stacking and aggregation. Next, graphene oxide (GO) is spin-coated five times on the substrate. Each iteration comprises of pouring the GO solution on more than four-fifths of the wafer, spinning it for 60 s at 1000 rpm with 1000 rpms acceleration and soft baking it at 100 °C after every spin. Post-spin-coating, the wafer is baked at 100 °C overnight to remove the water concentration from the coated films. (Figure 3.4(c), 3.5(c)).

CNFs

The growth of CNFs requires a metal catalyst on which the carbon-containing gases can decompose into carbon precursors. The precursor is adsorbed on the catalyst, in our case, AuTi, and diffuses into the surface. Once, the catalyst is saturated with the carbon precursor, the incoming precursor precipitates below it, lifting the catalyst nanoparticle above the substrate. This controlled precipitation can be used for growing CNTs, vertically aligned CNTs, and CNFs through different mechanisms which are

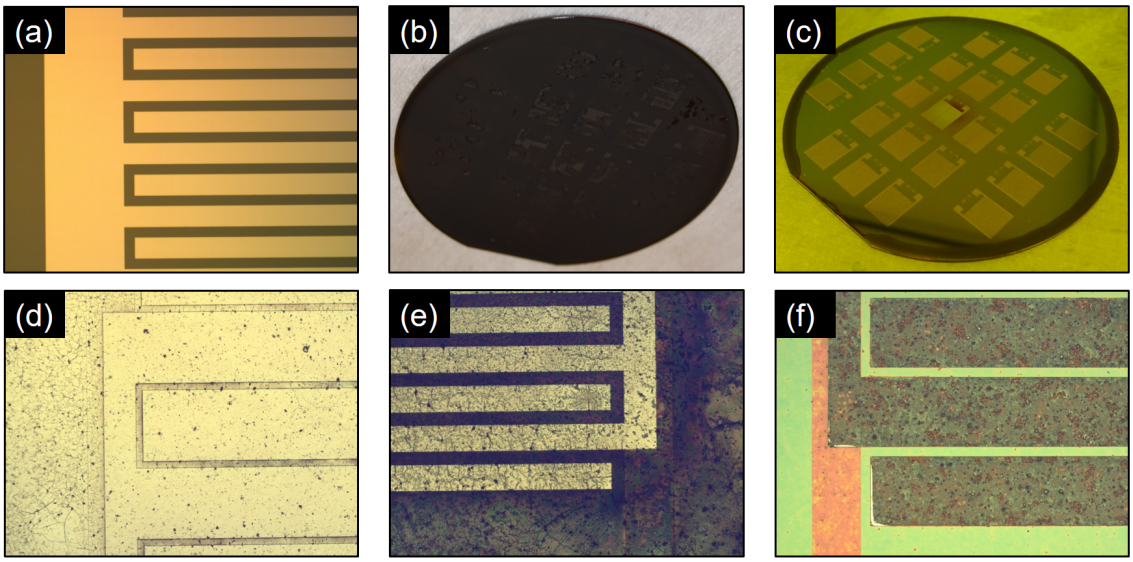

Figure 3.5: Results from the fabrication process for MSCs: (a) Au/Ti current collectors after lift-off. (b) growth of VACNS over the 2" $SiSiO_2$substrate (c) spin coated GO solution after repeating the coating process five times (d) deposition of photoresist for etching the Al hard mask (e) Al etch and (f) subsequent etching of uncovered GO and annealing at 500 °C for 5 min.

similar in nature. In our case, the recipe that was followed has been mentioned in article published by Saleem et al. [105].

VACNS

VACNS was grown on the prepared substrates in a cold-wall low-pressure PECVD reactor (Black Magic, Aixtron). The ordinary recipe is that the substrate was heated to 775 °C with the ramp rate of 300 °Cmin and annealed for 1 min with the mixing of 20 sccm H_2 gas and 1000 sccm Ar gas flow. The plasma was then turned on with a DC bias with the power of 75 W. The plasma voltage is 800 V with the current limit of 0.5 A. The actual growth was initiated by introducing acetylene gas (C_2H_2) and maintained for 10 min. After the growth, the system was evacuated to be less 0.2 mbar and cooled down to room temperature. Growth time and C_2H_2 flow rate used in this process can be changed to control the size of VACNS. Figure 3.5(b) shows the fabricated VACNS on a 2" Si/SiO_2 wafer.

3.3.3 Al hard masking

Further, an Al hard mask is fabricated on the solvent-free GO surface. This enables etching of carbon material in areas outside the interdigitated pattern. A thin film of Al, 70 nm, is evaporated on the substrate. S1813 resist is spin-coated on it for 60 s at 4000 rpm with 2000 rpm/s acceleration. It is soft baked for 2 min and dried overnight at 110 °C. Figure 3.5(d) shows the device after this step. The Al film area which is not covered by the resist is dry-etched in Oxford Plasmalab using a standard recipe mixture of Cl_2 and $SiCl_4$ in presence of Ar (Figure 3.4(d), 3.5(d)). When Cl_2 reacts with Al, it produces $AlCl_3$

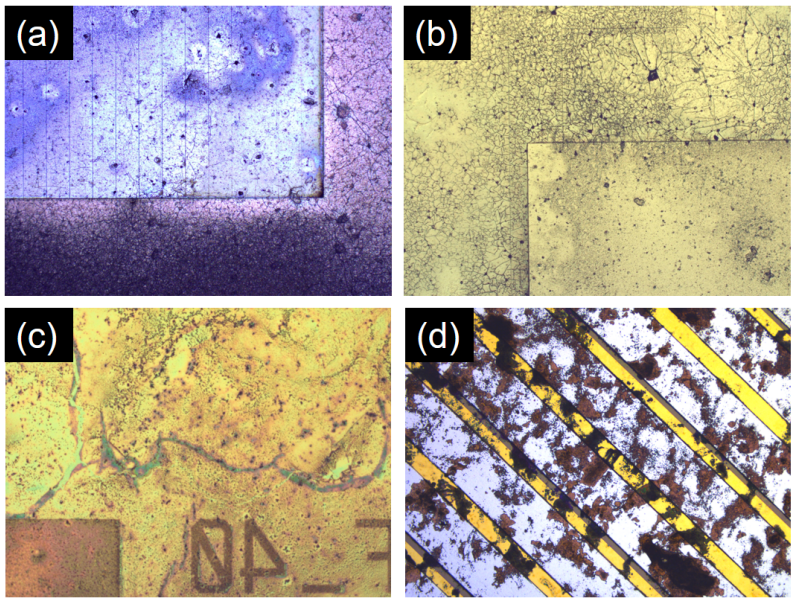

Figure 3.6: Issues in the fabrication process (a) Photoresist could not be completely developed during the fabrication of the Al hard mask. (b) Undeveloped resist leads to unetched Al (c) and unetched GO in the pre-final step. (d) Incomplete etching of GO on the devices at the edges of the wafer is also an issue related to uneven etching.

that is volatile enough to get removed during the gas exchange in the plasma chamber. $SiCl_4$ is generally used to protect the Al layer from an undercut.

3.3.4 Electrode etching

With the hard mask on top, GO is dry-etched in Plasmatherm using O_2 plasma at 100 W in a 100 mTorr pressure chamber for 4 h, shown in Figure 3.4(e). During this step, the resist on top of Al hard mask is also ashed away. Once the GO is completely etched from uncovered areas, Al is completely etched away using the dry etch recipe discussed in the previous step. Figure 3.5(f) shows the result after the final fabrication step.

3.3.5 Annealing

This step is required only for GO electrodes. The reduction of GO to rGO can performed chemically or thermally. In this work, we have used thermal annealing of GO substrates for the material reduction. Conductivity and surface area are maximum for GO solutions annealed at 500 °C [107] which is an ideal temperature for a CMOS compatible process. The annealing process commences at 150 °C, ramping up every minute by 10 °C until 500 °C. The temperature is held for 5 min at that instance and then ramped down 10 °C/min till the substrate is cooled down to room temperature. The Raman micrographs for the rGO can be seen in the manuscript by Smith et al. [27]. (Figure 3.4(f))

3.4 Issues in fabrication

Although the fabrication process is reproducible, there were several issues that still existed in the process. Figure 3.6 shows the different issues that existed in the described process plan. Al deposition on the electrode surface was the main issue that led to several other problems in the subsequent step. The spin-coated GO solution was not uniform across the surface of the substrate. It had a difference of height of more than 70 nm across 1 mm of surface, and since the optimum thickness supported by the GO layers was 70 nm of Al, several cracks developed across the surface. When a resist was spin-coated and developed on the Al coating, the water from the developer solution invaded these cracks, which expanded into steam during soft baking. This led to uneven etching of the Al hard as can be seen in Figure 3.6(b). Furthermore, in the subsequent GO etching step, the electrodes could not be fully etched out from the surface, seen in Figure 3.6(c, d). It eventually led to short-circuiting in different regions of the wafer. The wafer yield accrued after electrochemical wafers was around 8 - 10 working MSC devices on a wafer of 23. Thus, there was an urgent need for optimization in the process plan which would provide a higher yield which is a standard in a CMOS process. We shall discuss the optimization step in section 3.5 after a review of the electrochemical results of the MSCs fabricated.

Regarding the CNF and VACNS process, we found that the CVD process does not behave in a uniform fashion while occurring on a full, 2" Si/SiO_2 wafer. The results indicated that there is a non uniform temperature gradient in the growth chamber which leads to uneven electrode heights. In some cases, the MSCs were found to be highly resistive. These results could be easily mitigated when the growth was performed on individual chips of 1 cm^2 area. Thus, as of now, we cannot consider the CVD of CNFs and VACNS a viable option of CMOS compatible process.

3.5 Electrochemical results

The electrochemical results for rGO based MSCs are shown in 3.7 and 3.8. The formulation of results from the electrochemical measurements have been documented by Qi Li in his thesis work [74]. The MSCs fabricated were evaluated on Karl Süss PM 5 probe station coupled with a Gamry Reference 3000AE potentiostat. For the sake of consizeness, we have presented the results from only one of the devices on the substrate. More results and discussion are performed in Papers 2 and 3. This device was chosen for its high power density during the characterization of all devices. Cyclic Voltammetry (CV) at scan rates of 100-5000 mV s^{-1}. The Galvanostatic Charge Discharge (GCD) measurements were performed at 1, 2 and 5 μA current input. For the Electrochemical Impedence Spectroscopy (EIS) measurements, the graphs shown in Figure 3.8 are produced at a 0.2 V input sinusoidal signal.

Figure 3.7(a) shows the cyclic voltammograms of the intedigitated MSC with 20 fingers with a 60 μm spacing between them (20F-60). These curves demonstrate a cyclic with strong capacitive behavior. With increasing scan-rates, the capacity of the MSC increases also. In Figure 3.7(b), the GCD measurements demonstrate the MSC can be charged up to 1 V within 10 s at a current density of 1 μA. At higher current densities, the

MSC expectedly can be charged within 1 s. These results are extremely positive when it comes to an on-chip power supply as the power management circuitry will require less current to charge the MSC completely.

Figure 3.8(a) shows the Nyquist plot of the EIS measurements. This graph is used to measure the effective serial resistance of the supercapacitor (R_{esr}), its Warburg impedence (IW) and real capacitance (C_{msc}, C_{real}). These results are described more extensively in Paper 3.

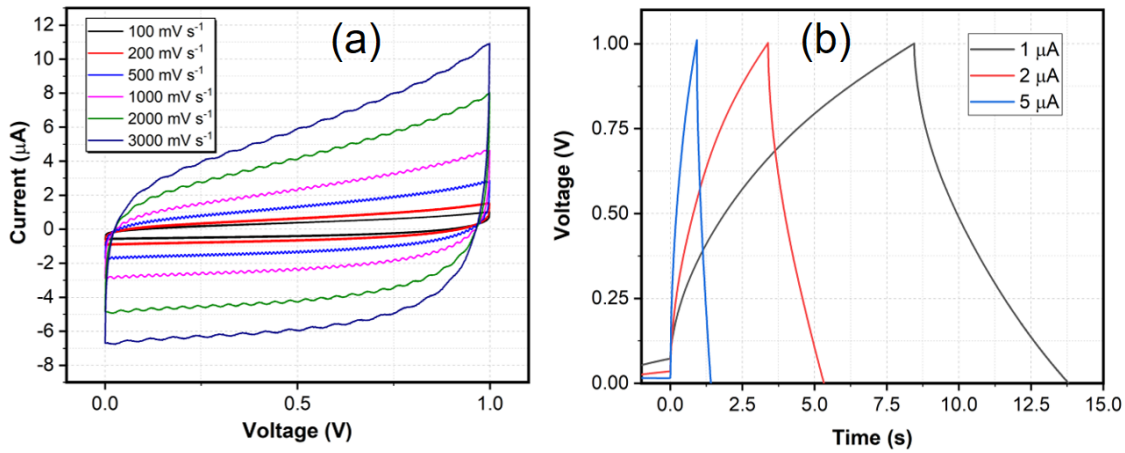

Figure 3.7: Electrochemical results for spin coated rGO (a) Cyclic voltammograms of 20F-60 devices at different scan rates (b) GCD curves for MSCs at varying current densities.

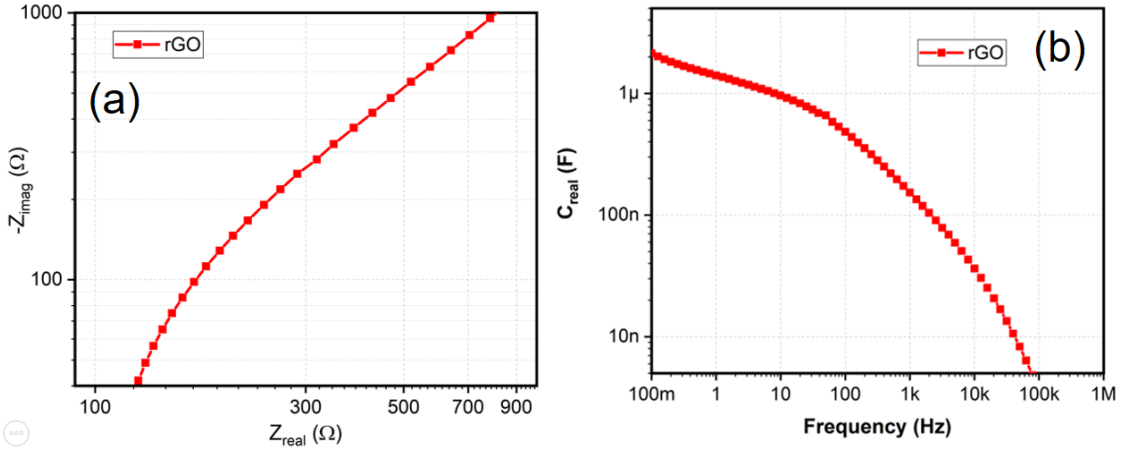

Figure 3.8: (a) Nyquist plot for the EIS of rGO 20F-60 samples (b) Actual capacitance (C_{real}) vs. frequency of operation.

3.6 Surface optimization for effective spin coating

As discussed previously, wafer yield is a vital statistic for achieving a reliable process. The CVD processes cannot be considered a viable option as the results on different

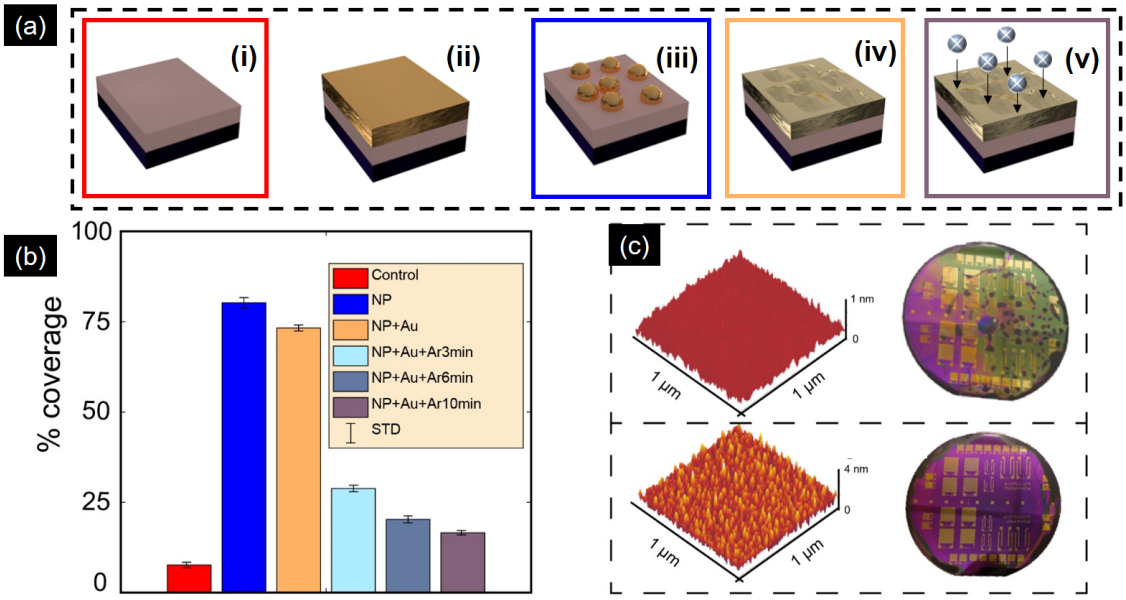

Figure 3.9: (a) Schematic fabrication process for the surface optimization of MSCs for an improved spin coating process. (b) Coverage of the wafer surface after using different optimization techniques. (c)(a) AFM comparison of roughened and non-roughened sample sufaces along with optical microscopy images showing the coverage of the electrode spin-coating.

regions of the wafer produced widely different electrochemical output. Also, the CVD tool could not sustain a temperature for a long duration leading to loss or development of irreparable cracks in the thermal plate.

However, the spin coating process has the potential to provide a reliable wafer yield, provided either the characteristics of the solution are optimized, or a novel solution is used to enhance the process plan's outcome. One solution to achieve a layer uniformity, thin layers can be coated multiple times in succession. However, this is not necessarily true. The main issue with the solution spin coating is that it misses a proper adhesive link to the substrate. This leads to loss of electrode material in every process that involves submersion of the wafer into a liquid solution. We also encountered another issue which suggested that the GO could not be coated at outer regions of the wafer. This is a substantial issue that can be mitigated only by improving the adhesion of the electrode material, in this case, GO, to the substrate surface. Also, MSC electrodes must survive the aqueous electrolyte for long cycling lifetimes. Therefore, increasing adhesion, uniformity, and coverage are critical in making the fabrication process robust.

Various sample treatments were carried out to determine surface treatment for improved carbon adhesion, including iron nanoparticle deposition, oxygen plasma etching, and adhesive coatings. These were compared by stressing the coated material and testing how well the carbon adhered. An evaporator is used to deposit the metals on SiO_2, starting with 20 nm of Al_2O_3 and 2 nm of Fe. The substrate is heated to 500 °C for 3 min to anneal the Fe into nanoparticles, creating a rougher surface. Various thicknesses of iron, annealing times and temperatures were tested to find an optimum value. The nanoparticles were then coated in 10 nm of Ti as an adhesion layer and 100 nm of Au as a current collector for the supercapacitor. To further improve adhesive properties, the

substrate is coated with HMDS; an organic chemical often used to improve the adhesion of photoresist. After roughening is performed on the surface, surface roughness is measured for each sample using the Bruker Dimension 3100 SPM. R_a, arithmetic mean deviation, is used to characterize the material's surface roughness. Each sample is measured in multiple locations, avoiding visible scratches or debris, and the values were averaged. A detailed analysis of the approach is provided in Paper 2 and Paper 3.

Figure 3.9 shoes the schematic of the surface optimization processes and the percentage (%) coverage on a 2" Si wafer with different surfaces based on the technique used. It is clear from the graph in Figure 3.9(b) that the control surface, which is bare SiO_2 grown on Si, has the worst % coverage. This is also evident in Figure 3.9(c) where the surface is smooth, and there is nearly no coverage on one of the outer regions of the wafer. The highest percentage of coverage is with a layer of Fe nanoparticles, followed by NP+Au surface. This is one of the initial evidence of the retention of surface roughness after the current collector deposition on the nanoparticle surface. Further evidence is provided in Papers 2 and 3, which show AFM micrographs of the surface before and after the lift-off process of Au/Ti. The second wafer in Figure 3.9(c) shows the GO coverage on the wafer after the nanoparticle evaporation, which correlates to the coverage in Figure 3.9(b).

The strength of adhesion can be qualitatively evaluated by measuring the change in carbon coverage before and after sonication. The samples were weighed before coating, after coating and after sonication at 50% power and 35 kHz. This allowed for calculation the amount of GO deposited and retained after stress to determine the sample with the most substantial adhesion. Evidence of the improved adhesion provided by the nanoparticle roughness is provided in Paper 2 where results from the sonication experiments are presented.

3.6.1 Surface enhancement study

In this section, we shall describe the results for improved coverage and uniformity after the surface optimization through the layering of Fe nanoparticles.

Figure 3.10(a) shows the difference in thickness between the two spin coating processes, standard, i.e., without the adhesive nanoparticle layer, and surface-enhanced, i.e., the wafer with a 4 nm Fe layer annealed at 600 °C for 3 min. As it can be seen in the graph, the surface-enhanced wafer has a significant improvement across the entire wafer ranging from 20 % at the leftmost end of the wafer to even more than 100 % at the mid regions of the wafer. A deeper study of this improvement is presented in Paper 3, where we demonstrate a 78 % average improvement in the thickness of the electrodes on the surface-enhanced wafer. Figure 3.10(b) shows the distribution of average height of the GO material across a 1 mm range. The mean and standard deviation of the curves is also calculated by projecting the histogram data through numerical analysis. The curve is similar to a Gaussian distribution where the mean is the average height of all the samples, while the standard deviation is the average divergence of the thickness from the mean. As the starting point of the surface profiling probe is assumed to be at the same height as the endpoint, the mean value of the Gaussian distribution holds no bearing on the result. However, the standard distribution (σ) attribute of the curve can

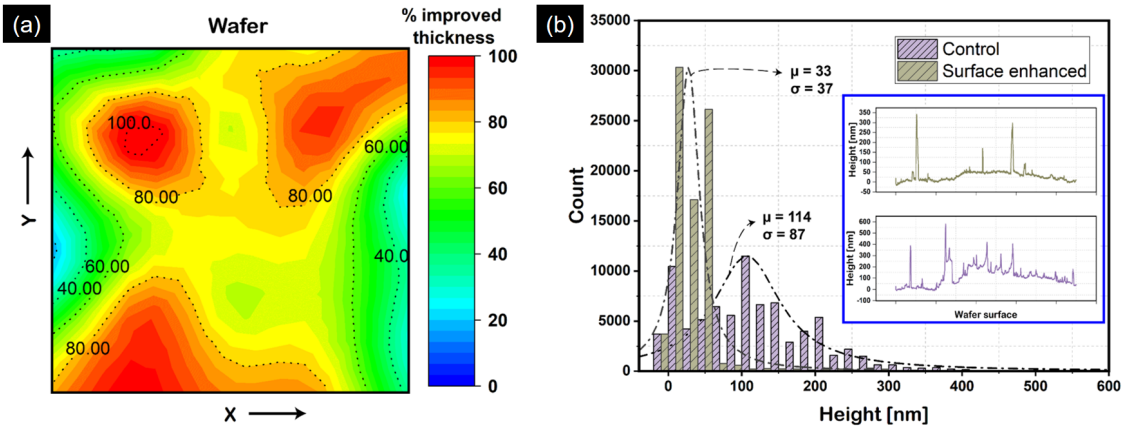

Figure 3.10: (a) Graphical contour representation of the measured thicknesses of the electrodes fabricated on the C- and SE-MSCs on a 2 × 2 inch substrate. (b) Histogram of the thickness distribution over the two substrates. (Inset) A representative 1 mm length evaluation of the surfaces with a Dektak Profiler.

suggest to us the average deviation of height across 1 mm substrate. The σ = 87 nm for the standard while it is σ = 37 nm for the surface-enhanced wafer. 37 nm is the smallest resolution in any fabrication process occurring above the electrode layer. Moreover, it leads to improved uniformity of heights across the wafer regions. This leads to a uniform yield in working devices and can further give way for increased synchronization in the performance characteristics. More information about these measurements and subsequent electrochemical characterization and comparison is provided in the Paper 3.

Chapter 4

On-chip integration

In this concluding chapter, we shall discuss the feasibility of our fabricated designs (VEH and MSC) in demonstrating an on-chip power supply that can power a sensor node. We shall also discuss the performance of the fabricated devices if they are integrated with a rectifier circuit. Then, we will examine the fabrication and packaging methods that can be utilized to devise the on-chip power supply.

4.1 Circuit design

The VEH and MSC are connected through a power management unit (PMU) which acts as a rectifier and a voltage regulator for the output from the VEH. The main task of a PMU in a WSN is to provide with sufficient power to function during its time of operation. The power requirement for any application varies according to its nature, for example, a sensor architecture may require only 1 μW for functioning, whereas a sensor in a phone requires up to 1 W power. For the sake of discussion, we have restricted our parameters to powering up to 100 μW WSNs. These power requirements for different devices have been obtained from Vullers et al. [108].

Figure 4.1 shows a schematic representation of different circuit components of an on-chip power supply. The energy harvester, as discussed in chapter 2 can be considered as an MKS system which can be further analogized to an LCR circuit (Figure 4.1(1)), where m is the mass of the cantilevers that acts as an inductor, k is the stiffness matrix, and $1/k$ is the capacitors and β is the ratio of the mechanical to electrical power conversion, also called the power efficiency of the energy harvesting system. C_p is the piezoelectric capacitance and R_p is the resistance in the material. Figure 4.1(3) shows the supercapacitor equivalent circuit derived from Gamry Echem analyst [109].

The output of the energy harvester is an AC waveform that needs conversion to DC through a rectifying circuit and a voltage regulator, as shown in Figure 4.1(2). For the power management unit (PMU) of the power supply, we require microwatt level energy harvesting systems for VEH. The primary design considerations for the IC involve having a low threshold voltage, a high power efficiency across a range of voltage outputs, good conductivity, and a high drain-source breakdown voltage. Additionally, regulation of voltage, smoothing of output, and level shifting of the output voltage is required for a robust architecture. There have been several solutions conducted in

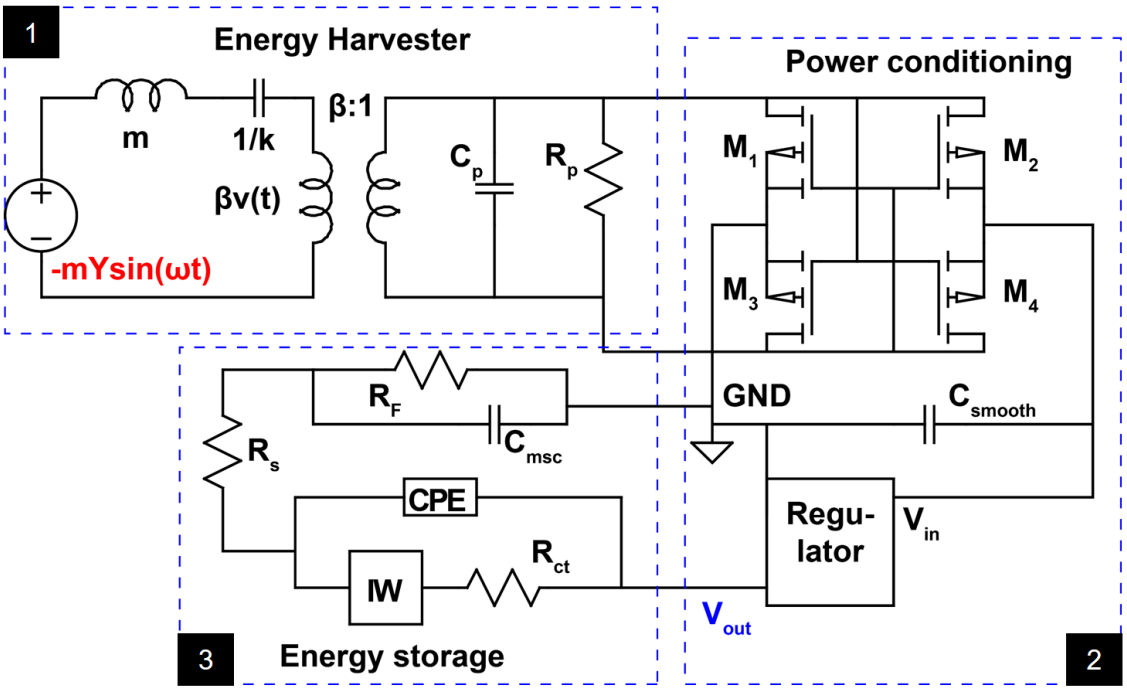

Figure 4.1: Schematic circuit diagram of the on-chip power supply including the energy harvester, power conditioning and energy storage elements.

the literature regarding these special power requirements. One of the methods is a boot-strapping technique [17]. However, it is quite complicated. Another technique for the requirements is to handle these wide ranges of outputs through separate pathways. Ramadas et al. designed an efficient harvesting interface circuit which is improved by several designs [110] by demonstrating either ultra-low-power self-oscillating switched capacitors or capacitive power management units for self-supplied PMUs.

More recently, work by Neilson et al. [110] demonstrated an extremely robust PMU that can take input voltages from 0.45 - 5 V while providing an 8 μW power at 24 Hz even in failsafe conditions. Figure 4.1(2) is a general representation of the circuit demonstrated in their article. Their system consists of two rectifiers (M_{1-4}) that act as negative voltage converters followed by active diodes and a voltage regulator. The rectifier circuit is a combination of four pMOS transistors that can be fabricated in 0.18 μm technology. Using transistors in place of p-n junction diodes has several advantages due to the presence of extremely low resistance in the transistors leading a lower power loss. The output of the rectifiers is converted to DC by a smoothing capacitor C_{smooth} which is then connected to a voltage regulator and the supercapacitor, both in parallel to each other. The regulator has three switched-capacitor DC-DC converters to either step up or step down the input voltage from the harvester. The output voltage can charge the supercapacitor and the load at the same time if needed. Once the supercapacitor is fully charged, it can start supplying power to the load sensor architecture in the absence of vibrations in the surrounding. The PMU post-fabrication is a 3 mm^2 die which can be bonded in a variety of fashions to the VEH and MSC dies.

Now, coming to the feasibility of integration of VEHs and MSCs with the PMU designed by Neilson et al. [110], we see that their input requirements are as low as 0.45 V

up to 5 V. So, according to this constraint, our energy harvester must supply at least this voltage to the PMU. According to simulations performed in COMSOL, currently, M-big has the highest potential to be integrated with the PMU. The simulation model suggests that between the working frequencies of 400 - 500 Hz, the M-big can supply up to 8 V easily, even in extreme damping conditions. Similarly, on checking the performance of the MSCs fabricated in chapter 3, we see that the volumetric capacitance of the 20F-40 MSC is 1.1 F cm^{-3}, which directly translates to 1.5 mF capacitance if we have a 10 μm thick electrode film. As of now, the thickness of the rGO films is approximately 1.1 μm. However, we are confident that with more spin-coating cycles, 10 μm thick films can be achieved. In terms of power density, it demonstrates a value of 100.5 μW cm^{-2} at 1 V. This amount of power matches with our initial constraint of over 100 μW for WSNs. Therefore, it is, in principle, possible to use our micro-energy harvesters discussed in chapter 2 with our MSCs fabricated in chapter 3 with the PMU discussed. In the next section, we shall describe the different packaging mechanisms that are used in current CMOS processing technology which can be used to package our devices.

4.2 Integration possibilities

The final step in the integration of VEH and MSC devices with an IC for an on-chip power supply revolves around either fabrication of these devices in an integrated fabrication process for all the three devices or processing them separately and integrating them in the final step. The former form of integration is called front-end-of-line (FEOL). FEOL covers the main fabrication processes required for MEMS and CMOS processing, which we have previously discussed on numerous occasions. The second method is called back-end-of-line (BEOL). BEOL process mainly deals with metallization of contacts and fabrication of connections to the metal layer in CMOS processing. It also includes processing of dielectrics and bonding sites for a chip-to-package interface. After BEOL, there is a back-end-process that includes wafer back-grinding, die separation, packaging of IC, and failure tests [111]. Figure 4.2 shows their schematic representation.

FEOL integration of these devices is possible with an integrated VEH-PMU-MSC

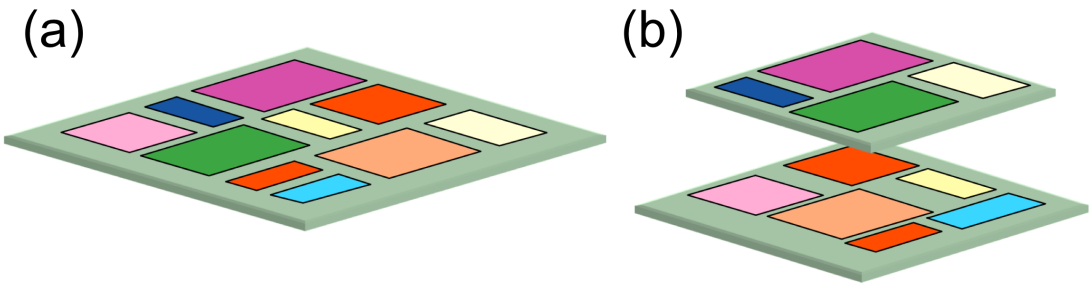

Figure 4.2: Schematic representation of (a) FEOL, (b) BEOL processes. [111]. The colored fields represent the generic areal space that MEMS or CMOS fabricated devices can take up in an on-chip platform. Images are reproduced after permission from the author.

process plan. These processes can be intertwined with each other through parallel processing during conventional techniques such as photolithography, evaporation, and etching. For such a process, these devices should be fabricated with the same materials too. As discussed previously in chapters 2 and 3, the VEH and MSC fabrication processes are CMOS compatible. However, there are material differences between the devices. For instance, the VEH current collectors are made of Pt/Ti while the MSC has Au/Ti. This can be easily mitigated in the next processing of MSC devices. Another way of fabrication can be compartmentalization of device processes and then protecting the fabricated devices through a layer of thick photoresist during the manufacturing of the other component. The IC fabrication can take place first, followed by MSC fabrication and VEH fabrication until electrode formation. The IC and MSC can then be protected through AZ4562 spin-coated on the surface during the lithography process for the top-side Si etch. The same resist layer can protect the devices during the entire back-side etching process. Finally, when the cantilevers are released, the photoresist can be washed off in the final cleaning step. The substrate on which these devices are fabricated would be diced in the back-end process and packaged for further analysis.

The main issue with FEOL is the additional 2D area that the process requires. The VEH has a surface area of 10 mm^2; IC has 3 mm^2; MSC has an area of 1 cm^2. So, overall the total surface area can be up to more than 1.5 cm^2. In comparison, BEOL processing can allow for a 3D integration of these devices in stacks. This reduces our overall device surface area to the device with the maximum area, which is the MSC. Alongside side reduction, with 3D packaging the interconnect bottleneck for long distances can be mitigated. Therefore, we can reduce the power consumption of the devices. Finally, it would allow for seamless integration of different microelectronic technologies at a wafer level. Therefore, the best way forward for on-chip integration would be through 3D packaging of different device dies.

Figure 4.3 shows an illustration of a possible integration scheme for the current VEH and MSC devices with a PMU. For a PMU, the IC designed in [110] has been chosen. The main task for a MEMS packaging process is to protect the device from dust, particles, and dicing process. It should also be chemical resistant, with an excellent thermal interface while having minimal impact on the MEMS characteristics, such as damping in case of

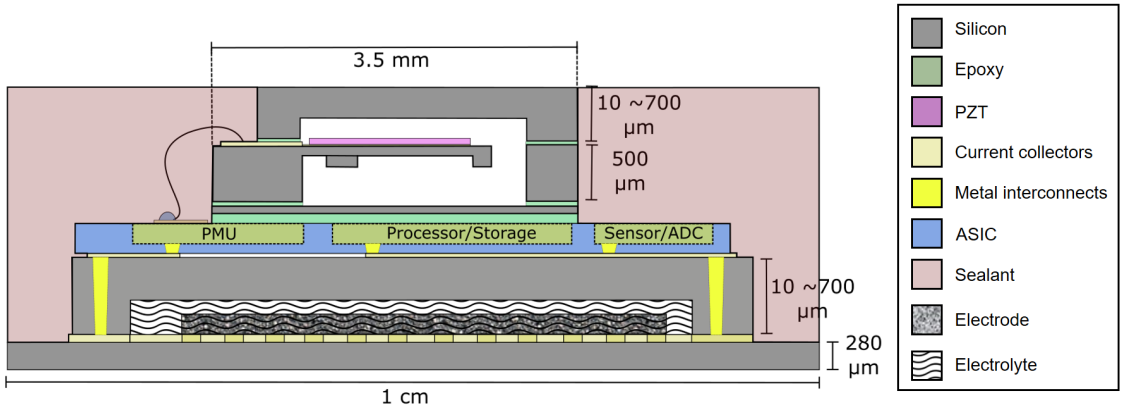

Figure 4.3: Illustration of a 3D package on-chip power supply with WSN architechture.

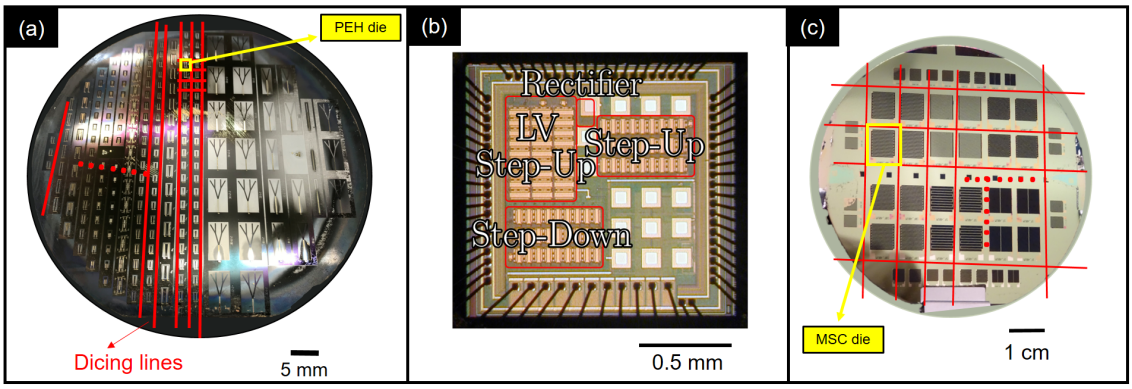

Figure 4.4: Optical images of the fabricated (a) VEH (b) PMU [110], and (c) MSC. The red lines are the dicing marks set up during lithography. The yellow VEH and MSC dies can be used for subsequent integration in a BEOL format.

VEH. Packaging of these devices require the following primary operations, packaging of VEH, MSC, and their integration with the IC through 3D interconnect technology. Packaging of VEH and MSC devices can be performed with the same process.

The wafer shown in Figure 4.4(a) is the final step in the VEH fabrication process. Once we dice this wafer, individual VEH devices can be procured, which would result in 10 mm^2 in size. These devices can be packaged in glass wafer caps on each side. The fabrication of glass wafers will be a separate process plan that will involve selective etching of the glass surface to allow for the complete harvester displacement at its natural frequency. The fabrication process has been described by Elfrink et al. in further detail. Mainly, the glass cap to be placed on top of the VEH are fabricated, and SU-8 epoxy layer is coated through a rolling-coating process. The glass cap is then mounted on the VEH, and the SU-8 is cured at a specific temperature. The bottom side of the harvester is sealed through the same epoxy and substrate. However, in this case, the glass wafer with a smooth surface is bonded to the back-side of the VEH. The wafer is then polished from its back to reduce the final device's thickness. These caps can be 10 to 700 μm thick depending on the robustness required.

The MSC wafer is shown in Figure 4.4(c), which is a post-fabrication optical image of the wafer. This wafer can also be diced along the dicing lines. There are, however, some steps still necessary for the integration of MSCs into an on-chip power supply. Firstly, the current collectors used for MSCs need to be changed to either a combination of Pt/Ti or Mo/Al. Au is CMOS processes has been prone to diffusion into the substrate layers during high-temperature annealing processes. Secondly, there are issues with using aqueous electrolytes. Use of liquids is hugely restricted in MEMS or CMOS facilities. Also, once the MSCs are packaged without electrolyte, there is no way to introduce them in the system. Therefore, it can be concluded that we require photopatternable electrolytes for MSC integration. These electrolytes can be spin-coated on the substrate and then solidified during the exposure just as a photoresist. They can then be subsequently removed in the unwanted areas, leaving us isolated MSC devices. However, more work needs to be performed on this aspect of the integration problem. Nonetheless, with improving technology, it is expected that we get some solutions in works such as Choi et al. [112]. Once we have solved the electrolyte issue, the packaging of MSCs would follow

a similar process as VEH packaging. In this process, we would be required to make 3D interconnects in the capping wafer. The standard approach for making 3D interconnects starts with etching a hole in Si wafer through RIE-ICP, followed by dielectric isolation of the walls, and finally metallization of the Si-holes by a CMOS compatible metal such as W.

The bonding of the wafer cap to the devices takes place on the first step of IC packaging, also called zero-level. The recessed capping chip or die is mounted on the MEMS device through a sealant ring which is typically 50 - 300 μm in width. The cap itself has a die thickness from 100 up to 700 μm. The mounting process is performed either die-to-wafer (D2W) or wafer-to-wafer (W2W) [111]. In the D2W process, the capping wafer and MEMS device wafer are diced separately, and then the cap is bonded onto or under the device. In W2W bonding, the capping wafer is first placed in link to the MEMS wafer and then bonded. The dicing is the final step in the process. The cap can also be fabricated through thin-film MEMS, but in case of our devices, this process is fundamentally not feasible. The bonding material can be solder bumps, Au/Au thermocompression, epoxy seals, or polymer adhesives. Using bonding material such as benzocyclobutane (BCB) which has a low curing temperature of < 300 °C is most suitable for a CMOS compatible process. So, as shown in Figure 4.3, the packaged VEH can be connected to the IC chip through 3D stack pins. The IC chip that can contain PMU and WSN architecture is connected to the MSC package through 3D metal interconnects. The final resulting package can be sealed with a sealant such as [113]. This configuration is also equivalent to the circuit discussed in 4.1. The energy harvester would be connected to the source of vibrations from which it will derive electrical energy and send it as an output to the IC through the wire bond. The PMU in the IC will then start charging the MSC through the metal interconnect attached to the each through conductive solder bumps. The MSC will then power the WSN architecture components such as the processor or the sensor through another set of interconnects.

Chapter 5

Conclusion

As microsystems shrink to form complex IoT networks, their power demands cannot be met entirely through conventional batteries that have a short life span. Having a miniaturized power supply that recharges itself based on the energy present in the surroundings will give the future IoT access to several relevant and challenging locations—inside engines, structures, and even drilling areas. Miniaturization of devices is essential for the design and fabrication for IoT applications. Micro-machining fabrication techniques have been used in manufacturing CMOS devices, sensors, actuators, and also energy harvesters at a large scale. Similarly, for energy storage, MSCs are miniaturized energy storage devices that can be combined in an on-chip platform as a component of a power supply for IoT's sensors. Integration of these on-chip devices requires them to be fabricated through CMOS compatible fabrication techniques.

An M-shaped 2DOF micro-cantilever for energy harvesting was designed based on the principle of reducing the gaps between the first two natural frequencies to achieve a broad bandwidth and improved stress distribution. The design was fabricated using micromachining techniques and was examined for dimensional and mechanical characteristics. The dimensional analysis showed the feasibility of the fabrication process. The mechanical evaluation further demonstrated that the device behavior is close to the intended simulation design. Also, the fabricated M-shape micro-cantilever design shows harvesting capabilities in beam vibrations which can be associated with the coupling mechanism in a single structure.

MSC fabrication for CMOS compatible process requires a feasible and facile technique that is pre-existing in IC industries. We have demonstrated the use of the spin-coating method as a method that is utilizable in CMOS compatible MSC fabrication. Use of spin-coating of carbon materials can further be optimized by improving the surface adhesion of the substrate through the fabrication of Fe nanoparticle through evaporation and annealing. The enhanced surface roughness results in 78 % improved thickness, 21 % increased mass retention and a 57 % uniformity enhancement of the electrode material coverage in a Si substrate.

These fabricated devices can be furthermore, integrated with an on-chip PMU and other application-specific ICs to realize an integrated power supply. For such realization, there is still substantial work that needs to performed. The future work on this project will include:

- Fabrication of a second version of VEHs based on the optimizations in the current plan.
- VEH electrical characterization and comparison with the simulated designs.
- MSC fabrication from different spin coated electrodes to improve their capacitive storage and energy density.
- VEH and MSC integration with PMU through
  - FEOL or
  - BEOL integration
- Analysis of the on-chip power supply in in-vivo environment.

Bibliography

[1] Kevin Ashton et al. “That ‘internet of things’ thing”. In: *RFID journal* 22.7 (2009), pp. 97–114 (cit. on p. 1).

[2] Jayavardhana Gubbi, Rajkumar Buyya, Slaven Marusic, and Marimuthu Palaniswami. “Internet of Things (IoT): A vision, architectural elements, and future directions”. In: *Future generation computer systems* 29.7 (2013), pp. 1645–1660 (cit. on p. 1).

[3] Jingzhu Zhao, Xiancao Zheng, Rencai Dong, and Guofan Shao. “The planning, construction, and management toward sustainable cities in China needs the Environmental Internet of Things”. In: *International Journal of Sustainable Development & World Ecology* 20.3 (2013), pp. 195–198 (cit. on p. 1).

[4] Chih-Ming Ho, Steve Tung, Gwo-Bin Lee, Yu-Chong Tai, Fukang Jiang, Thoma Tsao, Chih-Ming Ho, Steve Tung, Gwo-Bin Lee, Yu-Chong Tai, et al. “MEMS-A technology for advancements in aerospace engineering”. In: *35th Aerospace Sciences Meeting and Exhibit*. 1997, p. 545 (cit. on p. 1).

[5] John D Olivas and Stephen Bolin. “Advancements in MEMS materials and processing technology”. In: *JOM* 50.1 (1998), pp. 38–43 (cit. on p. 1).

[6] R Aigner, J Ella, H-J Timme, L Elbrecht, W Nessler, and S Marksteiner. “Advancement of MEMS into RF-filter applications”. In: *Digest. International Electron Devices Meeting,* IEEE. 2002, pp. 897–900 (cit. on p. 1).

[7] Gastone Ciuti, Leonardo Ricotti, Arianna Menciassi, and Paolo Dario. “MEMS sensor technologies for human centred applications in healthcare, physical activities, safety and environmental sensing: a review on research activities in Italy”. In: *Sensors* 15.3 (2015), pp. 6441–6468 (cit. on p. 1).

[8] Ian F Akyildiz, Weilian Su, Yogesh Sankarasubramaniam, and Erdal Cayirci. “Wireless sensor networks: a survey”. In: *Computer networks* 38.4 (2002), pp. 393–422 (cit. on pp. 1, 2).

[9] Chalermek Intanagonwiwat, Ramesh Govindan, and Deborah Estrin. “Directed diffusion: A scalable and robust communication paradigm for sensor networks”. In: *Proceedings of the 6th annual international conference on Mobile computing and networking*. ACM. 2000, pp. 56–67 (cit. on p. 2).

[10] Guannan Liu, Yanjun Yu, Jing Hou, Wei Xue, Xinhui Liu, Yanzhen Liu, Wanhua Wang, Ahmed Alsaedi, Tasawar Hayat, and Zhengtao Liu. "An ecological risk assessment of heavy metal pollution of the agricultural ecosystem near a lead-acid battery factory". In: *Ecological indicators* 47 (2014), pp. 210–218 (cit. on p. 2).

[11] Judith Rees. *Natural resources: allocation, economics and policy*. Routledge, 2017 (cit. on p. 2).

[12] Perrine Ribière, Sylvie Grugeon, Mathieu Morcrette, Simeon Boyanov, Stéphane Laruelle, and Guy Marlair. "Investigation on the fire-induced hazards of Li-ion battery cells by fire calorimetry". In: *Energy & Environmental Science* 5.1 (2012), pp. 5271–5280 (cit. on p. 2).

[13] Faisal Karim Shaikh and Sherali Zeadally. "Energy harvesting in wireless sensor networks: A comprehensive review". In: *Renewable and Sustainable Energy Reviews* 55 (2016), pp. 1041–1054 (cit. on p. 3).

[14] Haisheng Chen, Thang Ngoc Cong, Wei Yang, Chunqing Tan, Yongliang Li, and Yulong Ding. "Progress in electrical energy storage system: A critical review". In: *Progress in natural science* 19.3 (2009), pp. 291–312 (cit. on p. 3).

[15] S P Beeby, M J Tudor, and NM White. "Energy harvesting vibration sources for microsystems applications". In: *Measurement science and technology* 17.12 (2006), R175 (cit. on p. 3).

[16] Shashank Priya and Daniel J Inman. *Energy harvesting technologies*. Vol. 21. Springer, 2009 (cit. on p. 3).

[17] Gyorgy D Szarka, Bernard H Stark, and Stephen G Burrow. "Review of power conditioning for kinetic energy harvesting systems". In: *IEEE transactions on power electronics* 27.2 (2012), pp. 803–815 (cit. on pp. 3, 42).

[18] Nandakishore Kushalnagar and Gabriel Montenegro. "Transmission of IPv6 packets over IEEE 802.15. 4 networks". In: (2007) (cit. on p. 3).

[19] Usman Sarwar, Gopinath Sinniah Rao, Zeldi Suryady, and Reza Khoshdelniat. "A comparative study on available IPv6 platforms for wireless sensor network". In: *World Academy of Science, Engineering and Technology* 62 (2010), pp. 889–892 (cit. on p. 3).

[20] Oliver Brand, Gary K Fedder, Christofer Hierold, Jan G Korvink, and Osamu Tabata. *Micro energy harvesting*. John Wiley & Sons, 2015 (cit. on p. 3).

[21] MA Fetcenko, SR Ovshinsky, B Reichman, K Young, C Fierro, J Koch, A Zallen, W Mays, and T Ouchi. "Recent advances in NiMH battery technology". In: *Journal of Power Sources* 165.2 (2007), pp. 544–551 (cit. on p. 4).

[22] Naoki Nitta, Feixiang Wu, Jung Tae Lee, and Gleb Yushin. "Li-ion battery materials: present and future". In: *Materials today* 18.5 (2015), pp. 252–264 (cit. on p. 4).

[23] D Aurbach, E Zinigrad, H Teller, and P Dan. “Factors which limit the cycle life of rechargeable lithium (metal) batteries”. In: *Journal of The Electrochemical Society* 147.4 (2000), pp. 1274–1279 (cit. on p. 4).

[24] LGH Staaf, Per Lundgren, and Peter Enoksson. “Present and future supercapacitor carbon electrode materials for improved energy storage used in intelligent wireless sensor systems”. In: *Nano Energy* 9 (2014), pp. 128–141 (cit. on p. 4).

[25] SM Sze. “surface Micromachining”. In: *Semiconductor Sensors* (1994), pp. 58–63 (cit. on p. 4).

[26] A Vyas, Q Li, F Cornaglia, K Wang, A Anderson, M Haque, V Kuzmenko, AD Smith, P Lundgren, and P Enoksson. “Surface Roughening with Iron Nanoparticles for Promoted Adhesion of Spin Coated Microsupercapacitor Electrodes”. In: *MRS Advances* 4.23 (2019), pp. 1335–1340 (cit. on pp. 5, 24).

[27] AD Smith, Q Li, A Anderson, A Vyas, V Kuzmenko, M Haque, LGH Staaf, P Lundgren, and P Enoksson. “Toward CMOS compatible wafer-scale fabrication of carbon-based microsupercapacitors for IoT”. In: *Journal of Physics: Conference Series*. Vol. 1052. 1. IOP Publishing. 2018, p. 012143 (cit. on pp. 5, 24, 34).

[28] Majid Beidaghi, Zhifeng Wang, Lin Gu, and Chunlei Wang. “Electrostatic spray deposition of graphene nanoplatelets for high-power thin-film supercapacitor electrodes”. In: *Journal of Solid State Electrochemistry* 16.10 (2012), pp. 3341–3348 (cit. on pp. 5, 24).

[29] Cheolho Kim, Da-Young Kang, and Jun Hyuk Moon. “Full lithographic fabrication of boron-doped 3D porous carbon patterns for high volumetric energy density microsupercapacitors”. In: *Nano Energy* 53 (2018), pp. 182–188 (cit. on pp. 5, 24, 28).

[30] Jiantong Li, Szymon Sollami Delekta, Panpan Zhang, Sheng Yang, Martin R Lohe, Xiaodong Zhuang, Xinliang Feng, and Mikael Östling. “Scalable fabrication and integration of graphene microsupercapacitors through full inkjet printing”. In: *ACS nano* 11.8 (2017), pp. 8249–8256 (cit. on pp. 5, 24, 27).

[31] Shuaikai Xu, Yohan Dall’Agnese, Guodong Wei, Chao Zhang, Yury Gogotsi, and Wei Han. “Screen-printable microscale hybrid device based on MXene and layered double hydroxide electrodes for powering force sensors”. In: *Nano energy* 50 (2018), pp. 479–488 (cit. on p. 5).

[32] Chunsheng Du and Ning Pan. “High power density supercapacitor electrodes of carbon nanotube films by electrophoretic deposition”. In: *Nanotechnology* 17.21 (2006), p. 5314 (cit. on p. 5).

[33] Zhaoyang Liu, Zhong-Shuai Wu, Sheng Yang, Renhao Dong, Xinliang Feng, and Klaus Müllen. “Ultraflexible in-plane micro-supercapacitors by direct printing of solution-processable electrochemically exfoliated graphene”. In: *Advanced Materials* 28.11 (2016), pp. 2217–2222 (cit. on p. 5).

[34] Maher F El-Kady, Melanie Ihns, Mengping Li, Jee Youn Hwang, Mir F Mousavi, Lindsay Chaney, Andrew T Lech, and Richard B Kaner. "Engineering three-dimensional hybrid supercapacitors and microsupercapacitors for high-performance integrated energy storage". In: *Proceedings of the National Academy of Sciences* 112.14 (2015), pp. 4233–4238 (cit. on p. 5).

[35] An Cao, Wai Chan, and Jill Card. *Systems and method for lights-out manufacturing*. US Patent App. 11/199,815. Feb. 2006 (cit. on p. 6).

[36] Agin Vyas, Henrik Staaf, Cristina Rusu, Thorbjörn Ebefors, Jessica Liljeholm, Anderson Smith, Per Lundgren, and Peter Enoksson. "A Micromachined Coupled-Cantilever for Piezoelectric Energy Harvesters". In: *Micromachines* 9.5 (2018), p. 252 (cit. on pp. 7, 12).

[37] Arthur Ballato. "Piezoelectricity: history and new thrusts". In: *1996 IEEE Ultrasonics Symposium. Proceedings*. Vol. 1. IEEE. 1996, pp. 575–583 (cit. on p. 7).

[38] Samuel C Stanton, Clark C McGehee, and Brian P Mann. "Nonlinear dynamics for broadband energy harvesting: Investigation of a bistable piezoelectric inertial generator". In: *Physica D: Nonlinear Phenomena* 239.10 (2010), pp. 640–653 (cit. on p. 9).

[39] Hao Wu, Lihua Tang, Yaowen Yang, and Chee Kiong Soh. "Development of a broadband nonlinear two-degree-of-freedom piezoelectric energy harvester". In: *Journal of Intelligent Material Systems and Structures* 25.14 (2014), pp. 1875–1889 (cit. on pp. 9, 12).

[40] Alper Erturk and Daniel J Inman. "An experimentally validated bimorph cantilever model for piezoelectric energy harvesting from base excitations". In: *Smart materials and structures* 18.2 (2009), p. 025009 (cit. on pp. 9, 12).

[41] Lars-Cyril Julin Blystad and Einar Halvorsen. "A piezoelectric energy harvester with a mechanical end stop on one side". In: *Microsystem technologies* 17.4 (2011), pp. 505–511 (cit. on pp. 10, 11).

[42] Huicong Liu, Chengkuo Lee, Takeshi Kobayashi, Cho Jui Tay, and Chenggen Quan. "Investigation of a MEMS piezoelectric energy harvester system with a frequency-widened-bandwidth mechanism introduced by mechanical stoppers". In: *Smart Materials and Structures* 21.3 (2012), p. 035005 (cit. on pp. 10–12).

[43] MSM Soliman, EM Abdel-Rahman, EF El-Saadany, and RR Mansour. "A wideband vibration-based energy harvester". In: *Journal of Micromechanics and Microengineering* 18.11 (2008), p. 115021 (cit. on p. 10).

[44] SM Shahruz. "Design of mechanical band-pass filters with large frequency bands for energy scavenging". In: *Mechatronics* 16.9 (2006), pp. 523–531 (cit. on p. 10).

[45] Marco Ferrari, Vittorio Ferrari, Michele Guizzetti, Daniele Marioli, and Andrea Taroni. "Piezoelectric multifrequency energy converter for power harvesting in autonomous microsystems". In: *Sensors and Actuators A: Physical* 142.1 (2008), pp. 329–335 (cit. on pp. 10, 12).

[46] Huan Xue, Yuantai Hu, and Qing-Ming Wang. “Broadband piezoelectric energy harvesting devices using multiple bimorphs with different operating frequencies”. In: *IEEE transactions on ultrasonics, ferroelectrics, and frequency control* 55.9 (2008) (cit. on pp. 10, 11).

[47] Jing-Quan Liu, Hua-Bin Fang, Zheng-Yi Xu, Xin-Hui Mao, Xiu-Cheng Shen, Di Chen, Hang Liao, and Bing-Chu Cai. “A MEMS-based piezoelectric power generator array for vibration energy harvesting”. In: *Microelectronics Journal* 39.5 (2008), pp. 802–806 (cit. on pp. 10, 12).

[48] Shaofan Qi, Roger Shuttleworth, S Olutunde Oyadiji, and Jan Wright. “Design of a multiresonant beam for broadband piezoelectric energy harvesting”. In: *Smart Materials and Structures* 19.9 (2010), p. 094009 (cit. on pp. 10, 12).

[49] Shad Roundy, Eli S Leland, Jessy Baker, Eric Carleton, Elizabeth Reilly, Elaine Lai, Brian Otis, Jan M Rabaey, Paul K Wright, and V Sundararajan. “Improving power output for vibration-based energy scavengers”. In: *IEEE Pervasive computing* 4.1 (2005), pp. 28–36 (cit. on p. 10).

[50] Qing Ou, XiaoQi Chen, Stefanie Gutschmidt, Alan Wood, and Nigel Leigh. “A two-mass cantilever beam model for vibration energy harvesting applications”. In: *Automation Science and Engineering (CASE), 2010 IEEE Conference on*. IEEE. 2010, pp. 301–306 (cit. on pp. 10, 12).

[51] O Aldraihem and A Baz. “Energy harvester with a dynamic magnifier”. In: *Journal of Intelligent Material Systems and Structures* 22.6 (2011), pp. 521–530 (cit. on p. 10).

[52] M Arafa, W Akl, A Aladwani, O Aldraihem, and A Baz. “Experimental implementation of a cantilevered piezoelectric energy harvester with a dynamic magnifier”. In: *Active and Passive Smart Structures and Integrated Systems 2011*. Vol. 7977. International Society for Optics and Photonics. 2011, 79770Q (cit. on pp. 10, 12).

[53] Alper Erturk, Jamil M Renno, and Daniel J Inman. “Modeling of piezoelectric energy harvesting from an L-shaped beam-mass structure with an application to UAVs”. In: *Journal of intelligent material systems and structures* 20.5 (2009), pp. 529–544 (cit. on p. 10).

[54] Jia Wen Xu, Wei Wei Shao, Fan Rang Kong, and Zhi Hua Feng. “Right-angle piezoelectric cantilever with improved energy harvesting efficiency”. In: *Applied Physics Letters* 96.15 (2010), p. 152904 (cit. on pp. 10, 12).

[55] S-J Jang, E Rustighi, MJ Brennan, YP Lee, and H-J Jung. “Design of a 2DOF vibrational energy harvesting device”. In: *Journal of Intelligent Material Systems and Structures* 22.5 (2011), pp. 443–448 (cit. on p. 10).

[56] In-Ho Kim, Hyung-Jo Jung, Bo Mi Lee, and Seon-Jun Jang. “Broadband energy-harvesting using a two degree-of-freedom vibrating body”. In: *Applied Physics Letters* 98.21 (2011), p. 214102 (cit. on pp. 10, 12).

[57] Hao Wu, Lihua Tang, Yaowen Yang, and Chee Kiong Soh. “A novel two-degrees-of-freedom piezoelectric energy harvester”. In: *Journal of Intelligent Material Systems and Structures* 24.3 (2013), pp. 357–368 (cit. on p. 10).

[58] LGH Staaf, E Köhler, D Parthasarathy, P Lundgren, and P Enoksson. “Modelling and experimental verification of more efficient power harvesting by coupled piezoelectric cantilevers”. In: *Journal of Physics: Conference Series*. Vol. 557. 1. IOP Publishing. 2014, p. 012098 (cit. on p. 10).

[59] LGH Staaf, E Köhler, M Soeiro, P Lundgren, and P Enoksson. “Smart design selftuning piezoelectric energy harvester intended for gas turbines”. In: *Journal of Physics: Conference Series*. Vol. 660. 1. IOP Publishing. 2015, p. 012125 (cit. on pp. 10, 12).

[60] Skandar Basrour and Benoît Charlot. “Design and fabrication of piezoelectric micro power generators for autonomous microsystems”. In: *Ieee Dtip* June (2005), pp. 1–3 (cit. on p. 10).

[61] “No Title”. In: (2007), pp. 887–890 (cit. on p. 11).

[62] Y. B. Jeon, R. Sood, J. H. Jeong, and S. G. Kim. “MEMS power generator with transverse mode thin film PZT”. In: *Sensors and Actuators, A: Physical* 122.1 SPEC. ISS. (2005), pp. 16–22. ISSN: 09244247. DOI: 10.1016/j.sna.2004.12.032 (cit. on p. 11).

[63] W. J. Choi, Y. Jeon, J. H. Jeong, R. Sood, and S. G. Kim. “Energy harvesting MEMS device based on thin film piezoelectric cantilevers”. In: *Journal of Electroceramics* 17.2-4 (2006), pp. 543–548. ISSN: 13853449. DOI: 10.1007/s10832-006-6287-3 (cit. on pp. 11, 12).

[64] Hua-Bin Fang, Jing-Quan Liu, Zheng-Yi Xu, Lu Dong, Li Wang, Di Chen, Bing-Chu Cai, and Yue Liu. “Fabrication and performance of MEMS-based piezoelectric power generator for vibration energy harvesting”. In: *Microelectronics Journal* 37.11 (2006), pp. 1280–1284. ISSN: 0026-2692. DOI: https://doi.org/10.1016/j.mejo.2006.07.023 (cit. on pp. 11, 12).

[65] J. C. Park, S. Khym, and J. Y. Park. “Micro-fabricated lead zirconate titanate bent cantilever energy harvester with multi-dimensional operation”. In: *Applied Physics Letters* 102.4 (2013), pp. 1–5. ISSN: 00036951. DOI: 10.1063/1.4789754 (cit. on p. 12).

[66] Hua Yu, Jielin Zhou, Licheng Deng, and Zhiyu Wen. “A vibration-based MEMS piezoelectric energy harvester and power conditioning circuit”. In: *Sensors (Switzerland)* 14.2 (2014), pp. 3323–3341. ISSN: 14248220. DOI: 10.3390/s140203323 (cit. on pp. 12, 13).

[67] J. Lueke, M. Rezaei, and W. A. Moussa. “Investigation of folded spring structures for vibration-based piezoelectric energy harvesting”. In: *Journal of Micromechanics and Microengineering* 24.12 (2014). ISSN: 13616439. DOI: 10.1088/0960-1317/24/12/125011 (cit. on p. 12).

[68] Lan Zhang, Jian Lu, Ryohei Takei, Natsumi Makimoto, Toshihiro Itoh, and Takeshi Kobayashi. “S-shape spring sensor: Sensing specific low-frequency vibration by energy harvesting”. In: *Review of Scientific Instruments* 87.8 (2016). ISSN: 10897623. DOI: 10.1063/1.4960959 (cit. on p. 13).

[69] Lihua Tang and Yaowen Yang. “A multiple-degree-of-freedom piezoelectric energy harvesting model”. In: *Journal of Intelligent Material Systems and Structures* 23.14 (2012), pp. 1631–1647 (cit. on p. 14).

[70] Brian E Conway. *Electrochemical supercapacitors: scientific fundamentals and technological applications*. Springer Science & Business Media, 2013 (cit. on p. 23).

[71] H von Helmholtz. “Ueber einige Gesetze der Vertheilung elektrischer Ströme in körperlichen Leitern, mit Anwendung auf die thierisch-elektrischen Versuche (Schluss.)” In: *Annalen der Physik* 165.7 (1853), pp. 353–377 (cit. on p. 23).

[72] Adam Namisnyk and J Zhu. “A survey of electrochemical super-capacitor technology”. In: *Australian Universities Power Engineering Conference*. University of Canterbury, New Zealand. 2003 (cit. on p. 23).

[73] Otto Stern. “Zur theorie der elektrolytischen doppelschicht”. In: *Zeitschrift für Elektrochemie und angewandte physikalische Chemie* 30.21-22 (1924), pp. 508–516 (cit. on p. 23).

[74] Qi Li. “Electrochemical Capacitors for Miniaturized Self-powered Systems”. An optional note. MA thesis. Chalmers Reproservice: Chalmers University of Technology, Oct. 2018 (cit. on pp. 24, 35).

[75] Carmen M Lungoci and Ioan D Oltean. “Comparative analysis for the supercapacitors packaging characteristics”. In: *2010 IEEE 16th International Symposium for Design and Technology in Electronic Packaging (SIITME)*. IEEE. 2010, pp. 93–98 (cit. on p. 24).

[76] Lu Wang, Yuzhen Han, Xiao Feng, Junwen Zhou, Pengfei Qi, and Bo Wang. “Metal–organic frameworks for energy storage: Batteries and supercapacitors”. In: *Coordination Chemistry Reviews* 307 (2016), pp. 361–381 (cit. on p. 24).

[77] Han-Ki Kim, Sun-Hee Choi, Young Soo Yoon, Sung-Yong Chang, Young-Woo Ok, and Tae-Yeon Seong. “Characteristics of RuO2–SnO2 nanocrystalline-embedded amorphous electrode for thin film microsupercapacitors”. In: *Thin Solid Films* 475.1-2 (2005), pp. 54–57 (cit. on p. 24).

[78] Cheol-Min Yang, Yong-Jung Kim, Morinobu Endo, Hirofumi Kanoh, Masako Yudasaka, Sumio Iijima, and Katsumi Kaneko. “Nanowindow-regulated specific capacitance of supercapacitor electrodes of single-wall carbon nanohorns”. In: *Journal of the American Chemical Society* 129.1 (2007), pp. 20–21 (cit. on p. 24).

[79] Majid Beidaghi and Yury Gogotsi. “Capacitive energy storage in micro-scale devices: recent advances in design and fabrication of micro-supercapacitors”. In: *Energy & Environmental Science* 7.3 (2014), pp. 867–884 (cit. on p. 25).

[80] Qi Li, Shuangxi Sun, Anderson D Smith, Per Lundgren, Yifeng Fu, Peng Su, Tao Xu, Lilei Ye, Litao Sun, Johan Liu, et al. “Compact and low loss electrochemical capacitors using a graphite/carbon nanotube hybrid material for miniaturized systems”. In: *Journal of Power Sources* 412 (2019), pp. 374–383 (cit. on p. 25).

[81] Caiwei Shen, Sixing Xu, Yingxi Xie, Mohan Sanghadasa, Xiaohong Wang, and Liwei Lin. "A review of on-chip micro supercapacitors for integrated self-powering systems". In: *Journal of Microelectromechanical Systems* 26.5 (2017), pp. 949–965 (cit. on pp. 26, 27).

[82] Maher F El-Kady, Veronica Strong, Sergey Dubin, and Richard B Kaner. "Laser scribing of high-performance and flexible graphene-based electrochemical capacitors". In: *Science* 335.6074 (2012), pp. 1326–1330 (cit. on p. 26).

[83] Dongfang Yang and Christina Bock. "Laser reduced graphene for supercapacitor applications". In: *Journal of Power Sources* 337 (2017), pp. 73–81 (cit. on p. 26).

[84] Seung-Hwan Lee, Jin Hyeon Kim, and Jung-Rag Yoon. "Laser scribed graphene cathode for next generation of high performance hybrid supercapacitors". In: *Scientific reports* 8.1 (2018), p. 8179 (cit. on p. 26).

[85] Fusheng Wen, Chunxue Hao, Jianyong Xiang, Limin Wang, Hang Hou, Zhibin Su, Wentao Hu, and Zhongyuan Liu. "Enhanced laser scribed flexible graphene-based micro-supercapacitor performance with reduction of carbon nanotubes diameter". In: *Carbon* 75 (2014), pp. 236–243 (cit. on p. 26).

[86] Litty V Thekkekara, Baohua Jia, Yinan Zhang, Ling Qiu, Dan Li, and Min Gu. "On-chip energy storage integrated with solar cells using a laser scribed graphene oxide film". In: *Applied Physics Letters* 107.3 (2015), p. 031105 (cit. on p. 26).

[87] Nana Amponsah Kyerematen, Thierry Brousse, and David Pech. "Microsupercapacitors as miniaturized energy-storage components for on-chip electronics". In: *Nature nanotechnology* 12.1 (2017), p. 7 (cit. on p. 26).

[88] Rao R Tummala. "Moore's Law for Packaging to Replace Moore's Law for ICS". In: *2019 Pan Pacific Microelectronics Symposium (Pan Pacific)*. IEEE. 2019, pp. 1–6 (cit. on p. 26).

[89] S-Y Kim, K Kim, YH Hwang, J Park, J Jang, Yunyong Nam, Y Kang, M Kim, HJ Park, Z Lee, et al. "High-resolution electrohydrodynamic inkjet printing of stretchable metal oxide semiconductor transistors with high performance". In: *Nanoscale* 8.39 (2016), pp. 17113–17121 (cit. on p. 27).

[90] Wenwen Liu, Congxiang Lu, Hongling Li, Roland Yingjie Tay, Leimeng Sun, Xinghui Wang, Wai Leong Chow, Xingli Wang, Beng Kang Tay, Zhongwei Chen, et al. "based all-solid-state flexible micro-supercapacitors with ultra-high rate and rapid frequency response capabilities". In: *Journal of Materials Chemistry A* 4.10 (2016), pp. 3754–3764 (cit. on p. 27).

[91] Jianglin Diao, Jia Yuan, Ailing Ding, Jiushang Zheng, and Zhisong Lu. "Flexible Supercapacitor Based on Inkjet-Printed Graphene@ Polyaniline Nanocomposites with Ultrahigh Capacitance". In: *Macromolecular Materials and Engineering* 303.6 (2018), p. 1800092 (cit. on p. 27).

[92] Huan Pang, Yizhou Zhang, Wen-Yong Lai, Zheng Hu, and Wei Huang. "Lamellar K2Co3 (P2O7) 2· 2H2O nanocrystal whiskers: High-performance flexible all-solid-state asymmetric micro-supercapacitors via inkjet printing". In: *Nano Energy* 15 (2015), pp. 303–312 (cit. on p. 27).

[93] Zhong-Shuai Wu, Khaled Parvez, Andreas Winter, Henning Vieker, Xianjie Liu, Sheng Han, Andrey Turchanin, Xinliang Feng, and Klaus Müllen. "Layer-by-Layer Assembled Heteroatom-Doped Graphene Films with Ultrahigh Volumetric Capacitance and Rate Capability for Micro-Supercapacitors". In: *Advanced Materials* 26.26 (2014), pp. 4552–4558 (cit. on p. 28).

[94] David Pech, Magali Brunet, Hugo Durou, Peihua Huang, Vadym Mochalin, Yury Gogotsi, Pierre-Louis Taberna, and Patrice Simon. "Ultrahigh-power micrometre-sized supercapacitors based on onion-like carbon". In: *Nature nanotechnology* 5.9 (2010), p. 651 (cit. on p. 28).

[95] Karolina U Laszczyk, Kazufumi Kobashi, Shunsuke Sakurai, Atsuko Sekiguchi, Don N Futaba, Takeo Yamada, and Kenji Hata. "Lithographically integrated microsupercapacitors for compact, high performance, and designable energy circuits". In: *Advanced Energy Materials* 5.18 (2015), p. 1500741 (cit. on p. 28).

[96] Hui Pan, Dawei Wang, Qingfa Peng, Jun Ma, Xin Meng, Yaopeng Zhang, Yuning Ma, Shenmin Zhu, and Di Zhang. "High-performance microsupercapacitors based on bioinspired graphene microfibers". In: *ACS applied materials & interfaces* 10.12 (2018), pp. 10157–10164 (cit. on p. 28).

[97] Haibo Hu, Kun Zhang, Shuxin Li, Shulin Ji, and Changhui Ye. "Flexible, in-plane, and all-solid-state micro-supercapacitors based on printed interdigital Au/polyaniline network hybrid electrodes on a chip". In: *Journal of Materials Chemistry A* 2.48 (2014), pp. 20916–20922 (cit. on p. 28).

[98] Neelakandan Santhosh, Gregor Filipič, Elena Tatarova, Oleg Baranov, Hiroki Kondo, Makoto Sekine, Masaru Hori, Kostya Ostrikov, and Uroš Cvelbar. "Oriented carbon nanostructures by plasma processing: recent advances and future challenges". In: *Micromachines* 9.11 (2018), p. 565 (cit. on p. 29).

[99] Guoping Xiong, Chuizhou Meng, Ronald G Reifenberger, Pedro P Irazoqui, and Timothy S Fisher. "Graphitic Petal Micro-Supercapacitor Electrodes for Ultra-High Power Density". In: *Energy Technology* 2.11 (2014), pp. 897–905 (cit. on p. 29).

[100] Jianglin Ye, Huabing Tan, Shuilin Wu, Kun Ni, Fei Pan, Jie Liu, Zhuchen Tao, Yan Qu, Hengxing Ji, Patrice Simon, et al. "Direct Laser Writing of Graphene Made from Chemical Vapor Deposition for Flexible, Integratable Micro-Supercapacitors with Ultrahigh Power Output". In: *Advanced Materials* 30.27 (2018), p. 1801384 (cit. on p. 29).

[101] Lu Zhang, Derek DeArmond, Noe T Alvarez, Rachit Malik, Nicholas Oslin, Colin McConnell, Paa Kwasi Adusei, Yu-Yun Hsieh, and Vesselin Shanov. "Flexible micro-supercapacitor based on graphene with 3D structure". In: *Small* 13.10 (2017), p. 1603114 (cit. on p. 29).

[102] David Aradilla, Fang Gao, Georgia Lewes-Malandrakis, Wolfgang Müller-Sebert, Dorian Gaboriau, Pascal Gentile, Boyan Iliev, Thomas Schubert, Saıd Sadki, Gérard Bidan, et al. "A step forward into hierarchically nanostructured materials for high performance micro-supercapacitors: Diamond-coated SiNW electrodes in protic ionic liquid electrolyte". In: *Electrochemistry Communications* 63 (2016), pp. 34–38 (cit. on p. 29).

[103] Lushuai Zhang, Wesley Viola, and Trisha L Andrew. "High Energy Density, Super-Deformable, Garment-Integrated Microsupercapacitors for Powering Wearable Electronics". In: *ACS applied materials & interfaces* 10.43 (2018), pp. 36834–36840 (cit. on p. 29).

[104] Guoping Xiong, Chuizhou Meng, Ronald G Reifenberger, Pedro P Irazoqui, and Timothy S Fisher. "A review of graphene-based electrochemical microsupercapacitors". In: *Electroanalysis* 26.1 (2014), pp. 30–51 (cit. on p. 29).

[105] Amin M Saleem, Rickard Andersson, Vincent Desmaris, and Peter Enoksson. "Integrated on-chip solid state capacitor based on vertically aligned carbon nanofibers, grown using a CMOS temperature compatible process". In: *Solid-State Electronics* 139 (2018), pp. 75–79 (cit. on pp. 30, 31, 33).

[106] *Graphene Supermarket*. `https://graphene-supermarket.com/`. Accessed: 2019-09-24 (cit. on p. 30).

[107] Bing Zhao, Peng Liu, Yong Jiang, Dengyu Pan, Haihua Tao, Jinsong Song, Tao Fang, and Weiwen Xu. "Supercapacitor performances of thermally reduced graphene oxide". In: *Journal of power sources* 198 (2012), pp. 423–427 (cit. on p. 34).

[108] Rudd JM Vullers, Rob Van Schaijk, Hubregt J Visser, Julien Penders, and Chris Van Hoof. "Energy harvesting for autonomous wireless sensor networks". In: *IEEE Solid-State Circuits Magazine* 2.2 (2010), pp. 29–38 (cit. on p. 41).

[109] Gamry Instruments. "Basics of electrochemical impedance spectroscopy". In: *G. Instruments, Complex impedance in Corrosion* (2007), pp. 1–30 (cit. on p. 41).

[110] Martin Nielsen-Lönn, Pavel Angelov, J Jacob Wikner, and Atila Alvandpour. "Self-powered micro-watt level piezoelectric energy harvesting system with wide input voltage range". In: *Analog Integrated Circuits and Signal Processing* 98.3 (2019), pp. 441–451 (cit. on pp. 42, 44, 45).

[111] Chris Van Hoof. *MEMS Packaging*. University Lecture. 2015 (cit. on pp. 43, 46).

[112] Christopher S Choi, Jonathan Lau, Janet Hur, Leland Smith, Chunlei Wang, and Bruce Dunn. "Synthesis and Properties of a Photopatternable Lithium-Ion Conducting Solid Electrolyte". In: *Advanced Materials* 30.1 (2018), p. 1703772 (cit. on p. 45).

[113] Yizhou Ye, Zhenjun Wang, Zhenxiang Yi, Ming Qin, and Qing-An Huang. "Annular-Encapsulation Packaging to Realize High-Performance MEMS Thermal Wind Sensor". In: *2018 IEEE 13th Annual International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*. IEEE. 2018, pp. 456–459 (cit. on p. 46).