Investigation of palladium current collectors for vertical graphene-based microsupercapacitors

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Investigation of palladium current collectors for vertical graphene-based microsupercapacitors

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Abstract. As microsystems are reduced in size and become integrated in the Internet of Things (IoT), they require an adequate power supply which can be integrated at the same size scale. Microsupercapacitors (MSCs), if coupled with on-chip harvesters, can offer solutions for a self-sustaining, on-chip power supply. However, the implementation of reliable MSC wafer-scale production compatible with CMOS technology remains a challenge. Palladium (Pd) is known as a CMOS compatible metal and, in this paper, we investigate the use of Pd as a contact material for vertical graphene (VG) electrodes in wafer-scale MSC fabrication. We show that a Ti diffusion barrier is required to prevent short-circuiting for the successful employment of Pd contacts. The fabricated MSCs demonstrate a capacitance of 1.3 μF/cm^2 with an energy density of 0.42 μJ/cm^2. Thus, utilization of a Ti diffusion barrier with a CMOS compatible Pd metal electrode is a step towards integrating MSCs in semiconductor microsystems.

1. Introduction

The Internet of Things (IoT) will rely on smart microsystems connected over a cloud computing-based infrastructure that will encompass every aspect of our lives [1][2]. Much current work is devoted to optimization of microsystems size and integrability. However, ever-increasing demands for an on-chip power supply cannot be neglected [3]. As traditional thin-film batteries suffer from problems of poor rate capability and limited cycle lifetimes, microsupercapacitors (MSCs) provide an alternative energy supply solution through their high power and longer cycle lifetime [4].

MSCs, miniaturized forms of supercapacitors, are energy storage devices that store the harvested energy by utilizing the charges formed at the electrode-electrolyte interface (figure 1) [4]. To be truly integrable in CMOS technology, the MSCs need to overcome two main challenges. The first challenge is choice of material for the current collectors. Investigation into MSCs have been traditionally performed using electrodes deposited over Au current collectors for their electrical characteristics and chemical stability [5]. However, usage of Au should be avoided in semiconductor technology as it diffuses into the underlying layers even at moderate temperatures. Diffusion of Au causes a creation of a deep- level trap and hole recombination centers leading to a short-circuit [6]. Moreover, it is susceptible to electromigration [7] and is well known to critically contaminate subsequent process steps. In contrast, Pd can offer lower diffusion properties than Au and can improve the longevity of the devices [8]. Therefore, its utilization as the metal contact can provide a solution to this problem. In order to eliminate the diffusion problem, Ti has been found to act as a diffusion barrier for Pd by Nicolet et al. [9] and Tisone et al. [10]. The second challenge for MSCs to be integrable in CMOA technology is due to

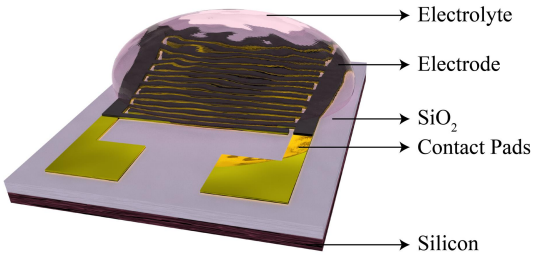


Figure 1. Graphical interpretation of a conventional MSC on a silicon substrate. Image acquired after permission from [13].

their organic electrode materials, that have required special techniques such as laser scribing, doctor blade coating, and reactive chemical growth for their deposition. The growth of vertical graphene (VG) at CMOS compatible temperatures provide an excellent replacement for conventionally used carbon electrodes such as CNTs [11], ACs [12], rGOs [13], and graphene [14]. VG has a several advantages over conventional carbon materials. Its non-agglomerated morphology with abundant open channels creates an advantage for devices that require maximum surface area. VG sheets possess advantageous characteristics such as exposed sharp edges, non stacking morphology and large surface to volume ratio. They demonstrate an exceptional surface area of 2600 m^2/g [15]. Also, their free standing structures create domains of aligned charge transport channels that improves the rate capability [16].

In this paper, we present a study of three wafer scale fabrication process schemes: one with Au/Ti current collectors (Ti/Au contact); and two with Pd current collectors – one without a diffusion barrier (control), and one with a Ti barrier (Ti-enhanced) for a CMOS compatible and wafer-scale MSCs with VG electrodes and H_3PO_4/PVA liquid electrolyte. Comparison of electrochemical analyses of the three samples: Au/Ti contacts, control, and Ti-enhanced devices support the conclusion of Ti as an effective diffusion barrier. The control sample forms a short-circuit while the Ti-enhanced sample demonstrates a quasi-rectangular capacitive behavior after the addition of Ti as a diffusion barrier.

2. Experimental

2.1. Fabrication of VG-based MSCs

The MSC wafer fabrication processes for the three devices follow the steps outlined in figure 2. The pathways Ti/Pd and Pd were made by lift-off, using a bi-layer resist masking technique which

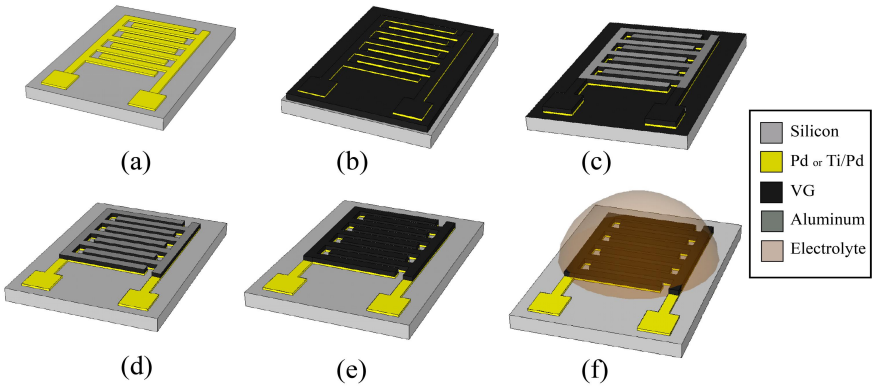
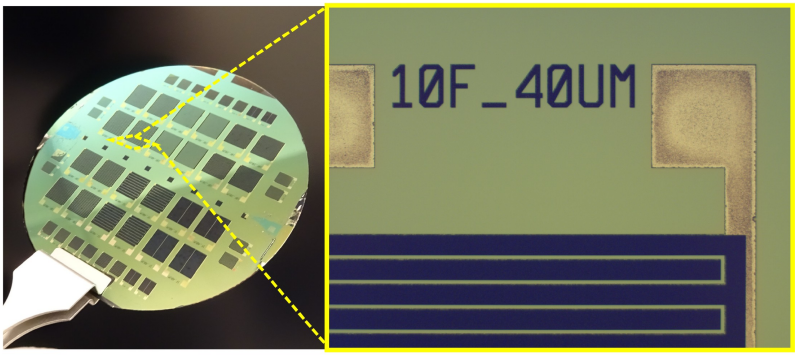


Figure 2. Schematic process plan of a conventional MSC on a silicon substrate.



(a) (b)

Figure 3. Post fabrication: (a) MSC devices on a wafer (b) Pd current collectors under an optical microscope. The interdigitated structure (in black) is the VG on Pd electrodes.

involves stacking a lift-off resist and positive photoresist. Bi-layer lift-off metallization techniques offer significant advantages in resolution, removal simplicity and yield over conventional single-layer lift-off processes [17]. Pd and Ti/Pd metal current collectors were evaporated on the patterned resist mask at thicknesses of 100 nm for the Pd control wafer and 20/100 nm for Ti/Pd wafer (figure 2(a)). VG was grown on the prepared substrates in a cold-wall low-pressure PECVD reactor (Black Magic, Aixtron). The growth was initiated by introducing acetylene gas (C_2H_2), which was maintained for 10 min (figure 2(b)). Growth time, C_2H_2 flow rate and temperature can be changed to control the size of VG. A 70 nm hard mask of aluminum was deposited (figure 2(c)) to protect the electrodes through oxygen reactive ion etching (RIE), then subjected to RIE as well (figure 2(d)). The aluminum hard mask was then etched using a mixture of $Cl_2/SiCl_4$ in presence of Ar (figure 2(e)). Figure 3(a) shows an optical image of fabricated devices on a 2" silicon wafer with an optical microscopy image of the contact pads and carbon electrodes figure 3(b). H_3PO_4/PVA liquid electrolyte was finally dispensed on electrode surface before the measurements (figure 2(f)).

2.2. Material Characterization

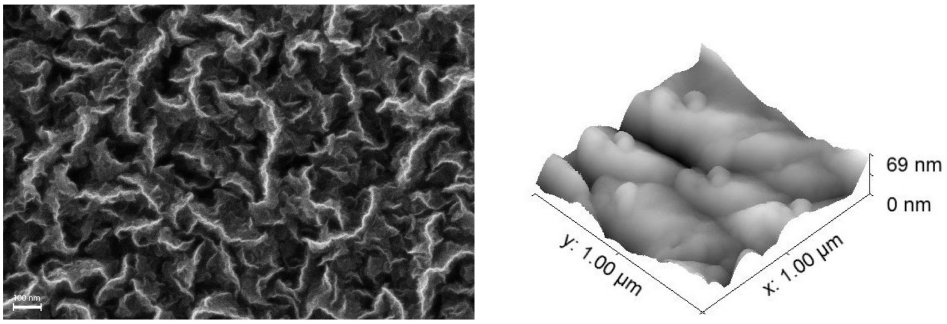
VG was characterized for its growth morphology, surface profile, and structural information. The growth morphology was viewed under a scanning electron microscope (SEM, Zeiss Supra 60 VP). SPM Bruker Dimension and Dektak Profiler were used to determine the surface profile and growth thickness. The structural information was accrued through Horiba Raman Spectrometer with a 638 nm excitation laser.

2.3. Electrochemical Measurements

The electrochemical tests were carried out using Gamry Reference 3000 potentiostat. The behaviour of VG electrode material was characterized by cyclic voltammograms (CVs) at 2 V/s scan rate. The areal capacitance of the device was obtained by evaluating the cyclic voltammograms using the following equation:

$$C_A = \frac{\frac{1}{2}\int IdV}{sA\Delta V} \quad (1)$$

where $\int IdV$ is the area of the CV curve, s is the scan rate (V/s), A is the area of the device (cm^2) and ΔV (V) is the potential window. A probe station with a two electrodes Gamry Reference 3000 system was used for measurements through the contact pads. The aqueous electrolyte, H_3PO_4/PVA was dispensed a day before measurements on the MSC devices.



(a) (b)

Figure 4. (a) SEM image of VG. (b) AFM image of 3D surface profile of a 1 μm × 1 μm window.

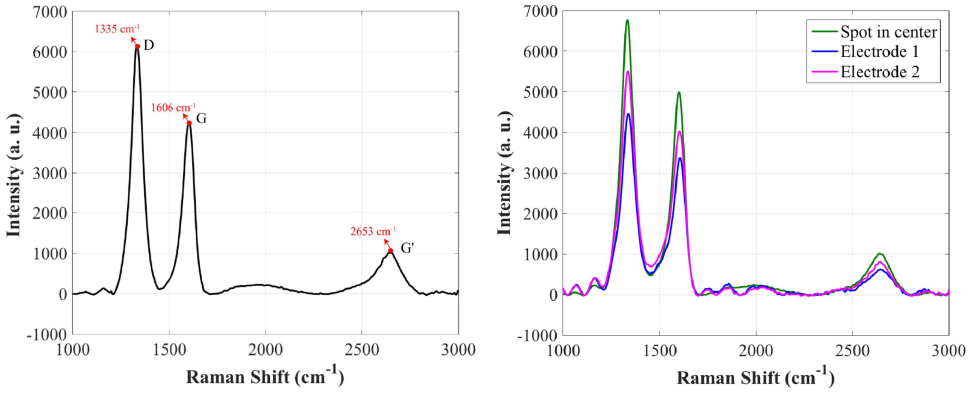
3. Results and Discussion

3.1. Material Characterization

The SEM micrograph of the VG is shown in figure 4a. The vein-like structures shaded white are the peaks of the VG nanosheets. The surface profile of a small section of the electrode is shown in figure 4b. The SEM images resemble previously reported VG topologies [18]. Results from the Dektak profiler showed a uniform thickness of 1.1 ± 0.08 μm over 16 different locations on the wafer.

Structural characterization of VGs for detecting defects and disorders was performed by Raman spectroscopy. Fig. 5(a) shows the Raman spectrum of the VG. The spectrum comprises of two prominent bands, G and G", visible at 1606 cm^{-1} and 2653 cm^{-1}. These are the characteristic shifts of a graphitic structure where G band is observed around 1575 cm^{-1} [19]. The slight shift towards a higher number denotes that the crystal sizes are extremely small [20]. The spectrum also consists of one defect-assisted scattering, D band at 1335 cm^{-1}. This defect is absent in pristine graphene [21].

The level of disorder in the VG structures can be determined through intensity ratio I_D/I_G, which provides a measure of disorder. VG has a ratio of 1.45, which indicates rather big amount of present defects and small crystallite sites mentioned above. Figure 5(b) displays the representative spectra at three different locations on the Ti-enhanced device. The I_D/I_G for the three locations are 1.33, 1.39, and 1.35. This indicates a homogeneity in the growth of VG over the device structure.



(a) (b)

Figure 5. Results from Raman Spectroscopy: (a) Raman spectra of VG after growth. (b) Comparison of Raman spectra at three different locations on the Ti-enhanced device.

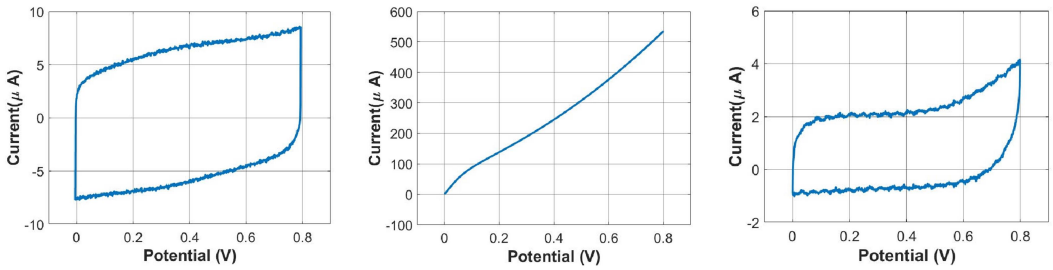


Figure 6. Cyclic Voltammograms of: (a) Ti/Au current collectors. (b) Control sample. (c) Ti-enhanced sample.

3.2. Device Performance

The CV measurements were performed using Gamry Reference 3000AE potentiostat and Karl Suss PM 5 probes station. Figure 6 displays the cyclic voltammograms of one MSC sample with 10 fingers with 40 μm interspacing on the three fabricated wafers – Au/Ti contact, control, and Ti-enhanced/ The control wafer devices showed a resistive behavior due to the short circuit as shown in figure 6(b). As discussed previously, we can pinpoint Pd diffusion into the insulating SiO_2 layer. Devices on Ti/Au contacts, and Ti-enhanced (figure 6(a), (c)) wafer showed a capacitive behavior at a scan rate of 2000 mV/s. The quasi rectangular shape of the CV curves for the potential windows 0-0.8 V indicates the electrochemical double-layer capacitive behaviour of the device. Unlike Ti/Au-contact devices, CV measurements for Ti/Pd show a peak at the upper limit of the electrolyte potential window due to the electrolyte degradation. This phenomenon usually happen in liquid electrolytes at voltage around 1 V, but since the used measurement setup is an open system where wafer interacts with environment, possible oxygen absorption of the electrolyte can cause the shift of degradation at lower potential.

The areal capacitance is of the Ti/Au contact and Ti-enhanced device are calculated from eq.1. MSCs with Ti/Au-current collectors demonstrated a capacitance of 5.5 μF/cm^2 while the Ti-enhanced sample showed 1.3 μF/cm^2. Their energy densities from $\frac{CV^2}{2}$ are calculated as 1.76 μJ/cm^2 and 0.42

μJ/cm^2. Ti/Au-contact devices demonstrate a higher capacitance and energy density than Ti-enhanced devices. This can be due to the fact that Au has a higher conductivity and stronger surface adhesivity and lower contact resistance than Pd [22]. However, the significant difference in capacitance requires further investigation, e.g. reaction of H_3PO_4 with Pd, or difference in electrode properties on different wafer samples.

4. Conclusion

In this paper, we have investigated the performance of three VG-based MSCs fabricated over Ti/Au, Pd, and Pd/Ti current collectors. The samples containing Pd current collectors showed a resistive behavior due to a short circuit. The other two device types; Ti/Au-contact based MSCs showed a capacitance of 5.5 μF/cm^2 at a scan rate of 2000 mV/s with an energy density of 1.76 μJ/cm^2, and the Pd/Ti device demonstrated a capacitance of 1.3 μF/cm^2 and an energy density of 0.42 μJ/cm^2. Thus, the fabrication method including Ti as a diffusion barrier aims towards a potential future integration in CMOS based microsystems for on-chip energy storage solutions.

Acknowledgements

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