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High linear power amplifier for multicarrier satellite communications

HIGH LINEAR POWER AMPLIFIER FOR C-BAND MULTICARRIER SATELLITE COMMUNICATIONS

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ABSTRACT

High linearity performance in transmitters is receiving continuously attention due to demands of higher data rates in satellite communication links. This paper presents a GaAs pHEMT MMIC high linear power amplifier intended for multicarrier operation at C-band. Junction temperature prediction methods are considered during the amplifier design to keep the temperature under control and achieve high reliability required for space applications. The design method is focused in high linearity optimizing the loads and using a non-linear transistor model to predict harmonic generation and intermodulation products. The amplifier was characterized in terms of S-parameters, single tone output power and two tone output power.

The measured S-parameters shows a flattened gain over 25 dB between 3 and 6 GHz. The 1dB compression point is measured at 26.7 dBm and the output third order intercept point (OIP3) is above 40 dBm in the band reaching a maximum of 41.7 dBm at 4.5 GHz. The power consumption is lower than 2.5 W and the junction temperatures are calculated under 105 °C.

INTRODUCTION

A satellite have several transponders, each of them receives many carrier signals that are shifted in frequency and retransmitted. Looking for channel efficiency improvement and reacting to higher data rates demands, more complex modulation methods are desired for multicarrier links. This requires a high linear operation of the electronic circuits involved in the signal path within the transponder. Specially, the power amplifier at the transmitter is the dominant block for the overall system linearity performance.

In addition, every electronic circuit intended for on board operation require high reliability to guarantee long lifetime. The power levels handled by the amplifier generate heat in the transistor and it is the limiting factor for the overall system reliability. The junction temperature in the active device is the main contributor to wearing and failures [1]. The transistor geometry, the material thermal properties and the power dissipation defines the temperature profile of the device. Junction temperature prediction methods are used to evaluate the reliability requirement in the amplifier design.

These special conditions set tradeoffs in the amplifier design to achieve the desired output power, gain, bandwidth and linearity keeping the junction temperature under the allowed value. For the amplifier design described in this paper, the HEMT non-linear Chalmers model is used for the active device [2]. This model takes into account the strong bias dependences of the current and capacitances and their derivatives, allowing the designer to analyze an optimal bias point for optimum linearity. By using this model, the designer can also determine the optimal loads through multi-tone load pull analysis and determine accurately the harmonic and intermodulation distortion.

In this work, A highly linear C-band power amplifier using a pHEMT GaAs technology is described achieving over 40 dBm third order intercept point at the output (OIP3) while keeping the required reliability operation.

JUNCTION TEMPERATURE PREDICTION

The prediction of the junction temperature is an important consideration during the circuit design to ensure long lifetime operation of the amplifier. There are different approaches to calculate the junction temperature. Some are based on numerical methods [3-5] or using specialized software to simulate the thermal profile [6]. However, the microwave circuit designer needs more practical tools that can be include in the design environment.

In this work, the methods proposed by Fukui [7] and Darwish [8] are analyzed and compared. In the method proposed by Fukui, the channel temperature is calculated using empirical relations of the measured voltage variations at different temperature levels. A relation between the absolute thermal resistance and the geometric dimensions of the transistors is defined with the backside temperature as parameter. The corresponding Fukui curves for the process used in this work are shown in [9] and the junction temperature is defined as:

$$T_{ch} = T_o + \left[R_{TH}\left(\frac{1000}{n*Wu}\right)\right] P_{diss} \quad (1)$$

Where T_o is the backside temperature, n the number of fingers and Wu the unit gate width.

The Darwish method is an analytical approach based on the three dimension Laplace equation using ellipsoids and cylindrical coordinates to represent thermal surfaces. The advantage of this method is that there is no need of previous measurements to determine the thermal resistance and it is defined analytically as:

$$T_{ch} = \left({T_o}^{-0.23} - 0.23(\theta P_{diss}){T_o}^{-1.23}\right)^{(-1/0.23)} \quad (2)$$

Where θ is the absolute thermal resistance of the device, and depends directly of the geometry and material characteristics.

TECHNOLOGY AND DEVICE MODELING

The amplifier is designed using space qualified GaAs technology from United Monolithic Semiconductors [9]. It is based on an active pHEMT device built over a 70 µm thickness wafer. The power density is 900 mW/mm and the cut-off frequency *ft* is 45 GHz which is appropriate for power C-band applications.

For the device modeling, traditional I-V and multi-bias S-parameter measurements were performed. In addition, Large Signal Vector Network Analyzer (LSVNA) measurements were implemented to evaluate the transistor strong nonlinear behavior up to 40 GHz. An active load pull setup based on the Maury/NMDG MT4463 was used for the large signal measurements [10]. A signal generator is used to create the fundamental test signal, and the injected wave at the output of the DUT is produced using a coupler followed by the vector modulator.

The large signal modeling utilizes data from load pull and power spectrum measurements to optimize the model parameters [11]. The measured and modeled transconductance for a 4 x 50 µm transistor is shown in fig. 1. The power spectrum measurement at 4 GHz with 4.5 V drain bias on the same device size is shown in fig. 2.

When analyzing the transconductance, power spectrum and model parameters variations, it can be concluded that a careful selection of the bias voltages leads to linearity improvements. On one side, the gate bias should be chosen in the region where the transconductance has its maximum and where power spectrum exhibits minimum harmonics. Other model parameters as the Cgs and Cgd capacitances indicate regions of the gate and drain bias voltages where the nonlinear effects are reduced [12].

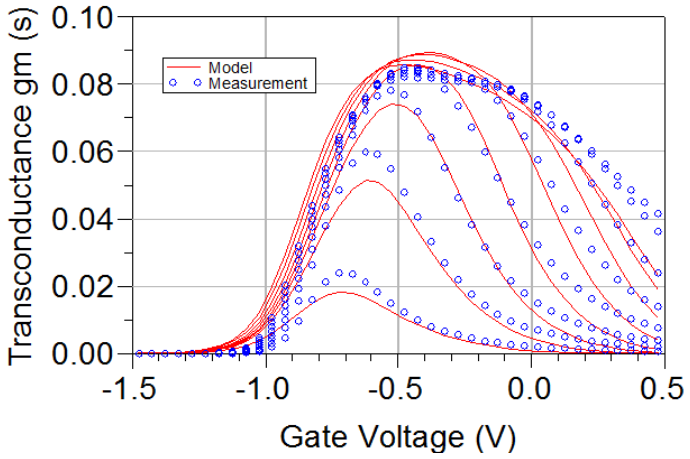

Fig. 1. Transconductance measured and modeled for a 4 x 50 µm transistor.

POWER AMPLIFIER DESIGN

Temperature condition

The amplifier should be designed to keep the junction temperature below the limited defined by the reliability condition. For GaAs devices a typical junction temperature is 115 °C. To calculate the channel temperature with the prediction methods studied, it is required to know the backside temperature. However, MMICs circuits are usually soldered over a lead frame that in turn is soldered over a PCB and mounted on a metallic carrier as shown in fig 3. The channel temperature (Tc) is limited by the reliability requirement. The ambient temperature (Ta) is typically defined in the system specifications, meanwhile the backside temperature (To) is not an absolute value and depends on the equivalent thermal resistance of the layers involved in the thermal flow. A maximum gradient between the backside and the channel temperatures is defined as:

$$\Delta T_{co-max} = \Delta T_{ca-max} - R_{th-eq}\ P_{diss-max}\ [\mathrm{K}] \tag{3}$$

Where:

$$\Delta T_{co-max} = T_{c-max} - T_o$$
$$\Delta T_{ca-max} = T_{c-max} - T_o$$

P_{diss} is the dissipated power and R_{th-eq} is the equivalent thermal resistance between the MMIC backside and the bottom surface. Equation (3) is used as design condition to achieve the required reliability.

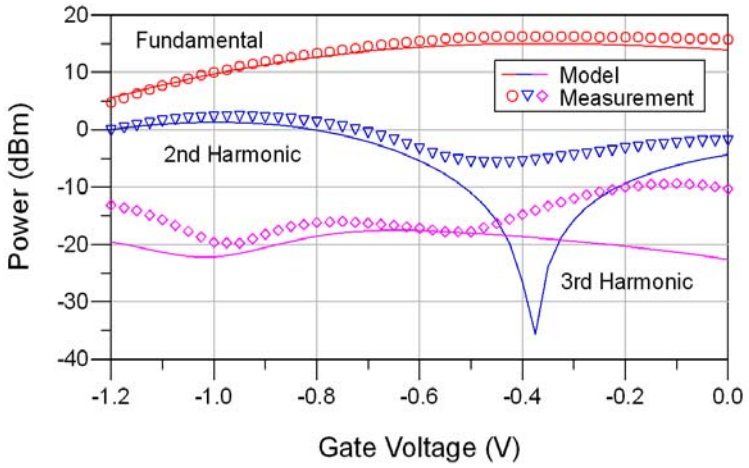

Fig. 2. Measured and modeled power spectrum for a 4 x 50 µm transistor. With 4.5 V drain bias at 4 GHz.

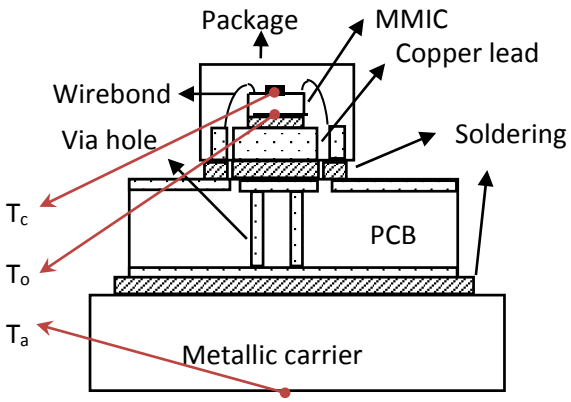

Fig. 3. Assembled MMIC showing the ambient (Ta) backside (To) and junction (Tc) temperatures.

Device selection

The device size selection is done taking into account the electrical and reliability requirements. The characteristic of the MMIC assembling are known and a relation of the shape of (3) is given:

$$\Delta T_{co-max} = 32 - 30\, P_{diss-max}\ [K] \tag{4}$$

The maximum junction temperature difference over the ambient is 32 °C. Using (4) together with (5) and assuming a backside temperature of 80 °C, an expression for the maximum dissipated power is found based on the Fukui relation:

$$P_{diss-max} = \frac{32}{\left[\frac{R_{th}*1000}{N*W_u}+30\right]} \tag{5}$$

The maximum power dissipation, and the maximum temperature increment for different transistor sizes is calculated. Fig. 4 shows the comparison of the calculated junction temperature for 12 x 60 µm and 12 x 80 µm transistor sizes as function of the dissipated power. Both methods agreed with a maximum difference of 4 degrees.

The bias point is chosen considering the variations of the transconductance, the model nonlinear capacitances and the maximum dissipation power from (5). A drain bias point of 4 V is far below the maximum ratings avoiding stress to the device and reduces the nonlinear dependence of the gate drain capacitance of the transistors model. A gate voltage around -0.45 where there is a broad minimum of the 2nd and 3rd harmonics keeps low intermodulation products and decrease the generated harmonics. For the 12 x 80 µm transistor, the drain current is 85mA what results in 344 mW, the calculated junction temperature is 104 °C.

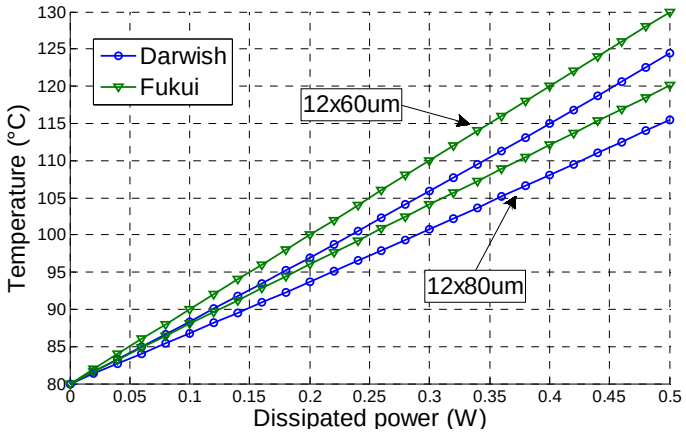

Fig. 4. Calculated junction temperature for a 12 x 60 µm and a 12 x 80 µm transistor size.

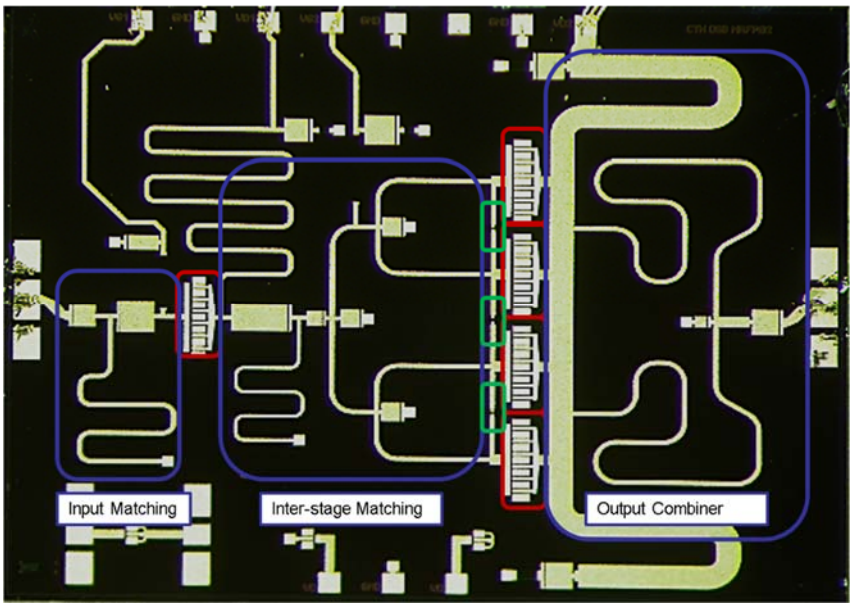

Fig. 5. Chip photograph of the MMIC linear amplifier

Topology

1-tone and 2-tone simulations are performed in the simulation software to evaluate power and linearity performance of different transistor sizes at the chosen bias point. The load was optimized to improve the output third order intercept point (OIP3). For the 12 x 80 µm transistor, the OIP3 found is 37.9 dBm and the 1dB compression point 21.7 dBm.

The first stage is formed by a single 12 x 60 µm transistor biased similarly at 4 V drain voltage and 63 mA drain current. It provides 19 dBm output power in the simulated 1dB compression point avoiding saturation in the first stage. The calculated junction temperature is 101.6 °C.

Fig. 5 shows the fabricated amplifier. The output stage combines four transistors using a bus-bar combiner followed by a tree structure [13]. The bus-bar offers a compact way to combine multiple cells and also a direct path to feed the transistors from the edge. The tree combining structure acts as matching network transforming the output port to the optimal loads for the transistors. An electromagnetic simulation is performed to consider possible line couplings and edge capacitances in the wide busbar.

The input matching follows a T network. The values were optimized to achieve a wideband input return loss for a 50 Ω source impedance. The interstage matching transform the input impedances of the output stage transistors to the chosen load for the first stage. The tree divider keeps phase and amplitude balance of the RF signal.

The interstage and the output combiner structures can create parasitic loops and odd mode oscillations. The stability of the amplifier is analyzed following the method explained in [14]. As result, the parallel resistors, shown in fig. 5 in the green boxes, are added between the branches at the input of the power stage.

MEASUREMENTS AND RESULTS

An Agilent E8361A vector network analyzer was used to measure small signal parameters up to 40 GHz. The S-parameters measurements and simulation results are shown on the left side of fig.6. The total DC power consumption of the chip is 2.0 W. The small signal gain has a flat response above 25 dB with an octave band of operation between 3 and 6 GHz.

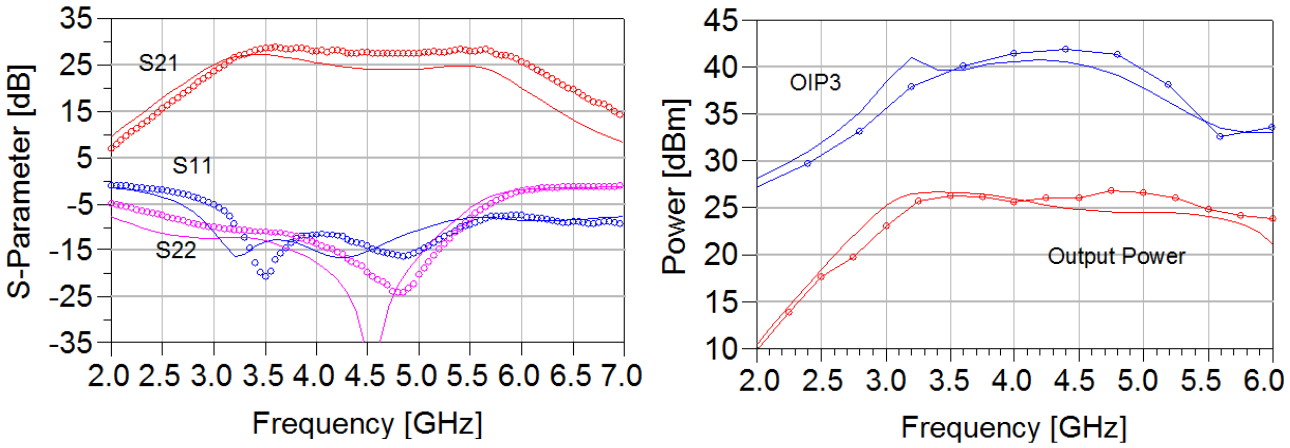

Fig. 6. Amplifier (left) S-Parameters and (right) output power and OIP3 simulations and measurements

Power measurements were performed using Agilent 83650 synthesizers and a Rohde & Schwarz FSUP50 analyzer. The measured 1dB compression point is 26.7 dBm at the selected bias point. The OIP3 is above 40 dBm reaching a maximum of 41.6 dBm at 4.5 GHz. The right side of fig. 6 shows the measured output power and OIP3 in the band of operation.

The junction temperature of the amplifier is measured with 80 °C backside temperature using a Quantum Focus Instruments infrared microscope. Fig. 7 shows a chip level image with inserted high resolution pictures of the transistors. The junction temperatures for the first stage and second stage reach maximum levels of 107 °C and 112 °C respectively.

CONCLUSIONS

A C-band MMIC linear power amplifier using GaAs pHEMT technology is reported and characterized. A comparison of published GaAs linear amplifiers is shown in Table 1. An additional figure of merit defined as the ratio between OIP3 and 1dB compression point is included to compare the linearity improvement over different output power levels

The reported amplifier presents one of the best linearity performance per power delivered. In addition, it keeps low junction temperature for high reliability operation. The OIP3 peak of 41.6 dBm is one of the highest reported OIP3 for C-band power amplifiers. Furthermore, this amplifier has the best bandwidth of the linear amplifier reported reaching an octave of operation.

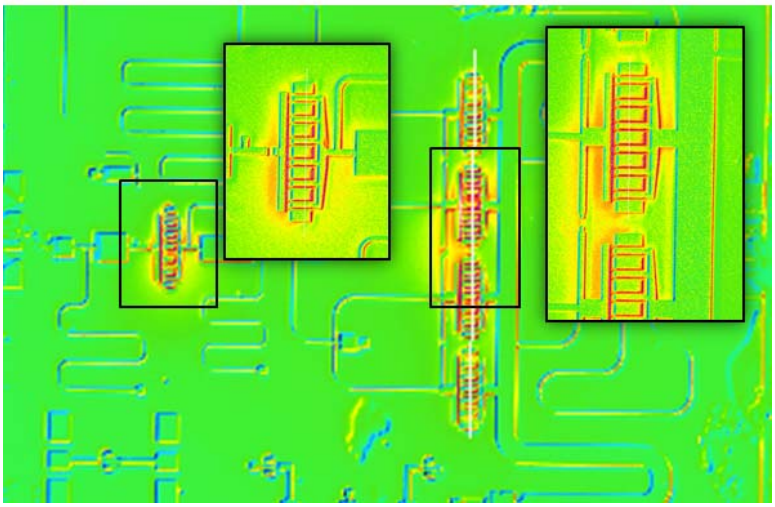

Fig. 7. Infrared imaging at chip level with high resolution images for the transistors.

Table 1. Published C-band power amplifiers

Reference	Technology	Freq. (GHz)	Gain (dB)	Bias (V/mA)	P1dB (dBm)	OIP3 (dBm)	OIP3/P1dB
[15]	GaAs HFET 0.5 μm	5.5-7.1	15	8/1300	36	50	14
[16]	GaAs pHEMT 0.5 μm	5.8	14	5/110	27	37,5	10,5
[17]	GaAs pHEMT 0.15 μm	5.2	15	4	13,3	22,5	9,2
[18]	GaAs pHEMT 0.4 μm	3.3-3.8	30.4	8/700	34	43,5	9,5
[19]	GaAs	4.9-8.5	20	5/98	19	31	12
[20]	GaAs pHEMT 0.15 μm	11-15	16	3/150	23	35	12
[21]	GaAs pHEMT 0.15 μm	17-27	19	4,5/890	28,5	38	9,5
[22]	GaAs pHEMT 0.25 μm	3,8	33	4/560	24	36,7	12,7
This work	**GaAs pHEMT 0.25 μm**	**3-6**	**25**	**4/580**	**26,6**	**41,6**	**15,1**

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