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Citation for the original published paper (version of record):

Roev, A., Ivashina, M., Maaskant, R. et al (2019). N-way spatial power combining in SIW for high power generation MMICs-scalability bounds. 2019 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting, APSURSI 2019 - Proceedings, July 2019: 1789-1790. http://dx.doi.org/10.1109/APUSNCURSINRSM.2019.8888342

# N-Way Spatial Power Combining in SIW for High Power Generation MMICs – Scalability Bounds

Artem Roev, Marianna V. Ivashina
Dept. of Electrical Engineering
Chalmers University of Technology
Gothenburg, Sweden
roev@chalmers.se

Rob Maaskant, Marion K. Matters-Kammerer
Dept. of Electrical Engineering
Eindhoven University of Technology
Eindhoven, The Netherlands
r.maaskant@tue.nl

***Abstract*—An N-way transition between an array of amplifiers and a single substrate integrated waveguide (SIW) is presented. Its operation principle is based on excitation of the spatially distributed TE10 mode with an array of parallel and strongly coupled microstrip lines (MLs). The paper discusses and evaluates the approximate scalability bounds of such a structure in terms of the number of input channels. The model shows that, by employing a thin substrate, more amplifiers are capable of interfacing a single SIW to increase the output power, which is an important conclusion in regards to a future on-chip implementation of the structure. The model has also been validated by numerical simulations.**

## I. Introduction

Increased propagation and material losses as well as output power limitations of semiconductor devices at mm-wave frequencies is a problem that is partly overcome by parallel and series power-combining of multiple active devices per single antenna element [1]. However, conventional circuit-level power combiner networks have inherent high insertion losses, which significantly increase with the number of channels [2]. A possible solution towards the efficient high power generation at mm-wave frequencies is the recently proposed multi-channel transition in [3], which directly interfaces an array of amplifiers to a single SIW via multiple closely separated microstrip lines (MLs), as illustrated in Fig. 1. This allows one to directly excite the spatially distributed TE10 SIW mode with high power. Since the output power is proportional to the number of input channels, it is important to investigate the scalability of such a structure.

## II. Scalability Study

The scalability of the structure will be examined with the help of an approximate impedance matching model. There are several definitions of the transmission line characteristic impedance, one of the most common are voltage-current and power-voltage [4]. For the quasi-TEM mode in a microstrip line (ML) all definitions converge to the same characteristic impedance (if pure TEM), i.e., one that is solely a function of the ML geometry and is frequency independent [4], [5].

Conversely, the characteristic impedance of the TE10 mode propagating in the SIW is not uniquely defined, however, the

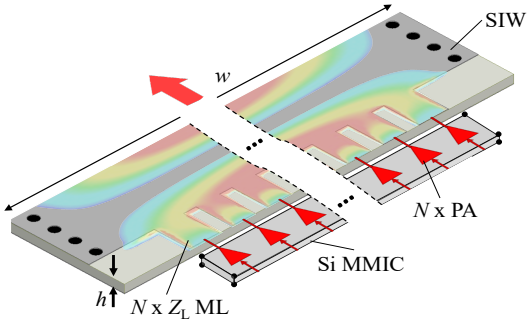



Fig. 1. Compact transition interfacing $N$ power amplifiers (possibly embedded in a single MMIC) to a single substrate integrated waveguide (SIW).

definitions differ by a scaling factor $k$ only:

$$Z_{\mathrm{TE10}} = k\frac{h}{w}\sqrt{\frac{\mu}{\epsilon}}\left(1-\frac{\lambda^2}{4w^2}\right)^{-1/2} \text{ where } \begin{cases} k=\frac{\pi}{2}, \text{ if V-I def.} \\ k=2, \text{ if P-V def.} \end{cases} \quad (1)$$

An impedance matching model of the parallel power combiner could to first order constitute a parallel connection of $N$ lines, each with an impedance $Z_{\mathrm{L}}$ connected to a common port. This implies that the equivalent impedance at this point is $Z_{\mathrm{L}}/N$. The obtained equivalent impedance should be equal to the characteristic impedance $Z_{\mathrm{TE10}}$ of the SIW TE10 mode to realize a good impedance match. Thus, increasing the number of channels demands decreasing the characteristic impedance. This could be done by increasing the SIW width $w$ or decreasing the height $h$. However, increasing $w$ might lead to the excitation of higher-order modes. Fig. 2 shows the estimated number of connected channels $N$ as a function of the ML impedance for different substrate thicknesses $h$. The upper bound of the filled areas corresponds to the maximum number of channels, geometrically limited by the SIW width (the spacing between the lines is assumed to be equal to the line width). The lower bounds are set by the optimal impedance matching criteria. As one can see, employment of a thin substrate and high ML impedance channels allow for interfacing more amplifiers to a single SIW, and hence significantly increase the output power as compared to a single channel transition [See Fig. 3]. Compactness of the proposed solution enables future on-chip realizations.

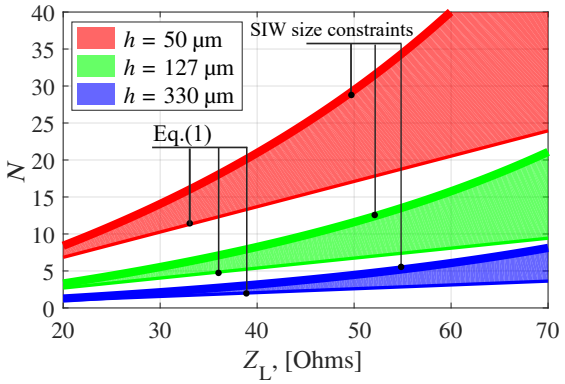



Fig. 2. Estimated number of the connected microstrip ports as a function of the port impedance for different substrate height values $h$.

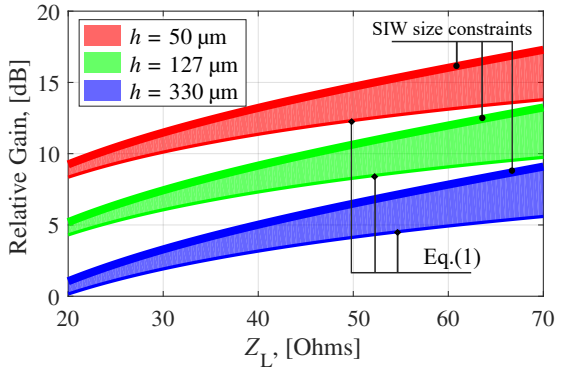
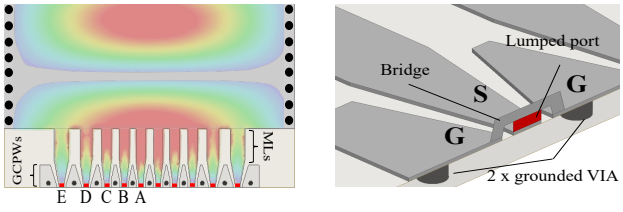



Fig. 3. Estimated relative gain of the proposed structure w.r.t. a single-channel case as a function of the microstrip port impedance for different substrate height values $h$.

## III. Numerical Results

To test the proposed scalability approach, a 10-way power combiner with 50 Ω coplanar waveguide (CPW) ports has been designed, as shown in Fig. 4. The port in Fig. 4(b) represents a ground-signal-ground chip interface. The employed SIW configuration is the same as the one used in [3], however the substrate thickness was reduced (from 254 μm to 127 μm) to interface more channels. The 10-way configuration was optimized to realize active impedance matching: the simulated SIW-port passive reflection coefficient $\Gamma_{\text{SIWport}}$ and active reflection coefficients $\Gamma_A$...$\Gamma_E$ of the CPW ports are below -15 dB and 10 dB, respectively, over more than 30% bandwidth, as shown in Fig. 5.




(a) (b)

Fig. 4. (a) Simulated E-field amplitude distribution in the 10-way power combiner with 50 Ω CPW input ports, when the input ports are uniformly excited at 31.5 GHz (real part); (b) The simulation model of the GSG port representing a chip interface.

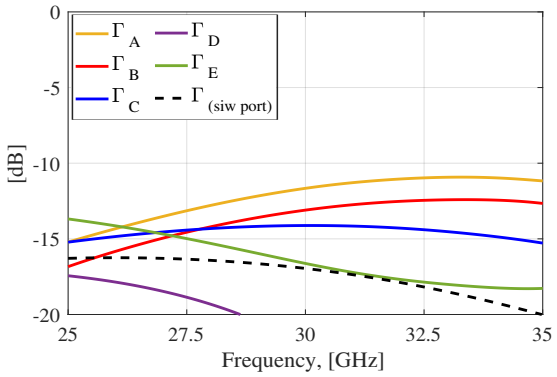



Fig. 5. Simulated active reflection coefficients of the 50-Ω CPW ports and SIW-port passive reflection coefficient (dashed) of the 10-way combiner, as shown in Fig. 4.

## Conclusions

The scalability of an array of $N$ microstrip lines interfaced to a single substrate integrated waveguide (SIW) has been studied. It was shown that employment of a thin substrate along with a high ML impedance allows to maximize the number of channels that can be interfaced to a single SIW, and hence significantly increase the output power. Compactness of the proposed solution enables its future on-chip realization, which is an important conclusion. The special case of a 10-way power combiner with 50-Ω co-planar waveguide (CPW) input ports is presented. The proposed configuration is optimized by minimizing the active reflection coefficient at each input port. The simulated active reflection coefficients of the CPW-ports and passive reflection coefficient at the wave port of the structure are better than -10 dB over more than 30% relative bandwidth (25–35 GHz). Numerical results validate the model and show that this configuration allows for efficient power combining from multiple amplifiers, and hence can generate 10× more power relative to a conventional single transition, while offering a larger bandwidth for a very low profile design.

The work is a part of the Silicon-based Ka-band massive MIMO antenna systems for new telecommunication services (SILIKA) project, funded by the European Unions Horizon 2020 research and innovation program under the Marie Sklodowska Curie grant agreement #721732.

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