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Exponential Modular Multilevel Converter for Low Voltage Applications

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Keywords

«Car Charger», «Cascaded», «dSPACE», «Electric vehicle», «Exponential Modular Multilevel Converter», «H-bridge», «MOSFET»; «Multi-level inverter», «Multilevel system».

Abstract

This paper presents the structure and control of a single phase Exponential Modular Multilevel Converter (EMMC), which works as a bidirectional AC/DC converter. In addition to the main H-bridge converter, it uses series connected H-bridges with DC link capacitors. The nominal voltage rating of the capacitors is increased with each module by factor of two. In this manner, the number of output voltage levels exponentially increases with the number of series connected H-bridges. By using low-voltage MOSFETs it is possible to achieve a very high efficiency, especially at partial loading. The high number of voltage levels reduces the output voltage THD, while using a low switching frequency. Thus, the required grid filter size can be substantially reduced. Furthermore, the additional capacitor modules increase the nominal output voltage at the AC side, so that the flow of the active and reactive power can be dynamically adjusted. Therefore, the EMMC could be used, for instance, as a vehicle charger directly connected to the grid.

Introduction

In recent years, multilevel converters have been receiving increasing attention throughout a wide range of applications [1], for example in power systems [2], transportation electrification [3, 4, 5, 6], energy generation/conversion, etc. In comparison to the conventional two-level converter, multilevel converters have several advantages, so that these can achieve a high system efficiency, resulting in an increased power density and a reliable system design. Several multilevel converter topologies can be found in literature as for example the Neutral Point Clamped converter (NPC) [7], the Modular Multilevel Converter (MMC) [8], the Flying Capacitor Converter [9] or the Modular Multilevel Series Parallel (MMSP) converter [10]. Using asymmetrical voltage levels can increase the number of output levels exponentially, which makes the charge balancing of the DC link sources quite challenging [11].

This paper introduces a cascaded H-bridge converter using one main module for the DC source and several series connected H-bridges with capacitors. The nominal voltage rating of each capacitor module is graded by factor of two, relative to the adjacent modules. This new topology is referred to as Exponential Modular Multilevel Converter (EMMC). Additionally, a control strategy to balance the capacitor voltages is briefly explained. This type of converter enables charging a 400 V vehicle battery, directly connected to the grid, while maintaining full control of the active and reactive power flow. Furthermore, the high number of output voltage levels reduces the required grid filter size, while keeping a low switching frequency. The main technical and economical aspects for the development of multilevel converters can be summarized as follows:

- Modular realization:
 - Operational redundancy in case of inverter switch faults
 - Independence of state of the art semiconductor power devices
 - Standard components
- Multilevel waveform:
 - Expandable to achieve very low voltage steps
 - Low total harmonic distortion (THD) of the output voltage [8]

Fundamentals of Exponential Modular Multilevel Converters (EMMC)

The following section describes the topology and the operational principle of the EMMC topology. A similar converter was presented in [12] using two single phase three-level NPC inverters with one additional capacitor H-bridge module.

Operation Principle of the EMMC

Including the main converter stage, which can also be realized by an NPC inverter, the EMMC consists of series connected H-bridge modules with capacitors. The possible switching states (1, 0, -1) of each individual H-bridge module are depicted in Fig. 1.

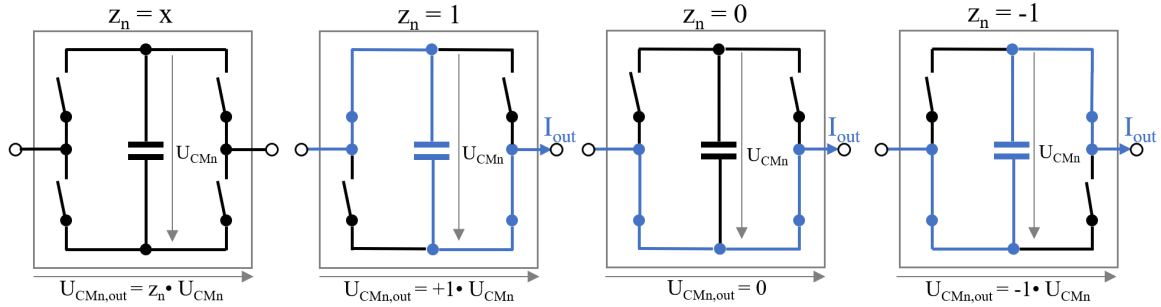


Fig. 1: Switching states of an H-bridge module: $z_n = +1$ of a H-bridge corresponds to a discharging, $z_n = -1$ to a charging and $z_n = 0$ to a bypassing of the capacitor with positive I_{out} .

Figure 2 illustrates one inverter leg or a single phase EMMC consisting of the main converter stage (MM) and 3 additional submodules (CMn). No additional external connections or energy transmission to the submodules CMn would be needed for full four-quadrant operation of the converter system. The chosen number of submodules is just an example and the number of submodules can easily be extended. To understand the basic concept, the submodules can be considered as constant voltage sources. Regardless of the sign of the output current i_{out} , each submodule can be bypassed or switched either into the corresponding phase in forward or reverse direction. To achieve the desired output voltage or a certain output

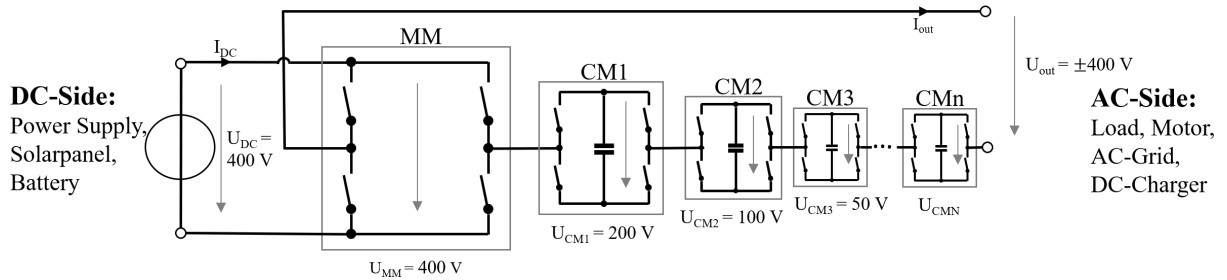


Fig. 2: EMMC with $U_{DC} = 400\text{ V}$ main module and 3 additional submodules.

voltage level, the sum of the modules' output voltages must be considered as

$$U_{out} = \sum_{n=1}^N z_n \cdot U_{DC} \cdot 2^{n-1} \quad (1)$$

Several switching combinations can be used to achieve a certain output voltage, whereas the number of redundant switching states changes with the output voltage. For example, all possible combinations to achieve an output voltage of $U_{out} = 50$ V are shown in Table I. Charging and discharging of the capacitors is also possible for all states of U_{out} until $|U_{out}| \leq U_{DC}$.

Table I: Possible combinations to represent $U_{out} = 50$ V or the first possible states for a 4 module configuration

Possibility	$z_1(400 \text{ V})$	$z_2(200 \text{ V})$	$z_3(100 \text{ V})$	$z_4(50 \text{ V})$	$U_{out} = \sum_{n=1}^4 z_n \cdot U_{DC} \cdot 2^{n-1} [\text{V}]$
1	0	0	0	1	50
2	0	0	1	-1	50
3	0	1	-1	-1	50
4	1	-1	-1	-1	50

This shows, that each capacitor module can be discharged ($z_n = 1$) or charged ($z_n = -1$) for a certain output voltage. Thus, the average output voltage level can be kept constant and the capacitors balanced for an infinite time by altering the switching states. Figure 3(a) shows the output voltage of the EMMC when loaded with a constant current. Furthermore, the module voltages and the used switching states

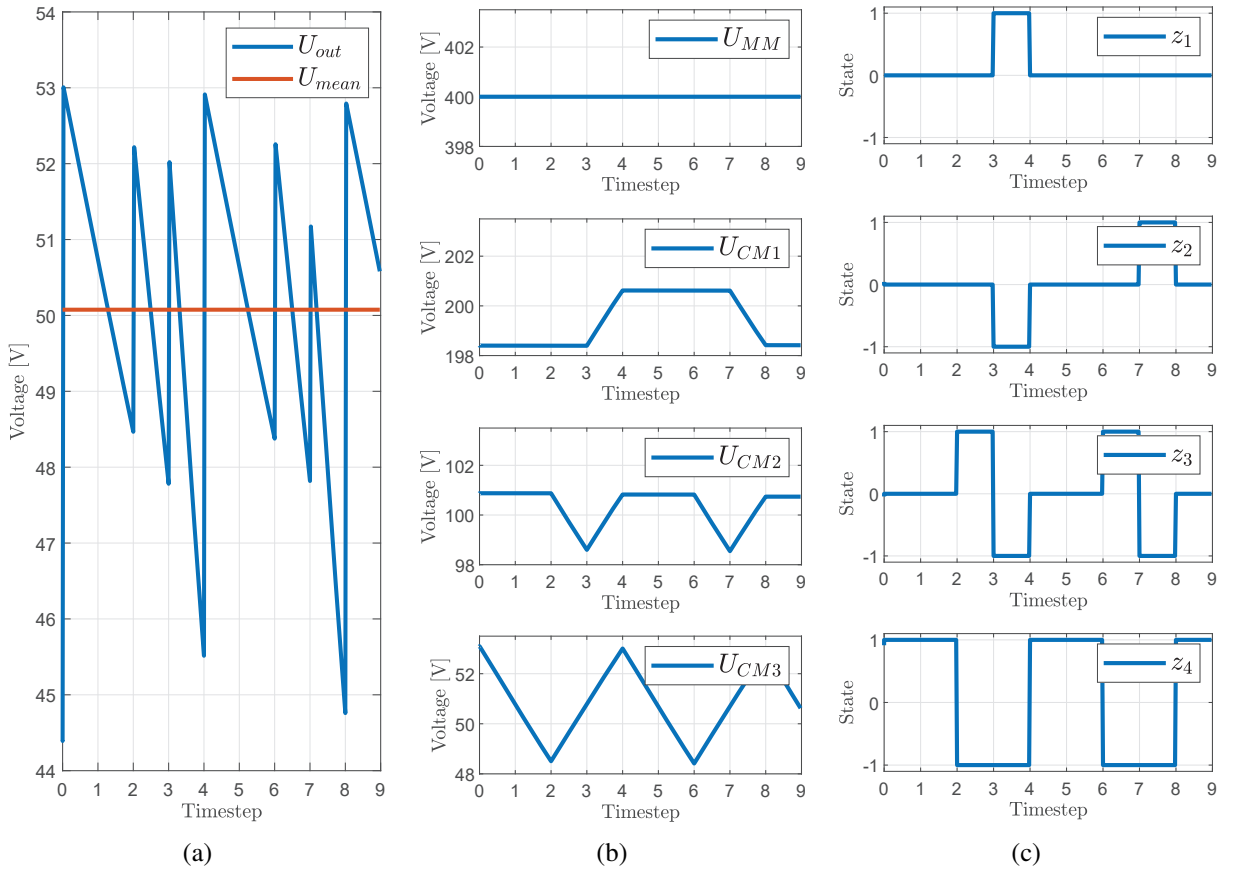


Fig. 3: (a) EMMC output voltage $U_{out} = 50$ V with equal capacitances ($88 \mu\text{F}$) on each module, a timestep size of $\frac{1}{50 \text{ kHz}} = 20 \mu\text{s}$ and an output current of $I_{out} = 5$ A. (b) Voltages of the individual modules at about nominal Voltage. (c) Switching states z_n of the modules to hold the nominal Voltage.

are depicted in Fig. 3(b) and 3(c), respectively. It can be seen, that the output voltage is kept at about 50 V by altering the switching states, charging and discharging the capacitors. It should be noted that the capacitor balancing must be executed with a several times higher control frequency than the output

voltage modulation frequency. The balancing of the voltages for an infinite time means that the quality of the output signal just depends on the capacitance/switching frequency (quality of holding a stage) and number of modules (high resolution).

Voltage Stage Height of the Output

The IEC61727 standard limits the harmonic current components and the current THD of grid connected converters. According to the IEC norm, the maximum current THD should be lower than 5.0% and the harmonic current components in the order of 3-9, 11-15, 17-21 and 23-33 should be limited to 4.0%, 2.0%, 1.5% and 0.6%, respectively.

Figure 4(a) depicts the output levels relative to the number of series modules for the EMMC and the H-bridge MMC. To compare the number of output voltage levels, the possible number of an MMC can be calculated as

$$n_{\text{MMC}} = N + 1 \quad (2)$$

and for an EMMC as

$$n_{\text{EMMC}} = 2^N + 1 \quad (3)$$

For a converter with four modules per phase ($N = 4$), the possible number of output levels for an MMC is $n_{\text{MMC}} = 5$, whereas the EMMC can achieve up to $n_{\text{EMMC}} = 17$ levels. This influences the output voltage THD. Therefore, the relationship between the number of series modules and the resulting voltage THD, using a pure resistive load, is shown in Fig. 4(b). Here, the capacitors are considered as constant voltage sources, which is of course only the case with extremely large capacitors. The output voltage of the converter is modulated using the fundamental switching technique nearest level control [13, 14]. From 4(b) it can be seen that voltage THD of the EMMC with a minimum stepsize of 50 V and four series modules is about 4.84%. Furthermore, 4(c) compares the normalized voltage harmonics with the IEC requirement on the current harmonics and it can be seen that the normalized voltage harmonics comply with the required normalized current harmonics. This, in turn, means that the current harmonics and the current THD of the EMMC fulfills the requirement of the IEC standard and, thus, the required grid filter theoretically becomes negligibly small (assuming a reasonable fundamental component). This conclusion assumes constant voltage sources in comparison to the capacitors being used, which have to be kept at a constant voltage through charging and discharging as shown in Fig. 3. It is also possible to build a overlapped PWM on the stairs to achieve a better THD with filtering, but without filtering just the stairs are resulting in a better THD.

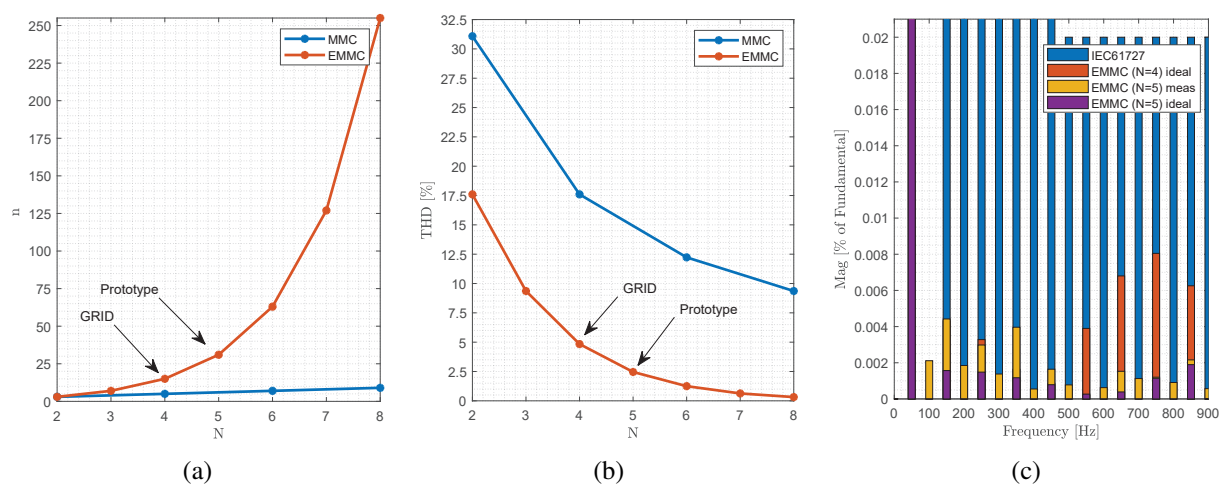


Fig. 4: (a) Voltage levels relative to the number of series modules. (b) Output voltage THD relative to the number of series modules. (c) Normalized output current harmonic components of the EMMC for ($N = 4$) and ($N = 5$), both idealized, and EMMC ($N = 5$) measurement of the real prototype ($P_{\text{out}} = 356 \text{ W}$), in comparison to the IEC61727 standard.

Voltage Balancing and Output Voltage Control

As mentioned before, each voltage level can be represented by different switching combinations, which gives the possibility to charge and discharge the capacitor modules depending on the current polarity. In order to simultaneously comply with the reference value of the output voltage U_{out} and the nominal voltages of the capacitor modules, the controller tries to minimize the voltage differences by selecting an optimal switching combination according to the weighting vector.

In order to select the most suitable combination, the voltage error vector must be calculated as

$$\Delta \vec{U}_{CMn} = \begin{pmatrix} u_{MM_{meas}} \\ u_{CM1_{meas}} \\ \vdots \\ u_{CM(n-1)_{meas}} \end{pmatrix} - \begin{pmatrix} u_{MM_{ref}} \\ u_{CM1_{ref}} \\ \vdots \\ u_{CM(n-1)_{ref}} \end{pmatrix} \quad (4)$$

With n , being the number of submodules per phase, and m , being the number of switching combinations for the i -th voltage level, all possible switching combinations can be gathered in the matrix M_i as

$$M_i = \begin{pmatrix} z_{11} & \cdots & z_{n1} \\ \vdots & \ddots & \vdots \\ z_{1m} & \cdots & z_{nm} \end{pmatrix} \quad (5)$$

Consequently, the weighting vector \tilde{g}_i can be calculated as

$$\tilde{g}_i = M_i \cdot \Delta \vec{U}_{CMn} \quad (6)$$

Thus, the effect of each switching combination on the global voltage error can be assessed. The switching combination achieving the most balancing effect is chosen from all switching combinations as

$$\max(\tilde{g}_i) \rightarrow z_{opt} \quad (7)$$

For example, if the reference output voltage level is set to $U_{out} = 50$ V and all capacitor modules show a voltage difference of about +1 V relative to their nominal rating, the weighting vector becomes

$$\tilde{g}_1 = M_1 \cdot \vec{U}_{CMn} = \begin{pmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & -1 \\ 0 & 1 & -1 & -1 \\ 1 & -1 & -1 & -1 \end{pmatrix} \cdot \begin{pmatrix} 0 \\ 1 \\ 1 \\ 1 \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ -1 \\ -3 \end{pmatrix} \quad (8)$$

From this weighting vector, the combination showing the best effect on the unbalance is chosen

$$g_{50V} = \max(g_{50V}) = 1 \rightarrow z_{opt} = (0 \ 0 \ 0 \ 1) \quad (9)$$

Since all capacitors have a surplus of charge, the combination discharging just one of them is chosen.

Proof of Concept

Simulation Results

Simulations were used to proof the concept's validity. Further, the capacitor sizing and the switching frequencies of the capacitor modules were tested. With respect to the built prototype, the DC voltage levels were chosen to comply with the IEC 60449 standard ($V_{DC} \leq 120$ V). In this manner, the concept of the system can be tested, while maintaining all safety requirements. Therefore, the before mentioned 400 V main module was down-scaled to 48 V. All series connected modules were down-scaled relative to the main module. Figure 5 shows the down-scaled system with five H-bridge modules.

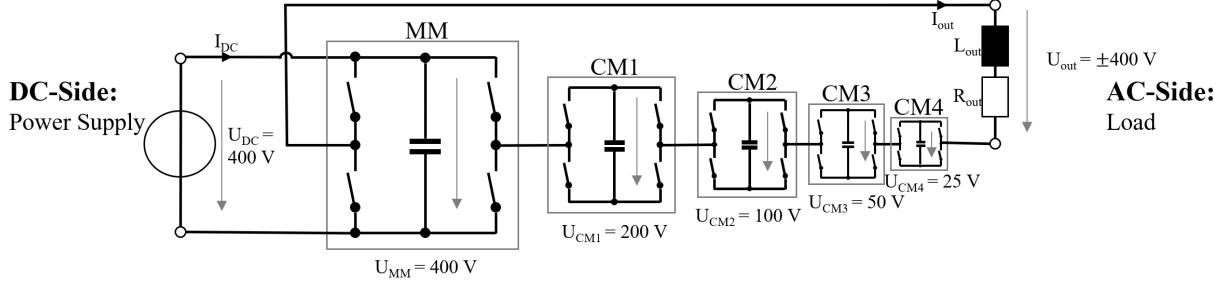


Fig. 5: Down-scaled EMMC with 48 V main module and four additional submodules.

Table II shows the basic configuration of the simulated EMMC and the down-scaled hardware setup, which was built. The capacitances are scaled by a factor of two in reverse order to the voltages of the modules. As a result, during quiescent state, the capacitors charge themselves to the proper voltages according to a capacitive voltage divider. This structure is reasonable, since the capacitor prices are relative to the energy density. This in turn means, that the low voltage capacitors are cheaper compared to the high voltage capacitors, despite having a higher capacitance rating. Table III shows the three

Table II: Voltages and capacitances of the grid connected EMMC (g) and the down-scaled version for simulation and demonstration purposes (s)

	MM_g	$CM1_g$	$CM2_g$	$CM3_g$	MM_s	$CM1_s$	$CM2_s$	$CM3_s$	$CM4_s$
$U_{Cn}[\text{V}]$	400	200	100	50	48	24	12	6	3
$C_{Cn}[\mu\text{F}]$	0.32	0.63	1.27	2.53	22	44	88	176	352

test cases and the obtained switching frequencies f of each individual module, which are determined by the controller using an update frequency of 50 kHz. Other possible test cases would be a different amplitude of the EMMC's sinusoidal output voltage. Here, the individual switching frequencies behave as expected, since these are increasing with the output current. This is due to the reason that a higher output current draws more charges from the capacitor modules. This results in a behavior comparable to a PWM, since the desired output voltage cannot be achieved directly. Figure 6 shows the EMMC's output voltages for different currents. Due to the load inductance L_{out} , the high voltage spikes are filtered out. Figure 6c shows the high fluctuations in the capacitor voltages. First ms of Fig. 6 shows how the

Table III: Simulation results of the EMMC prototype for a peak output voltage of 48V and an output frequency of 50Hz.

$U_{out}[\text{V}]$	$I_{out}[\text{A}]$	$P_{out}[\text{W}]$	$THD_U [\%]$	$THD_I [\%]$	$f_{MM}[\text{Hz}]$	$f_{CM1}[\text{Hz}]$	$f_{CM2} [\text{Hz}]$	$f_{CM3}[\text{Hz}]$	$f_{CM4} [\text{Hz}]$
33.97	0.38	12	2.49	2.47	7301	11802	12534	12032	8955
33.90	4.80	115	3.79	3.24	8851	14136	15282	13852	9681
33.80	11.28	381	10.53	5.97	9052	13912	14387	13484	9633

individual capacitors charge at the start up of the EMMC without precharging. This charging process can probably even happen connected to the grid. It can also be seen from simulations that higher currents lead to a worse sinus. Because the capacitor voltages vary more. However, it is still possible for the EMMC to build an sinus, even with a load current of $I_{out} = 11.28 \text{ A}$ which corresponds to a output power $P_{out} = 381 \text{ W}$ that would be in a real grid converter ($U_{DC} = 400 \text{ V}$) 2530 W.

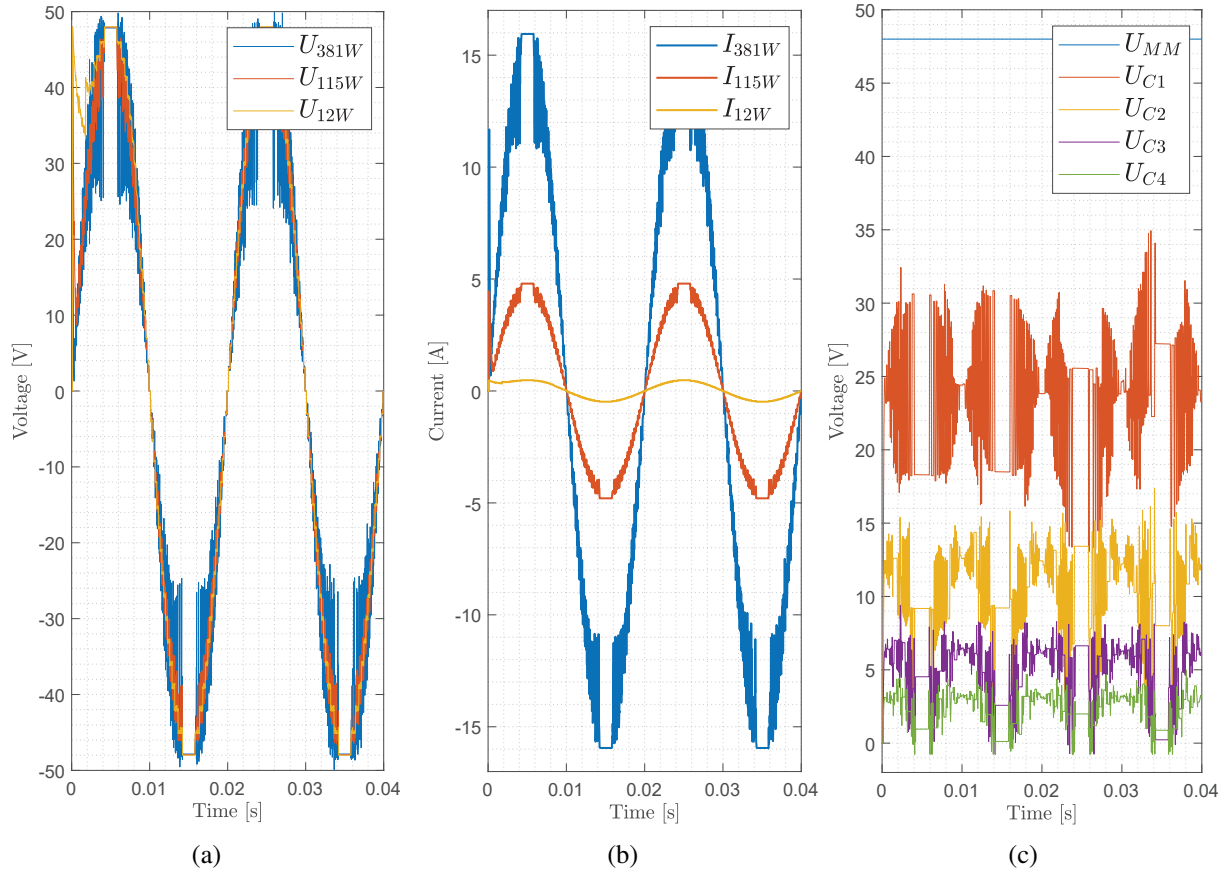


Fig. 6: (a) Effects of different currents on the quality of the prototype's output voltage $U_{out} = 48$ V. (b) Output currents for a load resistance of 3Ω , 10Ω and 100Ω . (c) Individual voltages of the capacitors for $R_{out} = 3 \Omega$.

Experimental Setup

Based on the data obtained by the simulations, an experimental setup was developed. An HDO6104 Oscilloscope (1 GHz and 2.5 GS/s) and four high-voltage differential probes of the type BumbleBee from PKM (bandwidth of 400 MHz, PKM GmbH, Germany) are used for the measurements. The control algorithm for the EMMC was developed in MATLAB/Simulink 2016a (MathWorks Inc., Natick, USA) and implemented on a dSpace MicroLabBox controller (dSPACE GmbH, Paderborn, Germany). The outputs of the switching signals are synchronized with the FPGA, included in the MicroLabBox. The EMMC prototype is based on MOSFETs (Infineon IPT012N08N5 [15]), isolated half-bridge gate drivers (Silicon Labs SI8233 [16]) and ceramic capacitors (X7S ceramic capacitor). To realize 15 isolated power supplies for the gate drivers, which are necessary for this prototype, a PCB-based planar transformer is used [17]. The built prototype has the same voltage and capacitance ratings as shown in Fig. 5. Figure 7 schematically depicts the experimental setup, including the controller interface and the data acquisition. If the EMMC should feed the grid, the voltages and capacitors would have to be selected as shown in Table V.

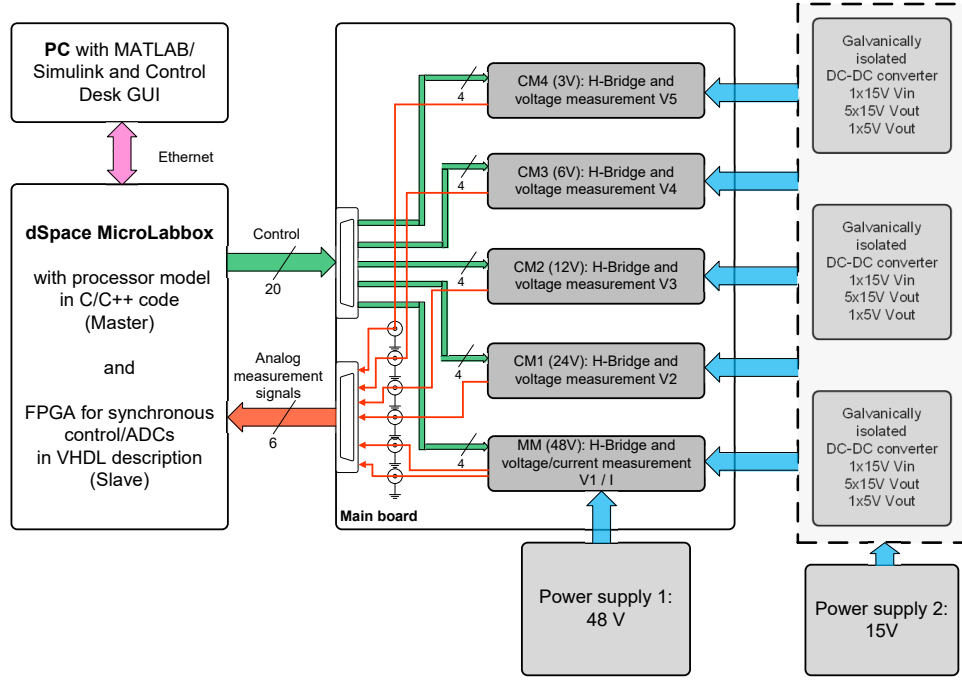


Fig. 7: System overview of the individual components of the down-scaled prototype.

The control algorithm is implemented on the dSpace system (MicroLabBox), which can be monitored and controlled from a PC via the Control Desk software. From the measured voltages and the nominal voltage curve, the MicroLabBox determines the next switching signals for the five modules of the EMMC. Only the largest module ($U_{MM} = 48 \text{ V}$) is supplied by a power supply unit and the other modules are recharged and balanced by the control algorithm. Three galvanically isolated DC-DC converters are used to supply the MOSFET-Drivers with the necessary 15 V and the logic components with the necessary 5 V. These DC-DC converters are powered by an additional power supply. In a later version of the EMMC it should be possible to power the individual modules from the capacitors.

Figure 8 shows the obtained measurements. The reference output voltage is set to $U_{out} = 33 \text{ V}$, while the resistance R_{out} is varied between 100Ω , 10Ω and 3Ω . The corresponding output inductance was estimated as seen in Table V. It can be seen that the output voltage U_{out} contains some noise due to the switching events. This is also due to the different turn-on/turn-off delays and the variation of the switching time instants of the used MOSFETs. This can be optimized with an FPGA. The obtained switching frequencies are shown in Table IV. The control algorithm behaves slightly different in comparison to the simulations, because of the voltage measurement of the modules. This leads to a higher switching frequency of the individual modules than predicted by the simulation. As a consequence, the capacitor voltages U_{Cn} are quite well balanced in comparison to the simulations, as can be seen in Fig. 8c. However, the output voltage U_{out} contains voltage spikes due to the overshoots caused by the switching events.

Table IV: Measurement results of the EMMC prototype for a peak output voltage of 48 V and an output frequency of 50 Hz.

$U_{out} [\text{V}]$	$I_{out} [\text{A}]$	$P_{out} [\text{W}]$	$THD_U [\%]$	$THD_I [\%]$	$f_{MM} [\text{Hz}]$	$f_{CM1} [\text{Hz}]$	$f_{CM2} [\text{Hz}]$	$f_{CM3} [\text{Hz}]$	$f_{CM4} [\text{Hz}]$
32.41	11.00	356	6.09	6.08	13032	21164	20438	19585	12765
33.18	3.35	111	5.68	5.64	14025	22055	26287	18714	12246
33.81	0.36	12	5.73	5.67	19818	22636	22266	18357	11367

The EMMC prototype, without the control unit, can be seen in Fig. 9a. The individual modules are

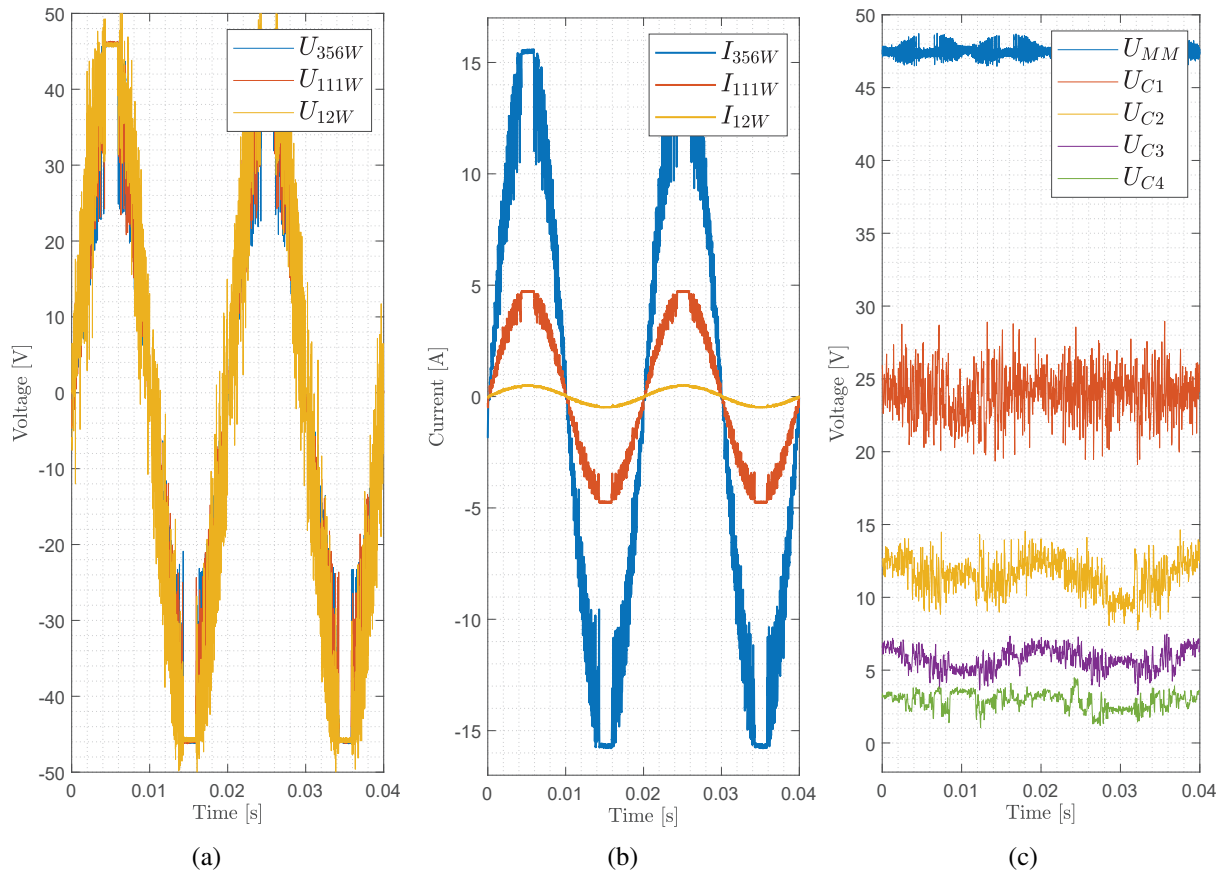


Fig. 8: (a) Effects of different loads on the quality of $U_{out} = 33$ V RMS output voltage in real hardware (b) Currents at different P_{out} 381 W, 111 W and 12 W (c) The right image shows how the individual voltages of the capacitors in the full bridge behave with $P_{out} = 381$ W

mounted on the mainboard, as can be seen on the right of the figure. This system was developed, so that defect modules can be quickly replaced. Next to the mainboard, the necessary DC/DC converters are connected. In the future, all auxiliary components should be integrated on the main PCB. The entire experimental setup including additional power supplies, the MicoLabBox, EMMC, oscilloscope, load resistor, probes and PC is shown on Fig. 9b.

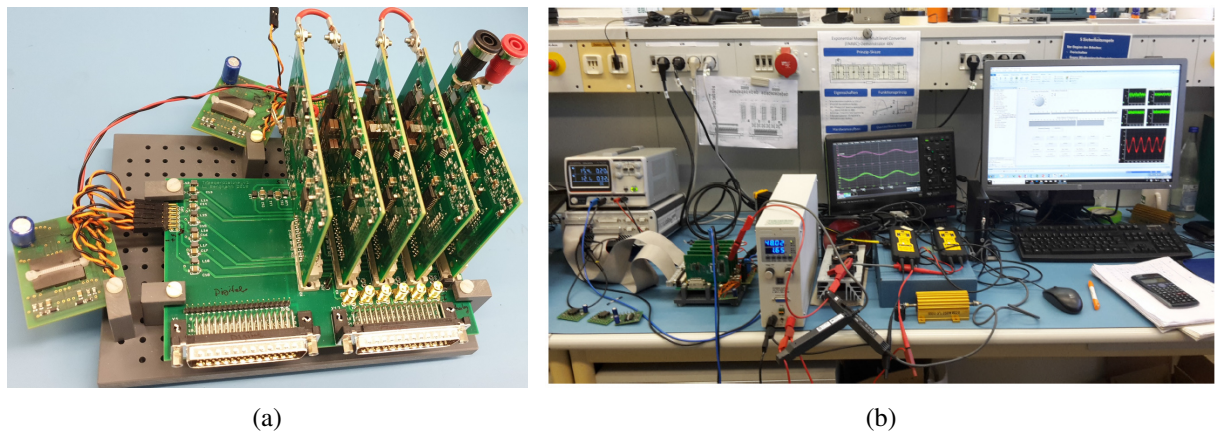


Fig. 9: (a) Detail picture of the prototype with mainboard and 5 power modules. (b) Complete workspace with prototype, measurement tools, etc.

The measured efficiency results can be seen in Table V. The measured peak efficiency of the down-scaled system was 97.5 %. The output power could have been increased further by using active cooling for the load resistance.

Table V: Different R_{out} and the corresponding Input Power P_{DC} , Supply Power P_{sup} and the Output Power P_{out} of the EMMC and the resulting overall efficiency of the prototype

U_{out} [V]	I_{out} [A]	R_{out} [Ω]	L_{out} [μ H]	P_{DC} [W]	P_{sup} [W]	P_{out} [W]	η
32.41	11.00	3	0.42	362.90	2.47	356.51	97.5%
33.18	3.35	10	0.12	112.30	2.58	111.15	96.7
33.81	0.36	100	0.10	11.84	2.75	12.17	79.7

Conclusion

This paper introduced the topology of the Exponential Modular Multilevel Converter (EMMC) and its relevant characteristics. It is possible to generate a much larger number of output voltage levels than with the conventional multilevel converter and the proposed control scheme is well suited for a different number of voltage levels. It has been shown that the control scheme allows to control the output phase-voltage and to balance the capacitor voltages, while achieving a low output voltage THD. Simulations and an experimental setup have demonstrated a good performance of the EMMC concept. Therefore, the EMMC could minimize the required grid filter size, when working as a grid connected converter. To make further analysis, a three-phase 11 kW EMMC is being built.

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