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Effects of Self-Heating on f_T and f_{max} Performance of Graphene Field-Effect Transistors

Marlene Bonmann, Marijana Krivic, Xinxin Yang, Andrei Vorobiev, *Member, IEEE*, Luca Banszerus, Christoph Stampfer, Martin Otto, Daniel Neumaier, and Jan Stake, *Senior Member, IEEE*

***Abstract*— It has been shown that there can be a significant temperature increase in graphene field-effect transistors (GFETs) operating under high drain bias, which is required for power gain. However, the possible effects of self-heating on the high-frequency performance of GFETs have been weakly addressed so far. In this work, we report on a experimental and theoretical study of the effects of self-heating on dc and high-frequency performance of GFETs by introducing a method that allows accurate evaluation of the effective channel temperature of GFETs with a submicron gate length. In the method, theoretical expressions for the transit frequency (f_T) and maximum frequency of oscillation (f_{max}) based on the small-signal equivalent circuit parameters are used in combination with models of the field and temperature-dependent charge carrier concentration, velocity and saturation velocity of GFETs. The thermal resistances found by our method are in good agreement with those obtained by solution of the Laplace equation, and by the method of thermo-sensitive electrical parameters. Our experiments and modeling indicate that self-heating can significantly degrade the f_T and f_{max} of GFETs at power densities above 1 mW/μm^2, from approximately 25 GHz to 20 GHz. This work provides valuable insights for further development of GFETs, taking into account self-heating effects on the high-frequency performance.**

***Index Terms*— field-effect transistors, graphene, microwave amplifiers, self-heating, thermal resistances**

I. Introduction

The implementation of the fairly new class of 2D materials, such as graphene [1] and MoS_2 [2], opens up opportunities for new device concepts within electronics and optoelectronics [3], [4]. Among the 2D materials graphene is considered as a promising new channel material for advanced high-frequency field-effect transistors due to its intrinsically high charge carrier mobility and saturation velocity [5]–[7]. Recently, graphene field-effect transistors (GFETs) with state-of-the-art extrinsic transit frequency $f_T = 34$ GHz and maximum frequency of oscillation $f_{max} = 37$ GHz at the gate length $L_g = 0.5\,\mu$m have been demonstrated [8]. These values of f_T and f_{max} are already comparable to those of the best reported Si MOSFETs, but still well below the III-V HEMTs [9]–[11]. It is well recognized that the development of GFETs, operating in the amplifying mode, i.e. with high f_{max}, is challenging due to relatively high drain conductance [12]. Additional degradation is possible due to Joule heating, i.e., self-heating, as it has been reported for other high-frequency devices, such as III-V HEMTs [13], [14], and Schottky and heterostructure-barrier-varactor diodes [15], [16]. A considerable increase in temperature, up to several hundred Kelvin, in a graphene sheet on a SiO_2/Si substrate has been shown via infrared microscopy and Raman spectroscopy at power densities above 0.1 mW/μm^2 [17], [18]. These power densities are typical for GFETs being developed for current and power amplification applications [8], [19]. This underlines the importance of taking into account the effects of self-heating in practical circuit applications such as GFET mixers and amplifiers [8], [20]–[22], device modeling [23] and optimization of the high-frequency performance, including the gain and noise performance [24]. Dc characteristics and the effect of self-heating on it have been studied theoretically and experimentally [17], [25]–[27]. However, to the best of our knowledge, there are no reported systematic theoretical or experimental studies addressing the effects of self-heating, and/or external heating on the high frequency performance, i.e., f_T and f_{max}, of GFETs with submicron gate length.

In this work, we provide a theoretical and experimental study of the effects of self-heating and external heating on dc and high-frequency performance of GFETs. In contrast to the test structures used in previous temperature studies, the GFETs considered in this work have the design and layout that are practical for advanced high-frequency amplifier applications, as presented in [8]. Theoretical models that have been developed for other device technologies are not applicable, because they either require the knowledge of the thermal conductivities [13] which is in the case of graphene hard to access [28], or technology specific temperature-dependent current-voltage dependencies [29]. Therefore, we develop a

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M. Bonmann, M. Krivic, X. Yang, A. Vorobiev, and J. Stake are with the Terahertz and Millimetre Wave Laboratory, Department of Microtechnology and Nanoscience, SE-412 96 Gothenburg, Sweden. (e-mail: marbonm@chalmers.se.)

A. Generalov is now with Aalto University, Helsinki, Finland.

L. Banszerus, and C. Stampfer are with the 2nd Institute of Physics, RWTH Aachen University, 52074 Aachen, Germany.

M. Otto, and D. Neumaier are with the Advanced Microelectronic Center Aachen, AMO GmbH, 52074 Aachen, Germany.

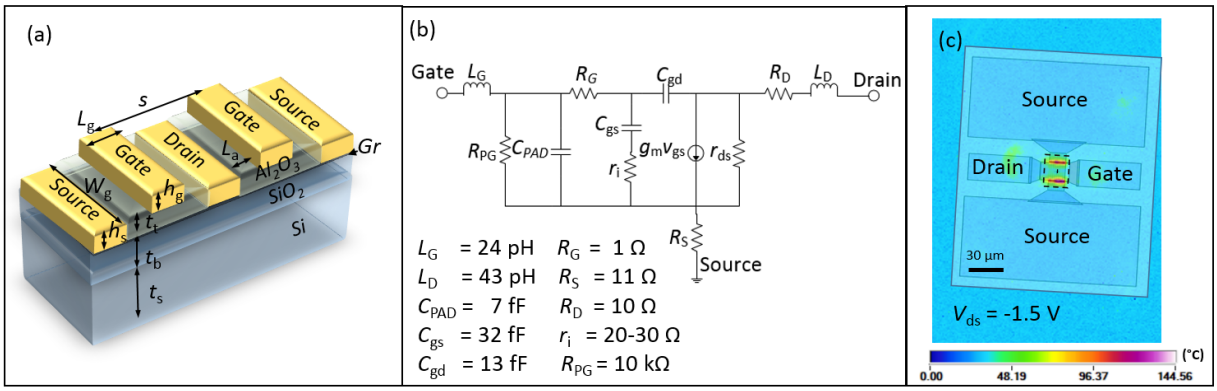

Fig. 1. (a) Device structure of the GFET. The GFET has two gate fingers with gate length $L_g = 0.5\,\mu$m and a total gate width of $W_g = 2 \cdot 15\mu$m. s is the separation between the gates, and $L_a = 0.1\,\mu$m is the ungated access length. The top oxide is $t_t = 18$ nm thick Al_2O_3. h_s =1 nm Ti+15 nm Pd+250 nm Au and h_g =10 nm Ti+290 nm Au, are the source and gate metal heights, respectively. The substrate is t_s=300 μm thick Si with t_b =1 μm thick SiO_2 on top. (b) The small-signal equivalent circuit of the GFET with extracted parameter values. (c) Infrared image of a GFET at $V_{gs} = 1.5$ V and $V_{ds} = -1.5$ V. The gate, drain and source pads of the transistor are labeled and the dashed square indicates the GFET area shown in (a).

method for evaluation of the effective GFET channel temperature using measured dependencies of f_T and f_{max} on the drain voltage, i.e., dissipated power densities, and at different external temperatures. For this purpose, theoretical expressions for f_T and f_{max} based on small-signal equivalent circuit parameters are used in combination with models of the field-dependent carrier velocity, and the temperature-dependent and charge carrier concentration-dependent mobility and saturation velocity of GFETs. In contrast to pulsed IV studies, which are usually employed to investigate thermal effects, all velocity saturation effects, such as optical phonon and remote optical phonon scattering, are included and can be studied under the real application conditions in this study [30].

We verify our method by comparing the values of the thermal resistance found by our method, by employing a thermal-resistance model based on the solution of Laplace equation [14] and by thermo-sensitive electrical parameters, i.e., the gate leakage current [31]. This work provides valuable insights for further device optimization considering the heating effects, enabling the development of GFETs for high-frequency applications.

II. Method

In the following, we introduce a new method for evaluating the field-effect transistor effective channel temperature using the measured values of the drain-source current (I_{ds}), f_T and f_{max}. The method allows us to analyze effects of self-heating and external heating on f_T and f_{max}, on the output conductance g_{ds}, on the effective charge carrier concentration n, on the effective velocity v, on the saturation velocity v_{sat}, and on the charge carrier mobility μ. Measurements are based on two-finger top-gated GFETs presented in [8] with L_g=0.5 μm and $W_g = 2 \cdot 15\,\mu$m, and the ungated access length $L_a = 0.1\,\mu$m. The top-dielectric is a $t_t = 18$ nm thick Al_2O_3 layer with relative permittivity $\epsilon_t = 7.5$, and the substrate is 1 μm/300 μm SiO_2/high resistive Si. The device structure is shown in Fig. 1(a). The properties are assumed to be interchangeable for the gate fingers, i.e., not affected by possible variations during fabrication.

A. Measurements

We used three different methods and cooresponding set-ups for the measurements.

In the first set-up a QFI InfraScope was used to demonstrate self-heating of the GFET, while using a dual-channel Keithley Source Meter 2604B for biasing between the source-gate and source-drain contact. The connection to the GFET is made with ground-signal-ground dc probes. A reference measurement with an unpowered device at a QFI InfraScope stage temperature of 60 C° is conducted to attribute for different emissivity of the different materials on the device sample surface (gold, silicon oxide). Then the temperature is measured under different bias conditions.

In the second set-up, S-parameters were measured using an Agilent E8361A VNA, together with a Keithley Source Meter 2604B for biasing and a Temptronic ThermoChuck for controlling the temperature of the sample holder. The connection to the GFET is made with ground-signal-ground rf probes. Calibration at the rf probe tips is performed with a standard calibration substrate. The temperature was swept from room temperature (RT) up to 100 °C and at each temperature the bias between source and drain was swept from $V_{ds} = 0$ to -1.4 V and the source-gate bias is kept at V_{gs}=-1 V as optimal bias for highest measured f_T and f_{max}. For each bias point, the measurements are delayed for 30 s to ensure measurement conditions that do not incur fast charging effects of traps in the gate oxide [32]–[34].

S-parameters were measured in the frequency range of 1-50 GHz and were used to calculate the small-signal current gain (h_{21}) and the unilateral power gain (U) [35], [36]. f_T and f_{max} are defined as the frequencies at which the magnitudes of h_{21} and U, respectively, have decreased to 0 dB.

In the third set-up, IV-measurements were conducted with a Cascade Summit 12000 probe station with a Temptronic ThermoChuck System and an Agilent B1500A semiconductor

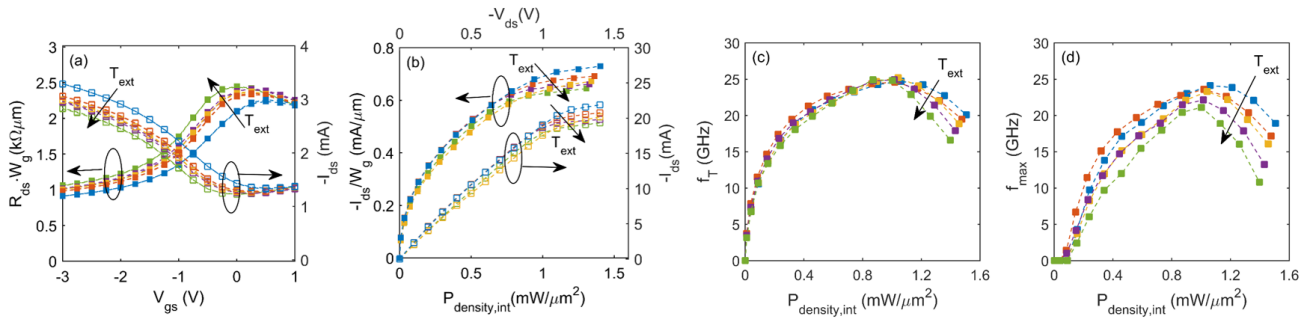

Fig. 2. (a) Normalised drain resistance curves ($\boldsymbol{R_{ds}} \cdot \boldsymbol{W_g}$) versus gate voltage $\boldsymbol{V_{gs}}$, together with the corresponding transfer curves at $\boldsymbol{V_{ds}} = \boldsymbol{-0.1}$ V. (b) Normalised drain current ($\boldsymbol{I_{ds}}/\boldsymbol{W_g}$) at $\boldsymbol{V_{gs}} = \boldsymbol{-1}$V versus intrinsic power density $\boldsymbol{P_{density,int}}$, together with the corresponding output characteristics. (c) Transit frequency $\boldsymbol{f_T}$ and (d) maximum frequency of oscillation $\boldsymbol{f_{max}}$ versus $\boldsymbol{P_{density,int}}$. The arrows indicates external temperatures from $\boldsymbol{T_{ext}}$=60, 70, 80, 90, and 100 °C.

analyzer. For this measurements, dc probes were used and connected to one gate finger at a time. The external chuck temperature and the dc bias were swept in the same way as in the second set-up.

B. Parameter extraction

First, the output conductance g_{ds} is estimated by using the measured values of f_T and f_{max} and the equations for f_T and f_{max} based on small-signal equivalent circuit parameters of the equivalent circuit shown in Fig. 1(b) [37], [38]:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \frac{1}{1+g_{ds}R_C+\frac{C_{gd}g_mR_C}{C_{gs}+C_{gd}}+\frac{C_{PAD}}{C_{gs}+C_{gd}}}, \quad (1)$$

$$f_{max} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}(r_i+R_S+R_G)+g_mR_G\frac{C_{gd}}{C_{gs}}}}, \quad (2)$$

where C_{gs} and C_{gd} are the gate-source and gate-drain capacitances, C_{PAD} is the parasitic pad capacitance and $C_{ox} = \epsilon_t/t_t$ is the oxide capacitance per unit area, r_i is the charging resistance, and R_D=R_S=$R_C/2$ are the drain/source resistances, where R_S and R_D consist of the metal-graphene contact resistance and the resistance of the ungated channel access length L_a of the graphene channel. The contact resistance R_C is found from fitting the drain-source resistance model to the measured drain-source resistance [39] and changes in the range of 20-23 Ω with temperature varying in the range of 60-100 °C. The other small-signal parameters are found from fitting of the small-signal equivalent circuit model to the measured S-parameters and are summarized in Fig. 2(b). In contrast to semiconductor MOSFETs, the capacitances C_{gs} and C_{gd} of GFETs are not significantly changing with V_{ds}, due to the lack of a bandgap in graphene which prevents the formation of a depletion region at the drain, and can be considered constant within the studied bias range. The capacitance values can be taken from [8] as $C_{PAD} = 7$ fF, and $C_{gs} \approx 0.5C_{ox}L_gW_g$ and $C_{gd} \approx 0.2C_{ox}L_gW_g$. The value $r_i \approx 1/(3 \cdot g_m)$ is the charging resistance of the gate-source capacitance [37].

To obtain g_{ds}, (1) is rewritten to solve for g_m and substituted into (2), which is then solved for g_{ds}.

Second, the found g_{ds} is used to calculate g_m.

Third, the effective charge carrier velocity v is estimated using (3):

$$v = \frac{g_m \cdot L_g}{C_{gs}+C_{gd}}. \quad (3)$$

Equation 3 is derived from the expression for the intrinsic transit frequency $f_{T,int} = g_m/(2\pi C_{gs}) = v/(2\pi L_g)$ [37], with the difference that C_{gd} needs to be included since GFETs exhibit no real depletion region in the channel [40]. Fourth, knowing the effective charge carrier velocity allows estimating the effective charge carrier concentration n using the measured drain current I_{ds} and the relation:

$$n = \frac{I_{ds}}{q \cdot W_g \cdot v}. \quad (4)$$

In the last step, the field-dependent velocity model [41]:

$$v' = \frac{\mu \cdot E_{ds,int}}{(1+(\frac{\mu \cdot E_{ds,int}}{v_{sat}})^{\gamma})^{\frac{1}{\gamma}}}, \quad (5)$$

is used together with the temperature- and charge carrier concentration-dependent saturation velocity v_{sat} [27]:

$$v_{sat}(n,T) = \frac{2}{\pi}\frac{\omega_{OP}}{\sqrt{\pi \cdot n}}\sqrt{1-\frac{\omega_{OP}^2}{4\pi \cdot n v_F^2}}\frac{1}{N_{OP}+1} \quad (6)$$

and temperature- and charge carrier concentration-dependent low-field mobility μ [27]:

$$\mu(n,T) = \frac{\mu_0}{1+(n/n_{ref})^{\alpha}} \cdot \frac{1}{1+(T/T_{ref}-1)^{\beta}}. \quad (7)$$

to solve for the channel temperature T at $v = v'$. $E_{ds,int} = (V_{ds} - R_C \cdot I_{ds})/L_g$ is the intrinsic electric field and $\gamma = 3$ is a model parameter, $N_{OP} = 1/[exp(\hbar\omega_{OP}/k_BT) - 1]$ is the phonon occupation, $\hbar\omega_{OP} \approx 81$ eV the optical phonon energy, $\mu_0 = 0.17\,m^2/Vs$ is the low-field mobility found from fitting the drain-source resistance model [39] to the measured drain-source resistance, and the parameters $n_{ref} = 1.1 \cdot 10^{13}\,cm^{-2}$, $T_{ref} = 250$ K, $\alpha = 2.2$, and $\beta = 3$ [27]. The analysis of the results below focuses on the bias range $V_{ds} = -0.5$ to -1.4 V since (7) is limited to $n > 2 \cdot 10^{16} m^{-2}$ [27].

The derivative of the found temperature T with respect to the intrinsic dissipated power $P_{int} = P_{density,int} \cdot L_g \cdot W_g = (V_{ds} - R_C I_{ds}) \cdot I_{ds}$ is used to estimate the thermal resistance R_{th} of the GFETs.

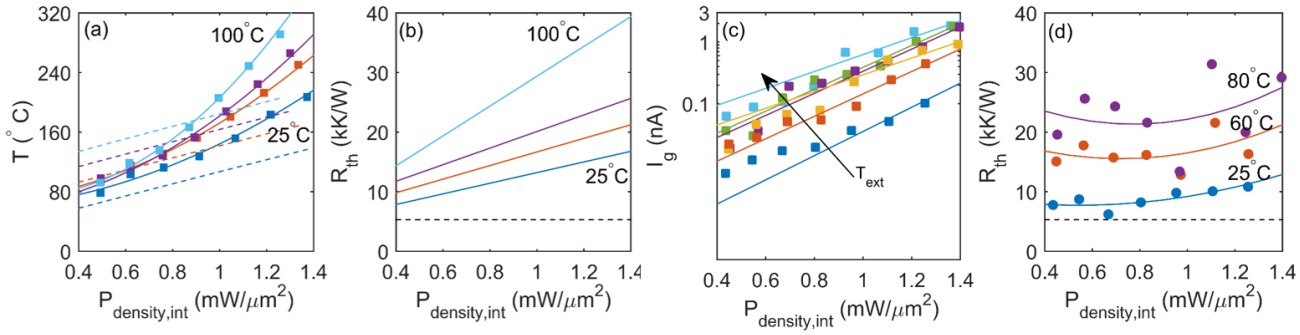

Fig. 3. (a) The effective channel temperature $\boldsymbol{T}$ derived using (1-7) (symbols) versus intrinsic dissipated power density $\boldsymbol{P}_{\text{density,int}}$ (corresponds to $\boldsymbol{V}_{\text{ds}}$ in the range -0.3 to -1.4 V) at external temperatures $\boldsymbol{T}_{\text{ext}}$=25, 60, 80 and 100 °C. The lines are polynomial fitting curves. The temperatures calculated by the thermal-resistance model (dashed lines) [14] are also shown. (b) Thermal resistance $\boldsymbol{R}_{\text{th}}$ versus intrinsic dissipated power density $\boldsymbol{P}_{\text{density,int}}$ estimated as derivative of the polynomial fit in (a) and estimated by the thermal-resistance model (dashed line). (c) Gate leakage current $\boldsymbol{I}_{\text{g}}$ versus $\boldsymbol{P}_{\text{density,int}}$ and $\boldsymbol{T}_{\text{ext}}$ ranging from 25 °C to 100 °C. (d) $\boldsymbol{R}_{\text{th}}$ versus $\boldsymbol{P}_{\text{density,int}}$ estimated by the method of thermo-sensitive electrical parameters (circles) with polynomial fitting curves (solid lines).

Additionally, the method of thermo-sensitive electrical parameters (TSEP) is used to estimate R_{th}. The TSEP method relies on the thermal dependence of electrical properties, such as the threshold voltage and saturation current, to estimate the temperature of semiconductor devices where the channel is not accessible by direct temperature measurement methods [31]. In this work, we employ the temperature dependence of the gate leakage current (I_{g}). Fig. 2(c) shows that I_{g} increases exponentially with $P_{\text{density,int}}$ and T_{ext} due to external heating and self-heating in agreement with the most probable conduction mechanisms, such as Poole-Frenkel transport mechanism and the field-enhanced Schottky mechanism [42]. R_{th} is found based on the differential of the gate leakage current I_{g} with respect to P_{int} and the temperature T as $R_{\text{th}} = (\partial I_{\text{g}}/\partial P_{\text{int}}) \cdot (\partial T/\partial I_{\text{g}})$. For $P_{\text{density,int}}$ below 0.4 mW/μm^2 the leakage current is too small to observe a significant change in I_{g} with changing $P_{\text{density,int}}$ or T_{ext}. The estimate of R_{th} analyzed below is evaluated for $P_{\text{density,int}} > 0.4$ mW/μm^2.

Furthermore, we calculated R_{th} by an analytical thermal-resistance model [14].

Finally, we analyze the potential performance of GFETs assuming that there is no degrading due to self-heating by using the charge carrier concentration found from measurements and then estimating v' using (7), (6), and (5) at different external temperatures. Knowing v and n allows us to calculate I_{ds} as:

$$I_{\text{ds}} = q \cdot W_{\text{g}} \cdot v' \cdot n, \tag{8}$$

and g_{m} using (3). Since, in this case, I_{ds} is not affected by self-heating at high fields, we can estimate g_{ds} as the derivative I_{ds} with respect to the intrinsic drain-source voltage $V_{\text{ds,int}} = V_{\text{ds}} - R_{\text{C}} I_{\text{ds}}$ as:

$$g_{\text{ds}} = \frac{\partial I_{\text{ds}}}{\partial V_{\text{ds,int}}}|_{V_{\text{gs}}=const.} \tag{9}$$

Then, f_{T} and f_{max} are calculated using (1) and (2), respectively.

III. Results and Discussion

Investigation of the GFETs by IR microscopy shows clearly that the temperature in the channel region increases with drain bias, as seen in Fig. 1(c). Since the top oxide layer and metal layer are very thin, the temperature on the top of the gate metal can be assumed to be the same as in the channel. However, we can assume that the IR microscope underestimates the real channel temperature, due to resolution limitations of approximately 1.6 μm per pixel which is larger than $L_{\text{g}} = 0.5\,\mu$m.

Fig. 2 shows the measured drain-source resistance divided by the gate width and the drain current divided by the gate width as well as f_{T} and f_{max} versus the intrinsic dissipated power density at different external temperatures of T_{ext}= 60, 70, 80, 90, and 100 °C. It can be seen from Fig. 2(a) that the voltage for minimal conductance, e.g. the Dirac voltage (V_{Dir}) shifts with the measurements which can be explained by charge carrier detrapping [34]. Detrapping is a thermally activated process leading to the release of more electrons from traps with increasing temperature supported by the negative bias at the gate. This leads to the observed shift from positive V_{Dir} for the first few measurement sweeps to $V_{\text{Dir}} \approx 0$ V. The resistance is larger at higher external temperatures. This can be associated with a decrease of the low-field mobility with higher temperature (eq. 7), but also with the charge detrapping from the oxide, which leads to a reduction of the residual charge carrier concentration, which originates from charge inhomogeneities in the channel. Additionally, the contact resistance increases slightly from 20 Ω to 23 Ω.

Fig. 2(b) shows that the drain-source current I_{ds} is saturating at intrinsic power densities $P_{\text{density,int}} = (V_{\text{ds}} - R_{\text{C}} \cdot I_{\text{ds}}) \cdot I_{\text{ds}}/(L_{\text{g}} \cdot W_{\text{g}})$ of approximately 1 mW/μm^2, which corresponds to $V_{\text{ds}} = -1$ V and an intrinsic lateral field of $E_{\text{ds,int}} \approx 1$ V/μm consistent with previous publications [27], [32]. Depending on the bias condition, it is possible to observe a so-called "kink" in the output curve of GFETs. This is attributed to the lack of a bandgap of graphene, which leads to the change of the charge carrier type at the drain side of the GFET channel instead of the formation of a depletion region as in semiconductor counterparts. In our measurements, this condition can be reached at $V_{\text{ds}} \approx -1$ V (for $T_{\text{ext}} = 100$°C) when $V_{\text{ds}} \approx V_{\text{gs}} - V_{\text{Dir}}$. Taking into account the typical width of the kink of approximately 0.5 V [8], one can expect observing the kink at -V_{ds} above

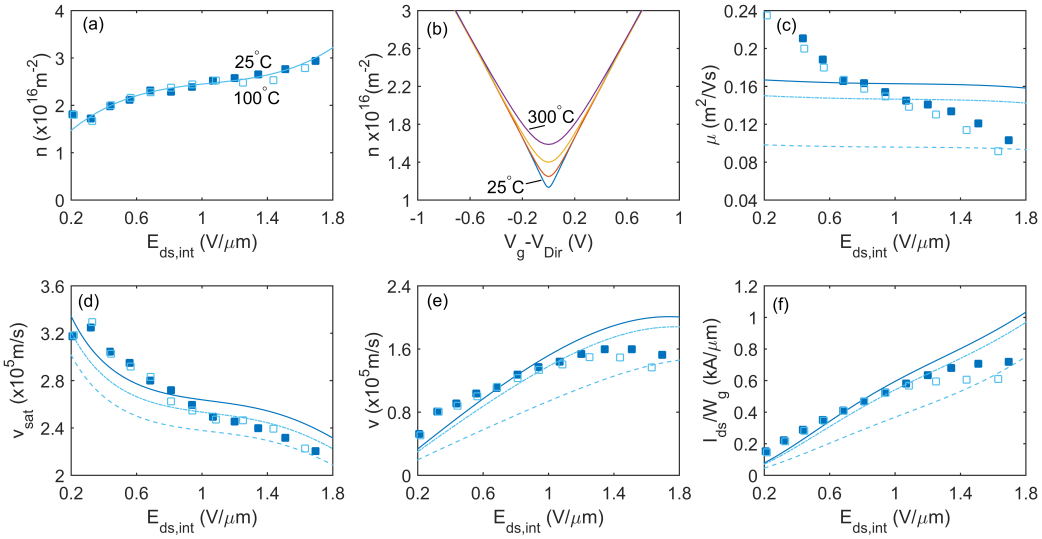

Fig. 4. (a) Charge carrier concentration n derived from measurements at T_{ext} = 25 and 100 °C versus intrinsic electric field $E_{ds,int}$ (solid and open squares, respectively) together with a polynomial fitting curve of the average of these two that is used for the calculations of the solid and dashed lines in (c)-(f). (b) Charge carrier concentration n versus applied gate voltage $V_{gs} - V_{Dir}$ at $T_{ext} = 25, 100, 200, 300$ °C calculated as in [43]. (c) Low-field mobility μ calculated using (7), (d) velocity saturation v_{sat} calculated using (6), (e) effective drift velocity v calculated using (5), and (f) drain current divided by gate width I_{ds}/W_g versus drain-source intrinsic electric field $E_{ds,int}$, where I_{ds} is measured or calculated using (8). In (c)-(e), the lines are dependencies simulated without self-heating for T_{ext} = 25, 100, and 250 °C (solid, dashed-dotted and dashed lines, respectively).

1.5 V, which is out of the studied V_{ds} range, see Fig. 2(b). The weak decrease in saturation current of 5 % above V_{ds}¿1 V with larger T_{ext} can be explained by the decreasing saturation velocity and mobility with temperature. Fig. 2(c-d) shows that both the values of f_T and f_{max} decrease rapidly starting from $P_{density,int} \approx 1$ mW/μm^2. The strong decrease of f_T has been similarly observed in InGaP/GaAs heterojunction bipolar transistors [44]. As seen, the effect of the extrinsic temperature on f_{max} is more remarkable than on f_T. It will be shown below that the decrease in f_T and f_{max} at higher $P_{density,int}$ can be fully explained by self-heating. Fig. 3(a) shows the effective channel temperature found using (1-7) and calculated by the thermal-resistance model [14] for different T_{ext}. The temperatures extracted by the method presented in this work increase strongly for $P_{density,int} > 1$ mW/μm^2 while the thermal-resistance model predicts lower temperatures. Fig. 3(b) shows the thermal resistance extracted as the derivative of the polynomial fit in Fig. 3(a) together with R_{th} estimated by the thermal-resistance model. For low $P_{density,int} \approx 0.6$ mW/μm^2, the thermal resistance estimated by the thermal-resistance model $R_{th} \approx 6$ kK/W agrees well with the temperatures extracted by the method presented in this work. The disagreement at higher P_{int} and external temperatures can be explained by an increase in the thermal resistances, which is not taken into account sufficiently by the thermal-resistance model for the GFET system. To evaluate R_{th} by yet another method we use the temperature and dissipated power dependence of I_g to extract R_{th} using the TSEP method [31], [45] as described in the METHOD section. Fig. 3(c) shows the gate leakage current (I_g) versus $P_{density,int}$, which is used to estimate R_{th} estimated by the TSEP method shown in Fig. 3(d). The resolution ratio of the TSEP method is approximately 0.2. Fig. 3(d) shows the R_{th} estimated by the TSEP method versus $P_{density,int}$. It can be seen that the R_{th} evaluated by the TSEP method agrees fairly well with that calculated with our proposed method. The R_{th} increases with $P_{density,int}$ and T_{ext}, explaining, as expected, the deviations of temperature evaluated by the method presented in this work and the thermal-resistance model at higher $P_{density,int}$ and T_{ext}; see Fig. 3(a) and (b). The temperature dependence of R_{th} can be explained by the temperature dependence of the thermal conductivity of the involved materials that may decrease by half for an increase in the temperature by self-heating of approximately 300 K [46], [47]. This is associated with more intensive phonon scattering at higher temperatures, since the thermal conductivity is related to the mean-free path and the phonon group velocity [46], [47]. Analysis of Fig. 2(c),(d) and Fig. 3(a) allows us to conclude that the decrease in f_T and f_{max} and higher $P_{density,int}$, respectively, can be fully explained by self-heating. Indeed, $\Delta P_{density,int}$ of approximately 0.4 mW/μm^2 results in ΔT of approximately 40 °C; see Fig. 3(a). On the other hand, the corresponding increase in $P_{density,int}$ from 1.0 to 1.4 mW/μm^2 results in the decrease of f_{max} from approximately 20 to 10 GHz, which is similar to that caused by the increase in T_{ext} from 60 to 100 °C in the same power region; see Fig. 2(d). Other mechanisms that are causing irreversible degradation, such as oxide breakdown or current breakdown can be ruled out since the GFETs recovered after measurements and the gate leakage current is low, i.e., in the nA range, even at high fields and temperatures, and the breakdown current density of graphene has been shown to be three orders of magnitude larger than the maximum current density in this work [48].

Thus, self-heating clearly affects the high-frequency performance of GFETs limiting f_T and f_{max} at higher source-

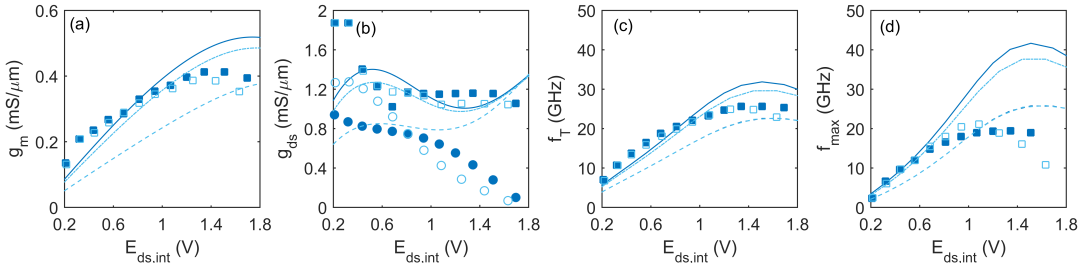

Fig. 5. (a) Transconductance divided by gate width g_m/W_g, (b) output conductance divided by gate width g_{ds}/W_g, (c) f_T, and (d) f_{max} versus intrinsic drain-source electric field $E_{ds,int}$ (corresponding to V_{ds} in the range from -0.2 to -1.4 V) derived from measurements using (1)-(2) for T_{ext} = 25 and 100 °C (solid and open squares, respectively) and simulated without self-heating using (9) for T_{ext} = 25, 100 and 250 °C (solid, dashed-dotted and dashed lines). In (b), g_{ds}/W_g is also shown, calculated using (9) from the measured I_{ds} shown in Fig. 4(f) for T_{ext} = 25 and 100 °C (solid and open circles, respectively).

drain fields. However, the self-heating effect can be controlled and minimized by optimizing the transistor layouts and selecting substrate materials with higher thermal conductivity. Calculations, using the analytical thermal-resistance model, indicate that the GFET thermal resistance associated with the SiO_2 layer dominates and is approximately 80 % of that of the total SiO_2/Si substrate. For comparison, the thermal conductivity of sapphire, which, for example, can be used as the GFET substrate without the SiO_2 layer, is ≈ 35 W/mK [49], which is significantly higher than that of SiO_2 with 1.4 W/mK [50]. In the analysis below, we simulate the GFET high-frequency performance with and without the self-heating effect. Applying the equations discussed in the METHODS section, we estimated the mobility μ, the saturation velocity v_{sat}, the effective channel velocity v, the drain-source current I_{ds}, the output conductance g_{ds}, and f_T and f_{max} assuming $T = 27, 100$ and 250 °C. Fig. 4(a) shows the charge carrier concentration n estimated from the measured f_T, f_{max}, and I_{ds} using (1)-(4). The increase of n with $E_{ds,int}$ can be explained mainly by self-gating since there is no significant difference in n for different T_{ext}. Applying V_{ds} results in an effective gate bias at the drain side of the channel which will alters the charge carrier concentration. For illustration, Fig. 4(b) shows the charge carrier concentration n versus the applied gate voltage overdrive, $V_{gs} - V_{Dir}$, at different temperatures. The charge carrier concentration constitutes the sum of thermally generated charge carriers n_{th}, residual charge carriers n_0 due to charged impurity doping [51], and gate induced charge carriers n_g. In our calculations $n_0 = 1 \cdot 10^{16}$ m^{-2} and $n_{th} + n_g$ dependent on the position of the Fermi level is calculated as in [43] and the relation between gate bias V_{gs} and E_F is established as $V_{gs} = (Q_g + Q_{ox})/C_{ox} + E_F$ where Q_g is the charge in the graphene sheet and Q_{ox} the charge in the oxide, which constitutes the charge trapped in deep traps and interface states [43]. Fig. 4(b) shows that higher temperatures only affect n noticeably close to $|V_{gs} - V_{Dir}| = 0$ V. Therefore, we use the average charge carrier concentration n, shown in Fig. 4(a), in (4), (6), and (7) to estimate I_{ds}, μ, and v_{sat} without the effect of self-heating.

Figs. 4(c) and (d) show the low-field mobility μ and saturation velocity v_{sat} versus $E_{ds,int}$. Comparing Figs. 4(c-d) and Fig. 4(a) indicates that both μ and v_{sat} correlate with variations in the charge carrier concentration. When removing the effect of self-heating (lines), the mobility increases from $\mu \approx 0.1$ to 0.16 m^2/Vs and v_{sat} from $\approx 2 \cdot 10^5$ to $2.3 \cdot 10^5$ m/s, for external temperatures up to 100 °C. For T_{ext} above 100 °C, μ and v_{sat} and, hence, v are strongly degraded. The low-field mobility below $E_{ds,int} =$ increases sharply due to the limitation of (7) being only valid for $n > 2 \cdot 10^{16} m^{-2}$ [27]. Fig. 4(e) shows the effective drift velocity v in the channel versus $E_{ds,int}$ calculated by (5). The velocity increases with increasing $E_{ds,int}$ according to the field-dependent velocity model. At $E_{ds,int}$ ≈1.2 V/μm, the velocity drops rapidly due to self-heating. If self-heating is avoided, the velocity in the channel continues to increase by approximately 20 % compared to the measurements with self-heating. In Fig. 4(f), the measured drain-source current divided by the gate width and I_{ds}/W_g calculated without self-heating using (8) are shown. The I_{ds} without self-heating is larger at high fields due to the larger velocity for T_{ext}=25 °C and 100 °C and smaller for T_{ext}=250 °C due to a strong decrease in μ and v_{sat}. The good agreement of the measured and modeled I_{ds} at $E_{ds,int} = 1.8$ V/μm and T_{ext}= 250 °C indicates that the temperature estimate shown in Fig. 3(a) of approximately 250 °C at $P_{density,int}$ =1.4 mW/μm^2 is reasonable.

Fig. 5 shows g_m/W_g, g_{ds}/W_g, f_T and f_{max} versus $E_{ds,int}$, where g_m and g_{ds} are estimated from measurements using (1)-(2). The values of these parameters without self-heating calculated using (9) are also shown. Due to the relation between v and g_m given by (3) the transconductance exhibits the same dependence as v on $E_{ds,int}$ and T_{ext}. Fig. 5(b) shows that g_{ds} extracted from f_T and f_{max} is almost constant with $E_{ds,int}$. In addition, g_{ds} calculated using (9) and measured I_{ds} from Fig. 4(f) is shown. Due to self-heating effects, I_{ds} exhibits a slightly negative slope at high fields that results in negative g_{ds} (out of bounds in Fig. 5(b)). Negative g_{ds} is also observed in MOSFETs and HEMTs and is associated with trapping and heating effects that lead to the reduction of the effective applied gate voltage and a reduction of the saturation velocity and mobility [52], [53]. The g_{ds} calculated without self-heating follows first the slope of g_{ds} with self-heating and then increases again at higher fields due to larger current I_{ds} (see Fig. 4(f)). Fig. 5 shows that f_T and f_{max} are not notably affected by self-heating for fields below 1 V/μm, which is not surprising since g_m and g_{ds} are not affected. Channel temperatures below $T_{ext} \approx 200$ °C do not significantly affect the temperature-dependent mobility and saturation velocity

[27] and, thus, the high-frequency performance. However, at high fields above $E_{\mathrm{ds,int}} = 1\,\mathrm{V}/\mu\mathrm{m}$ self-heating leads to a significant increase of the channel temperature, which is additionally boosted by an increase of the thermal resistance. Therefore, there would be a clear improvement in f_{T} and f_{max} at $E_{\mathrm{ds,int}}$ above $1\,\mathrm{V}/\mu\mathrm{m}$, if the self-heating case is avoided, from approximately 18 GHz up to approximately 30 GHz and 40 GHz, respectively.

IV. Summary and Conclusions

In summary, we studied the effects of self-heating and external heating on the high-frequency performance of graphene field-effect transistors. We presented a new method, that allows for evaluation of the thermal resistance of GFETs with a submicron gate length. The method has the advantage that in addition to the temperature, it also allows for evaluation of the output conductance, the effective channel velocity, the charge carrier concentration, the saturation velocity and the mobility. Hence, it allows for studying the effect of self-heating and external heating on these parameters. Another advantage is that our method does not rely on the estimate of the charge carrier concentration derived from the applied gate voltage, since there is typically some shift of the Dirac point during extensive measurements due to charge trapping and detrapping in the gate oxide, that is dependent on the measurement sweeping rate [33], [34]. Analysis of the experimental and theoretical dependencies of the transit frequency and maximum frequency of oscillation of GFETs on the drain-source voltage and different external temperatures indicates that at the power densities above approximately $1\,\mathrm{mW}/\mu\mathrm{m}^2$ the high-frequency performance significantly degrades due to self-heating. For instance, the extrinsic f_{T} and f_{max} decrease from approximately 25 GHz down to 20 GHz explained by a decrease in the low-field mobility and saturation velocity, although he drain conductance decreases with temperature. This work provides valuable insights for further development of GFETs for high-frequency applications, taking into account self-heating as well as external heating effects on the high-frequency performance. The self-heating effect can be significant, particularly for GFETs on flexible polymer substrates [54], in which the thermal conductivity is typically lower than that of rigid substrates. In future work, a temperature dependent nonlinear R_{th} model for the GFET system is required for more accurate simulations of the GFET channel temperature and corresponding further optimization of the device design.

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