Thesis for the Degree of Doctor of Philosophy

Enabling Solutions for Integration and Interconnectivity in Millimeter-wave and Terahertz Systems

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Abstract

Recently, Terahertz (THz) systems have witnessed increasing attention due to the continuous need for high-data-rate transmission which is mainly driven by next-generation telecommunication and imaging systems. In that regard, the THz range emerged as a potential domain suitable for realizing such systems by providing a wide bandwidth capable of achieving and meeting the market requirements. However, the realization of such systems faces many challenges, one of which is interconnectivity and high level of integration. Conventional packaging techniques are not be suitable from performance perspective above 100 GHz and new approaches need to be developed.

This thesis proposes and demonstrates several approaches to implement interconnects that operate above 100 GHz. One of the most attractive techniques discussed in this work is to implement on-chip coupling structures and insert the monolithic microwave integrated circuit (MMIC) directly into a waveguide (WG). Such approach provides high level of integration and eliminates the need of galvanic contacts; however, it suffers from a major drawback which is the propagation of parasitic modes in the circuit cavity if the MMIC is large enough to allow such modes to propagate. To mitigate this problem, this work suggests and investigates the use of periodic electromagnetic bandgap (EBG) structures that suppresses those modes. Such structures can be realized using various approaches such as; bed of nails and mushroom-type EBG structures. The proposed techniques are used to implement several on-chip packaging solutions that have an insertion loss as low as 0.7 dB. Moreover, the solutions are demonstrated in several active systems using various commercial MMIC technologies.

The thesis also investigates the possibility of utilizing the commercially-available packaging technologies such as Embedded Wafer Level Ball Grid Array (eWLB) packaging. The technology has been widely used for integrated circuits operating below 100 GHz but was not attempted in the THz range before. This work attempts to push the limits of the technology and proposes novel solutions based on coupling structures implemented in the technology's redistribution layers (RDL). The proposed solutions achieve reasonable performance at *D*-band which is suitable for low-cost mass production while at the same time allowing heterogeneous integration with other technologies.

This work addresses integration challenges facing systems operating in the THz range and proposes high-performance packaging solutions demonstrated in a wide range of commercial technologies and hence enabling such systems to reach their full potential and meet the increasing market demands.

Keywords: Electromagnetic band-gap (EBG), Embedded Wafer Level Ball Grid Array (eWLB), Integration, Interconnects, Millimeter waves, Monolithic microwave integrated circuit (MMIC), Packaging, Terahertz (THz), Waveguide transitions.

List of Publications

Appended Publications

This thesis is based on work contained in the following manuscripts:

Journal Articles and Letters:

[A] **A. Hassona**, V. Vassilev, A. Zaman, Y. Yan, S. An, Z. Simon He, O. Habibpour, S. Carpenter, M. Bao, and H. Zirath, "Nongalvanic Generic Packaging Solution Demonstrated in a Fully-Integrated D-Band Receiver," *IEEE Transactions on Terahertz Science and Technology.*, vol. 10, no. 3, pp. 321-330, May 2020.

[B] J. Campion, **A. Hassona**, Z. Simon He, B. Beuerle, A. Gomez-Torrent , U. Shah, S. Vecchiattini, R. Lindman, T. Dahl , Y. Li, H. Zirath, and J. Oberhammer, "Toward Industrial Exploitation of THz Frequencies: Integration of SiGe MMICs in Silicon-Micromachined Waveguide Systems," *IEEE Transactions on Terahertz Science and Technology*, vol. 9, no. 6, pp. 624-636, Nov. 2019.

[C] **A. Hassona**, Z. Simon He, V. Vassilev, C. Mariotti, S. Gunnarsson, F. Dielacher, and H. Zirath, "Demonstration of +100-GHz Interconnects in eWLB Packaging Technology," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 7, pp. 1406-1414, July 2019.

[D] **A. Hassona**, V. Vassilev, Z. Simon He, C. Mariotti, F. Dielacher, and H. Zirath, "Silicon Taper Based D-Band Chip to Waveguide Interconnect for Millimeter-Wave Systems," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 12, pp. 1092-1094, Dec. 2017.

[E] **A. Hassona**, V. Vassilev, Z. Simon He, A. Zaman, C. Mariotti, F. Dielacher, and H. Zirath, "D-band Waveguide-to-microstrip Transition Implemented in eWLB Packaging Technology," *Electronics Letters*, vol. 56, Issue 4, p. 187 – 189, 20 Feb. 2020.

[F] **A. Hassona**, V. Vassilev, A. Zaman, V. Belitsky, and H. Zirath, "Compact Low-loss Chip-to-Waveguide and Chip-to-Chip Packaging Concept Using EBG Structures," A revision is submitted to: *IEEE Microwave and Wireless Components Letters.*

[G] **A. Hassona**, S. Gunnarsson, Z. Simon He, F. Dielacher, and H. Zirath, "A 220-280 GHz MMIC-to-Waveguide Transition in a Commercial SiGe Technology," Submitted to *IEEE Transactions on Terahertz Science and Technology.*

Conference Papers:

[H] **A. Hassona**, V. Vassilev, A. Zaman, and H. Zirath, "Packaging Technique of Highly Integrated Circuits Based on EBG Structure for +100 GHz Applications," Invited paper in the *14th European Conference on Antennas and Propagation (EUCAP)*, Copenhagen, 2020.

[I] **A. Hassona**, Z. Simon He, O. Habibpour, V. Desmaris, V. Vassilev, S. Yang, V. Belitsky, and H. Zirath, "A Low-loss D-band Chip-to-Waveguide Transition Using Unilateral Finline Structure," *2018 IEEE/MTT-S International Microwave Symposium (IMS)*, Philadelphia, PA, 2018, pp. 390-393.

[J] **A. Hassona**, Z. Simon He, C. Mariotti, F. Dielacher, V. Vassilev, Y. Li, J. Oberhammer, and H. Zirath, "A non-galvanic D-band MMIC-to-waveguide transition using eWLB packaging technology," *2017 IEEE/MTT-S International Microwave Symposium (IMS)*, Honololu, HI, 2017, pp. 510-512.

[K] **A. Hassona**, Z. Simon He, V. Vassilev, and H. Zirath, " F-band Low-loss Tapered Slot Transition for Millimeter-wave System Packaging," *49th European Microwave Conference (EuMC)*, Paris, France, 2019, pp. 432-435.

[L] Y. Li, M. Hörberg, K.Eriksson, J. Campion, **A. Hassona**, S. Vecchiattini, T. Dahl, R. Lindman, M. Bao, Z. Simon He, F. Dielacher, J. Oberhammer, H. Zirath, and J. Hansryd "D-band SiGe transceiver modules based on silicon-micromachined integration" *2019 Asia-Pacific Microwave Conference (APMC)*, Singapore, 2019, pp. 883-885.

Other Publications

The content of the following publications partially overlaps with the appended papers or is out of the scope of this thesis.

Journal Articles:

[M] T. Do, M. Bao, Z. Simon He, **A. Hassona**, D. Kuylenstierna, and H. Zirath, "A low-phase noise D-band signal source based on 130 nm SiGe BiCMOS and 0.15 um AlGaN/GaN HEMT technologies," *International Journal of Microwave and Wireless Technologies*, vol. 11 special issue 5-6: eumw 2018 (part i), Jun. 2019 , pp. 456-465.

[N] H. Zirath *et al.*, "Towards Cost-, Hardware-, Energy- and Spectrum-Efficient High Datarate Millimeter-Wave Communication," Submitted to *IEEE Microwave Magazine.*

Conference Papers:

[O] **A. Hassona**, V. Vassilev, and H. Zirath, "G-band Frequency Converters in 130-nm InP DHBT Technology," Accepted at the *50th European Microwave Conference (EuMC)*, Utrecht, 2020.

[P] **A. Hassona**, Á. Perez-Ortega, Z. Simon He, and H. Zirath, "Low-cost D-band Waveguide Transition on LCP Substrate," *48th European Microwave Conference (EuMC)*, Madrid, 2018, pp. 1049-1052.

[Q] **A. Hassona**, Z. Simon He, V. Vassilev, and H. Zirath, "D-band waveguide transition based on Linearly Tapered Slot Antenna," *2017 IMAPS Nordic Conference on Microelectronics Packaging (NordPac)*, Gothenburg, 2017, pp. 64-67.

[R] Z. Simon He, **A. Hassona**, Á. Perez-Ortega, and H. Zirath, "A Compact PCB Gasket for Waveguide Leakage Suppression at 110-170 GHz," Accepted at *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, 2020.

[S] Z. Simon He, M. Bao, Y. Li, **A. Hassona**, J. Campion, J. Oberhammer, and H. Zirath, "A 140 GHz Transmitter with an Integrated Chip-to-Waveguide Transition Using 130 nm SiGe BiCMOS Process," *2018 Asia-Pacific Microwave Conference (APMC)*, Kyoto, 2018, pp. 28-30.

[T] V. Vassilev, Z. Simon He, S. Carpenter, H. Zirath, Y. Yan, **A. Hassona**, M. Bao, T. Emanuelsson, J. Chen, M. Hörberg, Y. Li, and J. Hansrydl "Spectrum Efficient D-band Communication Link for Real-time Multi-gigabit Wireless Transmission" *2018 IEEE/MTT-S International Microwave Symposium (IMS)*, Philadelphia, PA, 2018, pp. 1523-1526.

Thesis

[U] **A. Hassona**, "Non-galvanic Interconnects for Millimeter-wave Systems," Tekn. Lic. Thesis, Dept. of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden, 2018

As part of the author's doctoral studies, some of the work presented in this thesis has previously been published in [U]. Figures, tables and text from [U] may therefore be fully or partly reproduced in this thesis.

Notations and Abbreviations

Notations

ε_r	Relative permittivity
δ	Loss tangent
ρ	Resistivity
σ	Conductivity
f	Frequency
ω	Angular frequency
C	Capacitance
T	Temperature

Abbreviations

AMC	Artificial Magnetic Conductor
Balun	Balanced to unbalanced
BEOL	Back end of line
BER	Bit error rate
BGA	Ball Grid Array
BiCMOS	Bipolar complementary metal–oxide–semiconductor
BSV	Back-Side Via
CMOS	Complementary metal–oxide–semiconductor
CNC	Computer Numerical Control
CPW	Coplanar Waveguide
DC	Direct Current
DHBT	Double heterojunction bipolar transistor
EB/mo	Exabytes per month
EM	Electromagnetic
eWLB	Embedded Wafer Level Ball Grid Array
f_{max}	Power gain cut-off frequency
f_T	Unity gain cut-off frequency
GaAs	Gallium Arsenide
Gb/s	Gigabit per second

GSG	Ground signal ground
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility transistor
HR	High Resistivity
IC	Integrated circuit
I/O	Input/Output
InP	Indium Phosphide
I/Q	In-phase/Quadrature
IR	Image rejection
LBE	Localized Backside Etching
LNA	Low Noise Amplifier
LO	Local oscillator
LTS	Linearly Tapered Slot
mHEMT	metamorphic High-electron-mobility transistor
MMC	Micro-machined
MMIC	Monolithic Microwave Integrated Circuit
mmW	Millimeter-wave
MS	Micro-strip
NF	Noise figure
PCB	Printed Circuit Board
PEC	Perfect Electric Conductor
PMC	Perfect Magnetic Conductor
RBW	Resolution Bandwidth
RDL	Redistribution Layer
RF	Radio Frequency
Rx	Receiver
SA	Spectrum analyzer
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SIW	Substrate Integrated Waveguide
SL	Slot Line
TFMSL	Thin-Film Micro-strip Line
THz	Terahertz
TS	Tapered Slot
TSV	Trough Substrate Via
Tx	Transmitter
USB	Upper sideband
VNA	Vector Network Analyzer
WG	Waveguide
WLP	Wafer-Level Packaging
WR	Rectangular Waveguide

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Chapter 1

Introduction

1.1 Background on Integration and System Packaging Challenges

Recent advances in semiconductor technologies, made the realization of integrated circuits in the millimeter-wave (mmW) and THz frequency ranges a reality [1], [2]. Such circuits have a wide range of applications, including, wireless communication, sensing and imaging [1], [2], [3]. Wireless communication is, however, one of the most rapidly growing industries and the forecast indicates continuing growth in that sector. This is mainly driven by the growing demand for higher data rates. Recent projections expect that the global mobile data traffic will reach ∼160 Exabytes per month (EB/mo) by the year 2025 [4] as shown in Fig. 1.1.

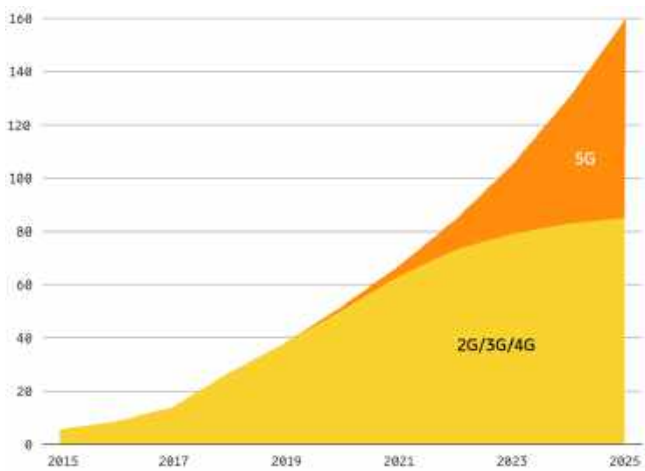


Figure 1.1: Global mobile data traffic (EB per month) [4]

Wireless links operating at D-band (110 – 170 GHz) with data rates of up to 48 Gigabit per second (Gb/s) were reported in [5], and a successful transmission with a data rate of 100 Gb/s is demonstrated at 230 GHz in [6].

However, the commercialization of such systems faces a set of challenges among which integration and low-loss interconnectivity rise as bottlenecks. Traditional packaging techniques such as wire bonding and flipchip do not achieve the performance requirements needed in high-data-rate systems such as low loss and wide bandwidth, and although compensation techniques to improve their performance above 100 GHz are proposed in literature [7], such techniques exhibit narrow-band performance and won't fully utilize the wide spectrum available in the mmW and THz ranges. In addition, wire bonding suffers from poor repeatability and manufacturability challenges in the mmW range and flipchip mounting introduces an additional ground plane, which can affect coupling structures on the MMIC, in addition to the relatively low thermal conductivity provided by solder bumps that can pose a limitation on using flipchip packaging for high-power applications [8].

Recently, this area gained attention and various approaches were proposed in literature to address such challenges. One approach proposed in [9] is to use a Coplanar Waveguide (CPW) to recangular waveguide transition based on metal ridge as shown in Fig. 1.2. The proposed solution is suitable for packaging large integrated circuits; however, it would be challenging to use it to package circuits that have much smaller dimensions relative to the metal ridge. In addition, the transition requires galvanic contacts between the waveguide and the ridge from one side and the ground and signal traces on the other side which risks stressing the chip mechanically.

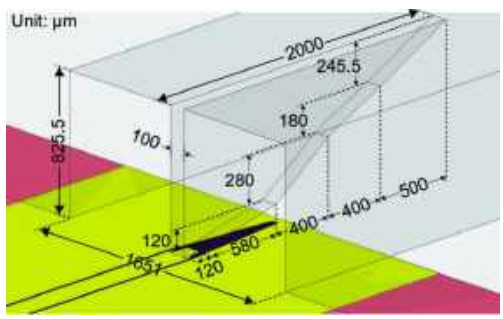


Figure 1.2: D-band CPW-to-waveguide transition based on metal ridge [9]

Another technique to realize THz interconnects is to use Substrate Integrated Waveguide (SIW) transitions [10], [11] as shown in Fig. 1.3. However, such technique does not provide standard waveguide connectivity and an additional transition to air-filled waveguides needs to be implemented to provide a standard interface, which increases the overall loss of the system and complicates the design. Moreover, SIWs require the use of Trough Substrate Vias (TSV) in most cases which might not be available in some MMIC technologies. In addition, SIWs could exhibit high dielectric loss depending on the used substrate materials, which could be avoided if efficient radiation to air is implemented instead.

Silicon (Si) micro-machined (MMC) structures were also reported in literature as a candidate for implementing high-frequency interconnects in [12], however, the proposed solution works mainly for chip-to-chip communication and might not be suitable for applications that require a standard waveguide

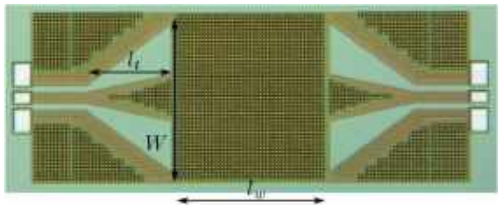


Figure 1.3: Substrate integrated waveguide transition [11]

interface.

In applications where a waveguide interface is not required, a radiating structure can be integrated on-chip and then radiate directly to free space or couple to an external optical component such as a lens. This concept was demonstrated in a 153 - 162 GHz power detecting receiver (Rx), in which the circuit was integrated with a double slot antenna on the same chip as shown in Fig. 1.4 and then mounted on a Si lens [13]. A similar approach was used in integrating a Low Noise Amplifier (LNA) and a mixer, together with a planar antenna in [14] at 220 GHz.

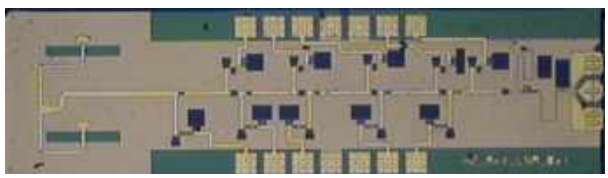


Figure 1.4: Power detecting receiver integrated with on-chip double slot antenna [13]

Another approach to realize interconnectivity is to use a beam lead transition as proposed in [15] and shown in Fig. 1.5. However, the presented solution utilizes a thin narrow membrane which can be mechanically challenging to assemble in addition to a potentially low repeatability.

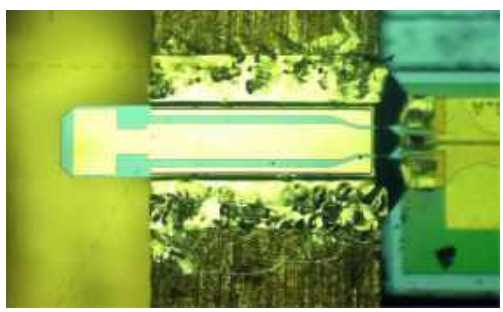


Figure 1.5: Beam lead connector-based transition [15]

One attractive solution is to integrate the waveguide transition on-chip instead, and couple directly to the waveguide and hence avoid galvanic contacts. The drawback of this technique is that it impose constraints on the chip size as the chip in this case needs to be narrow enough in order not to allow parasitic modes to propagate in the chip cavity. This is only suitable for simple circuits

with low level of integration as demonstrated in [16], [17]. Various solutions to address this issue have been proposed in literature including laser dicing [18] or chemical etching [19] to achieve a non-rectangular die shape as shown in Fig. 1.6.

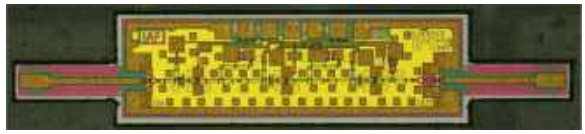


Figure 1.6: Non-rectangular die shaping to avoid exciting unwanted modes [18]

The proposed solutions address the issue of parasitic modes propagation; however, they require extra fabrication and processing steps. Moreover, the narrow part of the chip is fragile and more susceptible to mechanical stress which could lead to a lower yield.

Another candidate is eWLB technology which provides low-cost high-volume wafer level packaging and is widely used for system integration up to 100 GHz [20], [21]. It allows heterogeneous integration of several technologies in the same package and provides Ball Grid Array (BGA) which exhibits better electrical properties compared to traditional techniques such as wire bonding. Fig. 1.7 shows a highly integrated 60-GHz radar sensor packaged using eWLB technology [22]. The technology also provides several metal layers named redistribution layers, which not only can be used for connectivity but also for implementing passive structures such as inductors and capacitors [23], [24].

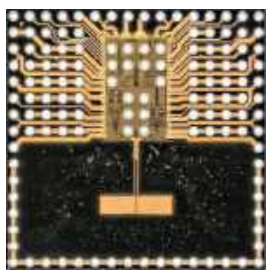


Figure 1.7: mmW radar sensor in an eWLB package [22]

However, despite that the technology has been widely used below 100 GHz, it has been seldom used for packaging systems operating beyond that frequency. This is mainly due to the relatively large size of solder balls provided by eWLB manufacturers which is not suitable for high frequency applications. In addition, the several discontinuities along the RF signal path introduced by going from chip to eWLB and then from eWLB to Printed Circuit Board (PCB), cause impedance mismatches which lead to losses due to reflections and undesired radiation.

1.2 Motivation and Contribution

This thesis aims to investigate and develop packaging solutions for systems operating beyond 100 GHz. First, on-chip waveguide transitions are investigated

for both III-V and Si-based semiconductor technologies. Integrating such transitions on chip has several advantages including achieving high integration and avoiding galvanic interfaces such as bondwires as explained earlier. Moreover, the use of waveguide interfaces provide a desirable packaging solution since waveguides are the preferred and most common media for signals above 100 GHz. The thesis also proposes the use of EBG structures to suppress parasitic modes and hence mitigate one of the main issues facing such packaging approaches. EBG structures realized by bed of nails are investigated and their performance is presented. Mushroom-based EBG structures are also discussed.

Several packaging solutions are proposed and experimentally verified in various semiconductor technologies such as Indium Phosphide (InP) [Papers A and H], Gallium Arsenide (GaAs) [Papers F and K] and Silicon Germanium (SiGe) [Papers B, G and L]. The proposed solutions rely on integrating coupling structures on the chip which is then mounted in a split-block waveguide module that includes periodic EBG structures to suppress the propagation of unwanted modes. The presented solutions do not impose any limitations on the chip's dimensions nor shape and exhibit an insertion loss as low as 0.7 dB covering up to 50% of bandwidth. Moreover, the proposed approaches are generic and can be implemented in most of the commercially-available semiconductor technologies. To demonstrate that, the solutions are also integrated in several MMICs including fully integrated D-band transceiver chipset to verify the performance of the presented techniques in active systems.

The thesis also investigates the use of eWLB technology for packaging mmW systems. The choice of eWLB technology is motivated by its low-cost high-volume capabilities which makes it a strong candidate for the commercialization of mmW systems in the future. The thesis proposes implementing coupling structures using the technology's Redistribution Layers (RDL) and directly couple the RF signal to a standard waveguide in order to provide high-frequency connectivity instead of using the conventional BGA. Several concepts are proposed using structures such as slots and patches and their performance is characterized and presented [Papers C, D, E and J].

All the packaging techniques presented in this thesis are experimentally verified. Moreover, the technologies used for fabrication and assembly are either commercial or compatible with industrial processes that are already in place and hence paving the way towards full system commercialization at those frequencies. In addition, most of the work presented in this thesis is implemented at D-band which offers a wide frequency range extending from 110 to 170 GHz making it a suitable candidate for the realization of future commercial high-data-rate systems since D-band has a low atmospheric attenuation window between two high attenuation points at 118 GHz and at 183 GHz as shown in Fig. 1.8. The attenuation in that window is below 1 dB/km, making it suitable for medium-distance backhaul gigabit communications [25]. Moreover, D-band enables the use of smaller antennas making it more attractive for dense urban areas.

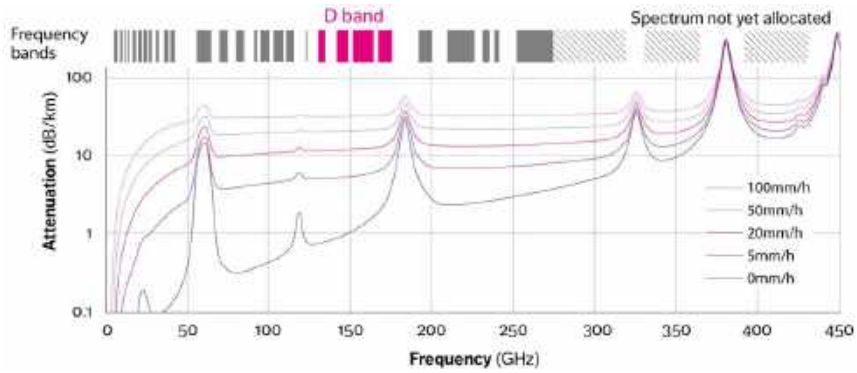


Figure 1.8: Atmospheric attenuation versus frequency [25]

1.3 Thesis Outline

This thesis consists of six chapters. Chapter 2 discusses the issue of unwanted parasitic modes and investigates the use of EBG structures such as bed of nails and mushroom-type EBG to suppress their propagation.

Chapter 3 proposes several packaging solutions for integrated circuits operating above 100 GHz in various technologies. Four different solutions are proposed for III-V semiconductor technologies [Papers A, I, K and F], three of which have a very low loss of less than 0.8 dB and can cover up to the entire D-band. Moreover, the chapter discusses the challenges of packaging MMICs in Si-based technologies and gives an overview of the solutions presented in literature in addition to two solutions that are proposed in the thesis and demonstrated in a commercial SiGe MMIC technology [Papers B and G].

Chapter 4 demonstrates two of the solutions presented in Chapter 3 in active circuits and systems. The first solution is the E-plane waveguide probe developed in InP double hetero-junction bipolar transistor (DHBT) technology which was integrated and successfully demonstrated in this chapter in a D-band receiver MMIC [Paper A] and a D-band amplifier [Paper H]. The second solution is the H-plane slot transition which is demonstrated in a 130-nm SiGe MMIC technology and integrated with a D-band transceiver chipset that is successfully demonstrated in a wireless link [Paper L].

Chapter 5 investigates the use of the commercial eWLB packaging technology above 100 GHz. Four different solutions are proposed and demonstrated in this chapter that show insertion losses ranging from 2 to 3.7 dB and operate up to 153 GHz [Papers C, D, E and J].

Finally, Chapter 6 concludes and summarizes the work presented in the thesis and discusses future expansions of the work such as demonstrating more of the presented solutions in active systems and pushing the frequency of operation higher. The development of alternative solutions for Si-based technologies is also of interest.

Chapter 2

Parasitic Modes Suppression

2.1 Unwanted Modes in High-frequency Integrated Circuits

MMIC substrates can allow the propagation of parasitic modes which can have many negative effects on the circuit's performance in addition to the unwanted cavity modes that can also be excited in the mechanical fixture housing the MMIC [26], [27]. This issue is more evident in large integrated circuits with metallization layers on both sides of the substrate. Various approaches are proposed in literature to mitigate the effects of such modes. One approach is to use TSVs and distribute them across the circuit [28]. However, the use of many TSVs would occupy a large area and hence decrease the integration density. This is especially critical at high frequencies since the via density across the circuit must increase in order to suppress the unwanted modes at such high frequencies [28].

Another approach is to use a process that provides low-permittivity low-loss dielectrics between the metal layers [29]. This enables the use of Thin-Film Micro-strip Lines (TFMSL) with one of the metal layers as ground which eliminates the need of back-side metallization and TSVs. This approach addresses the integration density issues in integrated circuits (IC), however, it still can suffer from parasitic modes if the chip size is large enough to allow such modes to propagate.

Eriksson et al. did a study on the phenomena of parasitic modes [30] and proposed placing the MMIC on a thick layer of Si, doped to a conductivity of 10 S/m to mitigate this issue. The Si acts as an absorber that effectively reduces the impact of those modes. The technique was tested in a TFMSL thru-line fabricated on a 100-um thick InP substrate and results show that the insertion loss is flat and smooth with no signs of any resonances/modes. However, the thermal conductivity of the Si carrier might be a limiting factor for circuits that consume high power. It is also noteworthy that such technique requires the absence of back-side metallization in order to be effective.

In order to better prevent the propagation of parasitic modes while not

sacrificing any major performance parameters, this work proposes using an Artificial Magnetic Conductor (AMC) surface realized by a periodic structure on top of the MMIC. This concept relies on the principal that placing an AMC surface along a Perfect Electric Conductor (PEC) surface would create a cut-off band for parallel plate modes when the spacing between the two surfaces is less than a quarter wavelength. Such concept, not only can be used to suppress parasitic modes but also to create a stop band for the wave propagation in undesired directions. A surface that can act as an AMC to achieve such property can be realized using a texture in the form of a periodic structure. The periodic structure should introduce a high impedance boundary at the band of interest. Valero-Nogueira et al. successfully demonstrated an AMC surface implemented using corrugations that was used to prohibit the propagation of higher order modes between metallic parallel plates and improve the performance of radiating slots [31].

An extensive study of the behavior of various periodic structures used to realize AMC surfaces is provided in [32]. The presented structures were successfully used to implement microstrip (MS) filters [33] and gap waveguide slot array antenna [34]. This thesis explores the possibility of using some of those structures such as bed of nails [35] and mushroom-type [36] EBG surface to suppress the propagation of parasitic modes in MMICs and their housing cavities while at the same time improve the performance of on-chip coupling structures that can be used to package mmW and THz circuits. The bed of nails does not require the use of dielectrics, and can be manufactured using Computer Numerical Control (CNC) machining in the sub-THz range or Si micro-machining in the THz range. On the other hand, mushroom-type EBG surface normally require a dielectric, however, it can be easily realized in low-cost PCB technologies.

The stop band in which the modes are suppressed has start and end frequencies which are determined by the dimensions of the EBG structure in addition to the distance d between the AMC textured surface and the PEC surface placed in parallel to it as shown in Fig. 2.1. The start and end frequencies of the stop band have limits that are dependant on the impedance presented by the AMC surface. For instance, the start frequency of the stop band comes from the frequency at which the AMC surface starts showing a high-enough impedance while the end frequency of the stop band comes from the frequency at which the AMC surface starts exhibiting a low impedance again. However, there is also another limit for the end frequency which is set by the gap d mentioned earlier. Such gap must be smaller than a quarter wavelength in order to avoid the propagation of undesired modes. The dependence of the end frequency of the stop band on the gap d is presented in [32] and can be seen in Fig. 2.2.

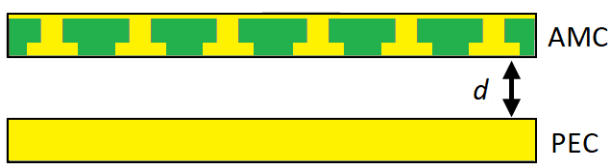


Figure 2.1: Cross-sectional illustration of how to realize parallel-plate cut-offs

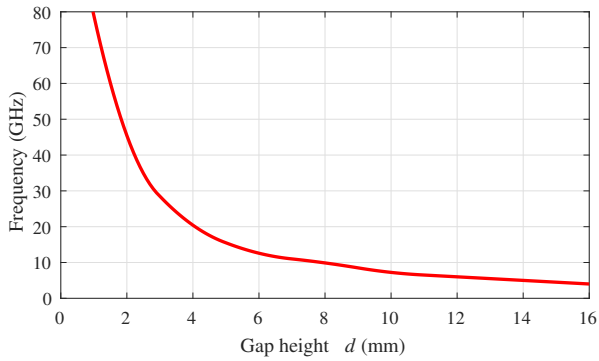
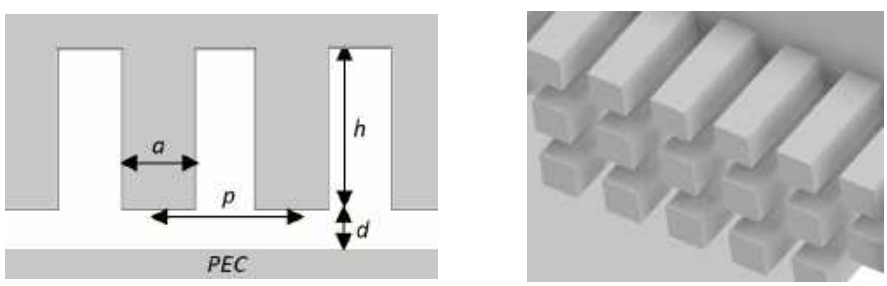


Figure 2.2: End frequency of the stop band vs. the gap height [32]

2.2 Suppression of Parasitic Modes Using Bed of Nails Structure

The bed of nails structure is proposed in literature and has been successfully demonstrated in gap waveguide applications [34]. Antenna integration solutions have been also presented using the same concept at frequencies as high as 100 GHz [37]. The cut-off bandwidth of the structure was thoroughly studied in [32]. The study presents the effect of the main parameters of the structure on its performance such as the height of the pins h, the gap to the conducting surface d, the period of the structure p and the dimension of the pin a as shown in Fig. 2.3.



(a) **(b)**

Figure 2.3: Illustration of the bed of nails structure and its design parameters (a) Cross-sectional view (b) 3D view.

The study used an eigenmode solver to compute dispersion diagrams and hence determine the impact of each parameter on the bandwidth of the structure. The outcome of the study is summarized in Fig. 2.4. The structure's stop band is defined by a start frequency (also referred to as lower limit) at which the propagation of the modes is stopped and an end frequency (referred to as upper limit) at which the waves can start propagating again and the structure stops being effective. The study shows that the stop band width increases when the gap d decreases as shown in Fig. 2.4a. In addition, the stop band

also widens when the period of the structure p increases. That is mainly due to the increase in the effective electrical length of the pins, however, this was only observed for large gaps, while for smaller gaps, smaller periods performed better as can be seen in Fig. 2.4b.

When it comes to the dimension of the pins, the start and end frequencies were observed to move in opposite directions as the dimension a increases. It as also noticed that the stop band reaches a maximum when such dimension is between $0.1\lambda_0$ and $0.2\lambda_0$ as shown in Fig. 2.4c.

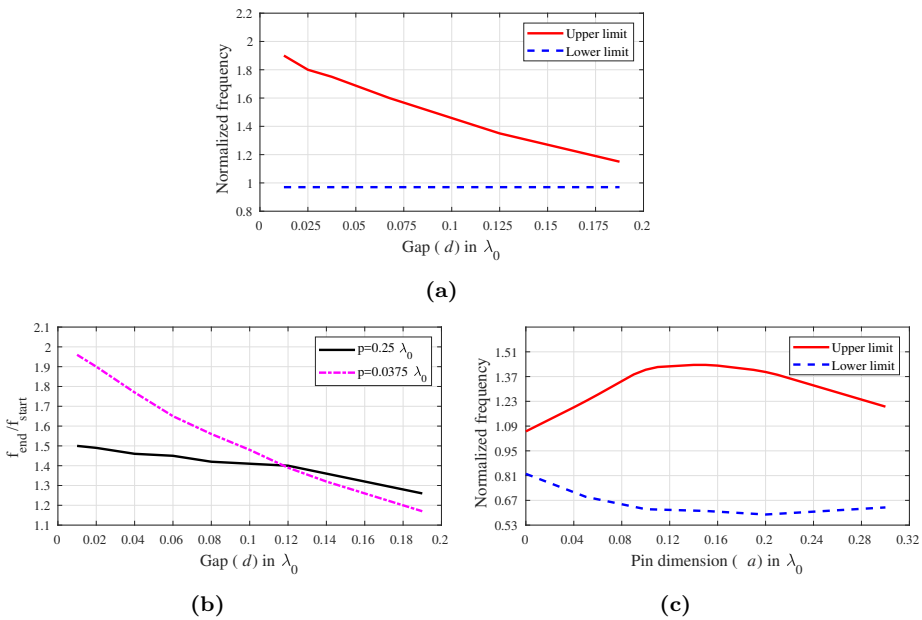


Figure 2.4: The impact of the different design parameters on the stop band (a) the gap to the PEC (b) the period of the pins (c) the dimension of the pins [32].

In order to assess the impact of the number of pin rows on the level of rejection of parasitic modes, 3D Electromagnetic (EM) simulations were performed. The simulations were done at D-band since it is of interest for the most of this work and it provides wide spectrum suitable for high-speed systems as discussed earlier. Results show that the structure provides an average rejection of the undesired modes of 42 dB with only 2 rows of pins. The structure also shows a very wide-band performance covering the entire D-band as can be seen in Fig. 2.5.

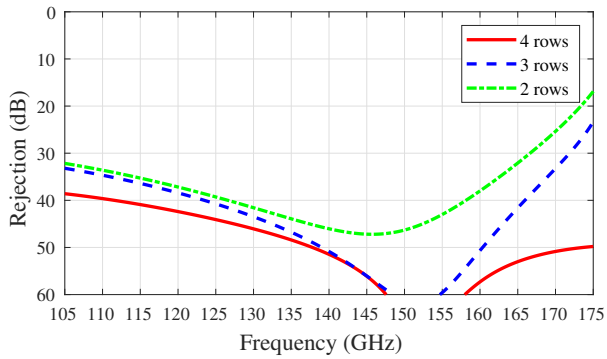
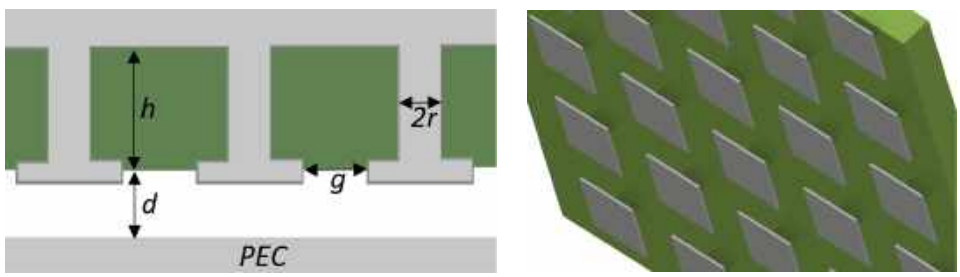


Figure 2.5: Simulated rejection of the bed of nails structure for different number of rows (Paper A).

2.3 Stop Bands Realized by Mushroom-type EBG

Mushroom-type EBG is also studied in [32]. The structure requires the use of a dielectric material to support the patches, however, for the sake of analogy with the bed of nails, no dielectric was employed in the study.

The study found it difficult to pinpoint a strong correlation between the centre frequency of operation of the structure and any specific dimension which can be used for normalization and hence, the dimensions in this case are presented in their absolute values. Similarly, the main parameters of the structure are studied and their impact on the stop band is analyzed. First, the gap g between the mushroom patches is considered as highlighted in Fig. 2.6.



(a) **(b)**

Figure 2.6: Illustration of the mushroom-type EBG and its design parameters (a) Cross-sectional view (b) 3D view.

It was noted that the gap g does not have a major impact on the stop band, however, that is only valid for large values of the distance d. For small values of d, the gap g can play a role in defining the width of the stop band as can be seen in Fig. 2.7a.

The radius of the grounding pin is also considered and its impact on the stop band is shown in Fig. 2.7b. Results show that the radius does not affect the width of the stop band but rather its center frequency since both limits (i.e., the start and stop frequencies) of the stop band move in the same direction as

the radius changes as shown in Fig. 2.7b. The frequency of operation seems to be proportional to the radius in the sense that, the larger the radius, the higher the frequency. Finally, the height of the mushrooms h is studied. Fig. 2.7c shows that the start frequency is depends on the value of h. The larger it is, the lower the frequency. It was also noticed that this behavior is independent of the distance d to the PEC. On the other hand, the upper limit of the stop band (i.e., the end frequency) shows no to very little dependency on the height of the mushrooms especially for small values of d.

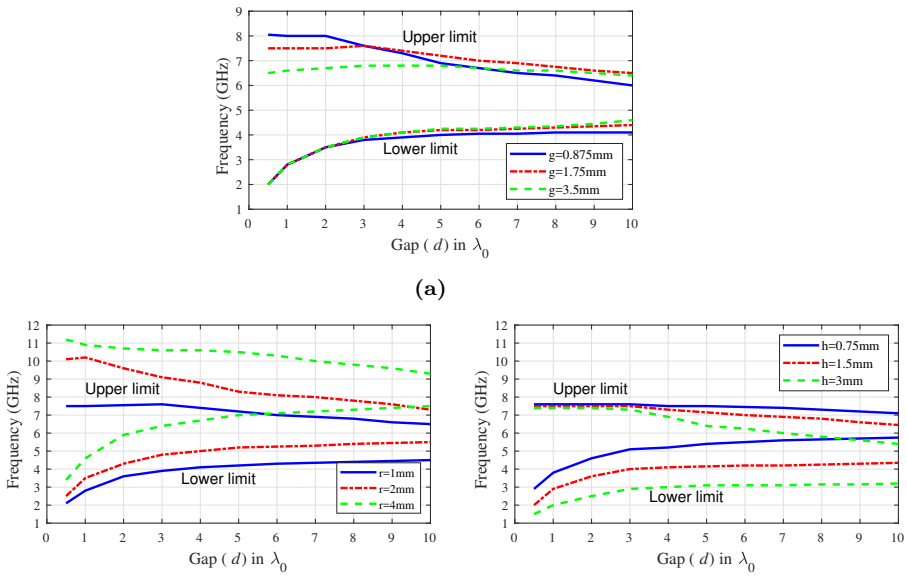


Figure 2.7: The impact of the different design parameters on the stop band of mushroom-type EBG (a) the gap between the patches (b) the radius of the pin (c) the height of the mushrooms [32].

The structure was used in Paper R to realize a waveguide gasket that can be used to suppress leakage at waveguide interfaces. The concept relies on the same principal of operation that the signal is prohibited to propagate at the stop band introduced by the mushroom structure and hence, the structure can be used to guide the signal at the waveguide interface and avoid any degradation in performance due to the air gap between the connected flanges as shown in Fig. 2.8.

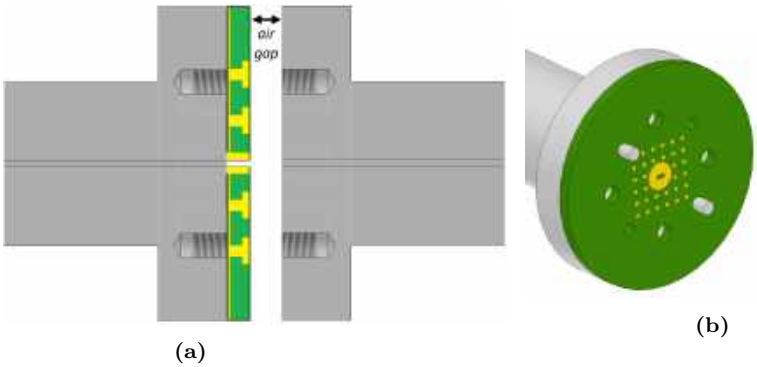


Figure 2.8: Illustration of the WG gasket based on mushroom-type EBG structure (a) Side view (b) 3D view.

The structure was implemented in a commercial PCB technology and demonstrated at D-band. A WR-6.5 sized opening was machined in the PCB with gold plated sidewalls. The gasket has two holes that are used for aligning the waveguide openings. Around the waveguide opening on the PCB, mushroom patches are implemented to suppress the leakage. The patches are connected to ground using via holes. Measurement results show that the gasket exhibit a low-loss wide-band performance and can withstand air gaps of up 75 um.

Chapter 3

Packaging Approaches for On-Chip Integration

3.1 Solutions for III-V Semiconductor Technologies

3.1.1 Integration of E-plane Waveguide Probe

This thesis proposes the use of E-plane waveguide probe as a packaging solution for mmW and THz MMICs. The probe is to be integrated with the circuitry on the same chip. The thesis also proposes using periodic EBG structure realized by bed of nails to suppress the propagation of undesired modes.

Transition Design

The complete proposed solution is shown in Fig. 3.1. The chip is mounted in the E-plane of a split-block D-band waveguide with the probe placed at a quarter-wave distance from the waveguide's back-short. The probe was designed to be half a wavelength at the center of D-band (i.e., 140 GHz) while taking into account the effect of the dielectric substrate on-which the probe is fabricated. That means that the equivalent length of the probe needs to be scaled down by the square root of the relative permittivity of the substrate material (i.e., to have a length of $\lambda_0/(2\times\sqrt{\epsilon_r})$, where λ_0 is the wavelength in free space and ϵ_r is the relative permittivity of the substrate material.

A bed of nails structure is used and mounted on top of the probe to provide a high impedance boundary that suppresses undesired modes in the circuit cavity as discussed earlier. The structure also helps prevent loss due to undesired radiation at the interface between the WG block and the chip. The results of the study conducted in [32], which was discussed in detail in Chapter 2, along with EM simulations were used to select the different parameters of the structure. The first parameter to be selected is the gap d which is chosen to be $0.06\lambda_0$ due to the physical limitation imposed by the thickness of the substrate used for this work (70 um). This is due to the fact that the chip needs to be placed between the pins and the conducting surface representing the ground plane which limits the minimum gap d to be at least equal to the

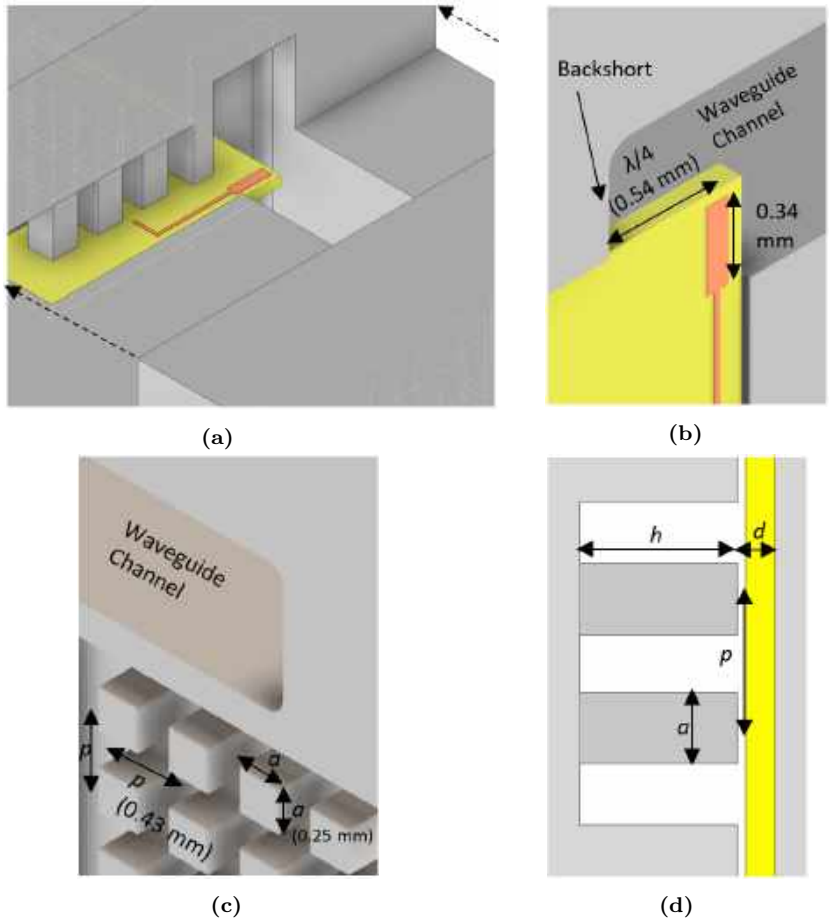


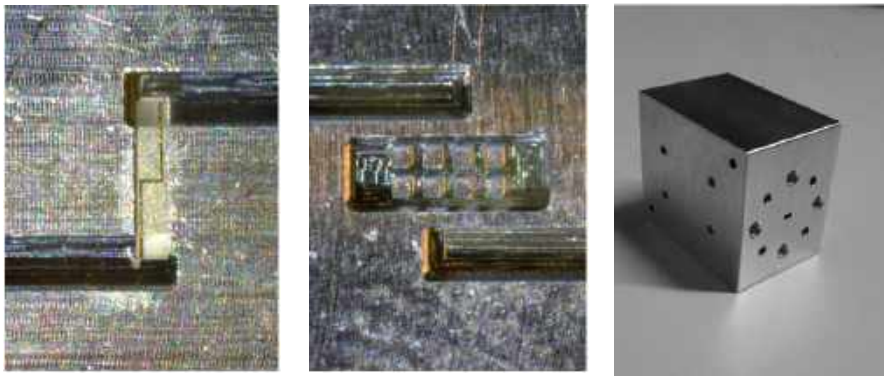
Figure 3.1: The proposed split-block packaging concept (a) 3D exploded section view (b) bottom part housing the waveguide probe (c) top part including the bed of nails structure (d) cross-sectional side view of the assembled parts.

substrate thickness plus an added margin to avoid contact between the chip's surface and the pins. Secondly, the period of the pins p and the dimension a were then chosen to be $0.2\lambda_0$ and $0.12\lambda_0$ respectively to achieve a wide stop band for the selected gap d. Such parameters correspond to the following values at D-band: a gap of 0.12 mm, a period of 0.43 mm and a pin dimension of 0.25 mm. Moreover, the effectiveness of the structure in suppressing EM propagation at D-band with the selected parameters values was verified using 3D EM simulations as was presented in Chapter 2 and shown in Fig. 2.5.

Experimental Results

The probe was fabricated on a 70 um-thick Silicon Carbide (SiC) substrate as a back-to-back transition as shown in Fig. 3.2. A split-block waveguide module was CNC machined to house the test chip. The module includes the bed of nails structure in its top part with two rows of pins to provide good rejection while at the same time maintain a compact design. The measurement

setup for the transition is shown in Fig. 3.3 and it consists of a Vector Network Analyzer (VNA) and a pair of WR-6.5 frequency extenders to up/down-convert the signal to D-band. The setup was calibrated to the outputs of the frequency extenders.



(a) (b) (c)

Figure 3.2: Photo of the fabricated module (a) bottom part housing the SiC chip (b) top part including the bed-of-nails structure (c) assembled module with standard WR-6.5 connectivity.

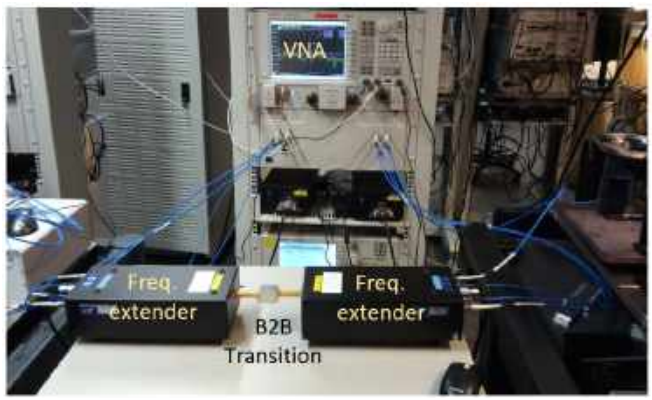


Figure 3.3: Measurement setup for the back-to-back waveguide transition.

Measurement results show that the transition exhibits a low insertion loss of only 0.7 dB per single transition and covers a very wide frequency band extending from 105 to 175 GHz as can be seen in Fig. 3.4a. It is noteworthy that the loss of the MS feed line is de-embedded in the presented results and it was estimated through simulations that it has a loss of 0.4 dB. The return losses of the back-to-back transition at both the input and output ports are also shown in Fig. 3.4b and Fig. 3.4c, respectively. Measurement results are also compared with simulation results of the same transition with and without the bed of nails. It can be clearly seen from Fig. 3.4a that the bed of nails effectively stops the propagation of undesired cavity modes in the band of interest.

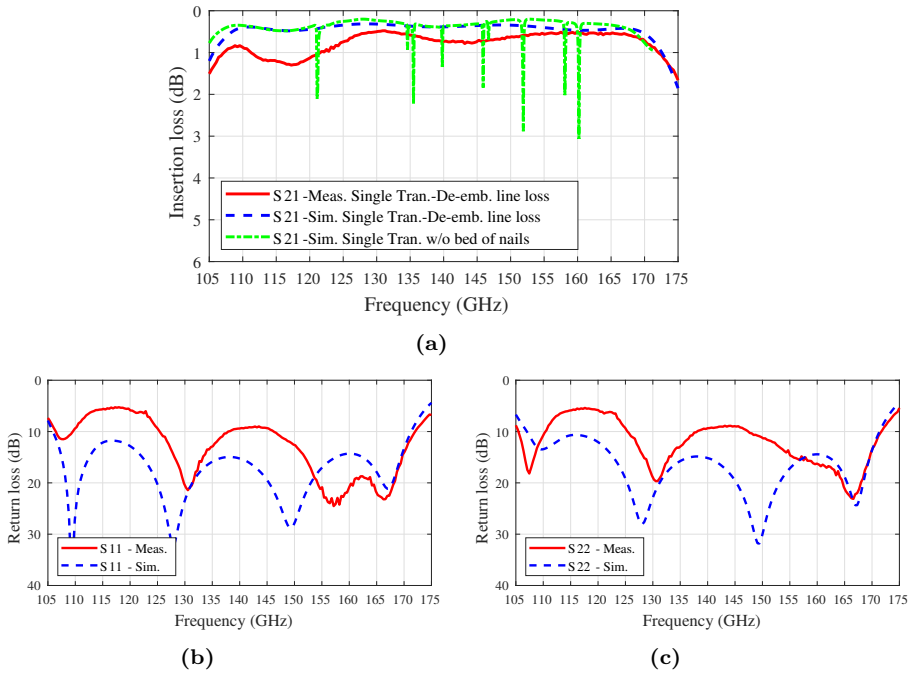


Figure 3.4: S-parameters of the E-plane WG probe transition (a) Insertion loss (b) Return loss at the input port (c) Return loss at the output port (Paper A).

The structure's sensitivity to fabrication tolerances was also simulated and shown in Fig. 3.5. The main parameters were varied by +/-25 um corresponding to the estimated fabrication tolerance for the bed of nails. Results show that the performance of the structure is not very sensitive to such variations and can still maintain good results across a wide frequency band.

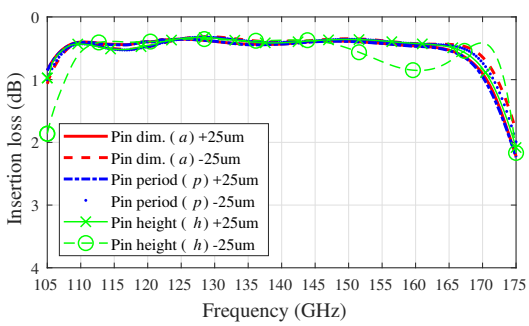


Figure 3.5: Simulated insertion loss of the transition across fabrication tolerances of the bed of nails structure (Paper A).

3.1.2 Chip-to-Waveguide Transition Using Unilateral Finline Structure

Introduction

Finlines are quasi-planar structures that exhibit large bandwidth and high compatibility with planar circuit technologies. Finlines can also be considered as shielded slot lines which are usually mounted in the E-plane of waveguides. The most common finline structures are unilateral, bilateral and antipodal as shown in Fig. 3.6a, 3.6b and 3.6c respectively.

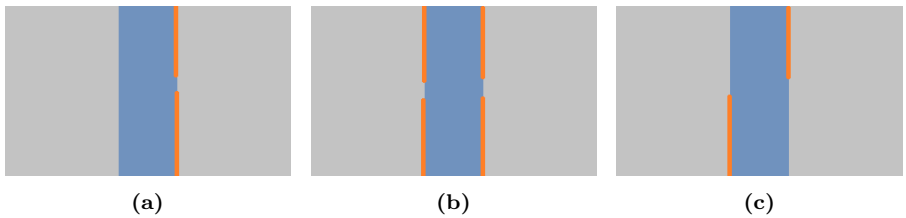


Figure 3.6: Cross section of common finline structures (a) unilateral (b) bilateral (c) antipodal

Unilateral finlines are the most convenient from fabrication perspective. Bilateral finlines produce lower losses and antipodal finlines are used to realize transitions with impedance levels in the order of 10 Ohms. Waveguide transitions based on finline structures were presented at V-band and W-band and promising results were demonstrated in [38], [39]. The presented transitions showed low insertion loss of 2.3 and 1.6 dB at V-band and W-band respectively.

This thesis proposes realizing a D-band interconnect using unilateral finline structure due to its simplicity and wide-band performance. The interconnect consists of a microstrip line implemented on a SiC substrate. The line then couples to a unilateral finline taper that is mounted in the E-plane of a standard WR-6.5 D-band waveguide. The interconnect achieves low insertion loss and covers very wide frequency range. The transition does not require any galvanic contacts nor any special processing and can be implemented in any of the commercially-available semiconductor technologies. In addition, the transition does not impose any limits on chip size nor shape and is implemented using only one metal layer. In the following sections, the transition design is discussed in detail and its performance is presented and compared to simulations.

Design of the Structure

The proposed transition is shown in Fig. 3.7. It consists of a mechanical split-block with two D-band waveguide channels split in the E-plane. A unilateral finline is then implemented on a 0.15 mm-thick metal shim that is placed in the E-plane of the waveguide channel and is attached to the bottom part of the split block using conductive epoxy. The finline slot then couples the signal from the waveguide to a microstrip line implemented on a 75 um-thick SiC substrate (representing the MMIC test structure) which lies on top of the finline structure as shown in Fig. 3.7b. The finline ends with a cavity acting as a backshort

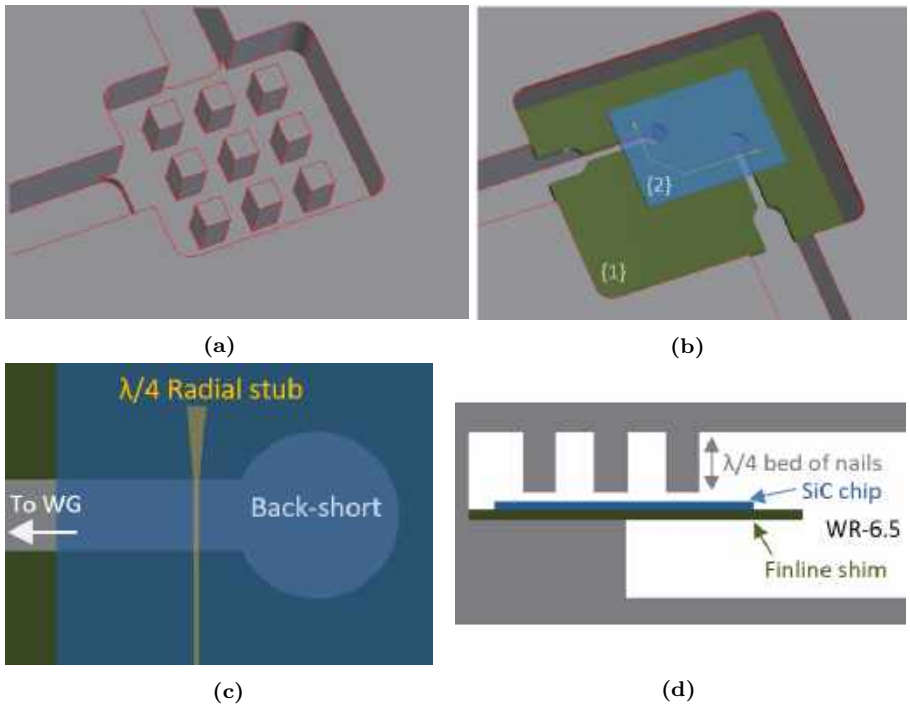


Figure 3.7: The proposed transition (a) top part of split-block (b) bottom part of split-block including {1} the finline metal shim and {2} the chip (c) top view of the transition (d) cross sectional side view of the entire solution

and the microstrip line crosses the finline slot perpendicularly as shown in Fig. 3.7b and 3.7c.

The microstrip line ends with quarter-wave radial stubs at both ends and hence eliminating the need for vias to provide RF grounding. The microstrip line and the radial stub can be placed at any location on the chip and does not require any special positioning (e.g., at the chip edge) as long as a crossing with the finline slot is made which provides more flexibility for MMIC design. Practically, the test chip presented here can be replaced with any MMIC fabricated on any high-resistivity substrate and the realization of the transition would require only the implementation of the radial stub from the MMIC perspective. The finline slot can either be machined in a separate metal shim similar to the presented work or it can be patterned on the back metal layer of the chip if the technology provides such feature. Similarly to the WG probe presented in the previous section, a bed of nails is used to address the issue of undesired modes and the dimensions of the structure were selected based on the same criteria. In the following section, the measurement results of the realized transition are presented and compared to simulations.

Measurement Results and Summary

Fig. 3.8 shows photos of the machined mechanical split-block module with the bed of nails structure implemented in the top part of the module as shown

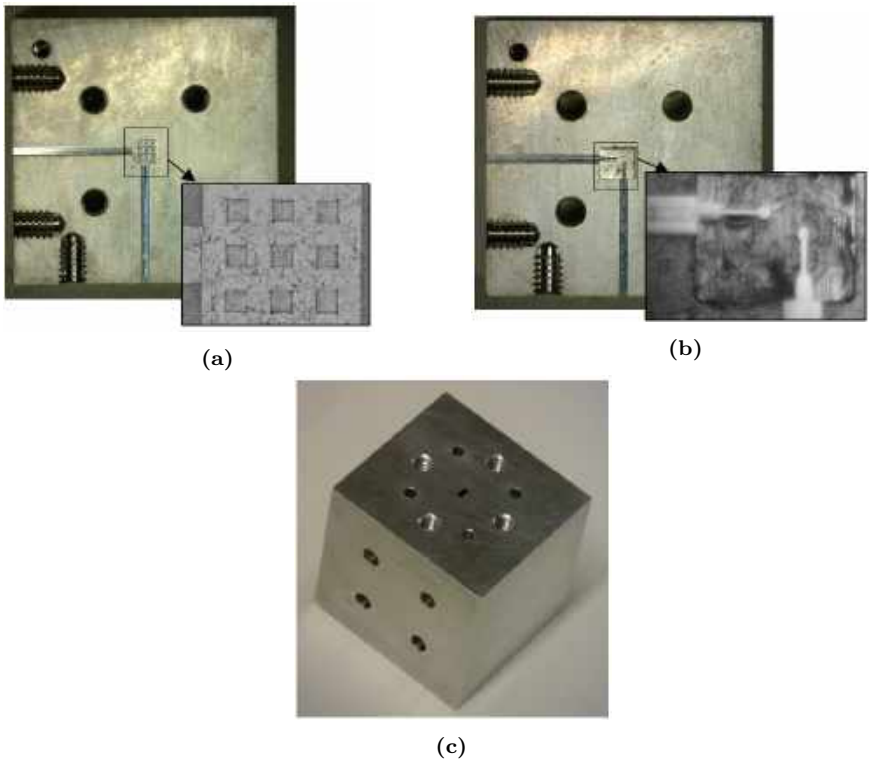


Figure 3.8: Photo of the fabricated mechanical split-block (a) Top part (b) Bottom part with the finline structure attached (c) Side view showing the standard WR-6.5 interface

in Fig. 3.8a and the unilateral finline structure with the bottom part of the module as shown in Fig. 3.8b. The module has standard WR-6.5 interfaces as shown in Fig. 3.8c.

The fabricated SiC chip is shown in Fig. 3.9. The radial stub occupies an area of only $35 \times 145\ um^2$ and the total test chip area is $1.8 \times 1.3\ mm^2$. Both the chip and the module are implemented as back-to-back to allow straightforward characterization and testing of the transition.

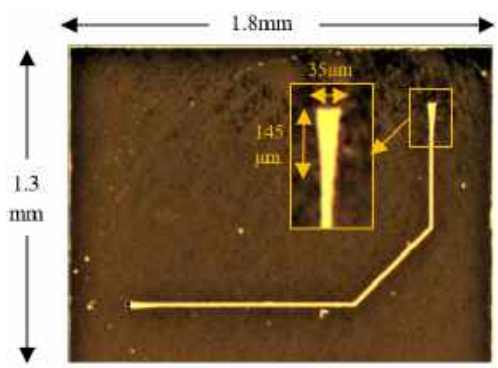


Figure 3.9: Photo of the fabricated SiC test chip

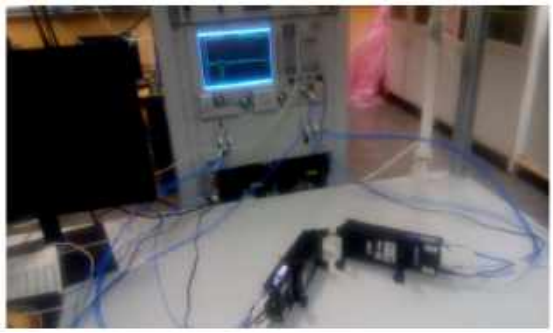


Figure 3.10: Measurement setup for the transition

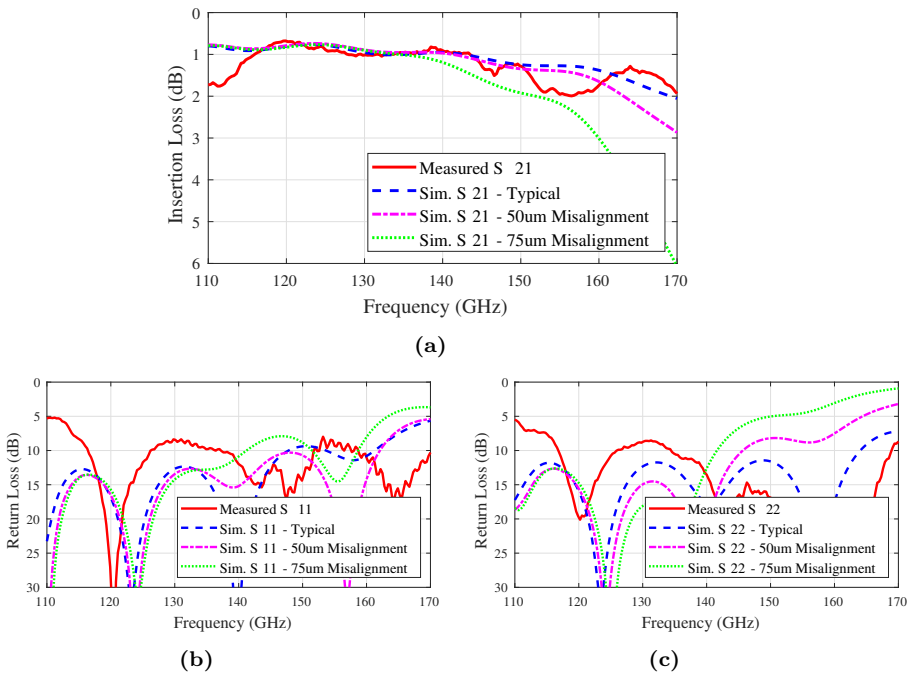


Figure 3.11: S-parameters of the finline transition (a) Insertion loss (b) Return loss at the input port (c) Return loss at the output port (Paper I).

The measurement setup is shown in Fig. 3.10 and it consists mainly of a VNA and two WR-6.5 frequency extension modules. Measurement results of the transition show a minimum insertion loss of only 0.7 dB per transition (i.e., 1.34 dB of loss for the back-to-back structure) and a maximum loss of 2 dB as shown in Fig. 3.11a. The presented loss includes the ohmic loss in the microstrip line and the losses in the split-block waveguide channels. The ohmic loss is estimated through simulations to contribute by 0.2 dB to the overall loss shown in Fig. 3.11a. The transition exhibits a very wide-band performance covering the entire D-band ranging from 110 to 170 GHz. The return losses of the transition at both sides are shown in Fig. 3.11b and 3.11c. The return loss

could be further improved using smoother tapering profile for the finline slot and by using through substrate vias if the technology provides such feature.

Simulations were performed using HFSS 3D EM simulator and were compared to measurements and the comparison show good agreement between both. The transition's sensitivity to misalignment was also simulated. Results show that the transition can withstand a misalignment of 50 um with slight degradation in bandwidth at the higher edge of the band. Moreover, for a 75-um misalignment, the transition can still maintain a maximum loss of 2 dB for up to 150 GHz. The presented transition does not require galvanic contacts nor special processing and can be used in most commercial MMIC technologies.

3.1.3 Novel Packaging Concept Suitable for Chip-to-chip and Chip-to-waveguide Interconnectivity

This section presents a novel approach that can be used for packaging MMICs in waveguide modules as well as for realizing chip-to-chip interconnectivity (Paper F). The technique relies on using an on-chip coupling structure that couples the signal to a quarter-wavelength cavity which in turn couples the signal to either a waveguide or another chip. The solution also utilizes a periodic EBG structure that guides the E-field and prevents leakage in undesired directions.

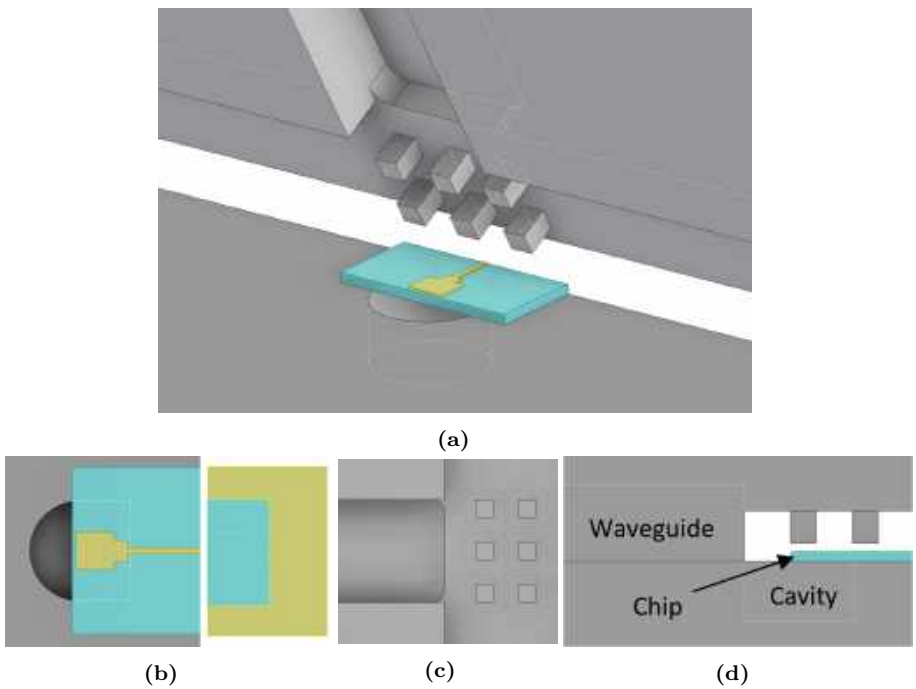
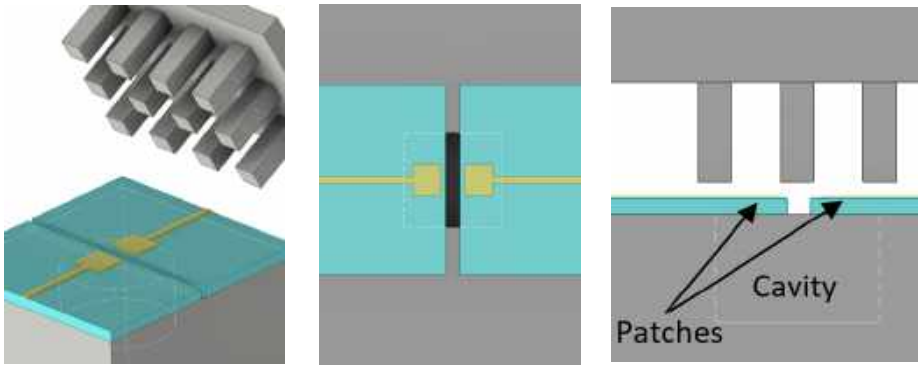


Figure 3.12: The proposed packaging solution (a) 3D view (b) bottom part showing the on-chip patch coupling to a cavity and the backside of the chip (c) the top cover showing the EBG structure and the waveguide channel (d) sideview of the assembled solution (Paper F).



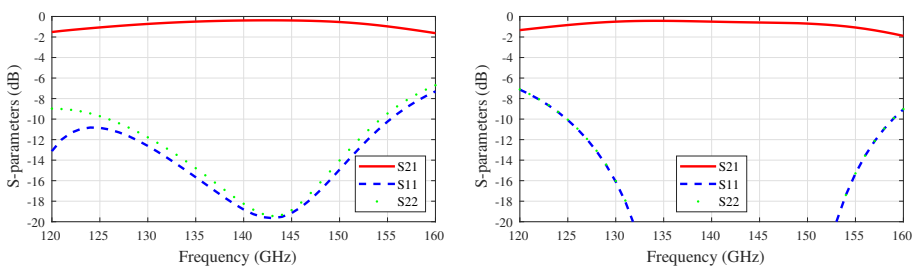
(a) (b) (c)

Figure 3.13: The packaging solution in the case of chip-to-chip interconnectivity (a) 3D view (b) bottom part showing the on-chip patches coupling to a cavity (c) sideview of the assembled solution (Paper F).

Design of the Interconnect

The proposed solution is implemented in two different scenarios. The first is to realize a chip-to-waveguide transition as shown in Fig. 3.12 while the second scenario is for chip-to-chip interconnection as shown in Fig. 3.13.

The principal of operation for both implementations is the same and relies on using an on-chip patch that couples the signal to a cavity underneath the chip. The cavity is implemented via CNC machining in the mechanical fixture housing the chip. The cavity then couples the signal either to a waveguide or another chip as illustrated in Fig. 3.12 and 3.13 respectively. A microstrip line is used to excite the patch with its ground plane implemented on the backside of the chip. However, the backside metal is removed in the area underneath the patch to allow coupling to the cavity through the chip's substrate as depicted in Fig. 3.12b.



(a) (b)

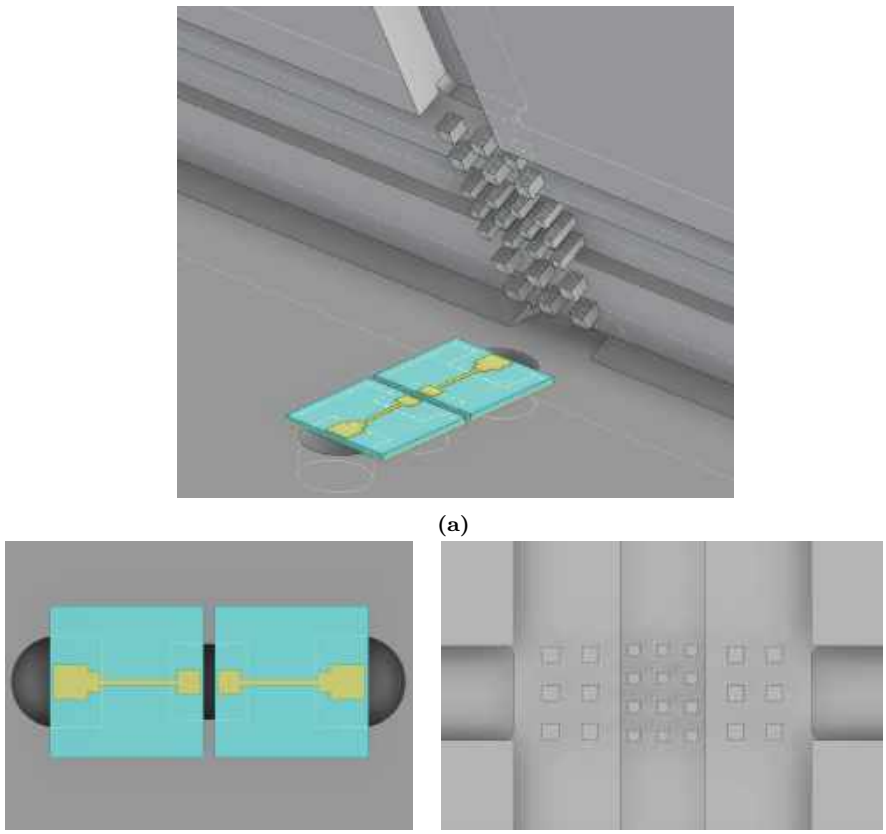
Figure 3.14: Simulation results for the proposed solutions (a) Chip-to-waveguide case (b) Chip-to-chip case (Paper F).

Similar to the previously-presented transitions, a periodic EBG structure realized by bed of nails is used to guide the E-field to the waveguide and stop undesired radiation to the air on the top side of the chip. The design parameters of the nails were optimized separately using 3D EM simulations to

achieve the best possible performance for each individual scenario.

Simulation results show that the chip-to-waveguide transition scenario exhibits a minimum insertion loss of 0.4 dB while the back-to-back chip-to-chip transition exhibits a similar loss of 0.5 dB as shown in Fig. 3.14.

Experimental Results



(a)

(b) **(c)**

Figure 3.15: Illustration of the test solution (a) 3D view (b) bottom part showing the chips and the coupling cavities (c) top part showing the bed of nails and the waveguide channels.

A full back-to-back solution consisting of a WG-to-chip-to-chip-to-WG was fabricated and assembled as illustrated in Fig. 3.15. The patches were implemented on a 100-um-thick GaAs substrate on 2 identical chips that were mounted back-to-back in a split-block waveguide module. The bottom part of the module housed the chips with 3 cavities for the 3 transitions as depicted in Fig. 3.15b. The top part of the module included the bed of nails structure and the waveguide channels as shown in Fig. 3.15c. The fabricated module is shown in Fig. 3.16. Alignment markers were implemented on the chip using the top metal layer to accurately align the patches to the openings of the cavities. Standard WR-6.5 interfaces were machined on both of the input and output ports of the module as shown in Fig. 3.16c.

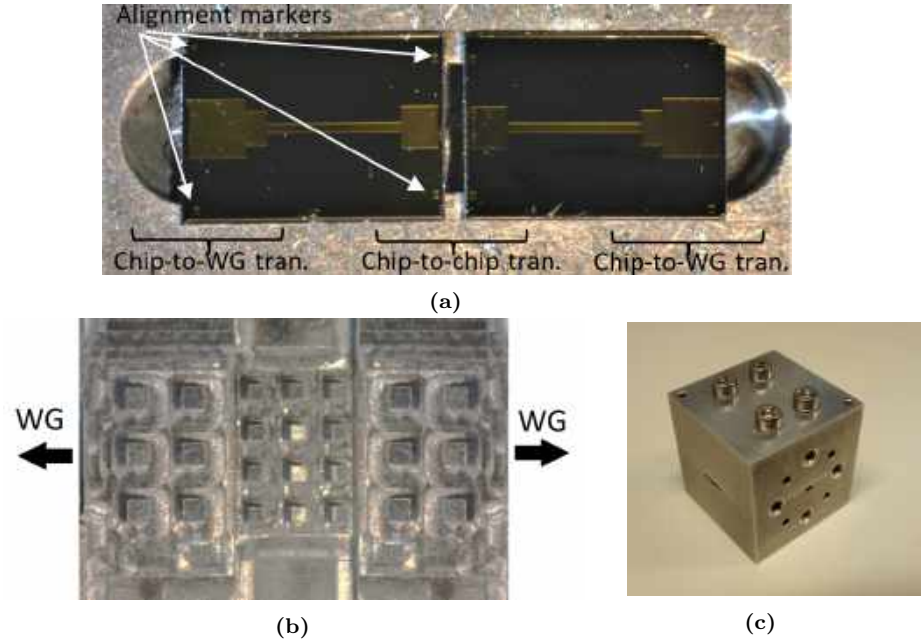


Figure 3.16: Photos of the fabricated module (a) bottom part showing the GaAs chips and the coupling cavities (b) top part showing the bed of nails and the WG channels (c) the assembled module with WR-6.5 interfaces (Paper F).

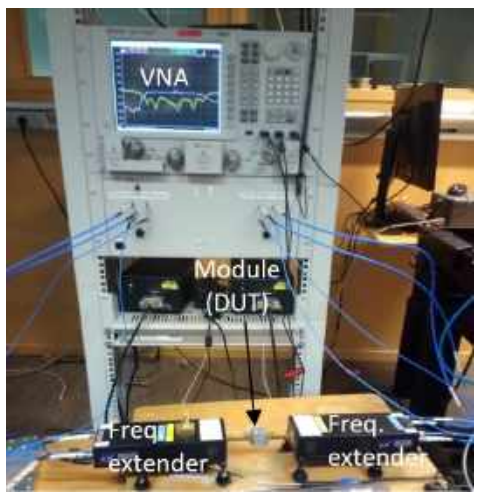


Figure 3.17: Measurement setup for the fabricated module (Paper F).

The measurement setup for the module is shown in Fig. 3.17 and it consists of two D-band waveguide frequency extenders connected to a 2-port VNA. The setup is calibrated to the waveguide outputs of the frequency extenders. Measurement results show that the cascaded 3 transitions combined (i.e., WG-to-chip-to-chip-to-WG) exhibit a minimum total loss of 2.4 dB as can be seen in Fig. 3.18, which translates to an estimated minimum loss per transition of

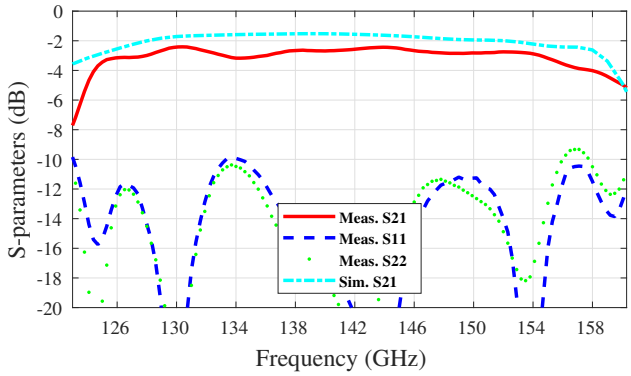


Figure 3.18: S-parameters for the full WG-to-chip-to-chip-to-WG lineup (Paper F).

approximately 0.8 dB. The 3-dB bandwidth of the cascaded lineup extends from 124 to 161 GHz. It's noteworthy that the losses in the transmission lines connecting the patches on the chip and the losses in the waveguide channels are not de-embedded and are part of the presented loss. The return loss of the transitions is also reported in the same figure and results show that the measured return loss is better than 10 dB over the same frequency band for both the input and output ports.

3.1.4 LTS-Based Waveguide Transition

In this section, a chip-to-waveguide transition is realized based on Linearly Tapered Slot (LTS). The slot is implemented on a 50-um-thick GaAs substrate and placed in the E-plane of an air-filled split-block waveguide. The transition shows low insertion loss and covers a wide frequency band. The proposed transition can be implemented directly on chip and provides direct coupling to the waveguide without the need of any intermediate solutions.

Design Methodology

The transition is based on LTS structure [40], [41]. Fig. 3.19 shows the proposed solution. The solution consists of an integrated tapered slot implemented on a 50-um-thick GaAs substrate. The structure is placed in the E-plane of an air-filled waveguide.

In order to overcome the area limitation imposed by the waveguide dimensions, a 100-um slot is made through the waveguide's sidewalls as shown in Fig. 3.19. The slot is used to accommodate the MMIC portion on-which the transition is implemented, that way the MMIC can have any arbitrary size independent of the waveguide dimensions. A wall of Back-Side Vias (BSV) is implemented around the slot to prevent field leakage within the substrate and act as a continuation of the waveguide backshort.

The transition is implemented in a commercial GaAs MMIC technology. The process provides two top metal layers and one back metal layer. The back metal has a dedicated mask and can be used to implement any structure. This feature allows the implementation of one of the sides of the slot on one of the

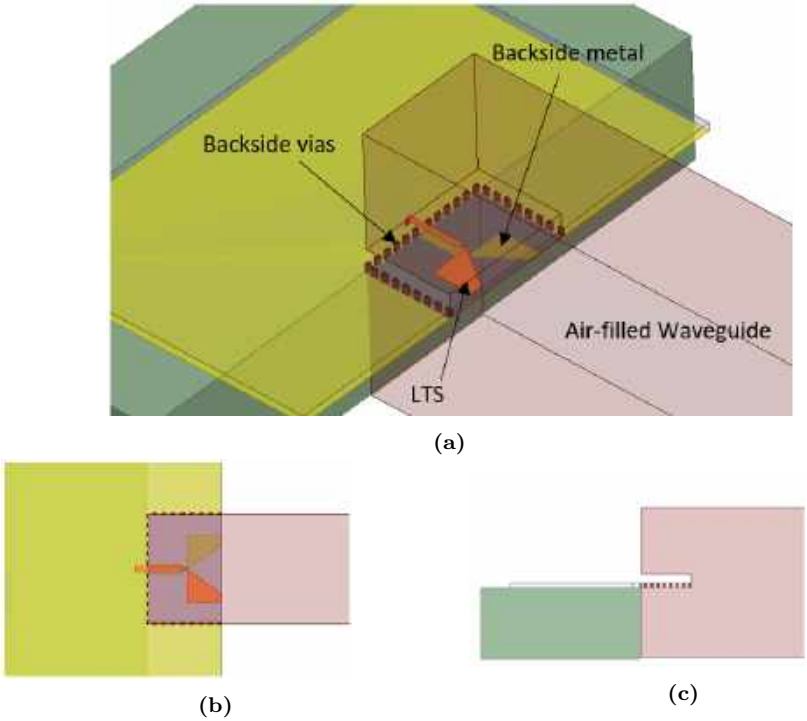


Figure 3.19: The proposed LTS-based solution (a) 3D view (b) Top view (c) Side view

top layers and the other side on the back layer and hence achieve better E-field confinement within the substrate and better coupling to the waveguide as can be seen from simulation results in Fig. 3.20.

The backside metal line feed for the slot is connected to the ground plane outside the transition so that it provides a differential to single-ended microstrip transformation. This approach eliminates the need of a Balanced/unbalanced conversion (Balun) and hence reduces the overall loss of the transition. A matching section is introduced between the slot and the 50-Ohm microstrip feeding line to compensate for the impedance mismatch between them.

Experimental Results and Conclusion

The fabricated LTS test chip is shown in Fig. 3.21. The structure was implemented in a back-to-back fashion to ease its characterization. A split-block waveguide module was CNC machined to house the test chip as shown in Fig. 3.22. The waveguide channel is split in the middle of its E-plane and the chip is mounted in the bottom part of the module and inserted by a quarter-wave distance into the channel. Waveguide flanges are machined on the sides of the module to provide standard connectivity.

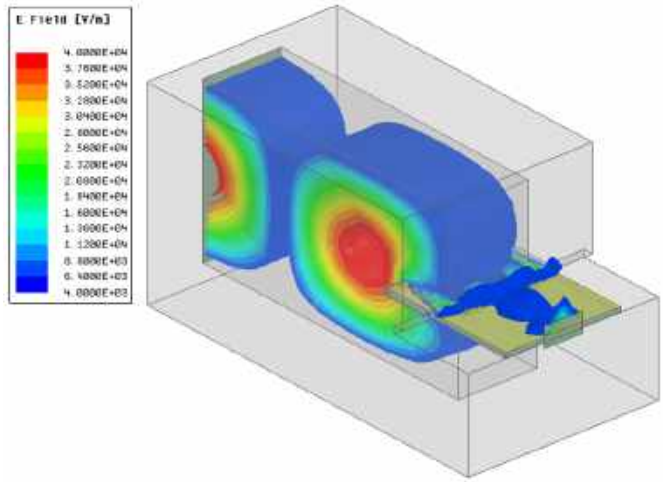


Figure 3.20: E-field magnitude distribution

(a) **(b)**

Figure 3.21: The fabricated LTS transition (a) top view (b) bottom view

(a) **(b)** **(c)**

Figure 3.22: Photo of the fabricated waveguide split-block module (a) top parts (b) bottom part (c) assembled module

The measurement setup used to characterize the transition is shown in Fig. 3.23. The module was connected to a pair of VDI's F-band frequency extenders at both the input and output which are in turn connected to a VNA. Two-port calibration was done to the waveguide interfaces of the frequency extenders.

Measurement results show that a single transition exhibits an average insertion loss of 1.7 dB over the frequency range 100 - 135 GHz as shown in Fig. 3.24a. Measurements were also compared to simulations in the same figure. It is noteworthy that loss of the microstrip transmission line connecting the

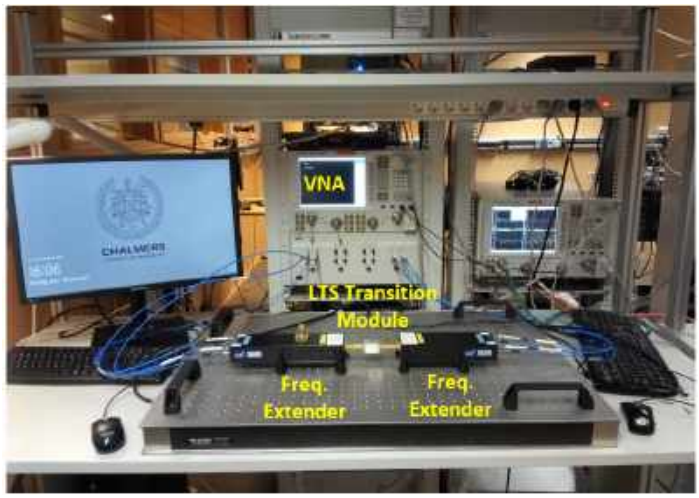


Figure 3.23: Measurement setup for the back-to-back LTS transition

back-to-back transition is de-embedded in the presented results.

The return losses at both the input and output ports are shown in Fig. 3.24b and 3.24c, respectively. Results show that the fabricated transition exhibits poorer return loss in comparison to simulations at a certain part of the frequency band. This was investigated, and is believed to be due to the discontinuity in the back-metallization layer that can be observed in Fig. 3.21b which was required to comply with the design rules dictated by the manufacturer regarding patterning of the backside metal layer. The discontinuity caused an impedance mismatch that resulted in the observed degradation in return and insertion losses at the higher part of the frequency band.

The transition's sensitivity to the air gap at the interface between the waveguide backshort and the top surface chip was also simulated as shown in Fig. 3.24. Results show that the transition can maintain good performance for air gaps up to 200 um, however, the performance starts to degrade and the bandwidth shrinks for gaps larger than that. Sensitivity to misalignment of the chip was also investigated earlier in Paper Q and results showed that the transition can withstand lateral misalignments of up to +/- 50 um with minor changes in performance.

A loss analysis was performed for the transition using 3D EM simulations and results are summarized in Table 3.1. Simulations show that the main contributors to the transition loss are ohmic losses and reflection losses. Other contributors include the loss due to undesired radiation through the air gap discussed earlier.

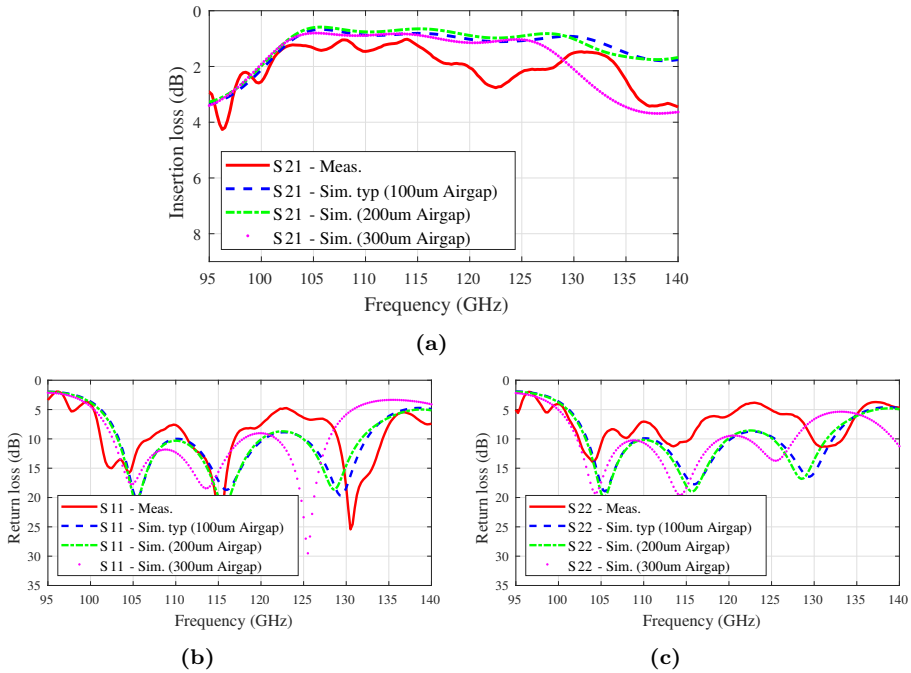


Figure 3.24: S-parameters of the LTS transition (a) Insertion loss (b) Return loss at the input port (c) Return loss at the output port (Paper K).

Table 3.1: Loss analysis for the LTS transition

Loss Source	Contribution to the Total Loss (dB)
Ohmic loss	0.4
Reflection loss	0.4
Loss due to undesired radiation	0.2

3.2 Integration in Si-based Technologies

3.2.1 Packaging Challenges in Si-based Technologies and Proposed Solutions in Literature

Nowadays, InP Heterojunction bipolar transistor (HBT) [29] and High-electron-mobility transistor (HEMT) [42] can provide gain in frequencies as high as 1 THz, with complete transceivers reported at up to 300 GHz [43], [44], [45]. However, the relatively high cost of such technologies restricts their use and pushes other low-cost alternatives such as Si-based devices to the front line. SiGe Bipolar complementary metal–oxide–semiconductor (BiCMOS) and HBT technologies have recently witnessed substantial performance improvement, achieving a power gain cut-off frequency f_{max} of up to 720 GHz [46]. Such technologies enable large-scale low-cost realization of MMICs in the THz range [47]. Similar to their III-V counterparts, multiple Si-based transceivers have been demonstrated in the frequency range 100 – 300 GHz [48], [49],

with data rates of up to 120 Gb/s. In addition to that, such technologies provide complementary metal–oxide–semiconductor (CMOS) transistors that are essential in meeting the demands of the digital IC market and hence, opens new possibilities and areas of application.

However, one major challenge facing Si-based technologies in the THz range is realizing packaging solutions. This challenge is even more difficult to address if integration with RF circuitry is required to be on the same chip. This is mainly due to the relatively low resistivity of Si compared to III-V semiconducting materials which makes integrating coupling structures on chip quite lossy in the case of Si. In addition, the metal density requirements superimposed by manufacturers prohibits the use of many of the packaging approaches presented earlier in this Chapter. However, several other packaging techniques are proposed in literature for Si-based technologies that exhibit reasonable performance while at the same time providing the advantage of integrating the solution with the RF circuitry on the same chip. One solution proposed in [50], [51], [52] is to use Localized Backside Etching (LBE) as shown in Fig. 3.25. The technique relies on removing the Si beneath a radiating structure using micromachining. Such approach helps improve the radiation efficiency of the structure. The technique was successfully demonstrated in a commercially-available BiCMOS SiGe technology using radiating structures such as end-fire Yagi-Uda antenna [50], double folded dipole [51], and differential patch antenna [52].

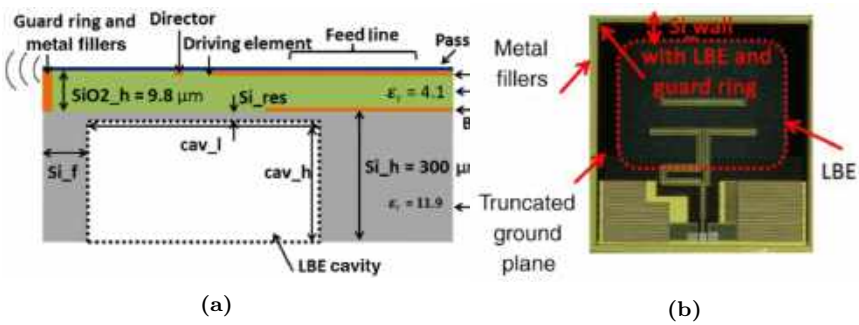


Figure 3.25: Illustration of the packaging concept based on localized backside etching (a) Cross-sectional view (b) Microphotograph of a Yagi-Uda antenna realized using the concept [50]

TSVs are also proposed in literature as a way to provide heterogenous integration through 3D interconnectivity as shown in Fig. 3.26. Their relatively low inductance makes them suitable for mmW and THz system packaging. In [53], annular-type TSVs were successfully demonstrated in two BiCMOS technologies with nodes of 0.25 um and 0.13 um using a via-middle approach.

Another approach to realize interconnectivity in Si technologies is SIW as discussed earlier [54], [55] and shown in Fig. 3.27. The approach is more suitable for high-resistivity Si processes and in such cases, losses as low as 0.4 dB/mm were reported in literature at D-band [55]. However, in such approach, an additional transition is needed to interface with standard air-filled waveguides, which could be a challenging task.

The above-mentioned packaging techniques are experimentally verified in

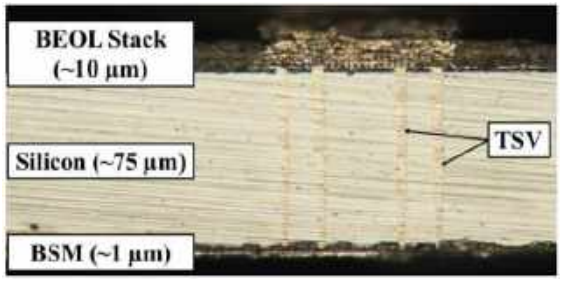


Figure 3.26: Cross-section view of BiCMOS IC with TSVs [53]

the mmW and sub-mmW ranges and hence paving the way towards higher integration and full system realization at those frequency ranges.

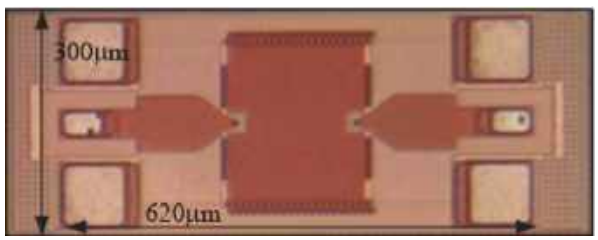


Figure 3.27: A 300-GHz substrate integrated waveguide transition [54]

3.2.2 H-Plane Slot Transition in SiGe MMIC Technology

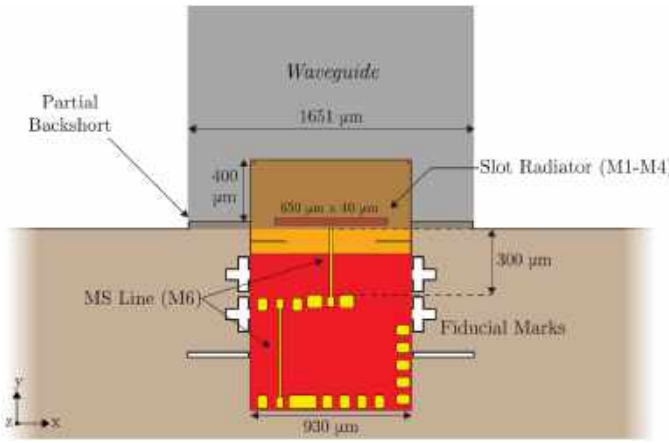
Introduction

This thesis proposes an in-line H-plane MMIC-to-waveguide transition to achieve interconnectivity between the two media. The transition is based on integrating a slot on chip as shown in Fig. 3.28. The choice of the slot topology is mainly motivated by the metal density requirements discussed earlier since a slot allows for metal filling and substrate doping requirements to be adhered to and hence provides a packaging solution that does not have special requirements and is suitable for high-volume production.

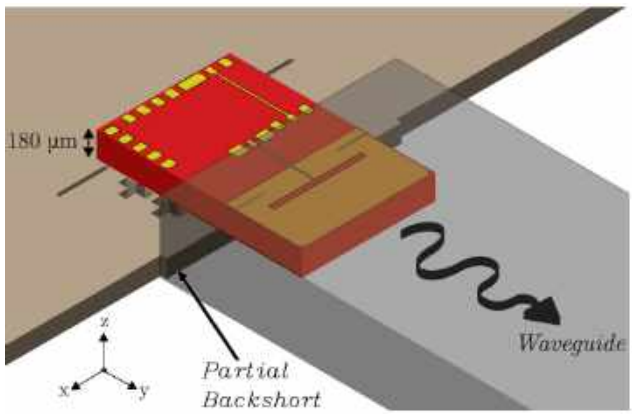
Moreover, designing the transition so that it is mounted in the H-plane of the waveguide allows doubling the width of the MMIC, compared to traditional E-plane mounting which increases the potential complexity of the circuity implemented in the MMIC and allows higher integration.

Technology Overview and Transition Design

The transition is realized in a 130 nm SiGe BiCMOS commercial technology provided by Infineon. The technology was recently used to demonstrate a D-band transceiver chipset (Paper L). The process offers a unity gain cut-off frequency f_t of 250 GHz, an f_{max} of 400 GHz, a breakdown voltage of 1.5 V [47] and a six-metal-layer Back-end-of-line (BEOL). The metal layers are separated by Si dioxide ($\epsilon_r = 4$) and Si nitride ($\epsilon_r = 6$) of thicknesses up to



(a)



(b)

Figure 3.28: Illustration of the packaging concept (a) Top view (b) 3D view (Paper B)

2.6 um. The conductivity of the Si substrate is 6.67 S/m, with a thickness of 180 um.

The transition was implemented by stacking the 4 bottom-most metal layers (M1–M4) while the topmost layer (M6) was used to form the microstrip line that feeds the slot as can be seen in Fig. 3.28. The E-field is coupled to the waveguide from the MMIC via capacitive coupling. A partial waveguide backshort is implemented in the platform on-which the MMIC is mounted to reduce undesired back-radiation. Fig. 3.29 shows the E-field 3D EM simulation result.

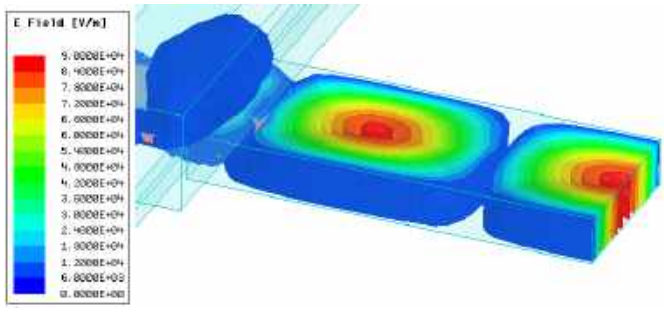


Figure 3.29: E-field simulation for the slot transition (Paper B)

A parametric analysis using Ansys HFSS was performed to tune and optimize the design parameters of the transition in order to minimize its insertion loss. The slot is excited using a microstrip line which in turn is connected to Ground Signal Ground (GSG) pads.

Experimental Results

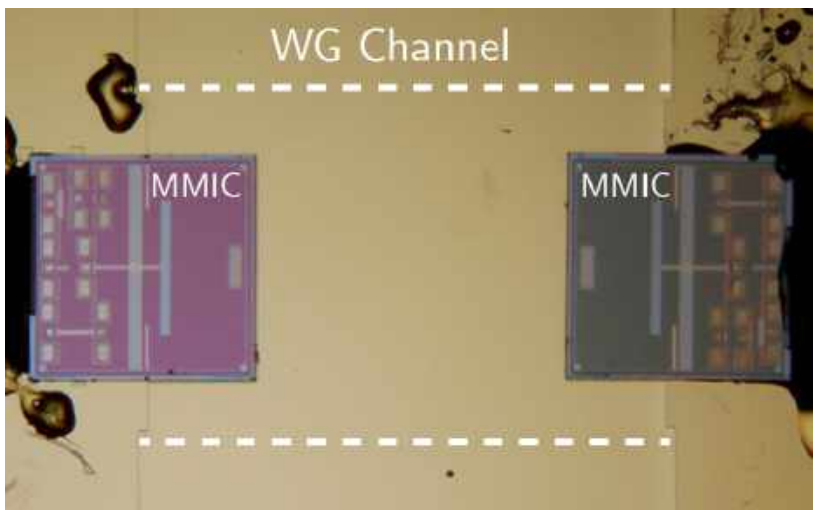


Figure 3.30: Photo of the fabricated test chips for the slot transition (Paper B)

The fabricated transition is shown in Fig. 3.30. Characterization of its performance was done using standard S-parameter measurements. CPW waveguide probes were used to excite the microstrip line and the calibration of the measurement setup was performed at the probe tips using a commercial calibration substrate (GGB CS-15 SOLT).

The measured S-parameters of the back-to-back transition are shown in Fig. 3.31. The transition exhibits a 3-dB bandwidth of 25 GHz centred at 148 GHz. The return loss at both ports is also measured and shown on the same figure. The insertion loss of the 300-um long microstrip feed line, which is part of the back-to-back loss shown in the figure, was measured separately to extract the loss of the single de-embedded transition, and was found to be ∼2–3 dB/mm,

while the pads add an additional 0.2 dB of loss. Such losses when de-embedded resulted in an average insertion loss of ∼5.8 dB per single transition, as plotted in the lower part of Fig. 3.31.

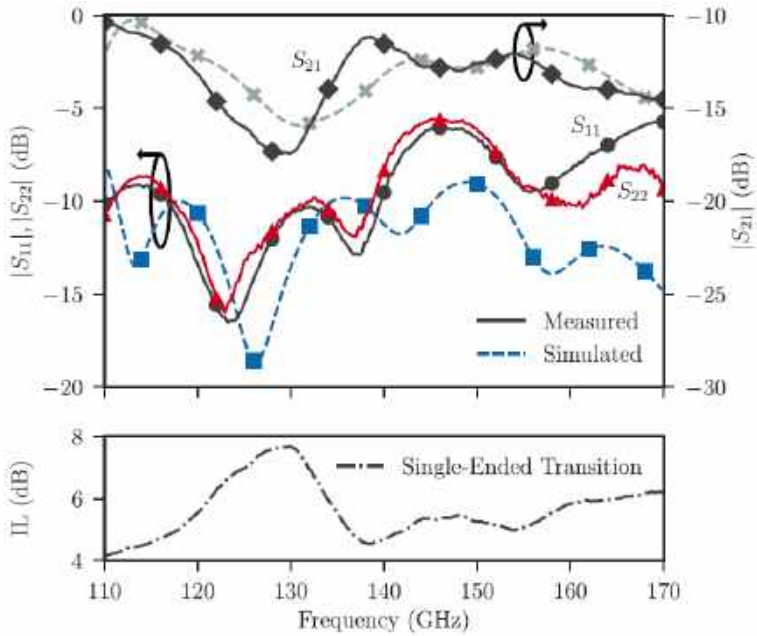


Figure 3.31: Measurement and simulation results for a back-to-back module, with a waveguide length of 3.4 mm. The estimated insertion loss of a single-ended transition is shown in the lower figure (Paper B)

It is noteworthy that the measured results show a downshift in frequency as compared to simulations. This could be due to inaccuracies in the simulation model. In addition, the observed spike in both the return and insertion loss at 125 GHz is believed to be due to the presence of substrate modes which was also confirmed via simulations.

The transition's sensitivity to positional tolerances was also analyzed. Offsets of +/-10 um in x-, y-directions and rotation of +/- 10° in the xy plane were simulated. The results are plotted in Fig. 3.32. Results show that the transition is not sensitive to the simulated range of offsets. The simulated transition exhibits an average insertion loss of 5.6 dB with return loss greater than 10 dB across the entire D-band and more or less maintains that performance across tolerances with only minor changes.

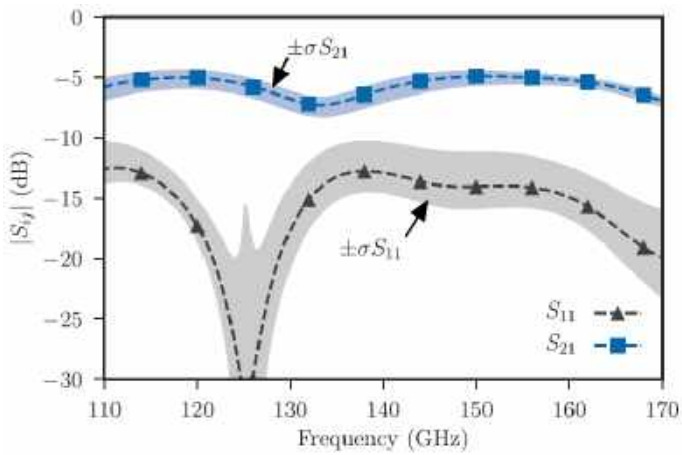


Figure 3.32: Simulated S-parameters of the single-ended chip to waveguide transition with nominal S-parameters indicated by the dashed traces while Shaded areas indicate the standard deviation of S11, S21 with +/-10 um and +/-10 degrees lateral offsets/rotation. (Paper B)

Loss Analysis

A loss analysis for the transition was performed using 3D EM simulations to determine the main contributors to its loss. Results show that most of the insertion loss of the transition is due to dielectric loss in the thick Si substrate as expected and shown in Table 3.2. Simulation with a lossless substrate reveals that the substrate dielectric loss accounts for 1.2 dB of the overall loss. Back-radiation from the slot, contributes an additional 0.8 dB of loss. This is mainly caused by the top open end of the waveguide in addition to back-radiation in the substrate. Ohmic losses in the microstrip feed line and pads account for 0.7 and 0.2 dB respectively. The remaining loss can be attributed to other contributors such as mismatches between the slot and waveguide and finite ground plane conductivity, etc.

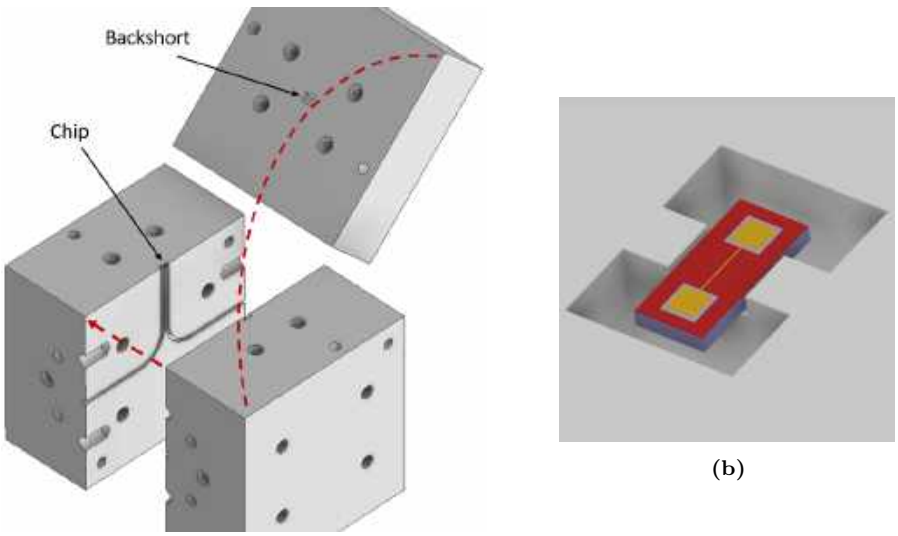
Table 3.2: Loss analysis for the H-plane slot transition

Loss Source	Contribution to the Total Loss (dB)
Dielectric loss in the substrate	1.2
Ohmic losses	0.9
Loss due to undesired radiation	0.8
Reflection loss	0.5

The transition's loss could be reduced by incorporating additional structures to block back-radiation such as the bed-of-nails structure presented earlier. Also, using a thinner substrate and/or a high-resistivity Si as a substrate material would help improve the transition's performance. A technology that provides TSVs would allow the implementation of an on-chip backshort and hence eliminate leakage in the substrate while preventing the excitation of substrate modes at the same time.

3.2.3 Rectangular Slot Ring Transition at H-band

This section presents another on-chip packaging concept implemented in the same SiGe MMIC technology used for the H-plane slot (3.2.2). The concept relies on implementing a rectangular slot ring mounted in the E-plane of a split-block waveguide (Paper G) as shown in Fig. 3.33. The slot couples to the waveguide through the SiGe substrate which has relatively high dielectric constant and hence guiding most of the field to the desired direction of the waveguide. In addition to that, a backshort was CNC machined and mounted on top of the chip to prevent any undesired radiation to air through the top side of the chip. The slot is excited using a microstrip line which is implemented using the top-most layer of the technology's BEOL (M6) with its ground plane at the fourth metal layer (M4) as described earlier in Sec 3.2.2.

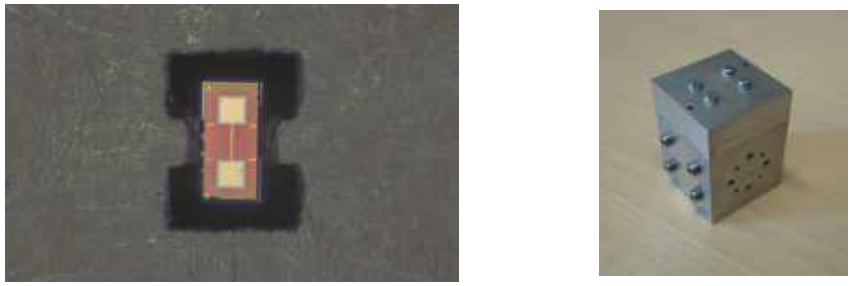


(a) (b)

Figure 3.33: Illustration of the concept (a) 3D view (b) Close-up of the chip (Paper G)

A back-to-back test structure for the transition was fabricated in addition to a split-block waveguide mechanical fixture to house the chip as shown in Fig. 3.34. The transition was designed to operate at H-band and hence the waveguide channels were chosen to have the dimensions of standard WR-3.4 rectangular waveguides. Moreover, in order to avoid exciting substrate modes at such high frequency band, the substrate was thinned down to a thickness of 130 um instead of the standard 180 um provided by the foundry. Alignment markers were implemented using the top metal layer in order to help align the chip accurately with respect to the waveguide channel in the mechanical fixture as shown in Fig. 3.34a.

Measurement results show that a single transition has an average insertion loss of 3.5 dB and a 3-dB bandwidth of 24% extending from ∼220 to 280 GHz as shown in Fig. 3.35a. The loss of the microstrip line feeding the slot is simulated and de-embedded in the presented results and it accounts for ∼0.5 dB of the original total loss. The return losses of the back-to-back transition



(a) (b)

Figure 3.34: Photo of the fabricated: (a) SiGe Chip (b) Waveguide housing module (Paper G).

was also measured at both the input and output ports and are reported in Fig. 3.35b and Fig. 3.35c, respectively. The transition's sensitivity to misalignment was also simulated and results show that the transition can withstand lateral misalignments of up to +/-100 um with reasonable degradation in performance as can be seen from Fig. 3.36.

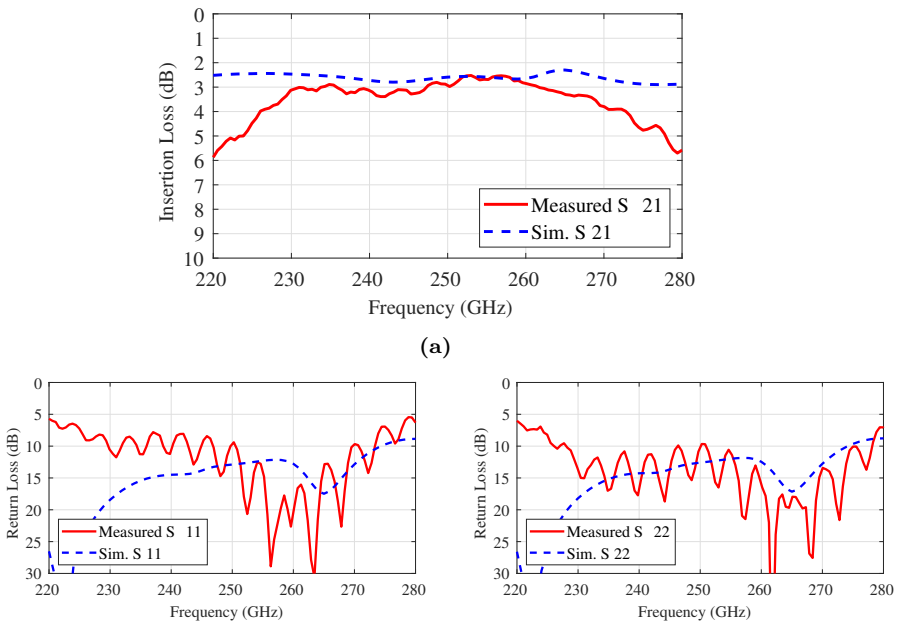


Figure 3.35: S-parameters of the slot ring transition (a) Insertion loss of the single transition (b) Return loss at the input port (c) Return loss at the output port (Paper G).

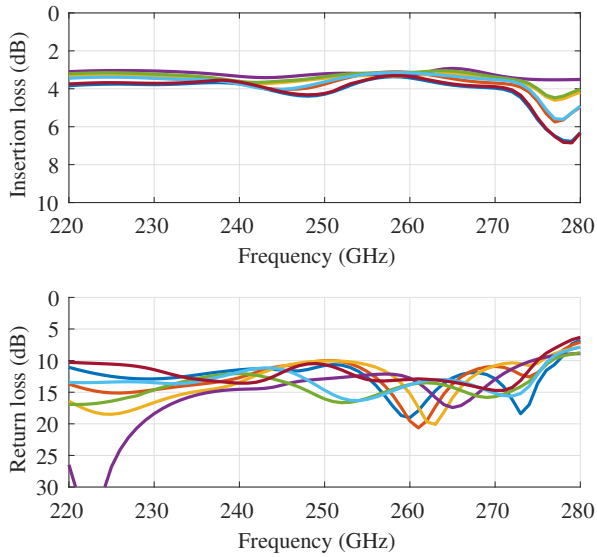


Figure 3.36: Simulated S-parameters of a single transition with +/-100 um lateral offsets. (Paper G)

Chapter 4

Demonstration of the Proposed Solutions in Active Circuits and Systems

4.1 E-plane Waveguide Probe in a Fully integrated D-band Receiver

4.1.1 Receiver Design

The E-plane waveguide probe presented in Section 3.1.1 is integrated in a D-band Rx on the same chip. The technology used to realize the Rx is a 250-nm InP DHBT technology [56] which offers an f_T of 350 GHz and an f_{max} of 650 GHz. Fig. 4.1 shows a block diagram of the Rx circuitry which consists of an LNA, an in-phase/quadrature (I/Q) downconverting mixer, and a frequency tripler at the Local oscillator (LO) port. The LNA has three common-emitter stages providing 20 dB of gain. The waveguide probe is connected to the input of the LNA while the output is connected to double-balanced Gilbert cell mixers with differential LO phase shifter [5], [57]. The external LO signal provided to the Rx is in the frequency range 36 – 56 GHz which is then multiplied by three using an on-chip frequency tripler [58] to provide D-band LO drive to the fundamental mixers. Using integrated LO tripler allows supplying a relatively low frequency externally at the LO port which simplifies the packaging of the MMIC by allowing the use of a simple bondwire interface and that port. The output of the tripler is connected to a bandpass filter to remove any unwanted harmonics. The Rx MMIC provides differential I and Q signals which are DC coupled while the LO signal is single-ended which is converted to a differential signal internally using an on-chip balun. Decoupling capacitors are used on the DC bias lines to avoid any unwanted feedbacks.

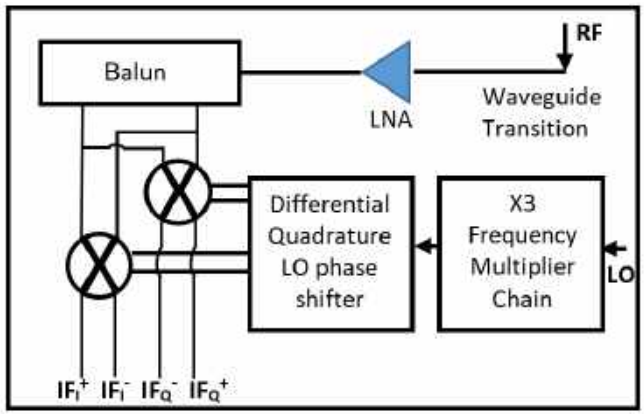
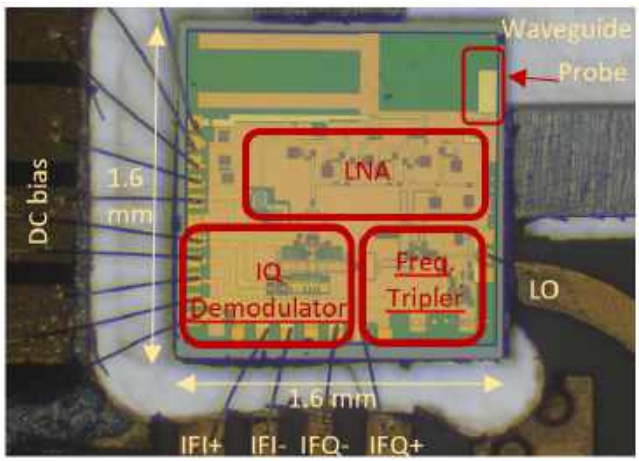
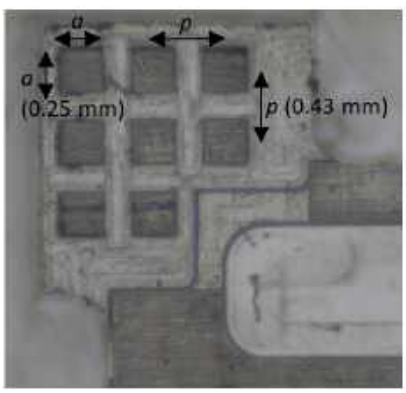


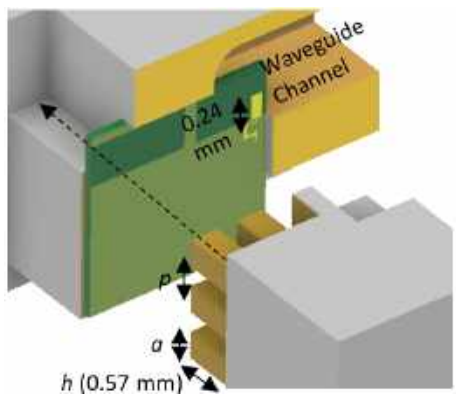
Figure 4.1: Simplified block diagram of the realized I/Q receiver (Paper A).



(a)



(b)



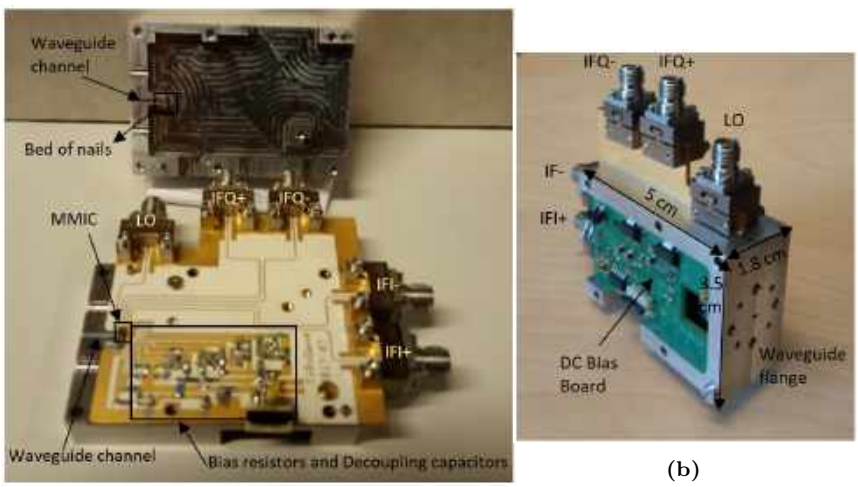
(c)

Figure 4.2: The D-band Rx module (a) Photo of the fabricated Rx MMIC housed in the bottom part of the module (b) Photo of the bed-of-nails structure machined in the top part of the module (c) Illustrative exploded view of the module's assembly (Paper A).

The photo of the fabricated Rx MMIC is shown in Fig. 4.2a. The MMIC is mounted in the E-plane of the split-block waveguide module. The technology's BEOL offers 4 top metal layers (M1-M4) and one backside layer. The probe and its microstrip feed line are implemented on the top-most metal layer M4 while the ground plane is implemented on M1 which is also connected to the back-side metal using BSVs that go through the substrate. The area of the chip that is inserted into the waveguide was cleared of all metal layers to avoid any perturbation to the E-field. The probe dimensions were chosen so that the width can provide a 50-Ohm impedance to the LNA as the LNA was originally designed to interface with a 50-Ohm source impedance while the length was chosen to be a quarter wavelength at the center of D-band as explained earlier in Chapter 3.

The Rx module also includes the bed of nails structure presented earlier which is CNC machined in the top part of the module as can be seen in Fig. 4.2b. Similar dimensions to the ones presented in Chapter 3 were used for the structure. It is noteworthy that the Rx MMIC utilizes one of the top metal layers (i.e, M1) as a ground plane which means that the bed of nails structure are going to be only effective in the circuit cavity above that layer.

A photo of the whole split-block Rx module is shown in Fig. 4.3. The bottom part houses the MMIC and a PCB that provides DC, IF and LO signals to the MMIC. The module has a standard WR-6.5 waveguide interface and utilizes a DC bias board to regulate the voltages supplied to the test PCB.



(a) (b)

Figure 4.3: Photo of the Rx module (a) Open split-block (b) Assembled module (Paper A).

4.1.2 Module Measurements

The four IF outputs of the module are combined using external hybrid couplers and the module is measured as an image reject Rx. The measurement setup used to characterize the module is shown in Fig. 4.4 and it consists of a 4-port VNA connected to a D-band waveguide frequency extender which in turn is

connected to the RF port of the Rx module while the LO and IF signals were provided directly using the VNA.

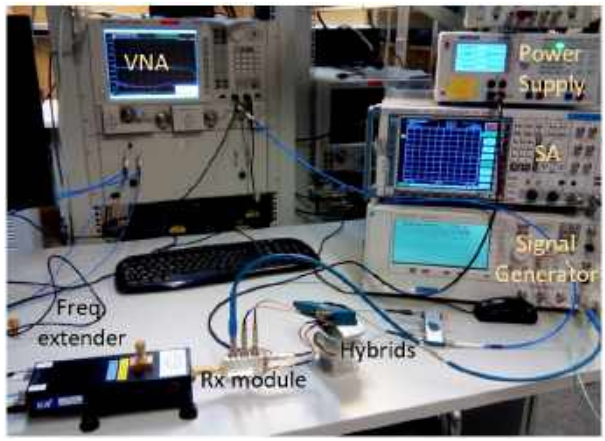


Figure 4.4: Measurement setup for the Rx module (Paper A).

A -40 dBm input RF signal was supplied to the Rx and its frequency was swept from 110 to 145 GHz. The LO frequency was also swept so that a fixed IF of 3 GHz is maintained. An LO power of +13 dBm was provided externally to the module. Measurement results show that the average Upper side-band (USB) conversion gain of the Rx module is 23 dB across the frequency range 110 - 145 GHz as shown in Fig. 4.5. Results are also compared to on-wafer measurements of an earlier generation of the Rx MMIC [5] and a comparable performance between both the packaged Rx module and the on-wafer measurements can be observed. It is noteworthy that although the Rx MMIC characterized in [5] has the same Rx circuitry as the one used for this work, it was realized in an earlier fabrication run and different biasing conditions might have been used for characterizing it. However, the comparison of both results can still be used to give a rough general assessment of the impact of packaging on the performance of the Rx but should not be used to provide exact accurate figures.

It was observed that the module covers less frequency band of up to 145 GHz only compared to the on-wafer case which has wider bandwidth. This was investigated, and is believed to be due to the lower LO power delivered to the packaged MMIC at the higher part of the band which is caused by the losses in the PCB trace and bondwire interface at the LO port.

Fig. 4.5 also shows the measured RF return loss and the conversion gain of the image band. The measured average image rejection (IR) is 19 dB across the frequency band 110 - 145 GHz. It is noteworthy that the amplitude and phase imbalances of the IF hybrid couplers are not de-embedded in the shown results, however, measurements of the couplers show that they exhibit low amplitude and phase imbalances that should not have large impact on the measured IR as shown in Fig. 4.6. This is verified by calculating the IR corresponding to the measured amplitude and phase imbalances of the couplers using the equation:

$$IR(dB) = 10 \times log(\frac{1+\gamma^2+2\gamma cos(\alpha)}{1+\gamma^2-2\gamma cos(\alpha)}) \tag{4.1}$$

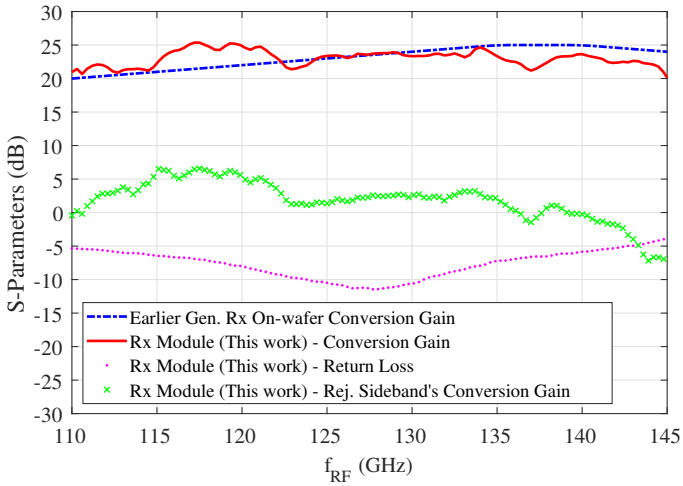


Figure 4.5: USB measurement results of the Rx module vs. on-wafer measurements (Paper A).

where γ is the amplitude imbalance and α is the phase imbalance. The equation yields an IR of 32 dB which is considerably higher than the measured IR of the module and hence is not limiting the measurement.

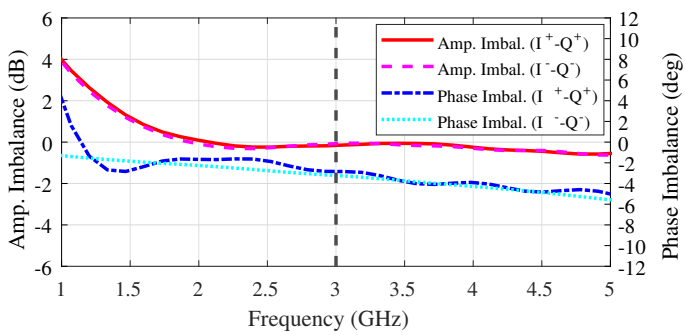


Figure 4.6: Measured amplitude and phase imbalances of the external IF hybrids (Paper A).

The noise figure (NF) was characterized using the Y-factor method. ELVA-1's ISSN-06 calibrated noise source was connected to the input of the Rx module using a WR-6.5 interface while the IF output was connected to an external LNA which in turn is connected to a spectrum analyzer (SA) as illustrated in Fig. 4.7.

The measurement was done by sweeping the frequency of the LO signal and at each point, the noise power level was observed using the SA at an IF of 3 GHz in two different cases, the first with the noise source ON, and the second with the noise source OFF. The noise factor of the entire line-up is then calculated using the Y-factor method summarized in the following equations:

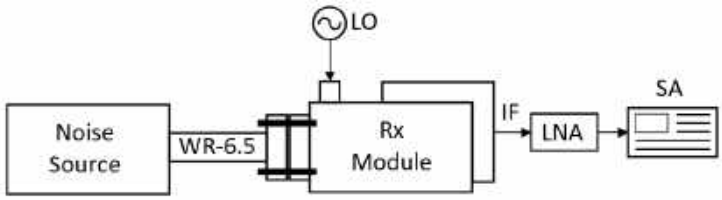


Figure 4.7: Noise figure measurement setup (Paper A).

$$Y = \frac{N_{ON}}{N_{OFF}} \tag{4.2}$$

$$F_{Tot.} = \left(\frac{T_H - Y \times T_C}{Y - 1}\right) / T_0 + 1 \tag{4.3}$$

Where N_{ON} and N_{OFF} are the measured noise powers when the noise source is in the ON and OFF states respectively, T_H is the noise temperature of the source, T_C is the OFF state temperature, and T_0 is the room temperature. The measured noise factor represents the combined noise of the Rx module, the LNA and the SA. In order to extract the noise factor of the Rx module only, both noise contributions of the LNA and the SA need to be de-embedded. The noise factor of the SA can then be calculated using the following equation:

$$F_{SA} = \frac{N_{SA}}{k \times T \times RBW} \tag{4.4}$$

Where N_{SA} is the noise floor of the SA, k is Boltzmann constant, T is the temperature in Kelvin and RBW is the resolution bandwidth of the SA.

The impact of the noise of the LNA and the SA is then corrected for using Friis equation which allows extracting the NF of the Rx module only as follows:

$$NF_{Rx} = 10 \times log\left(F_{Tot.} - \frac{F_{LNA} - 1}{G_{Rx}} - \frac{F_{SA} - 1}{G_{Rx} \times G_{LNA}}\right) \tag{4.5}$$

Where F_{LNA} is the noise factor of the LNA, F_{SA} is the noise factor of the SA while G_{Rx} and G_{LNA} are the gains of the Rx module and the LNA respectively.

The NF of the Rx that was calculated using the measured noise powers and equations 4.2 - 4.5 and the result is shown in Fig. 4.8. Results show that the minimum NF is 8.4 dB and the average is 10.6 dB over the frequency range 111 - 145 GHz. The NF of the module is also compared with simulations of the Rx MMIC without the use of the packaging solution and it can be clearly seen that packaging did not have high impact on the overall NF of the Rx except for the bandwidth limitation caused by the lack of LO power after packaging as discussed earlier. The module consumes a DC power of 440 mW and its dimensions are $3.5 \times 5 \times 1.8\,cm^3$ ($W \times L \times H$) while the Rx MMIC dimensions are $1.6 \times 1.6\,mm^2$.

The demonstrated packaging solution has the advantage of being scalable to the sub-mmW and THz ranges as the waveguide transition is implemented in MMIC technology which is capable of realizing fine structures and hence will

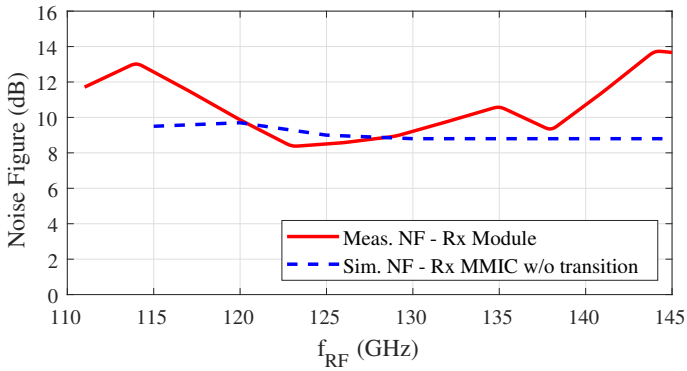
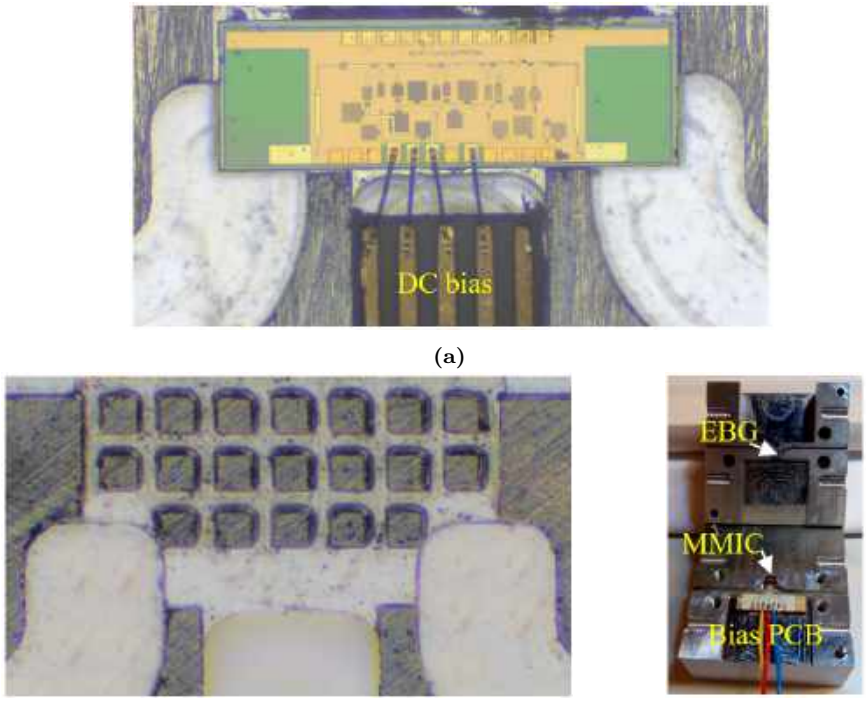


Figure 4.8: Measured noise figure of the Rx module vs. RF frequency (Paper A).

not face any fundamental limitations at the sub-mmW and THz frequencies unlike other traditional interconnectivity solutions such as wire bonding which would face considerable degradation in performance in terms of both the frequency of operation and bandwidth at such high frequencies. Moreover, the LO signal supplied to the packaged D-band Rx presented in this section can be fed using another waveguide transition if the LO frequency is higher or if a frequency multiplier is not used at the LO port and hence avoid galvanic contacts completely which leads to lower losses and wider bandwidth at the LO side. In addition, the bed of nails structure used to suppress the undesired modes can be implemented using Si micromachining instead of CNC machining which enables the realization of very small structures and hence push its frequency of operation to the THz range. Components operating up to 1 THz using Si micromachining were successfully demonstrated in [59] showing that there is no fundamental limitation to extend the presented packaging solution to the sub-mmW/THz range.

4.2 Demonstration of the E-plane Waveguide Probe in a D-band Amplifier



(a) (b) (c)

Figure 4.9: Photo of the fabricated D-band amplifier module (a) Bottom part housing the amplifier MMIC (b) Top part showing the machined EBG structure (c) The assembly of both parts of the module (Paper H).

The same packaging concept presented in 4.1 is also used to package a D-band amplifier MMIC using the same technology. The fabricated chip is shown in Fig. 4.9a and it consists of four common-emitter stages with both input and output connected to waveguide probes on the same chip. Similarly, a bed of nails is employed in the top part of the amplifier's module to suppress unwanted modes as can be seen in Fig. 4.9b. A PCB that is housed in the bottom part of the module in order to provide DC bias to the amplifier with the DC lines decoupled.

The measurement setup for the amplifier is shown in Fig. 4.10 and it consists of a VNA connected to a pair of WR-6.5 frequency extenders. The setup is calibrated to the waveguide interfaces of the frequency extenders.

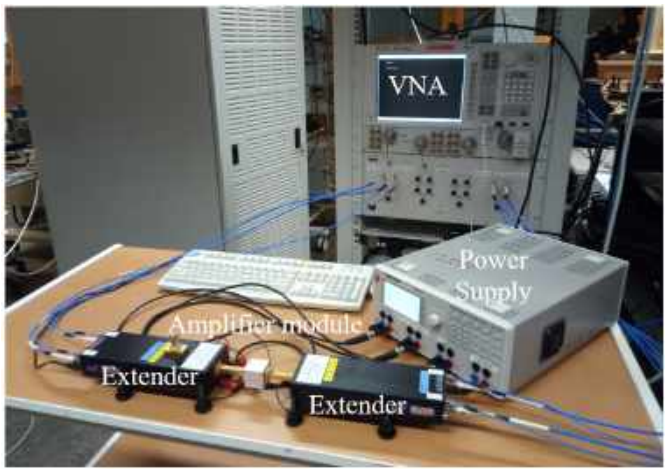


Figure 4.10: Measurement setup for the amplifier module (Paper H).

Fig. 4.11 shows the measurement results. The amplifier has a maximum gain of 18.5 dB and covers a 3-dB bandwidth of 20 GHz over the frequency range 110 – 130 GHz. The reverse isolation of the amplifier is also measured and it has an average of 41 dB over the same frequency band. The input and output return losses of the amplifier module are also measured and compared to on-wafer measurements as shown in Fig. 4.12. Results show that the waveguide probe does not have large impact on the amplifier's return loss, and hence it indicates that the amplifier maintains similar input and output impedances.

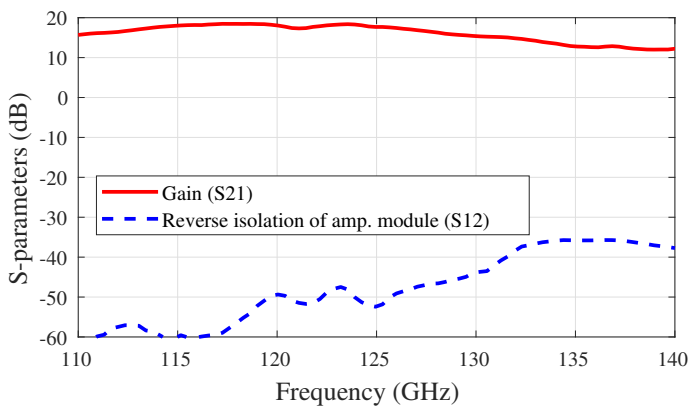


Figure 4.11: Measured gain and reverse isolation for the amplifier module (Paper H).

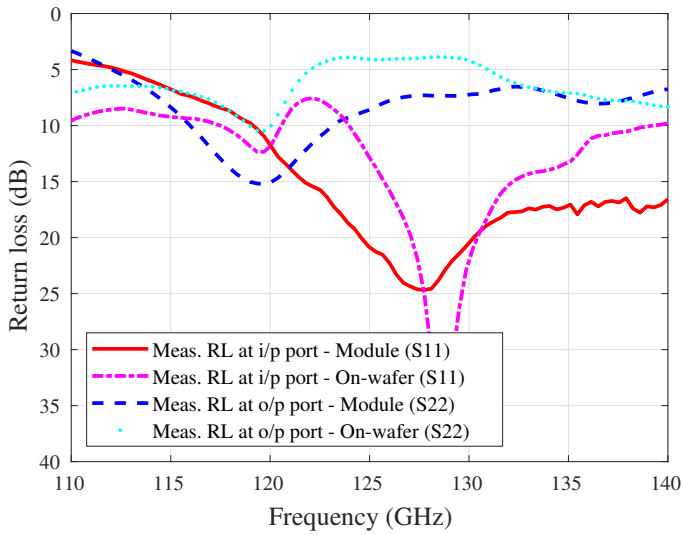


Figure 4.12: Measured return loss at both the input and output ports (Paper H).

4.3 H-Plane Slot Transition in D-band SiGe Transceiver Modules

4.3.1 Transceiver Design

The H-plane slot transition presented in Chapter 3 is used to package a fully-integrated transceiver chipset at D-band. The transceiver modules are used in this thesis as a demonstration of the packaging concept. The MMICs used in the modules are fabricated in Infineon's 130 nm SiGe BiCMOS technology described in detail in Section 3.2.2. The technology possesses high-frequency capabilities that support high linearity and output power for +100 GHz circuits.

The transmitter (Tx) MMIC consists of an integrated frequency sixtupler at the LO port, a single-balanced mixer, a 6-stage power amplifier and the H-slot MMIC-to-waveguide transition, all integrated on the same chip (Paper S). The Rx MMIC utilizes the same waveguide transition at its input, which in turn is connected to an LNA. The same sixtupler circuitry is used for the Rx LO. The downconverting mixer is a single-stage transconductance mixer in common-emitter configuration.

4.3.2 Modules Assembly and Packaging

A photo of the assembled module is shown in Fig. 4.13. The MMIC is placed on a cushion on a Si platform and glued to it using epoxy. The MMIC is partially inserted into a micromachined waveguide at the D-band signal interface. The Si platform on which the MMIC is mounted also provides DC, IF and LO connections to the MMIC via bondwires. The complete assembled module is shown in Fig. 4.14. The Si platform along with the MMIC are mounted on a PCB to provide fan-out for the DC and signal traces which in turn is

supported by a metal fixture containing a transition between the micromachined waveguide and a standard WR-6.5 waveguide interface.

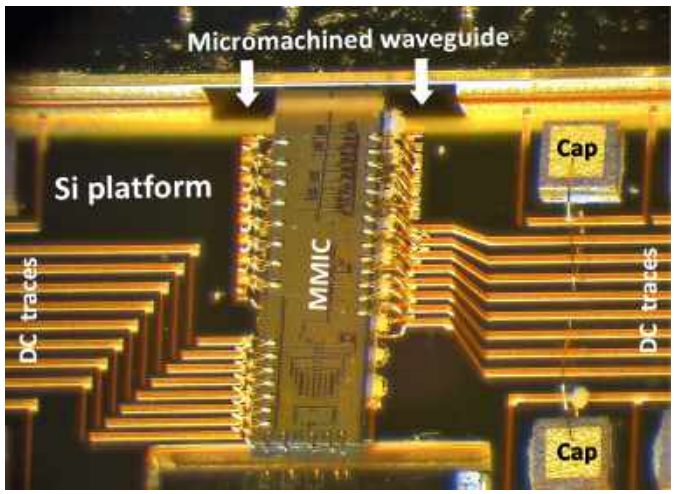


Figure 4.13: A close-up photo of the assembled transceiver module (Paper L).

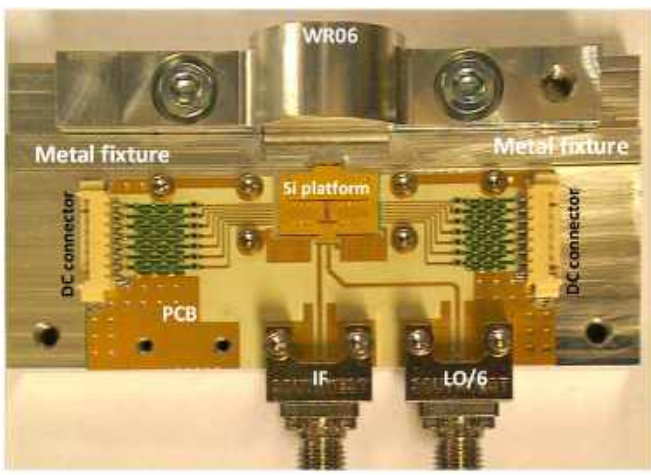
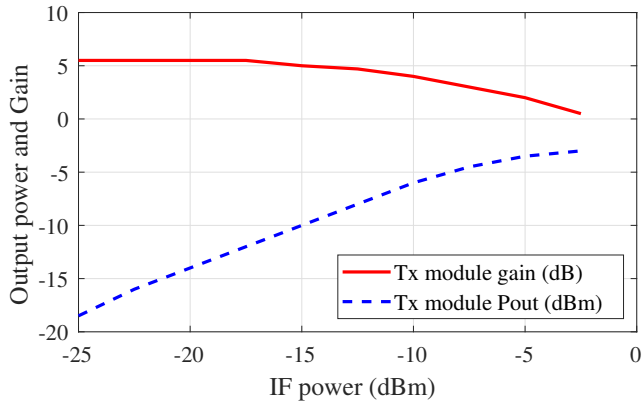


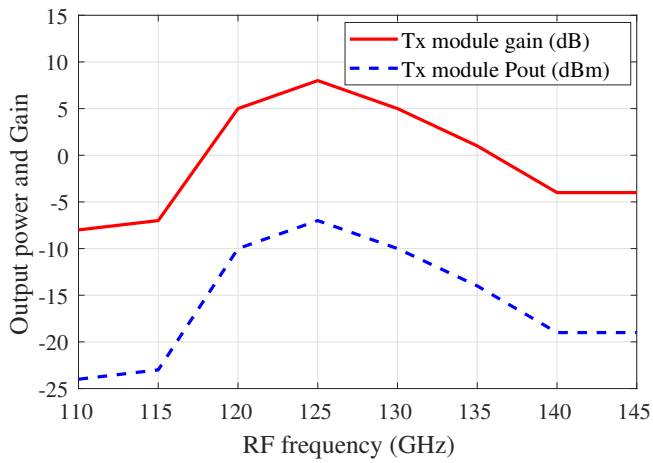
Figure 4.14: The complete assembled transceiver module (Paper L).

4.3.3 Demonstration of the Modules

A sinusoidal signal is used first to characterize the modules. An LO signal of +10 dBm power is fed to the frequency sixtupler. An IF of 1.3 GHz is chosen due to the bandwidth of the commercial sub-harmonic mixer used in the measurement setup.



(a)

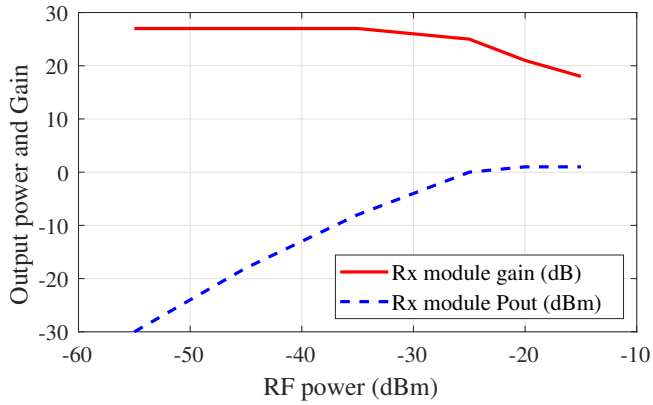


(b)

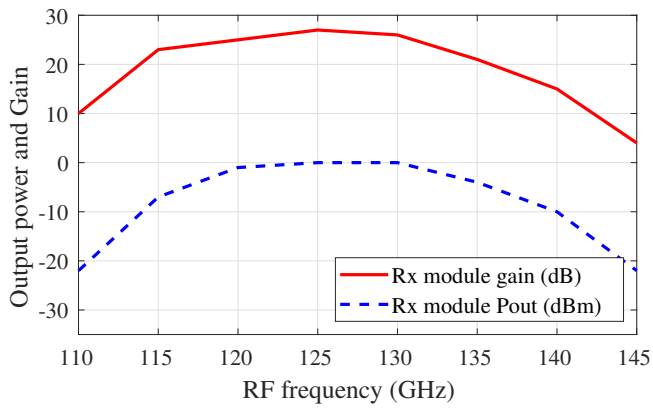
Figure 4.15: Measurement results for the Tx module (a) Output power and gain vs. input power (b) Output power and gain vs. RF frequency (Paper L).

Figure 4.15 shows the USB conversion measurement results for the Tx module. Results shows that the Tx exhibits a saturated output power of -2.9 dBm. The Rx module is measured using a Rohde and Schwarz ZVA67 VNA with a Z170 frequency extender that is used to generate the D-band input signal. Measurement results show that the module has a peak conversion gain of 25 dB and a maximum IF power level of +2 dBm as shown in Fig. 4.16a. The input-referred 1-dB compression point is measured to be -25 dBm and the 3-dB RF bandwidth covers the frequency range 118 - 134 GHz as shown in Fig. 4.16b.

The Tx and Rx modules were also connected using their waveguide interfaces with a waveguide attenuator in-between them. The overall measured link gain is shown in Fig. 4.17. It is noteworthy that the peak gain position and the bandwidth are dependant on the bias condition. In this specific situation, the DC biases were chosen to maximize the gain around 130 GHz. The Tx and Rx modules consume 370 mW and 350 mW of DC power, respectively.



(a)



(b)

Figure 4.16: Measurement results for the Rx module (a) Output power and gain vs. input power (b) Output power and gain vs. RF frequency.

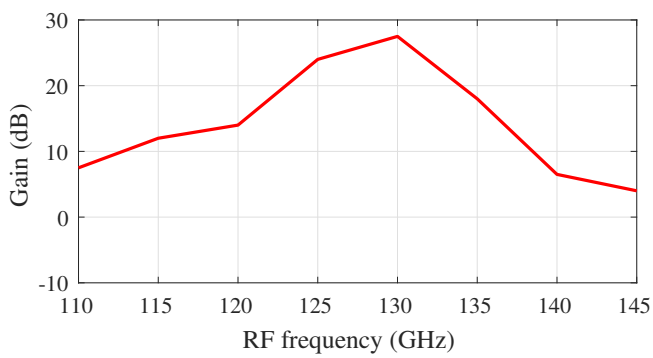


Figure 4.17: Measured link gain vs. RF frequency (Paper L).

The use of traditional bondwire interfaces to feed the IF and LO signals to the MMIC might restrict the transceiver architectures and frequency bands

suitable for the use of this concept similar to the E-plane waveguide probe concept. IF frequencies that are not suitable for bondwire interfaces need to be avoided. Higher multiplication factors for the LO signal may also be necessary when the frequency of operation approaches the sub-mmW/THz range which may limit the phase noise performance. The proposed transition presented in this thesis could also be used to feed high-frequency LO signals and hence avoid both higher multiplication factors and bondwire interfaces at the LO port completely.

This characterization of the proof-of-concept D-band Tx and Rx modules demonstrates that the waveguide transition works as expected. Moreover, the proposed packaging approach is scalable for frequency bands beyond D-band and serves as a milestone towards commercialization of such systems in the future.

Chapter 5

Utilizing the Commercially-available Packaging Technologies

Wafer-Level Packaging (WLP) has witnessed an increasing interest in the past decade. This is mainly driven by the increasing complexity of MMICs which require many input and output (I/O) interfaces in addition to integration between various technologies in a compact area to form a complete system. Conventional packaging techniques do not provide high integration and they exhibit poor performance in the mmW and sub-mmW ranges while WLP can provide higher integration in a smaller package [20], [23] as shown in Fig. 5.1.

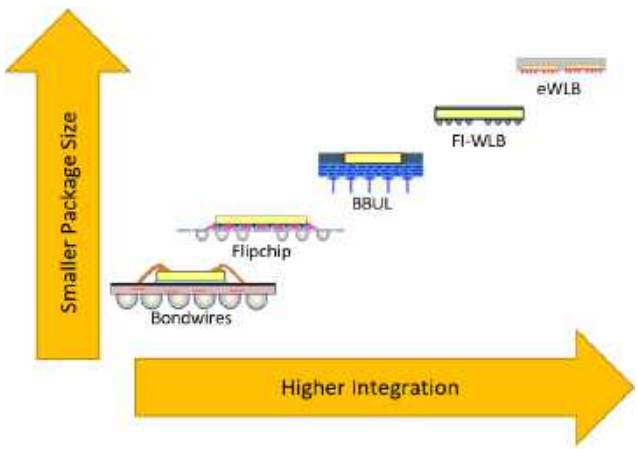


Figure 5.1: Evolution of packaging technologies (Paper C)

One strong candidate among such family of technologies is eWLB which provides an attractive low-cost packaging solution using BGA mountable module. eWLB technology serves as a system integration platform which is widely used nowadays for many applications [60], [61], [62]. eWLB provides superior electrical performance compared to traditional packaging approaches

due to the small size of its interconnections resulting in reduced parasitics. Moreover, the technology provides high integration and I/O density and the possibility to realize passive structures outside the MMIC using RDLs [20], [24].

Low-frequency interconnects in eWLB technology have been studied in [63] using standard BGA, however, such approach might not be suitable for systems operating above 100 GHz since the standard solder balls would exhibit high reactance at such frequencies [63] in addition to losses due to radiation caused by the discontinuities that the solder balls introduce along the RF path. For instance, the solder balls provided by the eWLB technology used in this thesis, which is detailed in the following section, show good electrical properties up to 100 GHz, however, their performance degrades quite dramatically after that frequency. This is due to two main reasons, the first is the high reactance that requires compensation, while the second and more prominent is the losses due to undesired radiation that comes from discontinuities along the CPW line as shown in Fig. 5.2.

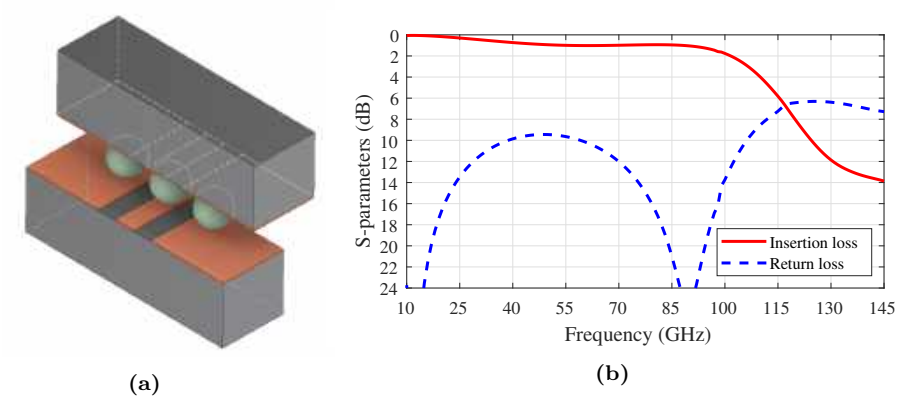


Figure 5.2: 3D EM simulations of the solder balls (a) The 3D model (b) Simulation results.

To overcome this challenge, this thesis proposes a different packaging approach that is based on realizing coupling structures in the eWLB instead of using solder balls. High-frequency interconnects have been proposed using such structures in literature [21]. The thesis investigates and proposes several solutions to realize similar interconnectivity from eWLB to standard waveguides instead by exploiting the technology's RDLs to realize such coupling structures at D-band. To the best of the author's knowledge, no waveguide interconnects above 100 GHz has been proposed before in eWLB technology.

5.1 Overview of eWLB Technology

The technology provides fan-in and fan-out areas with RDLs as shown in Fig. 5.3. The fan-in area is limited by the chip size, while the fan-out area extends beyond that, which is a unique feature in eWLB technology making it provide higher integration with higher interconnect density. This is made possible by the mold compound encapsulating the packaged chips, which enables the realization of the fan-out area that provides higher I/O count and the possibility to realize passive structures in the same package as discussed earlier.

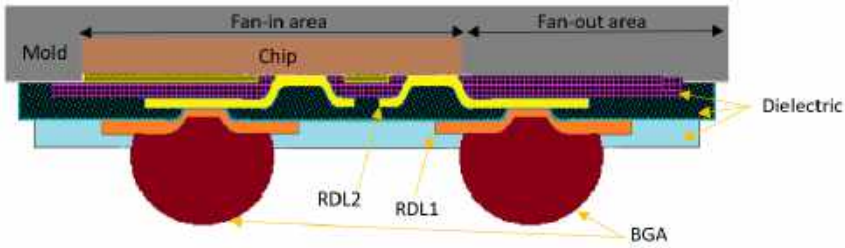


Figure 5.3: Cross-section of the eWLB package (Paper C)

The chip is placed upside down in the package encapsulated with the mold compound. The compound possesses good electrical properties with a loss tangent ($\tan \delta = 0.004$) and hence enabling the realization of relatively low-loss passives using thin-film technology [24]. The thin-film technology provides high precision at a relatively low cost with high design flexibility. The eWLB process used for the work presented in this thesis provides two thin-film RDLs separated by dielectric layers as shown in Fig. 5.3.

Both thin-film microstrip lines (TFMSL) [64], [65] and coplanar structures [66], [67], [68] can be realized using the technology's RDLs. TFMSL has the advantage of having the ground metallization act as a shield from the substrate while coplanar topologies allow easier connectivity to MMICs since the signal and ground connections are on the same level and can be provided in a GSG fashion that is compatible with the common interface for MMICs. Moreover, the performance of coplanar structures such as slot lines (SL) and coplanar waveguides (CPW) is less dependent on the thickness of the substrate compared to TFMSL and they can be realized using only one metal layer.

In following sections, generic approaches for implementing MMIC-to-waveguide transitions based on eWLB technology are presented with the support of experimental results.

5.2 Waveguide Transition Based on Patch Coupler

5.2.1 Transition Design

This thesis proposes using a microstrip-fed patch to couple the RF signal to a standard air-filled waveguide instead of using conventional BGA connectivity. The solution also includes a periodic EBG structure realized using mushroom patches to prevent leakage in undesired directions as discussed in Chapter 2, which also helps reduce the insertion loss of the transition.

Fig. 5.4 illustrates the proposed packaging solution which consists of an eWLB package, MMIC, PCB, and a standard WR-6.5 waveguide. A patch is implemented using the RDL which then couples the signal to a waveguide mounted perpendicularly to it, providing a non-galvanic transition. The proposed approach, however, suffers from undesired radiation at the interface between the patch and the waveguide due to the air gap between the eWLB surface and the waveguide opening. This gap is caused by the BGA

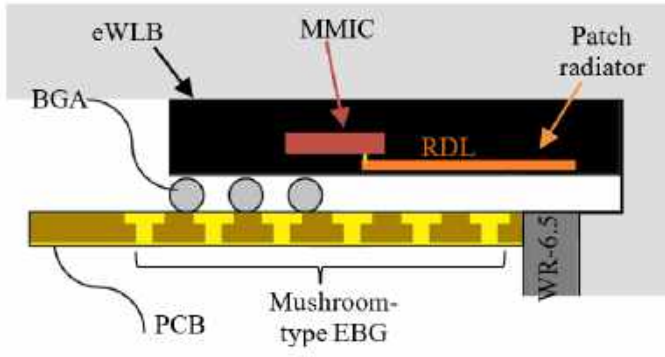


Figure 5.4: The proposed packaging concept (Paper E)

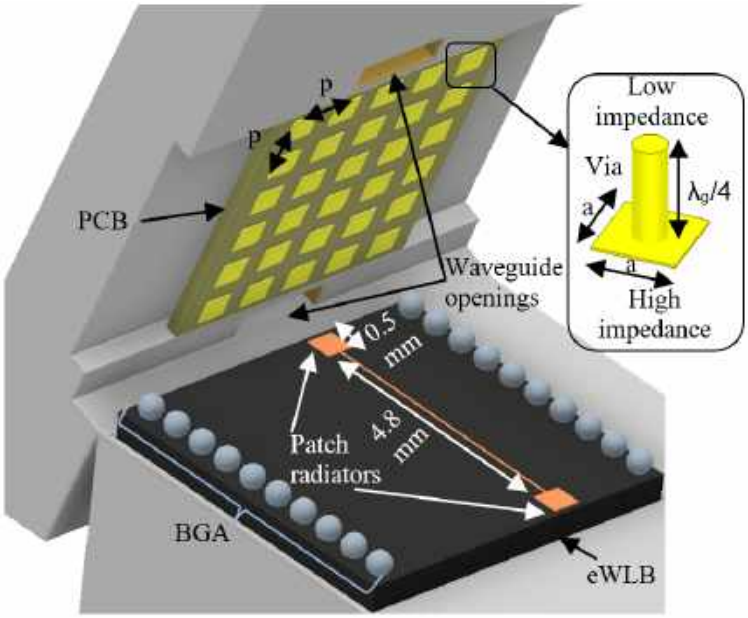
used in the technology to provide galvanic connections via the PCB which would cause field leakage at the interface and reduce coupling efficiency. To mitigate this issue, a mushroom-type EBG structure is implemented on the PCB on which the eWLB package is mounted. Moreover, the structure can provide parasitic mode suppression in case a ground plane or a PEC is used on the surface of the eWLB package. The simplicity of mushroom-type EBG and its compatibility with PCB technologies makes it suitable for eWLBs since it doesn't add a design overhead nor require extra components to be implemented as eWLBs are normally mounted on PCBs to provide DC and low-frequency connectivity.

The split-block waveguide module used to house the eWLB is shown in Fig. 5.5. The eWLB and PCB are mounted on opposite sides of the module. A back-to-back microstrip-fed patch is implemented on the eWLB's RDL as explained earlier.

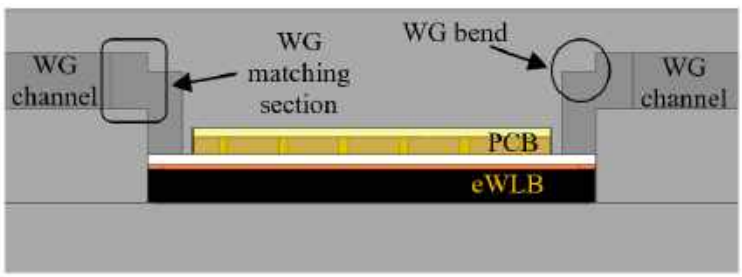
The patch's dimensions are chosen so that its length corresponds to approximately half wavelength at the centre of D-band while taking into account the dielectric constant of the mold compound. This results in an equivalent length that can be calculated using the equation $\lambda_0/(2\times\sqrt{\epsilon_r})$, where λ_0 is the wavelength in free space and ϵ_r is the relative permittivity of the mold which has a value of 3.2.

The mushroom-type EBG structure is implemented in the PCB which is mounted against the eWLB as shown in Fig. 5.5. The patch of the mushroom is implemented using the PCB's metal layer while the stem of the mushroom is implemented using vias to provide connectivity to the PCB's back metal which is grounded. The structure's size and period were chosen based on the criteria described in Chapter 2 to provide a high impedance boundary at D-band. This was also complemented with 3D EM simulations to verify and tune the performance of the structure to achieve the widest possible bandwidth.

The patch couples to a waveguide opening that is normal to its plane. The waveguide channel has a 90° bend and a matching section to improve the return loss. It's noteworthy that this work focuses on the implementation and characterization of the D-band waveguide transition part of the system since the conventional BGA-based connectivity is not within the scope of this thesis.



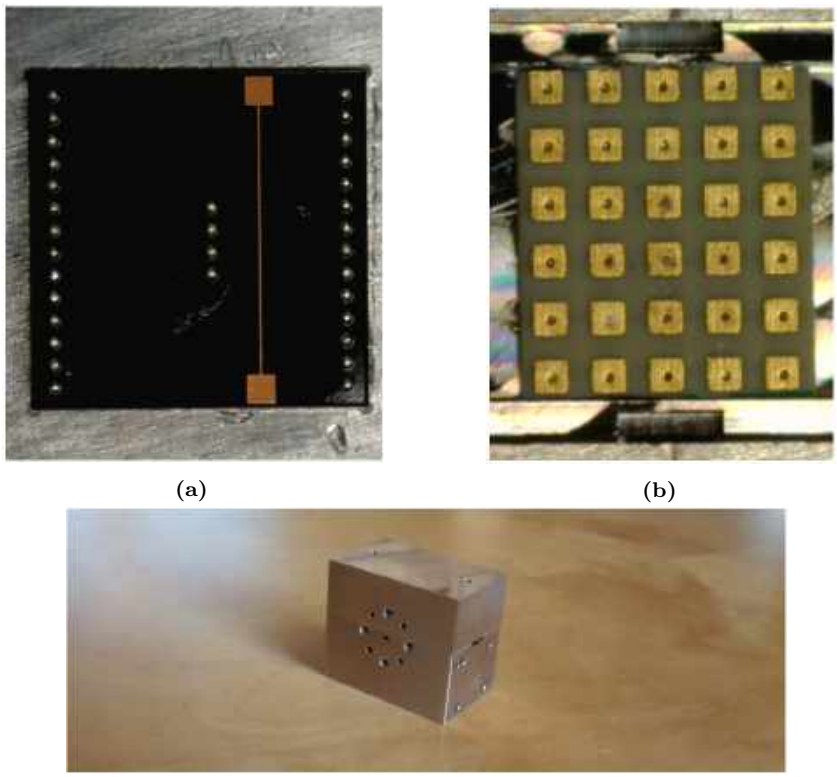
(a)



(b)

Figure 5.5: Illustration of the transition design (a) 3D exploded view showing the eWLB and the EBG structure (b) Cross-sectional sideview showing the waveguide channels (Paper E).

5.2.2 Experimental results



(a) (b)

(c)

Figure 5.6: Photo of the fabricated module (a) Bottom part with the mounted eWLB (b) Top part showing the PCB with the EBG structure and waveguide openings (c) Assembled module showing the standard WR-6.5 interfaces (Paper E).

Fig. 5.6 shows photos of the fabricated back-to-back transition module. The eWLB package is fabricated in Infineon's eWLB technology [20] while the PCB is fabricated in a simple 2-layer process with Roger's RO4350B laminate as the dielectric material separating the 2 layers. The split-block waveguide housing was fabricated using CNC machining with standard WR-6.5 waveguide interfaces.

Fig. 5.7 shows the measurement setup for the module and it consists of a pair of VDI's D-band frequency extenders connected to a 2-port VNA. The setup is calibrated to the waveguide outputs of the frequency extenders.

Measurements show that the single transition exhibits an average insertion loss of 2 dB over the frequency range 122 – 146 GHz as shown in Fig. 5.8. To the authors' knowledge, this is the lowest reported loss for a waveguide transition at this frequency band in eWLB technology. The loss of the microstrip line connected to the patch was simulated to be 0.4 dB/mm at D-band and it is de-embedded in the shown results. The return loss of the transition at both the input and output ports are shown in Fig. 5.9 and 5.10 respectively and results show that the transition has a minimum return loss of 9 dB and an

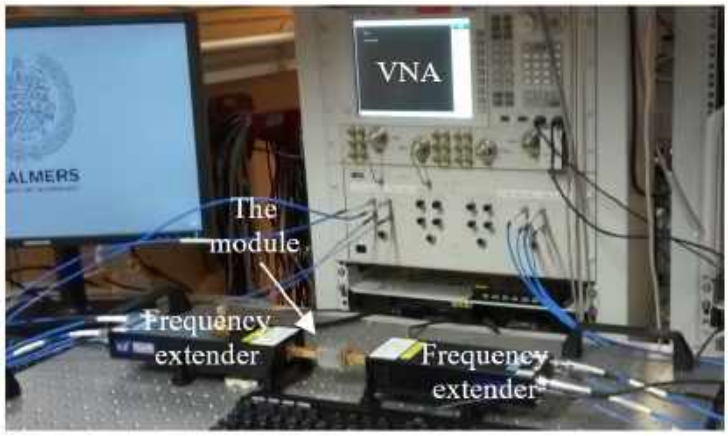


Figure 5.7: Measurement setup for the back-to-back transition module (Paper E)

average of 14 dB over the same reported frequency range.

The results are also compared with simulations and a down-shift in frequency is observed after fabrication. A loss analysis was also done using EM simulations and it shows that the main contributors to the transition's loss are the dielectric loss in the mold compound with a contribution of 0.7 dB to the overall loss and the reflection losses with a contribution of 0.4 dB. The presented solution provides a low-loss approach that enables packaging mmW systems using a low-cost high-volume commercial technology.

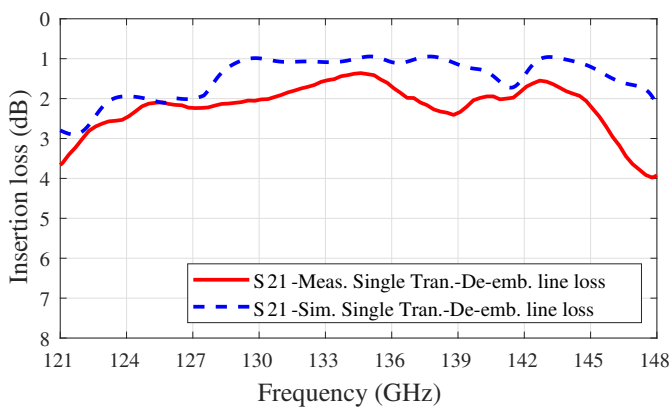


Figure 5.8: Insertion loss of the proposed transition (Paper E)

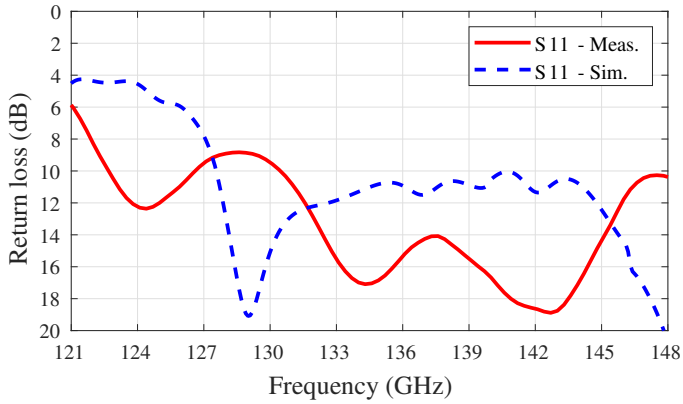


Figure 5.9: Return loss of the proposed transition at the input port (Paper E)

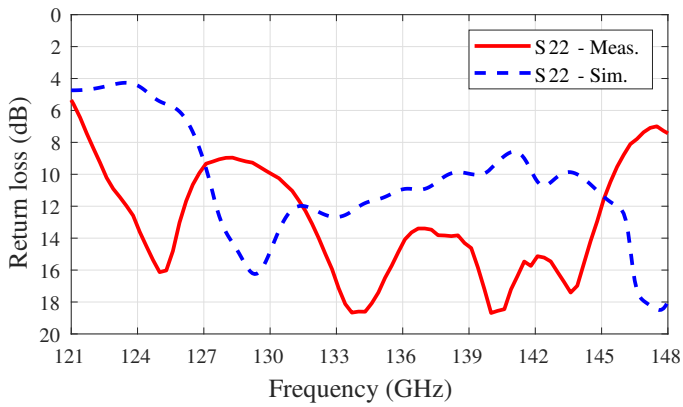


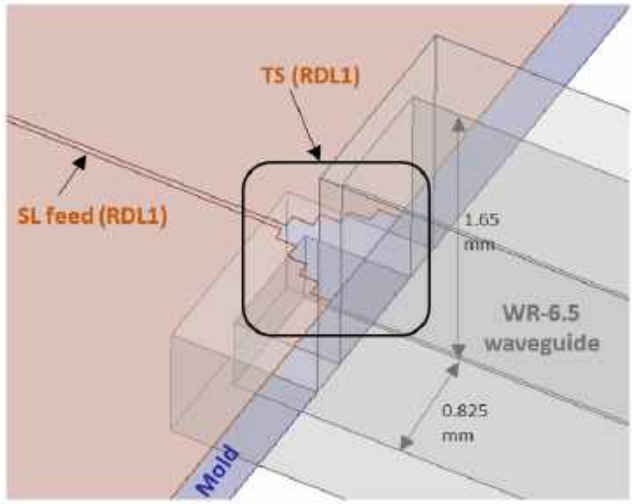
Figure 5.10: Return loss of the proposed transition at the output port (Paper E)

5.3 Tapered Slot Transition

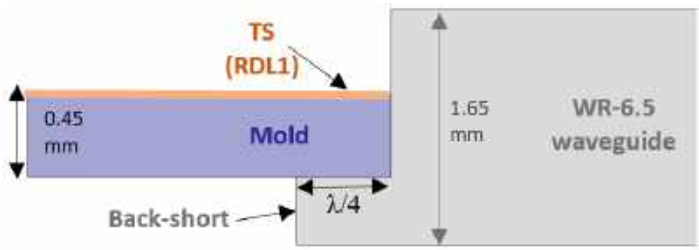
5.3.1 Transition Design

Tapered slots [69] (TS) are simple to design and have high efficiency exhibiting relatively wide bandwidth [70]. TS are fed using SL which can be either unilateral or bilateral. The gradual widening of the slot creates the radiating region, which can have various profiles such as: constant width, linear, and non-linear (e.g., Vivaldi and Fermi profiles). For simplicity and due to limitations imposed by design rules, a unilateral stepped width profile is chosen for the slot used in this specific work.

Fig. 5.11 shows the proposed transition which consists of a TS implemented in the RDL of the technology's layer stack. The TS is excited using a SL that is tapered in 4 steps. Such excitation method makes the design suitable for differential circuits. The eWLB package is mounted in the E-plane of a standard WR-6.5 waveguide and inserted in its channel by a quarter wavelength distance



(a)



(b)

Figure 5.11: The proposed TS-based waveguide transition (a) 3D view (b) Side view (Paper C).

allowing the implementation of a back-short to block back-radiation. The structure is implemented using only one metal layer and no galvanic contacts are needed between the eWLB and the waveguide.

The loss of the transition was analyzed using 3D EM simulations and two main contributors for loss were determined. The first and main contributor to the loss is the radiation in undesired directions such as in the mold compound and through the top open end of the waveguide. The mold used in this process has a thickness of 0.45 mm which is relatively high compared to the wavelength at D-band. This leads to the leakage of a considerable part of the E-field in the mold rather than being coupled to the waveguide as intended. This can be mitigated by using TSVs to act as a back-short and stop the field from propagating through the mold. Moreover, using a thinner mold layer would help reduce such leakage as well. The radiation through the top open end of the waveguide can be addressed using EBG structures as explained earlier. Another loss mechanism is reflection losses which can be improved by adding matching sections to the structure to help improve the transition's return loss and achieve better coupling.

5.3.2 Experimental results

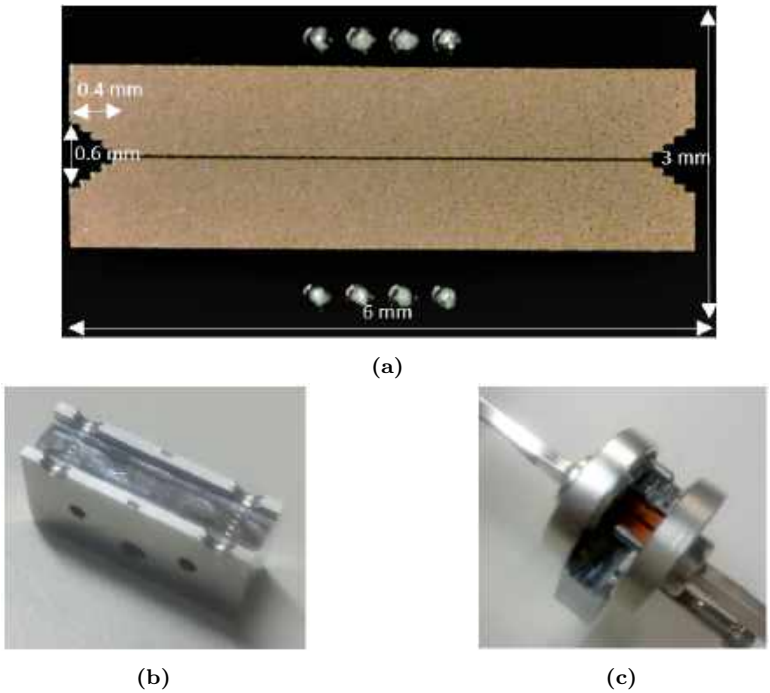


Figure 5.12: Photo of the fabricated eWLB package showing (a) The back-to-back TS transition (b) The standalone metal fixture (c) The assembled module connected to waveguide twists. (Paper C).

Fig. 5.12 shows photos of the fabricated eWLB package and the test fixture for the transition. The structure is implemented and measured in a back-to-back fashion. In order to realize the waveguide back-short discussed earlier, a simple metal fixture was machined and attached to the waveguide sections shown in Fig. 5.12c. The fixture has quarterwave cavities to act as extensions for the waveguide channel. The eWLB is mounted on the fixture and measured back-to-back. In order to avoid the excitation of undesired modes in the mold, a slot was also machined underneath the eWLB.

Fig. 5.13 shows the measurement setup which consists of a 2-port VNA connected to two D-band waveguide frequency extenders. The outputs of the frequency extenders are connected to WR-6.5 waveguide twists in order to be able to mount the package horizontally in the E-plane of the waveguide. Two-port calibration to the output of the waveguide twists was done. Results show that the structure exhibits an average insertion loss of 2.8 dB and a minimum of 1.8 dB per transition. The 3-dB bandwidth of the transition was measured to be 33% ranging from 110 to 153 GHz as shown in Fig. 5.14. It's noteworthy that the presented loss includes the loss of the 2.5 mm-long SL feeding the slot. Simulation results are also compared to measurements and results show that the average simulated insertion loss is 2.5 dB and over a similar frequency band. Similar to the previous transitions, a loss analysis was performed via simulations and results show that radiation in undesired

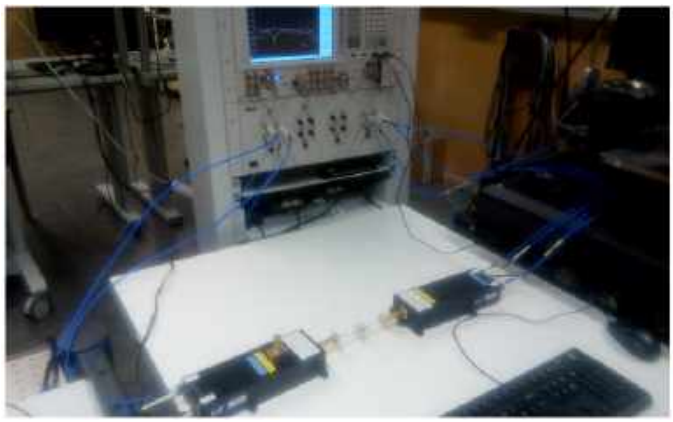


Figure 5.13: Measurement setup for TS transition (Paper C)

directions accounts for 1.6 dB of the overall insertion loss. The loss of SL is estimated to be contributing by 0.6 dB to the overall loss. The transition's sensitivity to misalignment in lateral directions is also investigated. Results show that the transition can tolerate a misalignment of up to 70 um with only minor impact on performance as can be seen from Fig. 5.14 - 5.16. The return losses were also measured at the input and output ports and are shown in Fig. 5.15 and 5.16 respectively. The design occupies an area of $0.4 \times 0.6\, mm^2$ while the overall package area is $3 \times 6\, mm^2$.

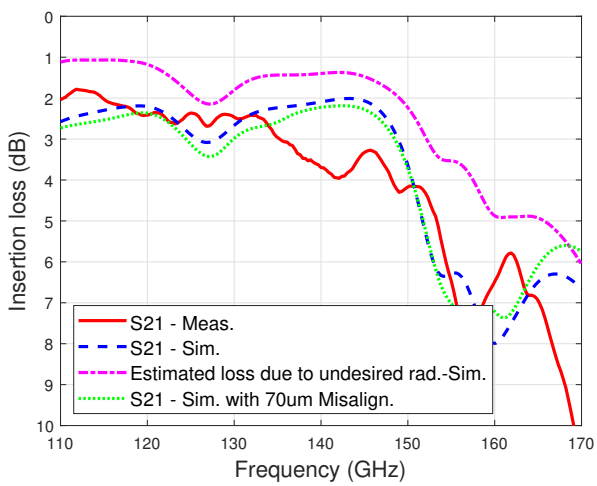


Figure 5.14: Insertion loss of a single TS transition (Paper C)

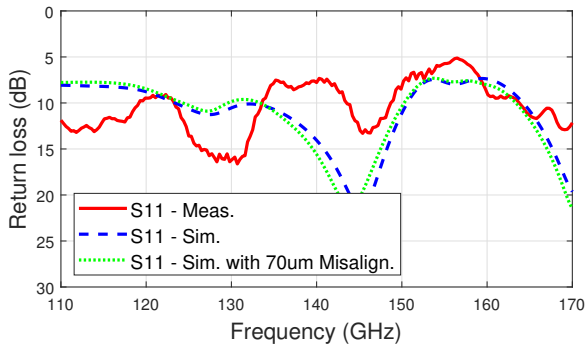


Figure 5.15: Return loss of the TS transition at the input port (Paper C)

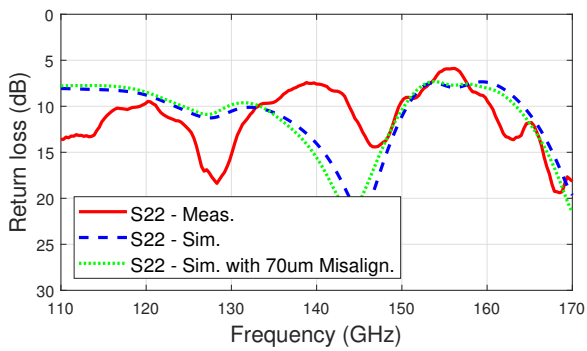


Figure 5.16: Return loss of the TS transition at the output port (Paper C)

5.4 Rectangular Slot Ring Waveguide Transition

5.4.1 Solution Overview

Fig. 5.17 shows another proposed packaging solution using eWLB technology. The full solution consists of an eWLB with an embedded MMIC, a PCB and an air-filled waveguide mounted normally to the PCB.

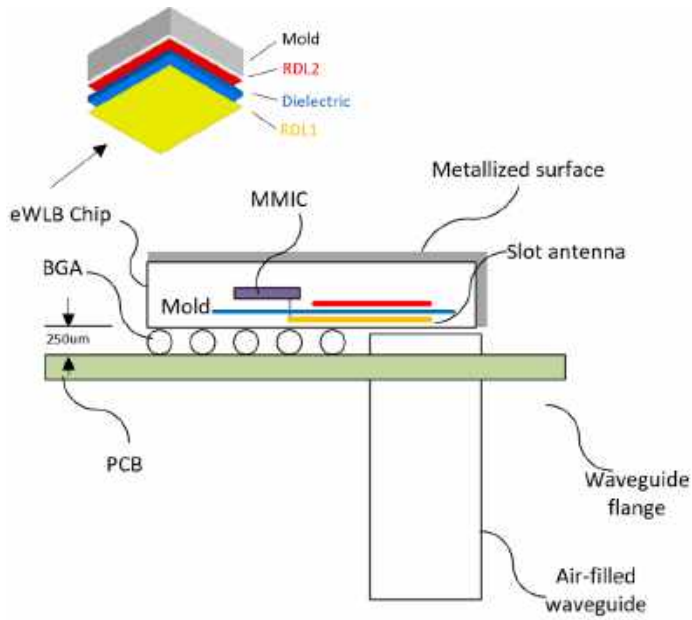


Figure 5.17: Simplified side-view of the proposed solution (Paper J)

A rectangular slot ring is implemented in the eWLB that coupled directly to an air-filled waveguide. The eWLB's mold height is 0.45 mm which is close to quarter wavelength at D-band and hence, metallizing the eWLB surface as shown in Fig. 5.17, makes it act as a backshort and hence achieve better coupling towards the direction of the waveguide. Simulations showed that the insertion loss of the transition improves by 0.5 dB if the eWLB surface is metallized. This metallization can be achieved either by applying reflective paint on eWLB surface or by simply placing the eWLB on a reflective surface.

5.4.2 Implementation of the Transition

An illustration of the proposed transition is shown in Fig. 5.18. A rectangular slot ring that is fed using CPW lines is implemented using the RDL. The eWLB is mounted perpendicularly to the waveguide. In order to avoid shorting the signal line to the ground in case the waveguide wall made contact with the eWLB surface, a 30-um deep channel was machined in the waveguide wall at the same position above the signal line as shown in Fig. 5.19 to avoid shorting it to the adjacent ground lines.

The transition is implemented as a back-to-back to allow straightforward characterization and calibration. The transition occupies an area of 1.9×1 mm^2 and the whole eWLB occupies an area of 3×6 mm^2. CPW line test structures were also included to calibrate line losses and extract the transition loss accurately.

It is noteworthy that the focus of this work is the realization of the mmW transition and hence no DC or low frequency connectivity were realized nor tested and no PCB was employed in the tested structure similar to the previous solutions.

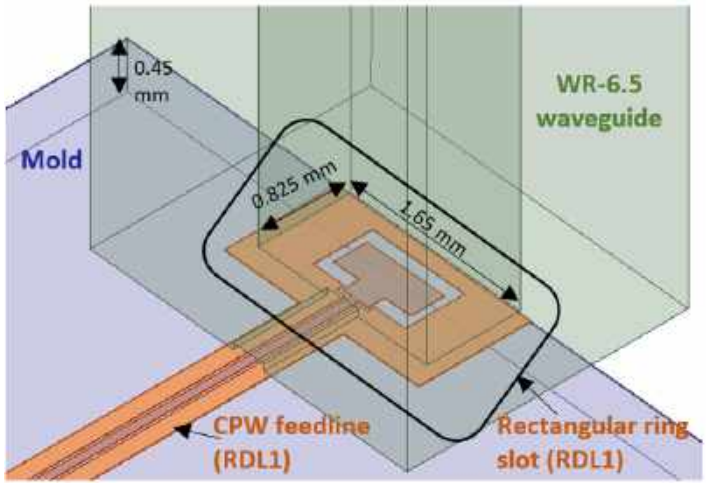


Figure 5.18: Illustration of the rectangular slot ring transition (Paper C)

Figure 5.19: Waveguide photo showing the machined channel

5.4.3 Experimental Results and Discussion

Fig. 5.20 shows a photo of the fabricated eWLB. The eWLB was placed upside down and open-ended waveguide bends were mounted perpendicular to the eWLB surface as shown in Fig. 5.21. The whole setup was mounted on a probe station to allow accurate alignment of the waveguide openings and the slots. The measurement setup consists of a Keysight VNA and WR-6.5 VDI frequency extension modules to up/down-convert the signal to D-band. Two-port calibration was performed to the inputs of the waveguide bends. The losses of the bends and the feed CPW lines were then processed and de-embedded in a later stage. The measured insertion loss of the single transition is shown in Fig. 5.22. Results show that the average loss of the rectangular slot ring transition is 3.7 dB covering a 3-dB bandwidth of 27% extending from 116 to 152 GHz. This translates to a bandwidth improvement of 5% compared to a previous version of the same design presented in Paper J that has poorer return loss. The improvement is mainly due to resizing the slot and using a matching section between the slot and the CPW lines.

Fig. 5.23 and 5.24 show the return loss of the transition at the input and output ports, respectively. Results show a considerable improvement

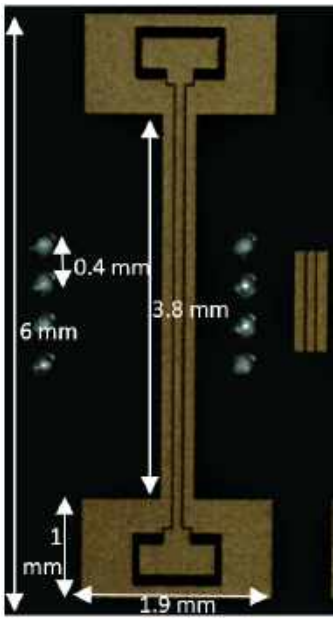


Figure 5.20: Photo of the fabricated eWLB (Paper C)

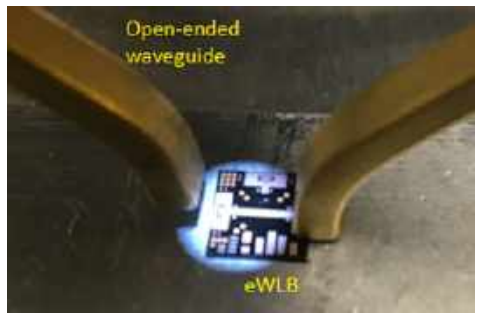


Figure 5.21: Photo of the measurement setup (Paper J)

in the return loss after introducing the matching section and the resizing of the slot compared to its predecessor. Measurements are also compared to simulations and reasonable agreement between both results is observed. The transition's sensitivity to misalignment was also simulated and results show that misalignments of up 40 um can be tolerated with only minor degradation in performance.

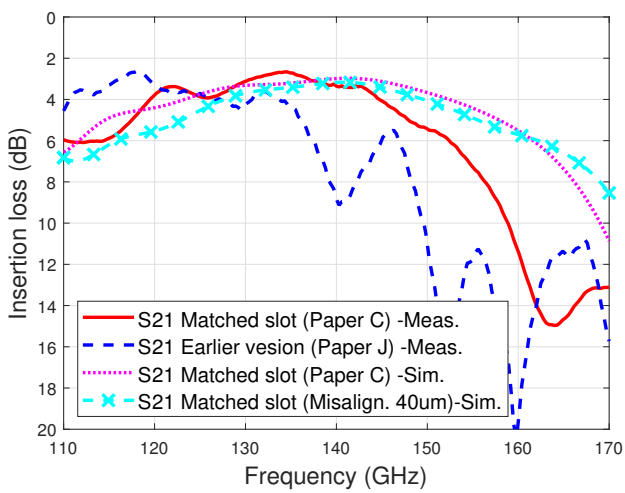


Figure 5.22: Insertion loss of the rectangular slot ring transition (Paper C)

A loss analysis was performed using simulations and results show that most of the loss is due to undesired radiation in the mold similar to the previous transitions, in addition to radiation at the interface between the eWLB surface and waveguide due to the air gap between them. The later can be minimized using EBG structures as explained earlier. Other sources of loss include reflection loss and the ohmic loss in the CPW feed lines.

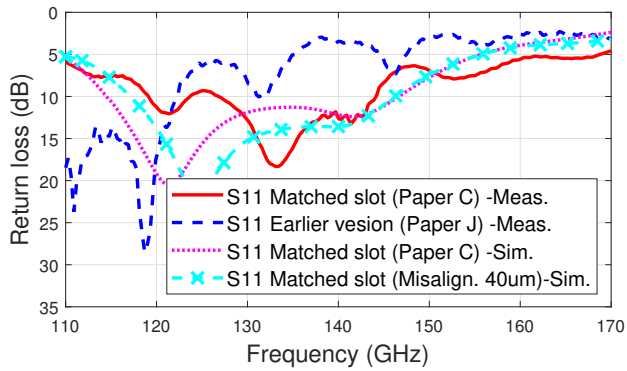


Figure 5.23: Return loss of the transition at the input port (Paper C)

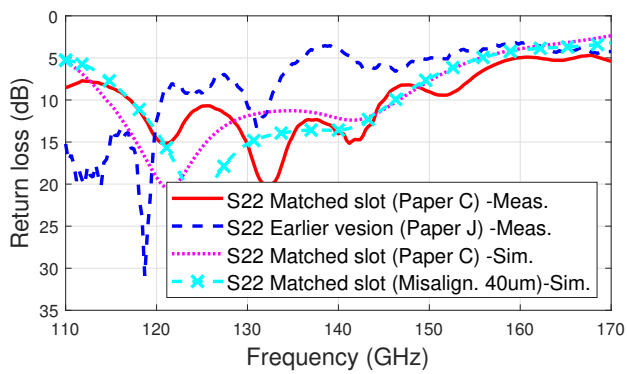


Figure 5.24: Return loss of the transition at the output port (Paper C)

5.5 Si Taper Based Interconnect

In this section, a D-band slot is implemented in the technology's RDL similar to the work presented in the previous section, however, the slot here couples to a high-resistivity (HR) silicon taper, which in turn couples to an air-filled waveguide instead of coupling directly to the waveguide. The proposed approach is also generic and the concept is supported and verified by experimental results.

5.5.1 Interconnect Realization

The proposed complete solution is shown in Fig. 5.25. The solution consists of an eWLB chip, MMIC, PCB, HR silicon taper and an air-filled WR-6.5

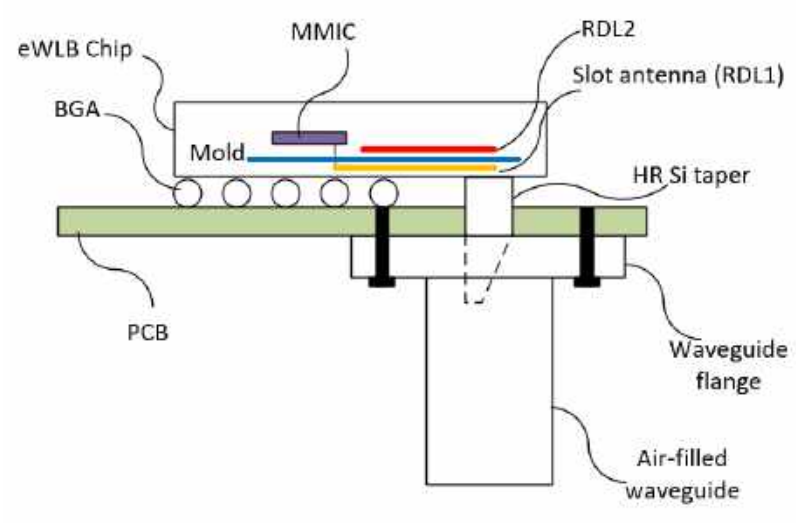


Figure 5.25: The proposed packaging system consisting of: The slot transition implemented in an eWLB chip, MMIC, PCB, HR Si taper and an air-filled waveguide (Paper D).

waveguide. The transition consists of a rectangular slot fed by a CPW line. The slot had to be implemented differently in this work since it couples to a relatively small Si taper and hence the design had to be more compact. This was achieved by using a rectangular slot instead of the slot ring that was employed in the work presented previously. The compact implementation of the slot allows using a small Si taper and hence avoid exciting higher order modes. The slot is implemented in RDL1 in the technology stack and the signal line transits to RDL2 at the waveguide wall position as shown in Fig. 5.26 to avoid shorting it to the adjacent ground lines. The slot dimensions are chosen to provide reasonable impedance matching to the silicon taper and minimize leakage at the interface. The taper is machined using a micro-dicing saw and its dimensions are shown in Fig. 5.27. The taper is mounted normal to the slot and is then inserted into the air-filled waveguide. The use of the Si taper helps guide the field to the air-filled waveguide and reduces leakage to the substrate due to the high dielectric constant of Si. This helps achieve better results compared to direct coupling to the air-filled waveguide as presented in the previous section.

5.5.2 EM Simulations and Loss Analysis

3D EM simulations were used to verify the performance of the structure as shown in Fig. 5.28. An air gap of 20 um between the slot and the taper is included in the simulation to model the non-galvanic contact effect. Simulations showed an average insertion loss of 3.8 dB with the main contributors to the loss as: the mold's dielectric loss and the radiation at the interface between the slot and the taper due to the air gap. Other sources of losses include the ohmic loss of the CPW lines and the dielectric loss of the taper and the adhesives used to assemble the interconnect.

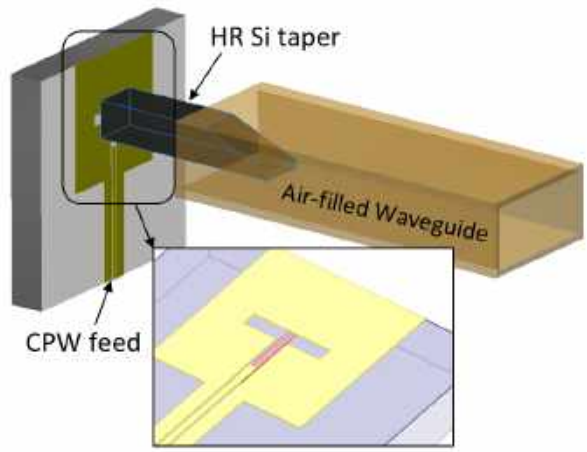


Figure 5.26: The proposed interconnect consisting of 3 parts: the slot transition implemented in eWLB chip, HR Si taper and air-filled waveguide.

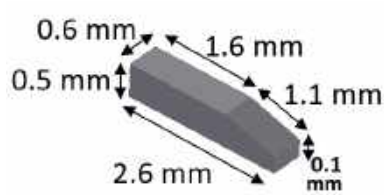


Figure 5.27: Dimensions of the machined HR Si taper (Paper D)

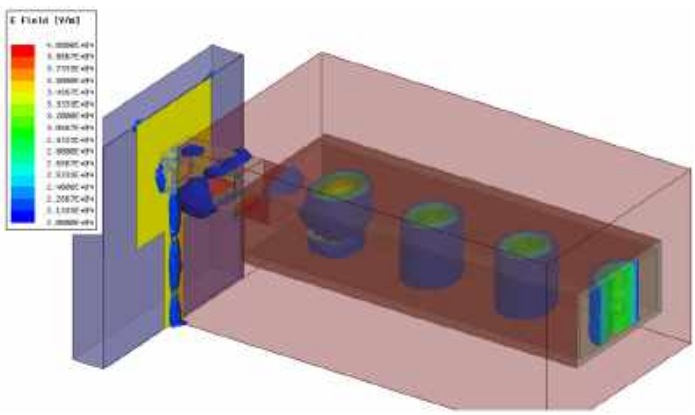


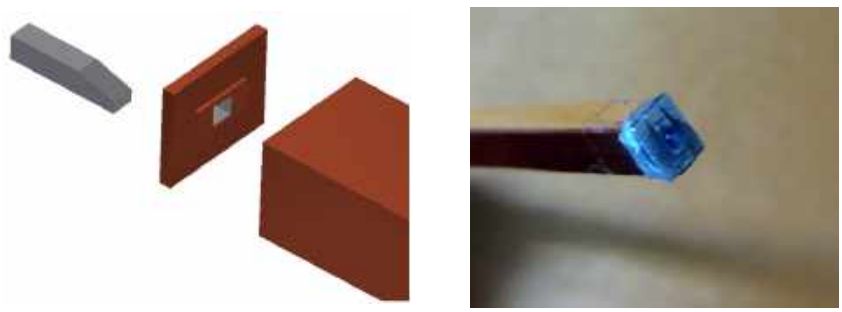
Figure 5.28: EM simulation of the complete solution.

Table 5.1 summarizes the analysis of the interconnect loss and details contributions to the overall insertion loss. Simulation results are presented in the following section and compared to measurement results.

Table 5.1: Interconnect Loss Analysis (Paper D)

Loss Source	Material	Material Parameters	Contribution to the Total Loss (dB)
eWLB mold dielectric loss	Plastic	ε_r=3.2 , δ=0.004	0.95
Undesired radiation due to slot-to-taper gap	-	20 um Air gap	0.71
Taper dielectric loss	HR Si	ε_r=11.7, ρ=4,000 Ω.cm	0.70
Transmission line loss	Copper	σ=5.9×10^7 S/m	0.65

A steel metal holder was machined and the taper slides through a hole in the holder that has the same dimensions of the taper as shown in Fig. 5.29. The taper is then glued to the holder using Glycol Phthalate wax and the holder is attached to the air-filled waveguide using conductive epoxy. The holder dimensions and features are designed to provide accurate alignment of the taper to the air-filled waveguide.



(a) **(b)**

Figure 5.29: Assembly of the interconnect using metal holder (a) Illustrative view (b) Photo of the realized interconnect

5.5.3 Experimental Results and Discussion

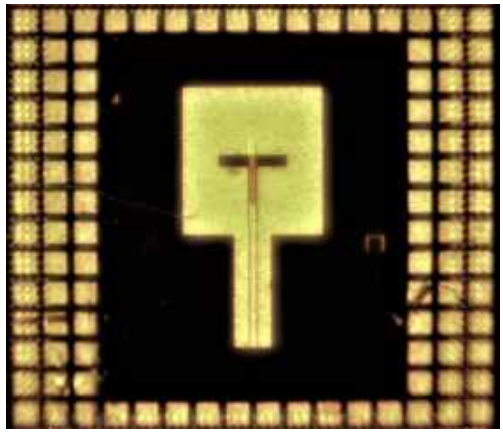


Figure 5.30: Photo of the fabricated eWLB (Paper D)

Figure 5.31: Measurement setup for the interconnect with the waveguide bend on the left and waveguide probe on the right (Paper D)

The fabricated eWLB is shown in Fig. 5.30. The test setup used to characterize it consists of a Keysight VNA and a pair of WR-6.5 VDI frequency extension modules to up/down-convert the signal to D-band as shown in Fig. 5.31. An open-ended waveguide bend is mounted perpendicular to the eWLB surface on one side of Cascade microtech's probe station allowing accurate positioning of the waveguide to the slot. The taper along with the metal holder are attached to the open end of the waveguide bend. A D-band waveguide probe is mounted on the other side of the probe station to probe the CPW feed lines as mentioned earlier. Two-port calibration is performed to the outputs of the frequency extenders. The waveguide probe is then de-embedded by measuring the S-parameters of the probe on a calibration substrate including open-circuit and matched loads to extract its insertion and return losses. The

waveguide bend is de-embedded by measuring a flanged waveguide of the same length and then de-embedding it.

De-embedded measurement results of the interconnect show an average insertion loss of 3.4 dB over the frequency range of 116 - 151 GHz and a minimum of 2.1 dB as shown in Fig. 5.32. The results show good agreement with simulations. Sensitivity to taper misalignment and the air gap to the eWLB surface was also simulated and compared to measurements. Results show that an air gap of up to 40 um and a misalignment of 100 um in both lateral directions can be tolerated. The interconnect shows a 3-dB bandwidth of 26%. The return losses at the WR-6.5 side and CPW lines side are shown in Fig. 5.33 and 5.34 respectively.

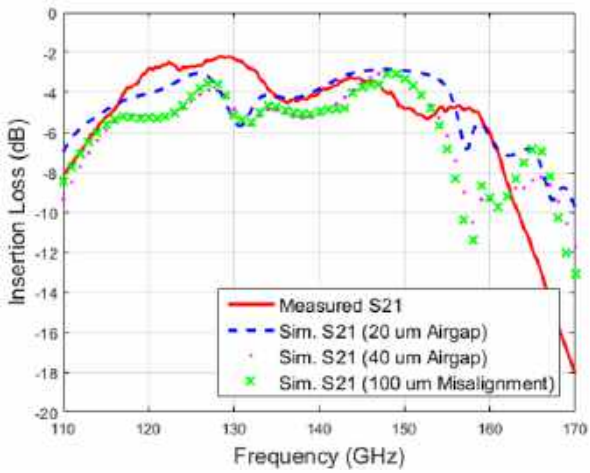


Figure 5.32: The insertion loss of the interconnect (Paper D)

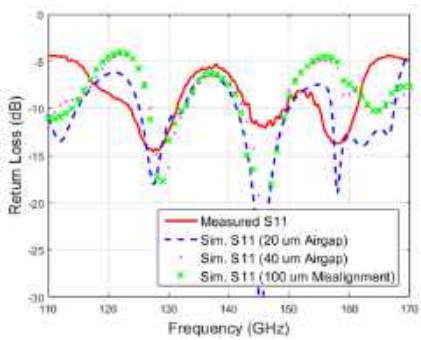


Figure 5.33: The return loss of the interconnect at the WR-6.5 side (Paper D)

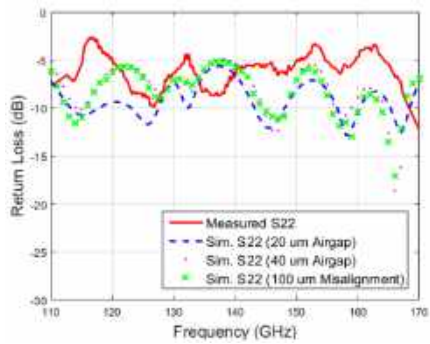


Figure 5.34: The return loss of the interconnect at the CPW side (Paper D)

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis presented several packaging and interconnectivity approaches in the mmW and THz ranges. Many of the presented solutions can be integrated on the same chip with the RF circuitry and hence provide higher integration. Several commercial MMIC technologies were used to realize and demonstrate the proposed solutions including InP, GaAs and SiGe technologies. The presented work achieves high performance with an insertion loss as low as 0.7 dB over a bandwidth as wide as 50%. The thesis investigated various topologies to realize such solutions that suits wide range of technologies/applications such as slots, patches and finlines. The thesis also proposed using EBG structures in combination with the presented transitions in order to mitigate the issue of parasitic modes.

Another packaging approach that was investigated in this thesis is the use of eWLB packaging technology. Several interconnects were demonstrated using the technology at D-band. The solutions include a patch coupler with mushroom-based EBG structure, a CPW-fed rectangular slot ring transition, a Si taper interconnect and a tapered slot transition, all interfacing with a standard D-band waveguide. Experimental results show that the solutions achieve insertion losses ranging from 2 to 3.7 dB at D-band. The use of eWLB technology as a packaging solution above 100 GHz enables high-volume commercialization of mmW and THz systems and achieves reasonable performance at a low cost.

The work presented in this thesis is summarized and compared with state-of-the-art packaging solutions reported in literature in Chart 6.1 and Table 6.1. The comparison shows that the presented work exhibits the widest reported bandwidth and some of the lowest insertion losses while at the same time providing fully integrated packaging approach. Moreover, the presented work does not require any special processing/chip shaping, nor galvanic contacts unlike some of the solutions reported in literature that has similar low loss but require non-rectangular shaping of the chip [18], [71]. Many useful conclusion can also be drawn from the comparison chart. For instance, fully integrated

on-chip solutions in III-V semiconductor technologies seem to have the lowest loss with quite wideband performance. This is due to the fact that III-V material have typically higher substrate resistivity which enables realizing low-loss on-chip coupling structures since the loss in the substrate would be relatively low. When such solutions are also combined with EBG structures as proposed in this thesis, better performance can be achieved due to the fact that such structures can stop any field leakage at the packaging interface. In addition, the structure prevents the unwanted parasitic modes from propagating and hence allows the use of relatively large chips. Another conclusion that can be drawn from the comparison is that, packaging solutions in Si-based technologies tend to exhibit higher losses compared to their III-V counterparts. This is due to several reason such as, the lower resistivity of Si compared to III-V materials and the lack of TSVs and backside metallization in many of the commercially-available Si technologies which are typically used to create back-shorts and limit undesired radiation through the substrate. Wafer level packaging solutions such eWLB seem also to exhibit relatively higher losses, however, the technology seem to have high potential as solutions beyond 100 GHz can be realized using the technology as demonstrated in this thesis. More development in the materials used in the technology and using smaller feature sizes would help lower the loss and extend the frequency of operation of the technology to several hundreds of GHz.

This work addressed the integration challenges facing mmW and THz systems and provided several approaches to address those challenges in various technologies that can serve a wide range of applications.

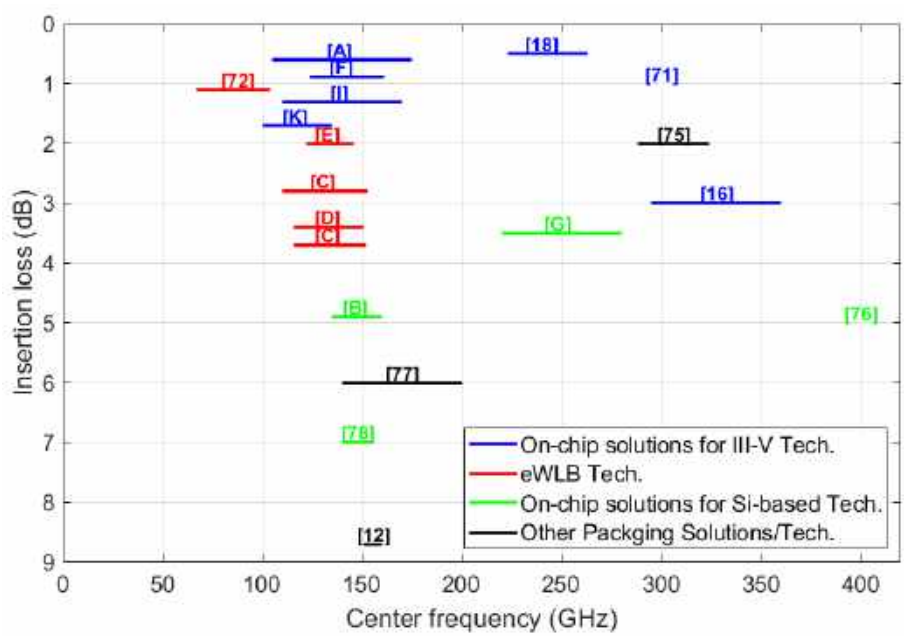


Figure 6.1: Comparison chart between the presented work and work reported in literature across different technologies.

6.2 Future Work

Realizing low-loss solutions for Si-based technologies requires further investigation. One of the main limitations of on-chip solutions in Si is the relatively low resistivity of the substrate. Investigating novel solutions either by manipulating the substrate or by using new techniques to suppress undesired radiation through the substrate is very important.

The work done in eWLB technology requires further investigation by integrating the presented transitions with MMICs and assessing the impact of such integration on performance. In addition, pushing the technology's capabilities and investigating potential bottlenecks in the future when extending the frequency of operation into the THz range is of interest. Materials used in the technology and feature sizes would require major changes to push the frequency of operation and experimenting with new low-loss materials is crucial to develop the technology further.

Implementing the fully-integrated solutions presented in this work at higher frequency bands is also of interest and the investigation of any further challenges that might arise in the THz range is of high importance. Using micromachining to realize the EBG structures and investigating fabrication tolerances and their impact on the performance of such structures in the THz range is also critical.

Table 6.1: Summary and Comparison to State-of-the-art Work

Ref	Freq. range (GHz)	3-dB band-width	Loss (dB)	Topology	Tech.
[18]	223-263	16%	0.5	MS-to-WG transition in 243 GHz LNA module	GaAs mHEMT
[71]	300	-	<1	Integrated WG probe in 300 GHz LNA	InP DHBT
[72]	67-110	48%	1	CPW to rectangular WG transition (Taper Concept)	eWLB
[73]	67-104	43%	1.1	CPW to rectangular WG transition (Via Concept)	eWLB
[74]	110-140	24%	-	Bondwiring SiGe MMIC in LTCC-based package	LTCC
[75]	288-324	12%	2	Coplanar-waveguide-fed slot radiator	LTCC
[16]	295-360	20%	3	B2B radial probe transition in HEMT amplifier module	InP
[76]	410	7%	5	Patch-to-waveguide transition	CMOS
[76]	400	10%	5	Folded dipole-to-waveguide transition	CMOS
[77]	140-200	35%	6	High-resistivity Si waveguide	Si MMC
[78]	140-156	10.8%	7	Patch radiator with a tapered dielectric waveguide	SiGe+Diel. WG
[12]	151-160	5.7%	8.7	Micro-machined Sub-THz Interconnect	Si Diel. WG
A	105-175	50%	0.7	E-plane waveguide probe	InP DHBT
I	110-170	43%	0.7-2	Finline chip-to-waveguide transition	SiC substrate
F	124-161	26%	0.8	Chip-to-chip and chip-to-WG using EBG struct.	GaAs subst.
K	100-135	30%	1.7	Linearly tapered slot transition	GaAs HEMT
E	122-146	18%	2	Patch waveguide transition with mushroom-based EBG	eWLB
C	110-153	33%	2.8	Tapered slot waveguide transition	eWLB
D	116–151	26%	3.4	Si taper interconnect	eWLB
G	220–280	24%	3.5	Rectangular slot ring	SiGe BiCMOS
C	116-152	27%	3.7	Matched rectangular slot ring transition	eWLB
B	135-160	17%	4.2-5.5	H-Plane slot transition	SiGe BiCMOS

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