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Finger Number and Device Performance: A Case Study of Reduced Graphene Oxide Microsupercapacitors

Qi Li, Anderson D. Smith, Agin Vyas, Fabio Cornaglia, Alec Anderson, Mazharul Haque, Per Lundgren, and Peter Enoksson*

Microsupercapacitors (MSCs) are recognized as suitable energy storage devices for the internet of things (IoTs) applications. Herein is described the work conducted to assess the areal energy and power densities of MSCs with 2, 10, 20, and 40 interdigital finger electrodes on a fixed device footprint area (the finger interspacing is fixed at 40 μm, and the finger width and length are allowed to vary to fit the footprint area). The MSCs are based on reduced graphene oxide (rGO) materials and fabricated with a spin-coating and etch method. The performance evaluation indicates a strong dependency of areal capacitance and energy density on the number of fingers, and the maximum (impedance match) power density is also influenced to a relatively large extent, whereas the average power density is not sensitive to the configuration parameters in the present evaluation settings (scan rate 20–200 mV s^{-1} and current density of 100 μA cm^{-2}). For the rGO-based devices, the equivalent distributed resistance may play an important role in determining the device resistance and power-related performance.

1. Introduction

Self-powered systems, defined as those that operate by harnessing ambient energy present within the environment of the system, have become increasingly important with the establishment of the concept of the internet of things (IoTs).[1,2] The push towards self-powered systems requires the development of miniaturized energy storage devices that can enable sustained, autonomous operation of electronic devices for applications. Microsupercapacitor (MSC) technology is recognized as a viable route for this purpose, because MSCs can be charged and discharged much more rapidly than batteries and have an almost unlimited lifetime.[3–9]

In addition to electrode material properties, the configuration of MSC devices' architecture plays a key role in determining their performance. The in-plane interdigital configuration, which has microelectrodes (fingers) interdigitally arranged on a substrate, is believed to be advantageous over the conventional layer-by-layer stack configuration in terms of low integration complexity.[10] Such MSCs can be fabricated through several complementary metal–oxide–semiconductor (CMOS) compatible methods such as spin coating.[11–13] Moreover, the interdigital configuration allows for accurate control of the distance between electrodes, by leveraging standard microfabrication methods, and thus, the ion transport resistance in cells can be manipulated. However, compared to the conventional stack configuration, the interdigital design results in less areal energy density when a very thin electrode material layer is used, which is typically the case. As a result, more footprint area is needed to accommodate the same amount of the electrode material for an equivalent energy density.

To reduce the loss of footprint area, one can pursue extremely small finger-to-finger spacing in the interdigital design.[14] The benefit of such an approach is twofold. On the one hand, it reduces the spacing area that does not contribute any capacitance, and on the other hand, the power density can be increased by reducing the spacing because of reduced electrolyte ion transport distance. The benefit is gained at a cost of increased fabrication complexity as high-resolution lithography techniques are required and that extreme accuracy in aligning electrode material layer to the current collector is also needed.

The second approach to reduce footprint area loss in an interdigital MSC design is reducing the number of fingers so that fewer spacing lines are required for the whole device. Compared to the former, this method relies on more facile device fabrication arguably correlated with an increased production yield. Despite the advantage of gaining energy density and simplifying fabrication, MSC reports available are mostly designed with more than one pair of finger electrodes.[15–17] The reason can be a

Dr. Q. Li, Dr. A. D. Smith, A. Vyas, F. Cornaglia, M. Haque, Dr. P. Lundgren, Prof. P. Enoksson
Department of Microtechnology and Nanoscience
Chalmers University of Technology
Gothenburg 412 96, Sweden
E-mail: qili@chalmers.se

Dr. Q. Li, Prof. P. Enoksson
Wallenberg Wood Science Center
Chalmers University of Technology
Gothenburg 412 96, Sweden

A. Anderson
University of California: Santa Barbara
Santa Barbara, CA 93106, USA

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssb.202000354.

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concern from a potential drawback that the accessibility of electrode material to the electrolyte is inferior to the device having more fingers, as fewer cross-sectional areas are exposed to the electrolyte. Consequently, the equivalent series resistance (ESR) of the device might be increased and power density decreased.

The effect of the number of fingers was previously investigated with a simple theoretical model considering resistance contribution from current collectors and electrolyte, and more fingers are beneficial for lower resistances.[18] However, the model assumes that the electrode materials are exempted from equivalent distributed resistance (EDR)—in principal, the electrode was regarded as a nonporous thin film. However, the case can be much more complicated when considering the electrode materials' property, and the exact influence of finger number on device performance may vary from material to material. In this article, we explore the question of whether one should "give" MSC more fingers, by comparing the performance of reduced graphene oxide (rGO)-based MSCs with fixed device footprint and finger interspacing.

2. Device Fabrication

To compare the influence of finger number on the performance of MSCs, four MSCs with different finger numbers (2, 10, 20, and 40), labeled 2F, 10F, 20F, and 40F, respectively, are designed at a fixed finger spacing of 40 μm, and within a fixed "device area" of about 0.21 cm^2. The width/length of electrodes was subjected to change accordingly. The device schematic and dimensions are shown in **Figure 1** and **Table 1**.

3. Device Fabrication

MSCs were fabricated with a spin-coating and etch method. The fabrication of MSCs started with a standard 2 in. silicon wafer with a 400 nm SiO_2 insulation layer (**Figure 2**a). The wafer was then patterned with 20/100 nm for Ti/Au interdigital fingers as current collectors by liftoff technique using a bilayer positive photoresist (Figure 2b). In the next step, a thin layer (≈2 μm) of graphene oxide (GO) with a density of 6 $g\,l^{-1}$ was spin coated to cover the whole surface of the wafer, followed by Al deposition to form a hard mask (Figure 2d) which is finely aligned to the current collector layer as shown in Figure 2b. The wafer was then transferred to the plasma chamber and oxygen plasma was applied to remove the unmasked GO material. In the end, the Al hard mask was etched by reactive ion etching (RIE) and the wafer was subjected to 500 °C annealing under argon flow to obtain rGO. The electrode materials and the current collectors were well aligned so that no mismatch between them was observed. As the final step of device fabrication, ≈10 μL 85% H_3PO_4 was applied on the device finger area prior to electrochemical performance characterization. The electrolyte was chosen considering that in the open-environment measurement condition, an 85% H_3PO_4 does not evaporate as quickly as other aqueous electrolytes, and relatively less sensitive to moisture content than for organic or ionic liquid electrolytes.

Table 1. Designed device dimensions.

Device	Finger number, N	Width, W [μm]	Length, L [μm]	Interspace, i [μm]	Active materials area, A_a [cm^2]	Device footprint, A_{ft} [cm^2]
2F	2	4760	2200	40	0.20944	0.211344
10F	10	440	4200	40	0.18480	0.211344
20F	20	200	4200	40	0.16800	0.211344
40F	40	80	4200	40	0.13440	0.211344

4. Electrochemical Performance

The electrochemical performance of MSCs was evaluated on Gamry Reference 3000AE potentiostat. The cyclic voltammograms (CVs) at scan rates of 20 and 200 $mV\,s^{-1}$ are shown in **Figure 3**. Mirror-like images are observed for all the MSCs of four configurations, suggesting dominant capacitive energy storage behavior in these devices. The areal capacitance of the device C_{ft} in $mF\,cm^{-2}$ was calculated by

$$C_{ft} = \frac{\int I dV}{2\nu \Delta V \cdot A_{ft}} \quad (1)$$

where I is the current response during the CV scan, V the voltage, ν the scan rate, ΔV the voltage window (0.8 V), and A_{ft} is the surface area of the device. The calculated values are shown in **Table 2**. Device 2F has the highest total capacitance of 99 μF

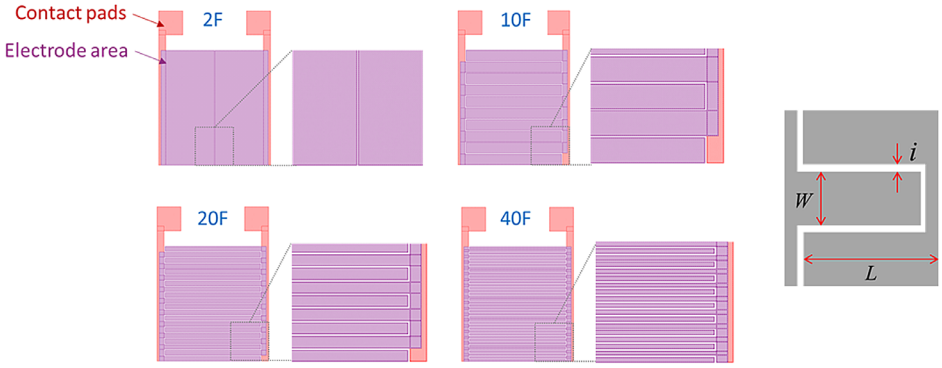

Figure 1. Schematics of device configurations.

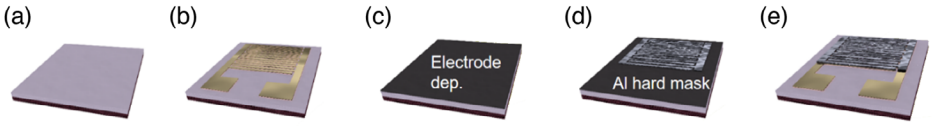

Figure 2. Schematic of key MSC fabrication steps. a) Si with 400 nm SiO_2; b) patterning of current collector metals by lithography, metal deposition, and liftoff; c) spin-coating GO solution; d) patterning of Al hard mask by lithography, metal deposition, and liftoff; and e) etching in oxygen plasma.

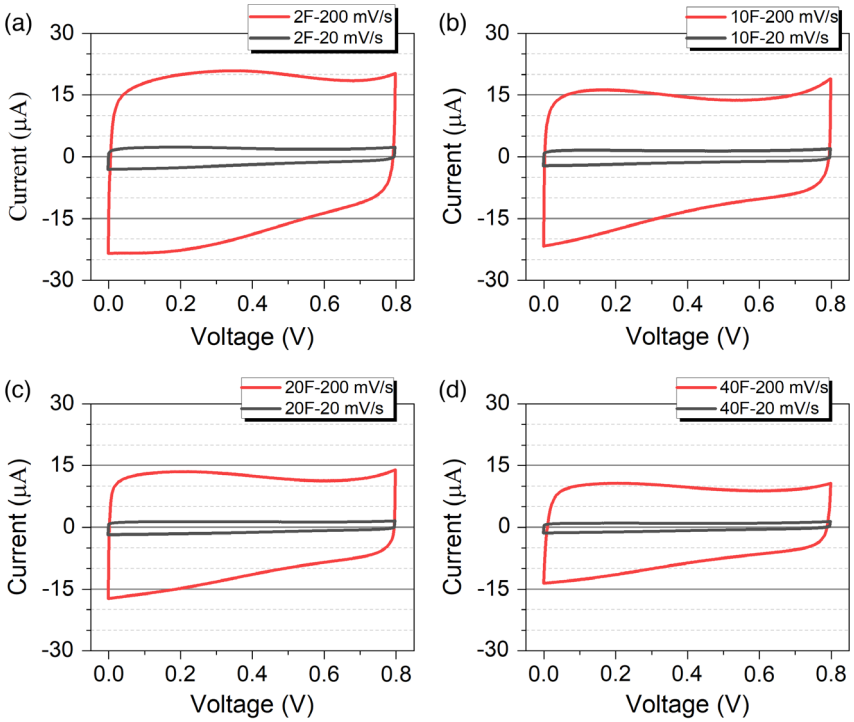

Figure 3. CVs at 20 and 200 mV s^{-1} with a) 2, b) 10, c) 20, and d) 40 fingers.

Table 2. Areal capacitances calculated from CVs.

Device	C_{ft}, 20 mV s^{-1} [mF cm^{-2}]	C_{ft}, 200 mV s^{-1} [mF cm^{-2}]	$C_{ft,\ 200\,mV\,s^{-1}}$: $C_{ft,\ 20\,mV\,s^{-1}}$
2F	0.47	0.44	93.6%
10F	0.35	0.33	94.3%
20F	0.30	0.28	93.3%
40F	0.21	0.20	95.2%

(0.47 mF cm^{-2} normalized to device footprint) which is more than double that of 40F. The ratio of capacitance at 200 to that at 20 mV s^{-1} is calculated as an indicator of rate capability. For all the four different types of devices, the ratios are greater than 93% with little variation from 93.3% for the 20F to 95.2% for the 40F MSC. The dependence of rate capability on finger numbers in this scan rate range (20 to 200 mV s^{-1}) is weak.

To further examine the power density of the devices, galvanostatic charge/discharge (GCD) measurements were conducted. A high current density of 100 μA cm^{-2} is selected, which is sufficient to evaluate their power performance, e.g., when being charged by a micro energy harvester in a self-powered system. As shown in **Figure 4**, the MSCs exhibit linear charge/discharge curves representing capacitive energy storage. The charge/discharge time varies as a result of different device capacitance, which is calculated by

$$C_{ft} = \frac{I_{ft} t_{dis}}{\Delta V} \tag{2}$$

where I_{ft} is the current normalized to device footprint area, t_{dis} is discharge time, and ΔV is the voltage window excluding IR drop. At the same time, ESR can be calculated through IR drop by the equation

$$\mathrm{ESR} = \frac{V_{IR}}{I_{chg} - I_{dis}} \tag{3}$$

energy density is calculated by

$$E_{ft} = 0.5 C_{ft} \Delta V^2 \tag{4}$$

average power density during discharge is

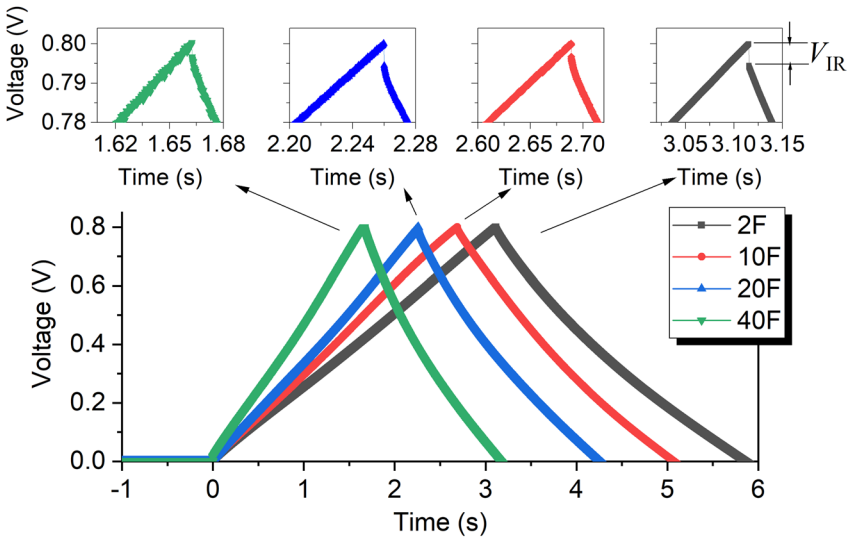

Figure 4. GCD measurements at a current density of 100 μA cm^{-2}.

Table 3. Performance metrics of different devices.

Device	V_{IR} [V]	Voltage [V]	ESR [ohm]	t_{dis} [s]	C_{ft} [mF cm^{-2}]	E_{ft} [μWh cm^{-2}]	$P_{avg,\ ft}$ [μW cm^{-2}]	$P_{max,\ ft}$ [mW cm^{-2}]
2F	0.0056	0.7944	129.8	2.74	0.345	0.0302	39.7	1.23
10F	0.0031	0.7969	72.8	2.38	0.299	0.0264	39.9	2.20
20F	0.0055	0.7945	129.1	2.00	0.252	0.0221	39.8	1.24
40F	0.0037	0.7963	86.9	1.53	0.192	0.0169	39.9	1.84

$$P_{avg,\,ft} = \frac{E_{ft}}{t_{dis}} \tag{5}$$

and maximum (impedance match) power density is

$$P_{max,\,ft} = \frac{V^2}{4 \cdot ESR \cdot A_{ft}} \tag{6}$$

The obtained performance metrics from GCD measurement are shown in **Table 3**. For the average power density, only a 0.2 μW cm^{-2} difference existed between the highest and lowest values among the four MSCs at the current density (0.1 mA cm^{-2}). A more significant difference is in the maximum power density, whereas the 10F doubled the value of 2F. The benefit of increasing areal capacitance and energy by reducing finger numbers is evident (Table 3).

5. Discussion

The configuration plays a key role in determining the performance of MSCs (capacitance, energy, and power densities, etc.). The configuration influences the capacitance and energy densities by the ratio of the active material area A_a to the device footprint area A_{ft}, i.e.

$$E_{ft}(\text{or } C_{ft}) \propto \frac{A_a}{A_{ft}} \tag{7}$$

Therefore, the capacitance and energy density can be optimized by maximizing the A_a/A_{ft} ratio through increasing the finger width W, decreasing the finger space i, and the number of fingers N.

As for the maximum power density, the influence of configuration is basically through the ESR. The current collector resistance R_{cc} and the electrolyte resistance R_e are two of the resistance contributors. R_{cc} can be modeled with, e.g., COMSOL, and it has been shown that R_{cc} varies slightly with W, i, and L.[7] The electrolyte resistance R_e is calculated by

$$R_e = K \cdot \rho_e \tag{8}$$

where K is the MSC cell constant[19] and ρ_e is the specific resistance of the electrolyte. The cell constant is related to the configuration parameters by[19]

$$K = \frac{1}{(N-1) \cdot L} \cdot \frac{2 \cdot K(k)}{K(\sqrt{(1-k^2)})} \tag{9}$$

$K(k)$ is the complete elliptic integral of the first kind

$$K(k) = \int_{t=0}^{t=1} \frac{dt}{[(1-t^2)(1-k^2t^2)]^{1/2}} \tag{10}$$

and for $N = 2$

$$k = \frac{i}{i+W} \tag{11}$$

for $N > 2$

$$k = \cos\left(\frac{\pi}{2}\frac{w}{i+w}\right) \tag{12}$$

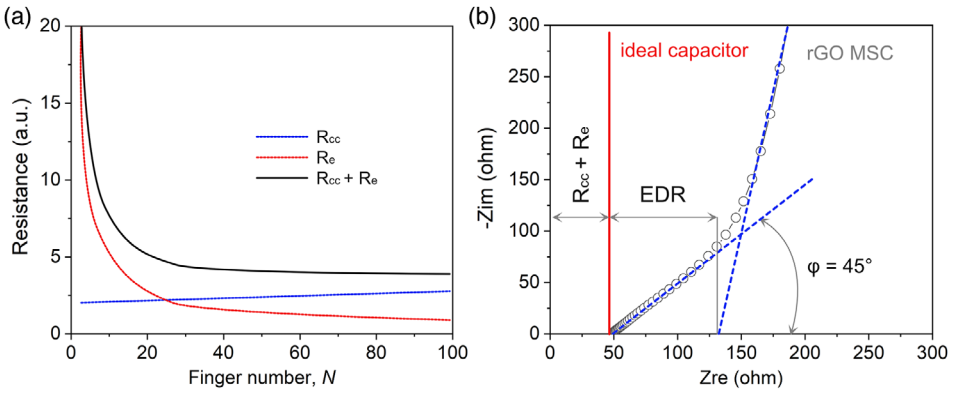

Figure 5. a) Schematic representation showing the variation trend of R_{cc}, R_e, and $R_e + R_{cc}$ as a function of finger number N (at fixed W, L, and i); b) schematic representation of the impedance of an ideal capacitor and the 2F rGO-based MSC.

Combining the equations, it can be solved that R_e increases with interspace i, and decreases in an exponential manner with the W, L, and N, as shown in **Figure 5**a.

It should be noted that device 2F configuration in this article maximizes the active material area (A_a) by parallelly arranging the two fingers along a different direction than for 10F, 20F, and 40F devices. In theory, device 2F of the current design may exhibit a higher R_e than for the conventional interdigital 2F design because of a longer transportation distance from the edge of one electrode to the edge of its counter electrode current collector. The current design will provide a closer look at how the extreme pursuit of maximized energy density will affect the power-related performance, though the exact impact on performance from different design concepts may warrant an independent study.

When considering ESR as the sum of R_{cc} and R_e, the maximum power density (per device footprint) is then calculated as

$$P_{\max,\,\mathrm{ft}} = \frac{V^2}{4 \cdot (R_{cc} + R_e) \cdot A_{\mathrm{ft}}} \tag{13}$$

where R_{cc} increases slightly with N, R_e drops exponentially with N, and A_{ft} scales linearly with N when fixing the value of i, W, and L. Therefore, $P_{\max,\,\mathrm{ft}}$ will reach a maximum value at a certain finger number N in this case. In the present study on the rGO-based MSCs, A_{ft} and i are fixed for the four devices, and L, W, and N are allowed to vary to fit in the footprint. According to the aforementioned considerations, the ESR ($R_{cc} + R_e$) should reach the minimum for 40F, and correspondingly, the $P_{\max,\,\mathrm{ft}}$ is maximized.

However, the results do not agree with the analysis: $P_{\max,\,\mathrm{ft}}$ shows a nonmonotonous variation from 2F to 40F and has a maximum for 10F. The aforementioned model bears a limitation that electrode material resistance is neglected and it is also based on the assumption that the MSCs are exempt from EDR. EDR is related to the electrode materials' porosity, thickness, nanostruction, etc. For electrode materials prepared with a certain technique, e.g., the RuO_2 by electrodeposition,[7] EDR might be omitted due to a the lack of transmission line effects since we would not have limitations related to ion transportation inside pores. In this case, the capacitor behavior is rather analogous to an ideal capacitor modeled by a series RC circuit (Nyquist plot shown in Figure 5b).

Although for most of the carbon-based electrodes (e.g., rGO in this work), the EDR can be significant and plays an important role in determining the power densities. A 45°—slope segment on the Nyquist plot indicates the existence of the transmission line effect[20] due to the ion distribution along the pores of the electrode materials. With the decrease of impedance, the Nyquist plot transits to a straight tail line corresponding to electrical double-layer formation. By back extrapolating the tail to the Z_{re} axis, EDR can be accessed as shown in Figure 5b.[21,22] It is clear that the influence of EDR on the performance cannot be overlooked since it is an even higher resistance than the $R_{cc} + R_e$. The dependence of EDR on the MSC configuration is unclear so far, and it is envisaged that great uncertainty exists for theoretical modeling because of the difficulty in reliably accessing the essential properties such as surface area and porosity of the deposited material, and also the EDR is dependent on the type of electrolytes and the matching between ions and the pore size of the electrode. In practice, it might be more convenient to find the optimized configuration through exploratory experimentation rather than relying on insufficiently accurate modeling.

In short, the benefit of gaining maximum power density and rate capability through designing more pair of fingers will be dependent on electrode and electrolyte materials type, in addition to other factors such as how well the interface between the electrode and current collector is engineered which determines whether the contact resistance should be taken into account for the analysis.

For the average power density, except for eq. (5), it can also be calculated through

$$P_{\mathrm{avg,\,ft}} = \frac{1}{2}\Delta V \cdot I_{\mathrm{ft}} \tag{14}$$

For the four MSCs in the present study, I_{ft} is the same, so that the only difference differentiating the average power is ΔV that is related to the ESR and the configuration. As shown in Table 3, the difference in $P_{\mathrm{avg,\,ft}}$ is insignificant among the devices at a current density of $I_{\mathrm{ft}} = 100\ \mu\mathrm{A\ cm}^{-2}$.

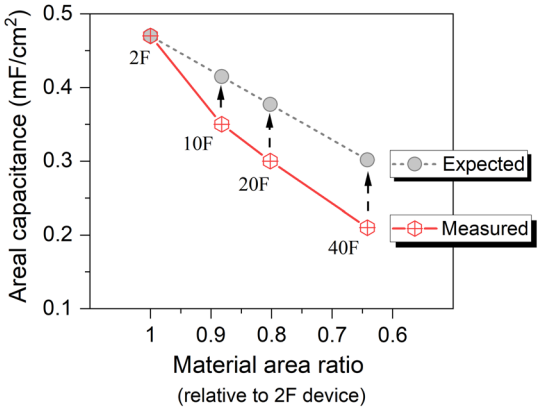

Figure 6. Areal capacitance of devices as a function of electrode material area ratio.

In terms of the areal capacitance, the difference among the devices is significant, with 2F (with highest A_a/A_{ft} ratio) displaying twice the capacitance of 40F (with lowest A_a/A_{ft} ratio) according to CV measurements at 20 and 200 mV s^{-1} scan rates, and a similar difference is observed in the GCD behavior at 100 μA cm^{-2}. To further investigate how the capacitance scales with the designed A_a/A_{ft} ratios, the expected and measured capacitances at 20 mV s^{-1} are normalized to the 2F device and are shown in **Figure 6**. The measured capacitance is less than what is expected from the active surface area; the more the fingers designed, the larger the loss of capacitance. This may be partly explained by multifinger designs having more circumferential area exposed to the plasma etching of the rGO materials. Even though, the plasma etching is anisotropic, materials on the edge of the fingers are likely to be etched during the O_2 ashing leading to a higher loss of electrode material in higher finger devices. The scanning electron microscopy (SEM) observation, shown in **Figure 7**a, indicates that close to the finger edges, there is a less coverage of rGO on the finger area (pointed by a blue arrow). The comparison in Figure 6 demonstrates the advantage of increased efficiency in material usage by using fewer fingers.

Previously, the influence of finger numbers on the performance was investigated for rGO-based MSCs.[12] It is worth noticing that the previous study[12] does not contradict the observations in this work, considering the very different experimental settings (different electrolyte types, different investigated scan rate range, as well as different rGO-coating thickness) as well as rGO thickness. Provided that the investigated scan rate range in the present study was shifted to 1000 mV s^{-1} and above, the same observation as the previous work [12] would be obtained that devices with the maximum finger number exhibit the maximum capacitance. However, the significantly high scan rate may be inappropriate for energy-optimized MSCs (thick micrometer scale rGO coating in this work), but suitable for power-optimized MSCs (thin 10 nm scale rGO coating in the study by Wu et al.[12]), from a practical point of view, thus the results should be interpreted correlating to target applications. Moreover, the ultrathin rGO coating in the previous work [12] can bear less influence from EDR, and thus, the performance may be reasonably well predicted by the influence of N on ESR (Figure 5). In contrast, the MSCs with a much thicker rGO coating (micrometer scale) do not scale intuitively. Thus, the porosity rendered by stacking of rGO layers may lead to a higher impact of EDR on the device performance. The coated rGO surface is shown in Figure 7b. The rGO surface is rather rough and seems to consist of a wide range of mesopores and micropores, which justifies the observed 45° line segment on the Nyquist plot (Figure 5), i.e., a transmission line effect due to porosity.

6. Conclusion

Energy and power densities of MSCs of four different configurations are investigated with an example of an rGO-based device fabricated by a spin-coating and etch method. The four different MSCs were designed on a fixed device footprint area and finger interspace, the finger number, together with finger width and length allowed for variations to fit the maximum of the footprint.

The results indicated that with the minimum finger numbers ($N = 2$ for 2F), the ratio of active material area to the footprint area is maximized, and thereby, capacitance and energy density can reach maximum value for 2F. Devices with more fingers can improve significantly the maximum power density, whereas the average power density is not as sensitive as the former. Accordingly, one can conceive the configuration depending on whether energy density or maximum power density is of prime interest for the specific application. However, the results should be interpreted carefully. The performance evaluation was performed within a relatively narrow scan rate range (20–200 mV s^{-1}) and low current density (100 μA/cm^2), which can be adequate for several practical applications, but the

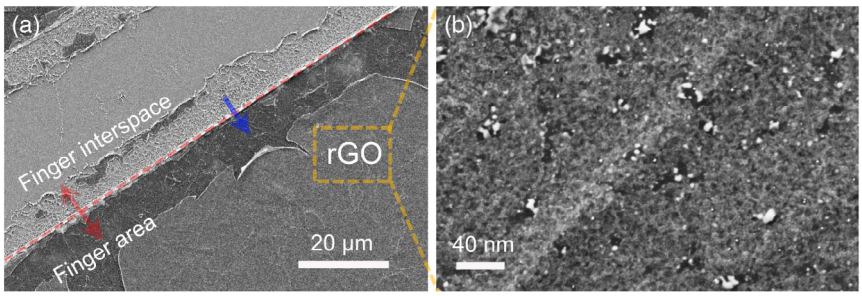

Figure 7. SEM images showing a) the finger edges of the devices and b) the morphology of rGO.

difference in average power density at higher rates can be more significant between few-finger and many-finger devices.

It should also be noted that the findings in this work are specific to a certain category of materials and fabrication methods. The EDR plays an important role for rGO-based devices, and the modeling from only current collector resistance R_{cc} and electrolyte resistance R_e may not cover the full picture of the device resistance. For electrode materials showing limited EDR contribution, the device resistance may be well represented with $R_{cc} + R_e$. A more comprehensive model considering contributions from all cell components and effects should be established to provide an answer to the question of how many fingers will result in optimized performances for a specific set of materials.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

areal energy density, areal power density, device configuration, microsupercapacitors, reduced graphene oxide

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