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Describing broadband terahertz response of graphene FET detectors by a classical model

Xinxin Yang, *Student Member, IEEE*, Andrei Vorobiev, *Member, IEEE*, Kjell Jeppson, *Life Member, IEEE*, and Jan Stake, *Senior Member, IEEE*

Abstract—Direct power detectors based on field-effect transistors are becoming widely used for terahertz applications. However, accurate characterization at terahertz frequencies of such detectors is a challenging task. The high-frequency response is dominated by parasitic coupling and loss associated with contacts and overall layout of the component. Moreover, the performance of such detectors is complicated to predict since many different physical models are used to explain the high sensitivity at terahertz frequencies. This makes it hard to draw important conclusions about the underlying device physics for these detectors. For the first time, we demonstrate accurate and comprehensive characterization of graphene field-effect transistors from 1 GHz to 1.1 THz, simultaneously accessing the bias dependence, the scattering parameters, and the detector voltage responsivity. Within a frequency range of more than 1 THz, and over a wide bias range, we have shown that the voltage responsivity can be accurately described using a combination of a small-signal equivalent circuit model, and the second-order series expansion terms of the nonlinear dc $I - V$ characteristic. Without bias, the measured low-frequency responsivity was 0.3 kV/W with the input signal applied to the gate, and 2 kV/W with the input signal applied to the drain. The corresponding cut-off frequencies for the two cases were 140 GHz and 50 GHz, respectively. With a 300-GHz signal applied to the gate, a voltage responsivity of 1.8 kV/W was achieved at a drain-source current of 0.2 mA. The minimum noise equivalent power was below 30 pW/ $\sqrt{\text{Hz}}$ in cold mode. Our results show that detection of terahertz signals in graphene field-effect transistors can be described over a wide frequency range by the nonlinear carrier transport characteristic obtained at static electrical fields. This finding is important for explaining the mechanism of detection and for further development of terahertz detectors.

Index Terms—terahertz detectors, graphene, field-effect transistors, broadband characterization, classical model, scattering parameters.

I. INTRODUCTION

TERAHERTZ (THz) electronics [1] plays an increasing role in emerging and traditional areas of spectroscopy, imaging, and wireless communication [2], as well as in earth and space sciences [3]. The direct power detector is an indispensable component for such applications [4], [5]. However, the required high sensitivity and stability of the detectors, over a wide frequency range and, preferably, at room temperature, are not readily available at the terahertz frequencies [6].

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The authors are with the Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Gothenburg, Sweden (e-mail: xinxin@chalmers.se).

Superconducting detectors, such as hot electron bolometers [7], can provide high sensitivity, but operate at cryogenic temperatures using relatively complex cooling systems, which can be justified only for specific applications. Nonlinear semiconductor devices, such as Schottky-barrier diodes [8], [9], backward tunnel diodes [10], heterojunction bipolar transistors [11] and field-effect transistors (FETs) [12], have been proven to be good candidates for high-sensitivity room-temperature detectors. In particular, development of broadband terahertz detectors based on FETs is being a target of intensive theoretical and experimental studies [13], [14], [15], [16] since the mid-90s. As a result, the complementary metal oxide semiconductor (CMOS) detectors with the noise equivalent power (NEP) as low as 10 pW/ $\sqrt{\text{Hz}}$ at 300 GHz have been demonstrated [17]. The NEP of the best published detectors based on the GaN high electron mobility transistors (HEMTs) is, currently, 26-31 pW/ $\sqrt{\text{Hz}}$ in the frequency range of 450-650 GHz [16]. Since the first demonstration of the graphene based [18] terahertz detector by Vicarelli et al. in 2012 [19], detectors based on the 2D materials have drawn increasing attention due to their unique properties, which open up possibilities for applications in a number of emerging areas requiring flexibility [20], and transparency while being compatible with state-of-the-art CMOS technology [21]. Apparently, a better understanding of device principles and the main limiting factors are important in order to exploit the full potential of graphene detectors. To explain the detection mechanisms, and corresponding modeling, at terahertz frequencies [22], many researchers have examined plasma wave mixing [19], thermoelectric [23], bolometric effects [24] and rectification, or resistive self-mixing, due to the nonlinearity of the dc $I - V$ characteristics [25].

However, these studies are not able to explain the underlying physics for detection at terahertz frequencies. Most research utilize antenna-coupled detectors [26], [16] and it is therefore difficult to perform accurate calibration of the available and reflected RF power. In addition, it is necessary to vary frequency, bias, temperature and other conditions to distinguish between different types of detection mechanisms. For example, the bias dependence of the detector responsivity was analysed by Khan et al. [27] at 500 GHz and by Sun et al. [28] at 900 GHz for antenna-coupled CMOS detectors and GaN HEMT detectors, respectively. On-wafer characterization [29] of FET detectors was recently demonstrated [30], but within a limited frequency band. In the research by Andersson et al. [25], on-wafer characterization was systematically applied to characterise GFET detectors using a Volterra series expansion

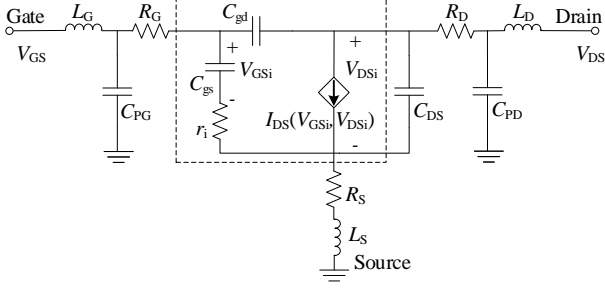


Fig. 1. Large-signal equivalent circuit of a GFET.

of the dc drain current, but only for a frequency range below 67 GHz and in cold mode. Nevertheless, no previous work has shown accurate broadband measurements that reveals the overall detection characteristics and only few report on classical quasi-static modeling of terahertz detectors.

In this work, we use recent advancements in terahertz on-wafer probe [31] characterization, which allow us to simultaneously measure the dc $I - V$ dependence, high frequency scattering parameters (S-parameters), and the GFET detector response from 1 GHz to 1.1 THz. The method provides accurate calibration of power in close vicinity of the device under test, and hence accurate characterization of the responsivity over an ultra-broad frequency range. The responsivity of the GFET versus frequency and bias with the input signal applied either to the gate or the drain terminals is investigated. Finally, it is shown that a standard FET equivalent circuit together with a series expansion of the nonlinear static $I - V$ characteristics [25], can reproduce the experimental data up to 1.1 THz and over a wide bias range. The main advantage of an empirical model is that no prerequisite knowledge of physical parameters or the level of model details are required in order to make conclusions about the main operating principles.

II. ELECTRICAL NONLINEAR MODEL

In this section the rectified output current of the GFET terahertz detector will be modeled using the nonlinear properties of the GFET as expressed by a second-order Taylor expansion of the dc $I - V$ characteristics of the GFET [27], i. e.

$$i_{\text{THz}} = \frac{1}{4}(g_{2,\text{gs}}v_g^2 + 2g_{2,\text{gs,ds}}v_gv_d \cos \theta + g_{2,\text{ds}}v_d^2), \quad (1)$$

where v_g and v_d are the intrinsic voltages of the ac signal applied to the gate and the drain terminals respectively, and where θ is the phase difference between them. The v_g , v_d and θ can be extracted using the equivalent circuit. The g_2 parameters are the second-order Taylor series coefficients obtained from the intrinsic voltage derivatives of the dc drain-source current (I_{DS}) with respect to the intrinsic drain-source

and gate-source voltages,

$$g_{2,\text{gs}} = \frac{\partial^2 I_{\text{DS}}}{\partial V_{\text{GSi}}^2}, \quad (2)$$

$$g_{2,\text{gs,ds}} = \frac{\partial^2 I_{\text{DS}}}{\partial V_{\text{GSi}} \partial V_{\text{DSi}}}, \quad (3)$$

$$g_{2,\text{ds}} = \frac{\partial^2 I_{\text{DS}}}{\partial V_{\text{DSi}}^2}, \quad (4)$$

where the intrinsic drain-source and gate-source voltages are given by $V_{\text{GSi}} = V_{\text{GS}} - R_{\text{S}}I_{\text{DS}}$ and $V_{\text{DSi}} = V_{\text{DS}} - (R_{\text{S}} + R_{\text{D}})I_{\text{DS}}$ as can be derived from the equivalent circuit in Figure 1. This model shows the intrinsic GFET (inside the dashed-line box) surrounded by external parasitic resistances (R_{G} , R_{D} and R_{S}), capacitances (C_{DS} , C_{PG} , and C_{PD}) and inductances (L_{G} , L_{D} and L_{S}).

For the voltage output, the detector can be modeled as a current source with an intrinsic source-drain resistance (r_{ds}). Thus the rectified voltage measured between the drain and the source terminals can be expressed as [32]

$$v_{\text{THz}} = \frac{i_{\text{THz}}r_{\text{ds}}R_{\text{M}}}{r_{\text{ds}} + R_{\text{D}} + R_{\text{S}} + R_{\text{M}}} \approx i_{\text{THz}}r_{\text{ds}}, \quad (5)$$

where R_{M} is the impedance of the voltmeter. The expression is simplified due to the relatively large value of R_{M} . Finally, the voltage responsivity of the detector is

$$\mathfrak{R}_{\text{V}} = \frac{v_{\text{THz}}}{P_{\text{ava}}(1 - |S_{ii}|^2)} \quad (6)$$

where P_{ava} is the available input signal power to the detector, and S_{ii} is the complex reflection coefficient S_{11} or S_{22} depending on whether the input signal is applied to the gate or the drain.

In the experimental section the g_2 parameters will be extracted from the measured dc $I - V$ characteristics and used for modeling the terahertz output voltage and responsivity. Finally, approximative analytical expressions for the g_2 parameters will be given in the appendix.

III. DESIGN, FABRICATION AND EXPERIMENTAL METHODS

Fig. 2 shows an optical micrograph of a GFET detector. The gate length (L) is 1.2 μm , and the gate width (W) is 5 μm (two 2.5- μm wide gate fingers in parallel). The devices were fabricated using single-layer chemical vapor deposition graphene (provided by Graphenea). Graphene was transferred onto Si/SiO₂ substrates (high-resistivity silicon with 1 μm SiO₂), and covered with a 6 nm Al₂O₃ layer to prevent any contaminations during following processing steps. The Al₂O₃ layer was deposited by repeating four times a sequence of e-beam evaporation and natural oxidation in air of a 1 nm Al layer. The area for the graphene mesa was defined by e-beam lithography, whereafter the Al₂O₃ and graphene outside the mesa were removed by buffered oxide etch and oxygen plasma, respectively. Source and drain electrodes were patterned by a standard sequence of the e-beam lithography, Al₂O₃ etch, Ti/Pd/Au (1 nm/15 nm/120 nm) deposition, and lift-off. After patterning of the gate area, a uniform Al₂O₃ gate dielectric was deposited by repeating six times a sequence of depositing 1 nm Al layers and natural oxidizing in air. Then

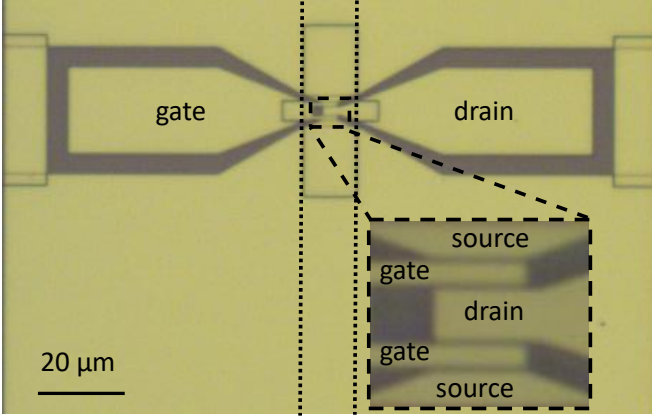


Fig. 2. Optical micrograph of a GFET detector where the dotted lines indicate the reference planes for the S-parameter calibration.

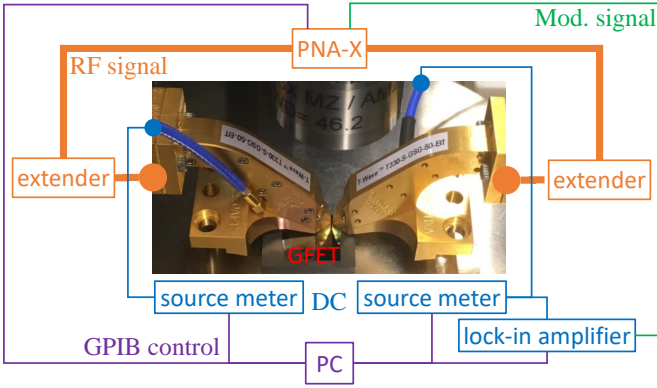


Fig. 3. A schematic block diagram of the on-wafer measurement setup including a photograph of the WR-3.4 T-waves probes.

Al/Au (100 nm/ 80 nm) gate electrodes were formed by using standard deposition and lift-off technology. Finally, Ti/Au (20 nm/280 nm) pad electrodes were formed by using deposition and lift-off.

The devices were characterized on-wafer at room temperature. Fig. 3 shows the schematic block diagram of the on-wafer measurement setup, together with a photograph of T-wave probes in WR-3.4 waveguide band. The signal obtained from a Keysight N5247A PNA-X microwave network analyzer with frequency extender modules from Virginia Diodes Inc. (VDI) was applied to the gate/drain using ground-signal-ground (GSG) probes. The rectified voltage between the drain and the source was measured using a SR830 lock-in amplifier with a modulation frequency of 1 kHz. The dc voltage and current were provided and measured by a Keithley 2604B Source meter.

For the frequency range of 1 to 67 GHz, the output signal power (P) was measured using a PNA power sensor 1-67 GHz at the end of coax cables. For other higher frequency ranges, the P was measured using a VDI Erickson PM5 Power Meter with taper waveguide section at the waveguide flange of the extenders. The available signal power (P_{ava}) was calculated from the measured P after subtraction of measured insertion loss and return loss of the probes. The S-parameters

were measured by the network analyzer with different on-wafer calibration procedures for different frequency ranges. For the frequency range of 1 to 67 GHz, a short-open-load-thru (SOLT) procedure was used by a CS-5 calibration kit from Picoprobe. For other higher frequency ranges, the on-wafer calibration is performed with thru-reflect-line (TRL) calibration kits which were designed and fabricated on the same substrate as GFET detectors. The TRL calibration kits consist of three kinds of standards, i.e., through, short and $\lambda/4$ line. To achieve a 50Ω line impedance and fit the device dimension at the same time, the width and the gap of the TRL calibration kits were designed to be 9 and 6 μm , respectively. Different extender modules, probes, power calibration tools, S-parameters calibration procedures and lengths of the $\lambda/4$ line for corresponding frequency ranges are listed in table I.

IV. RESULTS AND DISCUSSION

A. Second-order Taylor series coefficients

The second-order Taylor series coefficients, i.e., $g_{2,\text{gs}}$, $g_{2,\text{gs,ds}}$ and $g_{2,\text{ds}}$, were calculated from Eqs (2-3) based on the measured dc $I-V$ characteristics. To reduce the effects of noise in extracted data, a five-point moving average filter was applied while calculating the first-order derivatives. Fig. 4 (a), (b) and (c) show the $g_{2,\text{gs}}$, $g_{2,\text{gs,ds}}$ and $g_{2,\text{ds}}$ as a function of V_{GS} for a set of different I_{DS} in the range from -0.2 mA to 0.2 mA, respectively. Under cold condition (no bias), the $g_{2,\text{gs}}$ is zero, and the $g_{2,\text{gs,ds}}$ and $g_{\text{ds}2}$ are nonzero, which are displayed with black dashed curves in Fig 4. The observed increase of $g_{2,\text{gs}}$ with I_{DS} , in the vicinity of the Dirac point, can be explained by analyzing the corresponding expression derived from the analytical quasi-static GFET model (see Appendix). It can be seen, that for V_{DSi} much less than V_{GSi} , the $g_{2,\text{gs}}$ is linearly proportional to V_{DSi} . Analysis of the Eq. (8) in Appendix indicates that away from the Dirac point, i.e. at larger V_{GSi} , the $g_{2,\text{gs}}$ goes to zero, which is in agreement with dependences on Fig. 4 (a). It can be shown, that at larger V_{DSi} one can expect saturation of the $g_{2,\text{gs}}$, which can be associated with the charge carrier velocity saturation. With I_{DS} increasing, the curves of $g_{2,\text{gs,ds}}$ and $g_{2,\text{ds}}$ have positive shifts due to channel doping by the drain bias (see Eq. (9) and (10) in Appendix). Note that the polarities of the $g_{2,\text{gs,ds}}$ and $g_{2,\text{ds}}$ are opposite, which means that generated currents with opposite polarities can counteract each other.

B. Intrinsic ac signals

Fig. 5 shows the measured and modeled S-parameters at $V_{\text{GS}} - V_{\text{Dir}} = -0.2 \text{ V}$ and $I_{\text{DS}} = 0 \text{ A}$ versus frequency. For the last waveguide band (750-1100 GHz), we observed relatively large standing waves due to less accurate calibration and parasitics associated with the device. The parasitic capacitances (i.e., C_{PG} , and C_{PD}) and inductances (i.e., L_{G} , L_{D} and L_{S}) were extracted from measured S-parameters using open and short de-embedding structures, respectively [33]. The remaining circuit elements were then extracted from the measured GFET two-port S-parameters [34], as shown in table II. Based on these elements, the intrinsic ac signals were modeled using the equivalent circuit (see Fig. 1). Fig. 6 (a)

TABLE I
VDI FREQUENCY EXTENDER MODULES, PROBES, POWER CALIBRATION TOOLS, S-PARAMETER CALIBRATION PROCEDURES AND $\lambda/4$ -LINE LENGTHS FOR DIFFERENT FREQUENCY RANGES.

Frequency range	Extender	GSG probe	Power calibration tool	SP calibration	$\lambda/4$ -line length
1-67 GHz		coaxial infinity probe I67 - DC to 67 GHz	VNA power sensor 1-67 GHz	SLOT	
75-110 GHz	WR10	waveguide infinity probe I110-T-GSG-75-BT	Erickson PM5 Power Meter	TRL	347 μm
140-220 GHz	WR5.1	T-Wave Probe T220-T-GSG-75	Erickson PM5 Power Meter	TRL	191 μm
220-330 GHz	WR3.4	T-Wave Probe T330-T-GSG-75	Erickson PM5 Power Meter	TRL	111 μm
325-500 GHz	WR2.2	T-Wave Probe T500-S-GSG-50	Erickson PM5 Power Meter	TRL	74 μm
500-750 GHz	WR1.5	T-Wave Probe T750-GSG-25	Erickson PM5 Power Meter	TRL	49 μm
750-1100 GHz	WR1.0	T-Wave Probe T1100-GSG-25	Erickson PM5 Power Meter	TRL	31 μm

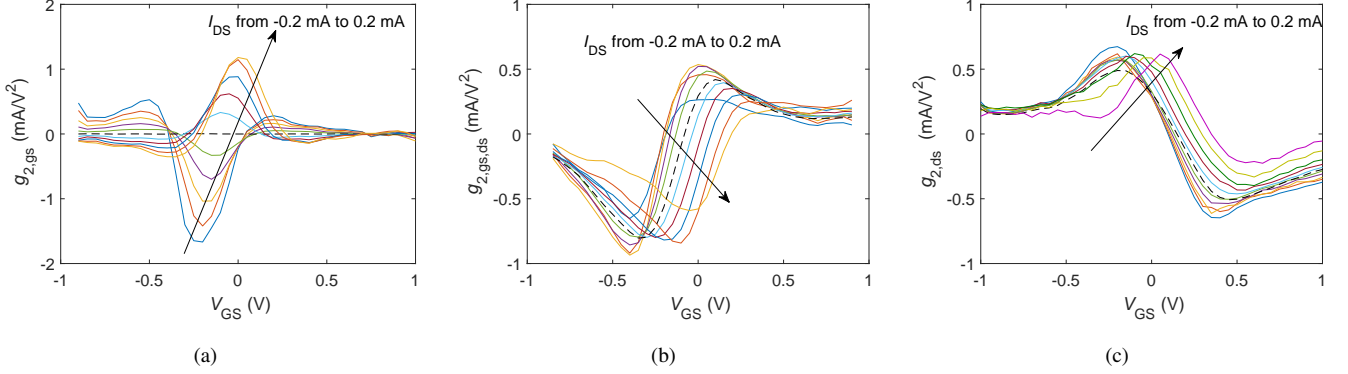


Fig. 4. $g_{2,gs}$ (a), $g_{2,gs,ds}$ (b) and $g_{2,ds}$ (c) versus V_{GS} for different drain currents in the range from -0.2 to 0.2 mA with 40 μA steps.

TABLE II
EXTRACTED PARAMETERS OF THE DEVICE (WITH PARASITIC $R_G = 1 \Omega$, $C_{PG} = C_{PD} = 1 \text{ fF}$, $L_G = 12 \text{ pH}$, $L_D = 8 \text{ pH}$ AND $L_S = 5 \text{ pH}$)

L (μm)	W (μm)	C_{gs} (fF)	C_{gd} (fF)	C_{DS} (fF)	$R_{S/D}$ (Ω)	r_i (Ω)	r_{ds} (Ω)
1.2	5	9	9	1	300	1	1400

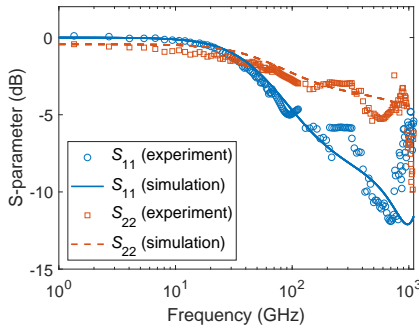


Fig. 5. Experimental and modeled device S-parameters at room temperature with $V_{GS} - V_{Dir} = -0.2 \text{ V}$ and $I_{DS} = 0 \text{ A}$.

and (b) show the modeled v_g , v_d and $\cos\theta$ with 1 μW signal applied to the gate and the drain, respectively. With the signal applied to the gate, v_g is much larger than v_d ; while with the signal applied to the drain, v_g is much lower than v_d .

C. Responsivity versus frequency

Fig. 7 (a) and (b) show the \Re_V versus frequency from 1 GHz to 1.1 THz with the signal applied to the gate and the drain, respectively. The \Re_V shows $1/f^2$ dependence at higher frequencies in agreement with the simulation results. Note that the \Re_V increases at lower frequencies with the signal applied to the gate because high-impedance mismatch at lower frequencies may reduce the accuracy of the characterization. The dash-dot lines indicate that the cut-off frequencies are around 140 GHz and 50 GHz with the signal applied to the gate and the drain, respectively. The cut-off frequency is mainly determined by the parasitic elements of the equivalent circuit in Fig. 1 [25]. Fig. 7 also shows the modeling results assuming only half of the parasitic resistance or/and gate capacitance, which demonstrates that further optimization can be achieved by increasing v_g and v_d via reducing the parasitic resistance and the gate capacitance.

D. Responsivity at 300 GHz versus bias

Due to effects of the high impedance and capacitive elements of the device at high frequencies, we assume that S_{11} , S_{22} , v_g and v_d are bias independent at 300 GHz. The top

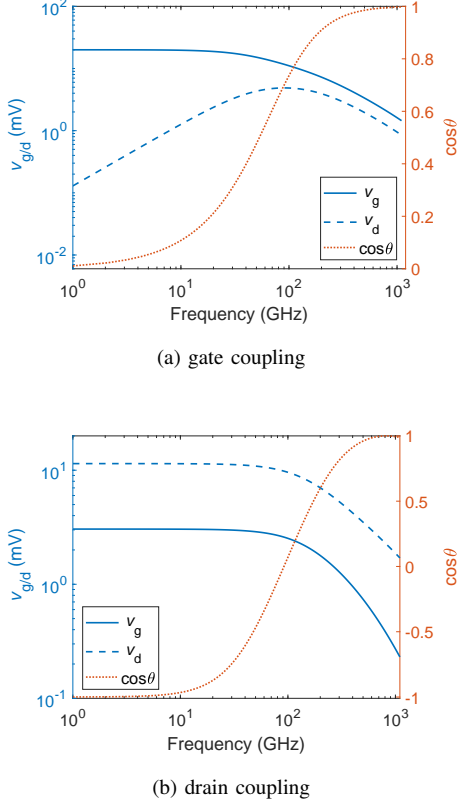


Fig. 6. Modeled v_g , v_d and $\cos \theta$ versus frequency of the device at $V_{GS} - V_{Dir} = -0.2$ V and $I_{DS} = 0$ A with $1 \mu\text{W}$ signal applied to the gate (a) and the drain (b).

row of Fig. 8 shows the experimental and simulation voltage responsivity \mathfrak{R}_V versus bias of the device with 300 GHz signal applied to the gate. The \mathfrak{R}_V , at V_{GS} close to the Dirac point (V_{Dir}), is proportional to I_{DS} , which follows the same trend as the $g_{2,gs}$ in Fig. 4 (a) except that under cold condition, as show in Fig. 8 (c). This is because, with the signal applied to the gate, v_g is much larger than v_d , as shown in Fig 6 (a), so the $g_{2,gs}$ term in Eq. (1) becomes the dominant part with the increase of the drain bias. When I_{DS} is zero, the \mathfrak{R}_V is not zero as $g_{2,gs}$ due to the contribution of the $g_{2,gs,ds}$ term. For negative biasing, the maximum value of the \mathfrak{R}_V increases up to 1.8 kV/W with $I_{DS} = -0.2$ mA. Compared with previously reported record value of 70 V/W [35], this is a breakthrough in GFET THz detection.

The bottom row of Fig. 8 shows the experimental and simulation \mathfrak{R}_V versus bias of the device with 300 GHz signal applied to the drain. The sign of the \mathfrak{R}_V changes from positive to negative with increasing V_{GS} . The maximum of \mathfrak{R}_V is approximately 300 V/W. As I_{DS} increases, there is a positive shift of the \mathfrak{R}_V curves with no obvious changes of the maximum of \mathfrak{R}_V , which follows exactly the trend of the $g_{2,ds}$. This is because v_g is much larger than v_d in the case of the signal applied to the drain (see Fig. 6). So the $g_{2,ds}$ term in Eq. (1) is the dominant part. As can be seen from Fig. 8, the nonlinear empirical quasi-static model shows excellent agreement with the experimental data.

According to above analysis, in the case of the signal

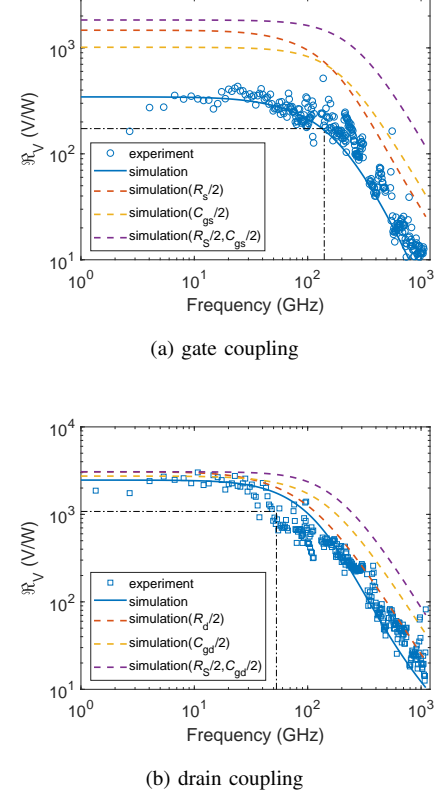


Fig. 7. Experimental and simulated voltage responsivity \mathfrak{R}_V versus frequency with the RF signal applied to the gate (a) and to the drain (b). Horizontal dash-dotted lines indicate $\mathfrak{R}_V/2$ at low frequencies, while vertical dash-dotted lines indicate the cut-off frequencies. Bias conditions during measurements were $V_{GS} - V_{Dir} = -0.2$ V and $I_{DS} = 0$ A.

applied to the gate, the response depends on the $g_{2,gs}$ and $g_{2,gs,ds}$ terms in the drain-biased and unbiased- mode respectively; while with the signal applied to the drain, the response depends on the $g_{2,ds}$ term only. Therefore, further performance improvements can be achieved using following approaches: i) increasing the $g_{2,gs}$, $g_{2,gs,ds}$ and $g_{2,ds}$ by reducing the residual carrier density (see Eq. (8-10) in Appendix) and experimentally demonstrated by Generalov et al. [35]; ii) increasing the v_g and v_d by reducing the contact resistance and the gate capacitance; iii) applying the signal at both the gate and the drain ports with 180-degree relative phase difference; iv) increasing $g_{2,gs}$ by increasing the drain biasing with the signal applied to the gate. Particularly, we can reduce the contact resistance and the residual carrier density via modifying the fabrication process [36], and a lower gate capacitance can be achieved by reducing the gate length.

E. NEP at 300 GHz versus bias

The sensitivity of a detector is evaluated by its NEP, which is given by $\text{NEP} = \sqrt{S_V}/\mathfrak{R}_V$ where S_V is the noise spectral density. Fig. 9 (a) shows the S_V at $V_{GS} - V_{Dir} = -0.2$ V and $V_{DS} = -0.1$ V, which was measured using a Keysight E4727A advanced low-frequency noise analyzer. The S_V reveals a $1/f$ spectral dependence with modulation frequency in the range of 1 Hz to 1 MHz. Therefore, the S_V noise with other bias

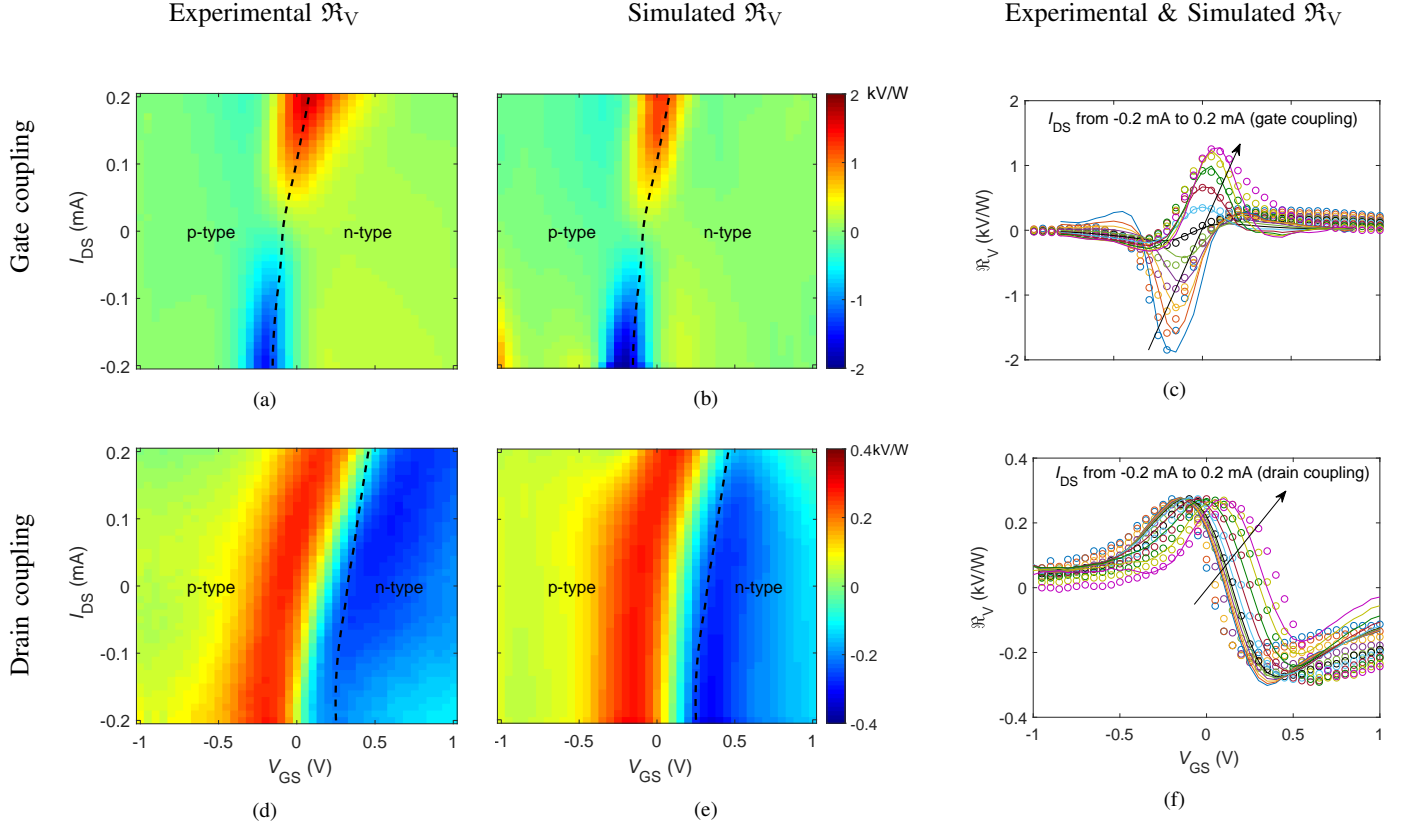


Fig. 8. 2D color plots of the experimental (left column) and the simulated (middle column) \mathfrak{R}_V versus V_{GS} and I_{DS} , and the experimental (symbols) and simulated (solid lines) \mathfrak{R}_V versus V_{GS} using I_{DS} (increasing in steps of $40 \mu A$ from -0.2 to 0.2 mA) as the parameter (right column), with a 300 GHz input signal applied to the gate (top row), and to the drain (bottom row) at room temperature. Dashed lines indicate position of Dirac point.

points can be estimated by the Hooge's model [37]. Fig. 9 (b) and (c) show the estimated minimum NEP at different V_{GS} (NEP_{min}) as a function of I_{DS} with 300 GHz signal applied to the gate and the drain, respectively. The solid and dashed lines indicate the NEP_{min} at modulation frequencies of 1 kHz and 1 MHz, respectively. The noise is lower at higher modulation frequency since the effect of $1/f$ noise is negligible and only dominated by the thermal noise, as shown by the dotted lines in Fig. 9 (b) and (c). At low modulation frequencies, the NEP increases with the drain biasing, since $1/f$ noise is the main noise of the detector. While at high modulation frequencies NEP decreases with the current biasing when the THz signal is applied to the gate, which is due to the increase of responsivity with the drain bias. At 1 kHz modulation frequency, the minimum NEP of 26 and 24 pW/\sqrt{Hz} with 300 GHz signal applied to the gate and the drain respectively, appears at zero drain biasing. To achieve a lower NEP, both higher \mathfrak{R}_V and lower noise are required. We have discussed four methods to increase the \mathfrak{R}_V above. However, the last method, i.e. increase of the drain biasing, can introduce extra noise source.

V. CONCLUSION

In conclusion, we have demonstrated accurate and comprehensive on-wafer characterization of GFET detectors, which allows for corrections of the impedance mismatch and thereby opens up possibility for detailed measurements up to terahertz frequencies. It is shown that the GFET response versus frequency and bias can be well predicted by a nonlinear empirical

model derived from the dc $I - V$ characteristics and the S-parameters. Previous research on large signal quasi-static device models [38] of GFETs has successfully been applied to design terahertz heterodyne mixers [39] and detectors. This indicates that drift-diffusive type charge-carrier transport or quasi-static models are sufficient to describe the operation of GFETs from dc to terahertz frequencies. Finally, we reported a voltage responsivity of 1.8 kV/W at I_{DS} of 0.2 mA and a minimum NEP less than 30 pW/\sqrt{Hz} under cold condition at 300 GHz. Table III compares the terahertz voltage responsivity and NEP achieved in this work with terahertz detectors fabricated by different technologies. The presented GFET detector reveals significant improvement in performance at terahertz frequencies, in comparison with previously published graphene based detectors, and approaching the semiconductor based counterparts. This work provides a basis for understanding of the broadband terahertz detection in the GFET based detectors, which will advance the development of FET based terahertz electronics.

APPENDIX

ANALYTICAL QUASI-STATIC GFET MODEL

According to the drain resistance model[44] of GFET, the dc drain current can be expressed as

$$I_{DS} = q\mu \frac{W}{L} \sqrt{n_0^2 + \left[\frac{C_{ox}(V_{GSi} - V_{DSi}/2 - V_{Dir})}{q} \right]^2 V_{DSi}}, \quad (7)$$

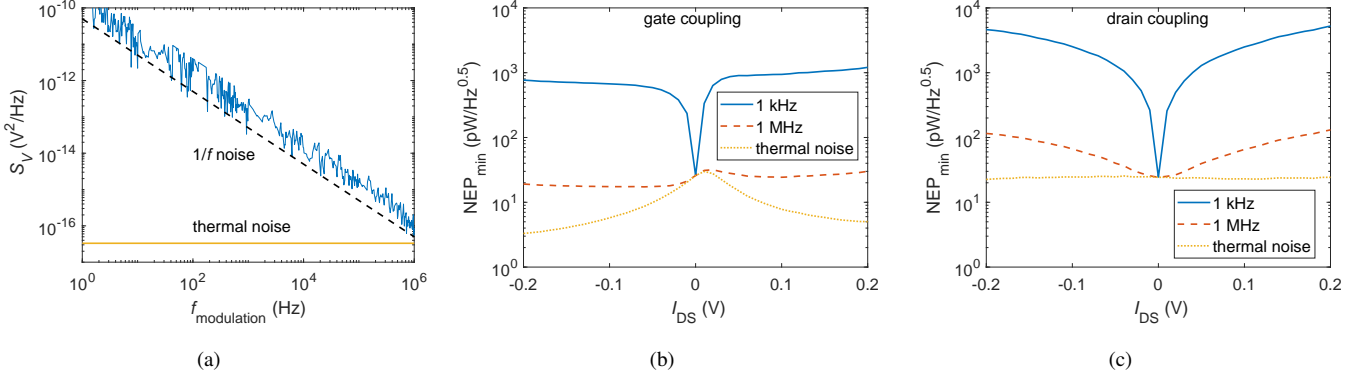


Fig. 9. Measured noise spectral density at $V_{GS} - V_{Dir} = -0.2$ V and $V_{DS} = -0.1$ V (a), estimated NEP_{min} versus I_{DS} with a 300 GHz signal applied to the gate (b), and the drain (c).

TABLE III
COMPARISON OF ROOM-TEMPERATURE THZ DETECTORS.

Technology	R_V (V/W)	NEP (pW/ \sqrt{Hz})	Frequency (GHz)	drain or base bias	Ref.
GFET	1800	1000	300	with	This work
GFET	300	24	300	without	This work
GFET	74	130	400	without	A. Generalov et al. [35]
GFET	14	515	600	without	A. Zak, et al. [40]
AlGaIn/GaN HEMT		25-31	450-650	without	M. Bauer et al. [16]
AlGaIn/GaN HEMT		30-20	700-900	without	H. Qin et al. [41]
Si CMOS	5000	10	300	without	F. Schuster et al. [17]
Si CMOS	1500	15	200	without	M. W. Ryu et al. [42]
SBD	400-4000	1.5-15	100-900	without	J. L. Hesler et al. [8]
SBD	250	33	280	with	R. Han et al. [9]
SiGe HBT	6121	21	315	with	H. Ghodsi et al. [11]
Sb-based HBD	2400	2.14	170	without	S. M. Rahman et al. [43]

where q is the elementary electron charge, μ is the carrier mobility, n_0 is the carrier density at the Dirac point, and C_{ox} is the gate capacitance per unit area. Then the Taylor coefficients in Eq. (2-4) can be expressed as

$$g_{2,gs} \approx \frac{\mu W}{q L} \frac{C_{ox}^2 V_{DSi}}{\sqrt{n_0^2 + [\frac{C_{ox}(V_{GSi} - V_{DSi}/2 - V_{Dir})}{q}]^2}}, \quad (8)$$

$$g_{2,gs,ds} \approx \frac{\mu W}{q L} \frac{C_{ox}^2 (V_{GSi} - V_{DSi}/2 - V_{Dir})}{\sqrt{n_0^2 + [\frac{C_{ox}(V_{GSi} - V_{DSi}/2 - V_{Dir})}{q}]^2}}, \quad (9)$$

$$g_{2,ds} \approx -\frac{\mu W}{q L} \frac{C_{ox}^2 (V_{GSi} - V_{DSi}/2 - V_{Dir})}{2\sqrt{n_0^2 + [\frac{C_{ox}(V_{GSi} - V_{DSi}/2 - V_{Dir})}{q}]^2}}. \quad (10)$$

Thus the rectified voltage at the signal applied to the gate and under drain current basing can be approximated as

$$v_{THz} \approx \frac{C_{ox}^2 V_{DSi}}{(qn_0)^2 + [C_{ox}(V_{GSi} - V_{DSi}/2 - V_{Dir})]^2} * v_g^2. \quad (11)$$

The rectified voltage at the signal applied to the gate and without drain current basing can be approximated as

$$v_{THz} \approx \frac{C_{ox}^2 (V_{GSi} - V_{DSi}/2 - V_{Dir})}{(qn_0)^2 + [C_{ox}(V_{GSi} - V_{DSi}/2 - V_{Dir})]^2} * v_g v_d \cos \theta. \quad (12)$$

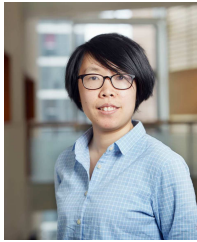
The rectified voltage response at the signal applied to the drain can be approximated as

$$v_{THz} \approx -\frac{1}{2} \frac{C_{ox}^2 (V_{GSi} - V_{DSi}/2 - V_{Dir})}{(qn_0)^2 + [C_{ox}(V_{GSi} - V_{DSi}/2 - V_{Dir})]^2} * v_d^2. \quad (13)$$

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Xinxin Yang (S'15) was born in Hebei, China in 1988. She received the B.Sc. degree in Materials Physics from Hebei University of Technology in 2011 and the M.Sc. degree in Electronics and Communication Engineering from University of the Chinese Academy of Sciences in 2014, and is currently working toward the Ph.D. degree at the Chalmers University of Technology. Her research involves graphene electronics for microwave and terahertz applications.



Jan Stake (S'95–M'00–SM'06) was born in Uddevalla, Sweden, in 1971. He received the degrees of M.Sc. in electrical engineering and Ph.D. in microwave electronics from Chalmers University of Technology, Göteborg, Sweden in 1994 and 1999, respectively.

In 1997 he was a Research Assistant with the University of Virginia, Charlottesville, USA. From 1999 to 2001, he was a Research Fellow with the Millimetre Wave Group at the Rutherford Appleton Laboratory, Didcot, UK. He then joined Saab Combitect Systems AB, as a Senior RF/microwave Engineer, until 2003. From 2000 to 2006, he held different academic positions with Chalmers University of Technology and, from 2003–2006, was also Head of the Nanofabrication Laboratory, Department of Microtechnology and Nanoscience (MC2). During summer 2007, he was a Visiting Professor with the Submillimeter Wave Advanced Technology (SWAT) Group at Caltech/JPL, Pasadena, USA. He is currently Professor and Head of the Terahertz and Millimetre Wave Laboratory, Chalmers University of Technology, Sweden. He is also cofounder of Wasa Millimeter Wave AB, Göteborg, Sweden. His research involves graphene electronics, high frequency semiconductor devices, THz electronics, submillimeter wave measurement techniques ("THz metrology"), and THz in biology and medicine.

Prof. Stake served as Editor-in-Chief for the IEEE Transactions on Terahertz Science and Technology between 2016–2018, and topical editor between 2012–2015.



Andrei Vorobiev (S'01) Andrei Vorobiev received the M.Sc. degree in physics of semiconductors and dielectrics from Gorky State University, Gorky, Russia, in 1986, and the Ph.D. degree in physics and mathematics from the Institute for Physics of Microstructures, Russian Academy of Sciences, Nizhny Novgorod, Russia, in 2000. In 2008, he was an Associate Professor in physical electronics from the Chalmers University of Technology, Gothenburg, Sweden. He currently holds a Senior Research Chair with the Chalmers University of Technology. His

main research interests are in development and application of emerging functional materials and phenomena in microwave devices. His current activities focus on materials, technology, and design of graphene-based field-effect transistors and components/systems for microwave/terahertz applications.



Kjell Jeppson (S'68,–M'76–SM'83–LM'12) is professor emeritus at Chalmers University of Technology, Gothenburg, Sweden. He received the Ph.D. degree from the same university in 1977 based on a thesis entitled "Studies of metal-insulator-semiconductor structures", the main focus of which concerned negative bias stress (NBS) of metal-oxide-semiconductor capacitors - a work that by now has been cited more than 800 times. In the seventies he was with Rockwell International in Anaheim, CA (1973–74), and he has been on sabbatical leaves at

Southampton University and at Shanghai University. He has published several papers on nonvolatile memories, transistor modeling and parameter extraction, CMOS gate delay and buffer optimization, and substrate-noise coupling. After retirement his research has focused on the use of carbon nanotubes for through-silicon-vias, and on the use of graphene for heat spreaders and for flexible terahertz detectors. He has also authored a book on semiconductor devices (in Swedish). He is a member of the technical program committee of the International Conference on Microelectronic Test Structures (ICMTS).