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Comparison of Thermally Grown Carbon Nanofiber-Based and Reduced Graphene Oxide-Based CMOS-Compatible Microsupercapacitors

Agin Vyas,* Simin Zare Hajibagher, Qi Li, Mazharul Haque, Anderson Smith,* Per Lundgren, and Peter Enoksson

Microsupercapacitors as miniature energy storage devices require complementary metal–oxide–semiconductor (CMOS) compatible techniques for electrode deposition to be integrated in wireless sensor network sensor systems. Among several processing techniques, chemical vapor deposition (CVD) and spin coating, present in CMOS manufacturing facilities, are the two most viable processes for electrode growth and deposition, respectively. To make an argument for choosing either of these techniques to fabricate MSCs utilizable for an on-chip power supply, we need a comparative assessment of their electrochemical performance. Herein, the evaluation of MSCs with CVD-grown carbon nanofiber (CNF)-based and spin-coated reduced graphene oxide (rGO)-based electrodes is reported. The devices are compared for their capacitance, energy and power density, charge retention, characteristic frequencies, and ease of fabrication over a large sweep of scan rates, current densities, and frequencies. The rGO-based MSCs demonstrate 112 $\mu F\,cm^{-2}$ at 100 $mV\,s^{-1}$ and a power density of 12.8 $mW\,cm^{-2}$. The CNF-based MSCs show 269.7 $\mu F\,cm^{-2}$ and 30.8 $mW\,cm^{-2}$. CVD-grown CNF outperforms spin-coated rGO in capacitive storage at low frequencies, whereas the latter is better in terms of charge retention and high-frequency capacitance response.

1. Introduction

The setup of wireless sensor networks (WSNs) for the Internet-of-things (IoT) is highly dependent on long-time collection of information without forgoing its autonomous nature.[1] This increases

the need for scrutiny of the lifetime of a WSN power supply. Batteries, which are conventionally used for powering such sensors, cannot wholly succeed in powering the device for a long time due to their inferior cyclic stability.[2] In such cases, increasing demands on the lifetime of the power supplies for WSNs for IoT can be met through microsupercapacitors (MSCs). MSCs are miniaturized supercapacitors that exhibit high power densities with long cyclic stability.[3]

To be integrated into wafer-scale fabrication of sensors for WSNs, MSCs must be compatible with complementary metal–oxide–semiconductor (CMOS) technology. There are several CMOS compatible techniques, for example, inkjet printing,[4–6] laser scribing,[7–9] chemical vapor deposition (CVD),[10–13] and spin coating[14–16] that have been used for MSC fabrication. Among these, the CVD and spin coating are among the most standard existing technologies used in a semiconductor foundry. Both processes are fast and highly scalable in terms of electrode thickness. Furthermore, these electrode deposition techniques are versatile in dispensing and growing electrode material. However, they inherit certain trade-offs that can limit their electrochemical performance in specific applications.

To adopt a well-reasoned option, we need to make a comparative evaluation of the two MSC fabrication techniques regarding both features and electrochemical performance. In this work, we have fabricated MSCs using CVD for growing CNFs, and spin coating GO for electrodes and tested their performance through electrochemical potentiometry with an ionic electrolyte, ethyl-3-methyl-imidazolium bis(trifluoromethylsulfony)imide (EMIM-TFSI). EMIM-TFSI is chosen for its high thermal stability and good conductivity. The devices are compared for their fabrication features, capacitance, energy density, and power density.

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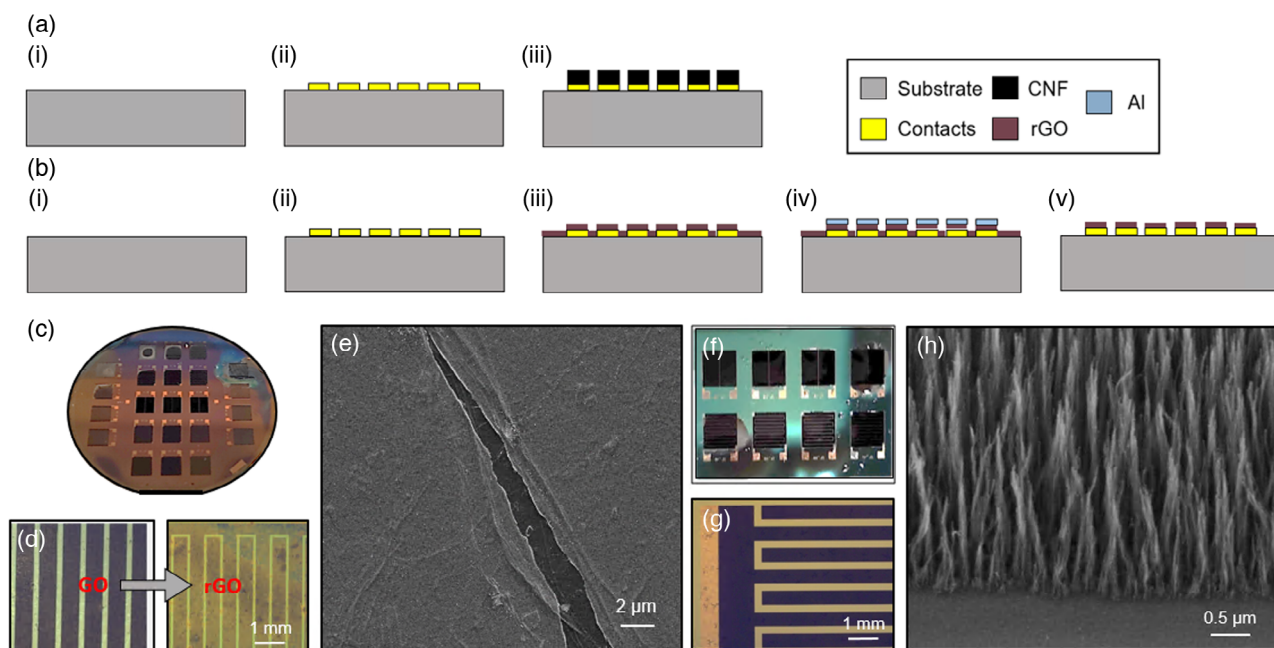The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssb.202000358.

2. Experimental Section

2.1. Fabrication

Figure 1a,b shows the fabrication process for the two MSC devices. These processes were carried out on separate 2″

Figure 1. a) Schematic fabrication process for CVD-CNF and b) spin-coated rGO MSCs (thickness not scaled). c) Captured image of the spin-coated rGO wafer through a conventional camera. d) Optical microscopic image of the current collectors with rGO electrodes before and after material annealing. e) rGO flakes as seen in SEM under high magnification. f) Scanning electron micrograph of CNF (reproduced under the terms of a CC-BY license.[13] Copyright 2020, The Authors, published by The Royal Society of Chemistry). g) Optical micrograph of the fabricated CNF-MSC. h) SEM image of the CNFs under high magnification.

Si wafers. A 400 nm SiO_2 was thermally grown on its surface after standard cleaning (Figure 1a,b(i)). The Au/Ti current collectors were defined by a lift-off sequence onto the wafer surface (Figure 1a,b(ii)). For CNF growth, the wafer was diced into smaller chips, which were processed separately. The CNFs were grown on the current collectors at 390 °C using a catalytic surface and a mixture of acetylene and ammonia as process gases. The details of the catalysis process were described thoroughly by Desmaris and coworkers.[17] The CNF was grown at 390 °C in a mixture of acetylene and ammonia (Figure 1a(iii)). Figure 1h shows the scanning electron micrograph of the material. The length of each fiber is ≈3 μm from ocular inspection. The total active material area on both the planar interdigitated electrodes combined was 0.81 cm^{-2}. The estimation of volume are observed further in Vyas et al.[13] and Saleem et al.[17]

For the second device, graphene oxide (GO) was prepared through conventional Hummer's method. The details for preparation of solution can be procured at Smith et al.[18] The prepared GO solution had a density of 3 g L^{-1}. The solution was sonicated at 35 kHz for 15 min before spin coating. The solution was spin coated at 1000 rpm five times, on the substrate of Si/SiO$_2$ (280 μm/400 nm) (Figure 1b(iii)). The substrate was later hard baked at 100 °C overnight. A layer of polymer was coated over the wafer surface at 1000 rpm. The deposited polymer layer was hard masked with Al through lithography (Figure 1b(iv)). Initially a 70 nm Al film was evaporated over the surface through e-beam evaporator (Kurt J. Lesker, PVD225). During the lithography step, a second photomask was developed over the surface of Al layer. The photoresist was developed under MF-319

(Microposit) until the exposed resist dissolved in the solution. The exposed Al area was etched through a Cl$_2$-based reactive ion etching recipe with a laser endpoint detector set for reflectivity of graphene layer underneath. The exposed GO was etched off using O$_2$ plasma. The hard mask is etched and GO is annealed at 500 °C into rGO (Figure 1b(v)). The recipe is discussed in further detail in corresponding literature.[14] The final fabricated devices are shown in Figure 1c,f. The wafer in 1(c) is a 2 in. wafer. Figure 1d shows the optical micrographs of GO and rGO electrode on the Au/Ti current collectors before and after annealing the wafer at 500 °C, respectively. The pink hue on the surface showed the presence of transparent rGO on metal current collector. Figure 1e shows the scanning electron microscope graphs of rGO electrode. The graphene sheets were visible in the large crack stack on top of each other in a uniformly dense fashion.

The heights of the rGO and CNF electrodes were measured using a surface profiler across the electrodes shown in Figure 1c,e. The rGO on the spin-coated devices amounted to 1.1 μm in height, whereas the CNF grown through the CVD process is 3 μm. The area of the devices considered is 0.13 cm^{-2} with the length and width of the MSC device as 4.7 and 4 mm, respectively. Each device has 20 interdigitated fingers for each electrode with a spacing of 40 μm between them.

2.2. Device Characterization

After fabrication, the devices are measured in open atmospheric conditions from 0 to 1 V. The cyclic voltammograms were

measured for different scan rates from 20 to 5000 mV S^{-1}. The capacitance of the devices is calaculting from integrating the area under the current to calculate the charge stored over the voltage window from the equation

$$C = Q/(2\Delta V) \tag{1}$$

where C is the total capacitance, Q is the total charge stored, and ΔV as the voltage window for the electrolyte. The energy density of the devices is calculated from

$$E = \frac{C\Delta V^2}{2} \tag{2}$$

The cyclic charge–discharge experiments were conducted with a constant current from 1 to 100 µA cm^{-2}. The maximum power is calculated from these experiments as

$$P = \frac{\Delta V^2}{4R_{esr}} \tag{3}$$

where R_{esr} is the total device resistance calculated from the IR-drop found in the charge–discharge curves. The areal and volumetric capacitances were calacuted from the aforementioned equations by normalizing the values over the total active electrode footprint and overall electrode volume, respectively. Electrochemical impedance spectroscopy (EIS) measurements were carried out in a frequency range of 10 mHz–10 MHz. The characteristic frequency (f_k), calculated at $-45°$ phase angle, is used to calculate the time required to discharge with more than 50% efficiency.[19]

3. Results

Figure 2 and **3** shows the results for each device's electrochemical measurements at varying scan rates and frequencies of operation. These scan rates and frequencies are chosen to represent expected voltage, current, and alternating current (AC) frequency ranges applicable in integrated wireless systems energy harvester scenario.[20] The devices chosen for both the cases are MSCs with 20 interdigitated fingers on each current collector with a spacing of 40 µm between them. The choice of finger geometry was based on the fact that 20 fingers demonstrate the highest power density in the smallest footprint area compared with five and ten fingers. The trends for cyclic voltammetry and chronopotentiometry were similar for all three finger geometries.

The two devices with rGO and CNF electrodes were measured using ionic liquid electrolyte EMIM-TFSI in Gamry Echem Analyst. Figure 2a shows the cyclic voltammograms of the MSCs at 100 and 1000 mV s^{-1} scan rates. The curves suggest a high capacitance for the CNF-MSC compared with the rGO-MSC at both the scan rates. The values for these devices are shown in **Table 1**. The rGO-MSCs show a more rectangular CV behavior compared with the CNF-MSCs. Figure 2b shows the galvanostatic charge–discharge curves for the MSCs at current densities of 2 and 5 µA cm^{-2}. The rGO-MSC shows a larger IR-drop (ΔV) of 1.6 mV compared with that of 0.6 mV for CNF-MSC at the current density of 2 µA cm^{-2}. We obtain a similar result for 5 µA cm^{-2} too. Figure 2c shows the Nyquist plot of the two devices. The internal resistance of the devices, rGO-MSC and CNF-MSC, measured at the x-axis intercept, is 127 and 89 Ω, respectively. Furthermore, we evaluated the impedance trends in Figure 2c by performing an equivalent circuit analysis using constant phase element (CPE) with diffusion model. The equivalent series resistance of the devices was 133 and 88 Ω, respectively, for rGO and CNF-MSC. Supercapacitors are imperfect capacitors whose degree of ideal device behavior can be measured by its dispersion coefficient measure which is between 0 to 1, the latter for an ideal capacitor.[21] For the rGO-MSC, the dispersion coefficient was 0.74, which is lower than that of the CNF-MSC, i.e., 0.89.

Figure 3a shows the normalized areal capacitance to increasing the scan rate for the rGO and CNF-MSCs. The rGO-MSC is significantly better at retaining its capacitance, steadily decreasing to just over 50% retention at 5 V s^{-1}. The CNF-MSC suffers a substantial drop in its charge retention at scan rates higher than 100 mV s^{-1}. The influence of frequency of the CNF-MSCs is even more significantly visible in Figure 3b,c where we see the maximum capacitance and phase angle trends over a sweep of different frequencies. In Figure 3c, we see that f_k for rGO-MSC was 1.25 kHz, whereas the CNF-MSC performed significantly worse with 45 Å phase angle at 158 Hz. Figure 3d shows the variation of device capacitance over a range of current densities.
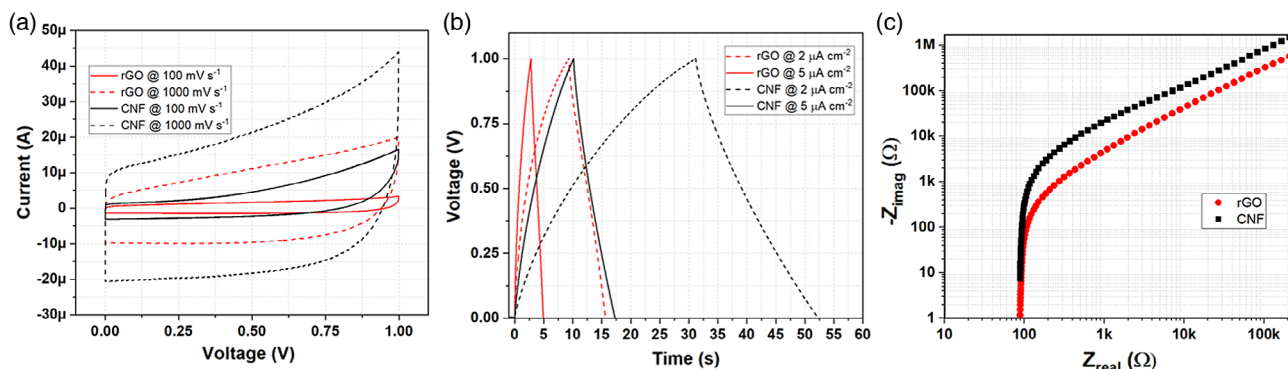
Figure 2. Electrochemical characterization results of the measured rGO- and CNF-MSCs. a) Cyclic voltammograms of devices at 100 and 1000 mV s^{-1}. b) Galvanostatic charge–discharge curves at constant current densities of 2 and 5 µA cm^{-2}. c) EIS Nyquist plot for the MSCs at alternating current of 0.5 mV.
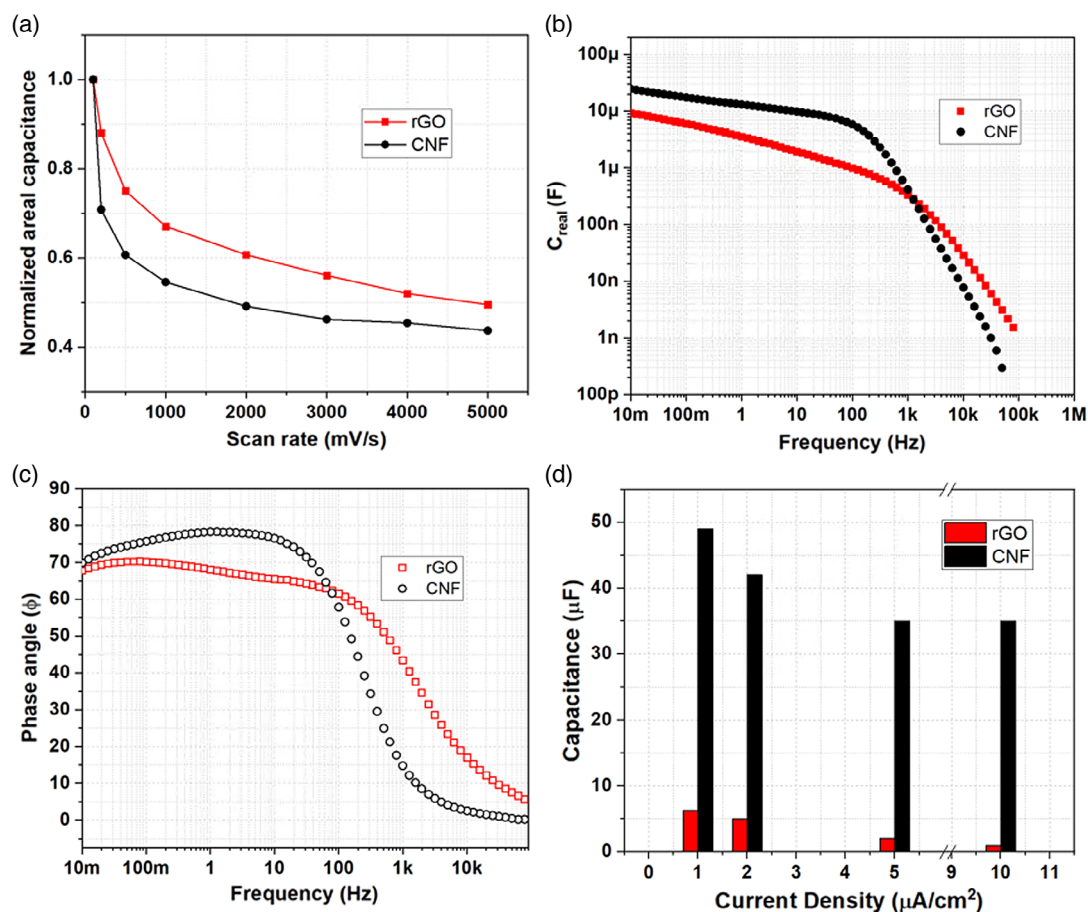
Figure 3. a) Normalized areal capacitance of the rGO- and CNF-MSCs over different scan rates. b) Bode plot for devices with maximum capacitance over a sweep of frequencies. c) Phase angle exhibited by the devices over different frequencies of operation. d) Capacitance of rGO and CNF MSCs at various current densities.

Table 1. List of capacitance, energy, and power density measurements from the CV and GCD characterization of the rGO- and CNF-MSCs.

Device	Areal capacitance [μF cm^{-2}]		Energy Density [μJ cm^{-2}]		Power density [mW cm^{-2}]	
Input signal	100 mV s^{-1}	1000 mV s^{-1}	100 mV s^{-1}	1000 mV s^{-1}	2 μA cm^{-2}	5 μA cm^{-2}
rGO	112.0	72.5	56.0	36.3	12.8	5.5
CNF	269.7	147.2	134.8	73.6	30.8	14.8

4. Discussion

After comparing the device performance of rGO-MSCs and CNF-MSCs, we see that both the devices come with certain advantages and trade-offs. Regarding fabrication, the CVD-grown CNFs are easier to fabricate as the electrodes can be grown directly on the current collectors. The fabrication through spin coating requires additional steps for etching the rGO material from the areas apart from the current collectors. Regarding the fabrication process's thermal budget, the CVD process is accomplished at 390 °C. Meanwhile, for the spin-coating process, the temperatures required for GO to rGO conversion is 500 °C. Even though in the current process, the temperatures are higher for rGO, spin coating preconditioned rGO, or using a variety of high surface

area electrode materials that do not require high temperatures can significantly reduce the process's overall thermal budget. The CVD process, also, is not uniform across a substrate larger than a few cm^{-2}.[18] Therefore, Si dies with current collector patterns are introduced in the CVD furnace. On the other hand, the spin-coating process is reproducible and scalable to a wafer substrate. Moreover, it is not dependent on the substrate itself. This factor can result in extremely high yields in a single process with similar uniformity of performance. Furthermore, the rGO-MSC revealed a maximum volumetric capacitance of 9.18 ± 0.06 F cm^{-3}, and the CNF-MSC showed 8.23 ± 0.2 F cm^{-3}. Scaling of capacitance with thickness is often debated as increasing the thickness reduces the inter- and intracolumnar distance between the electrodes leading to poor electrolyte penetration. However, this effect usually occurs

Table 2. Comparison of high performance supercapacitors fabricated through different fabrication techniques.

Ref.	Fabrication method	Electrode	Electrolyte	Voltage window	Power density [mW cm^{-2}]
[24]	C-MEMS	MoS$_2$@rGO-carbon-nanotube	H$_2$SO$_4$/PVA	0.8	1
[25]	CVD	Multilayer graphene	H$_2$SO$_4$/PVA	0.8	3.1
[26]	LbL	Heteroatom (b, N)-doped graphene	H$_2$SO$_4$/PVA	0.8	3.7
[27]	CVD	VG	PYR1,3TFSI	4	4
[28]	Ink-jet	rGO-PANI	H$_2$SO$_4$/PVA	0.8	5
[29]	CVD	Monolithic 3D graphene	H$_2$SO$_4$/PVA	0.8	14.4
[30]	CVD	Diamond-coated SiNWs	Et$_3$NH TFS	4	25
[31]	CVD	p-doped poly(3,4-ethylenedioxythiophene) polystyrene (PEDOT)-Cl	EMIMBF$_4$	4	61.2
[32]	LbL	3-layer graphene/PEDOT	H$_2$SO$_4$/PVA	0.8	131

at a higher thickness of over 10 μm. Another interesting observation on comparing areal capacitances shown in Table 1 is that the difference in measured capacitance between the two devices correlates with the difference in the rGO and CNF electrode thickness, i.e., more than a factor of 2 but less than 3. So, if we increase the number of spins and the electrode solution's density, we might achieve higher capacitance values by increasing the rGO electrode thickness. This can be considered as a future direction for improving the capacitance of spin-coated MSCs. Considering all the aforementioned factors, the spin-coating technique is a solution that is beneficial for the mass production of MSCs with a minimum thermal budget.

However, considering other factors of performance, such as demonstration of a low phase angle at low frequencies, it can be believed that defects can occur during fabrication, as conventional pure form rGO has demonstrated a phase angle of 84°.[22] The CNF-MSC, in comparison, performs much better than by having a high phase angle of about 80°. In literature, there are higher capacitance values found with electrode grown through the same technique.[23] **Table 2** shows the performance of some MSCs described in literature. The devices have been arranged in an ascending order of their power density. These devices are chosen for their high power densities among numerous devices studied by the author. The rGO and CNF MSCs lie in the middle of the comparison in Table 2. Overall, CNF-MSC grown through the CVD process performs better over rGO-MSC, fabricated via spin-coating electrode material on a wafer substrate, in terms of areal capacitance and low-frequency response, whereas the rGO-MSC demonstrates better performance in terms of charge retention and time constant.

5. Conclusion

A longer lifetime for the on-chip power supply is essential for the deployment of WSNs in remote area applications for IoTs. MSCs fabricated through CVD and spin-coating processes can be directly integrated into pre-existing CMOS circuits. In rGO-MSC, a layer of rGO is spin coated for a thickness of 1.1 μm, whereas in case of CNF-MSC, the CVD-grown CNF had a length of 3 μm. The capacitance and power density of CNF-MSCs are 270 μF cm^{-2} and 30.8 mW cm^{-2} approximately three times higher than rGO-MSCs' 112 μF cm^{-2} and

12.8 mW cm^{-2}. This can potentially be explained by the difference in their electrode thicknesses; however, further studies are required to study the impact of electrode thickness on both the processes. The charge retention capability of rGO-MSC is higher compared with CNF-MSC at 51% compared with 43% for high scan rates. The characteristic frequency of rGO-MSC is 1.25 kHz, whereas CNF-MSC performs significantly worse at 158 Hz. CVD process has a shorter duration of fabrication, and the control of the electrode thickness can be quite accurate depending on the temperature of growth for the CVD process. On the other hand, spin coating can be utilized to spin coat many different electrode materials with specific solution density and spin speeds to achieve thick electrodes. Both these devices have the capability to demonstrate utility in an on-chip power supply while having their respective advantages and trade-offs.

Conflict of Interest

The authors declare no conflict of interest.

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