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The Dependence of the High-Frequency Performance of Graphene Field-Effect Transistors on Channel Transport Properties

MUHAMMAD ASAD [1], MARLENE BONMANN [1], XINXIN YANG [1] (Graduate Student Member, IEEE), ANDREI VOROBIEV [1] (Member, IEEE), KJELL JEPPSON (Life Senior Member, IEEE), LUCA BANSZERUS [2], MARTIN OTTO [3], CHRISTOPH STAMPFER [2], DANIEL NEUMAIER [3], AND JAN STAKE [1] (Senior Member, IEEE)

1 Microtechnology and Nanoscience Department, Chalmers University of Technology, SE-41296 Gothenburg, Sweden
2 2nd Institute of Physics, RWTH Aachen University, 52074 Aachen, Germany
3 Advanced Microelectronic Center Aachen, AMO GmbH, 52074 Aachen, Germany

CORRESPONDING AUTHOR: M. ASAD (e-mail: asadmu@chalmers.se)

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ABSTRACT This paper addresses the high-frequency performance limitations of graphene field-effect transistors (GFETs) caused by material imperfections. To understand these limitations, we performed a comprehensive study of the relationship between the quality of graphene and surrounding materials and the high-frequency performance of GFETs fabricated on a silicon chip. We measured the transit frequency (f_T) and the maximum frequency of oscillation (f_{max}) for a set of GFETs across the chip, and as a measure of the material quality, we chose low-field carrier mobility. The low-field mobility varied across the chip from 600 cm^2/Vs to 2000 cm^2/Vs, while the f_T and f_{max} frequencies varied from 20 GHz to 37 GHz. The relationship between these frequencies and the low-field mobility was observed experimentally and explained using a methodology based on a small-signal equivalent circuit model with parameters extracted from the drain resistance model and the charge-carrier velocity saturation model. Sensitivity analysis clarified the effects of equivalent-circuit parameters on the f_T and f_{max} frequencies. To improve the GFET high-frequency performance, the transconductance was the most critical parameter, which could be improved by increasing the charge-carrier saturation velocity by selecting adjacent dielectric materials with optical phonon energies higher than that of SiO_2.

INDEX TERMS Graphene, field-effect transistors, high frequency, transit frequency, maximum frequency of oscillation, microwave electronics, contact resistances, transconductance.

I. INTRODUCTION

Owing to an extremely high intrinsic carrier mobility of up to 10^5 cm^2/Vs at room temperature [1], [2], graphene is considered a promising new channel material allowing for the development of new generation of field-effect transistors [3] for advanced mm-wave and sub-terahertz amplifiers. However, the high-frequency performance of state-of-the-art graphene field-effect transistors (GFETs) is significantly reduced. The highest published extrinsic (measured) transit frequency (f_T) and maximum frequency of oscillation (f_{max}) of GFETs are typically below 100 GHz [4]. For comparison, the high electron-mobility transistors (HEMTs) based on III–V compounds, with low-field mobilities above 10^4 cm^2/Vs, reveal a f_T and f_{max} up to 1 THz at deep-sub-μm gate lengths [5]. The high-frequency performance of GFETs is currently limited by a number of intrinsic and extrinsic factors. In particular, the intrinsic zero-bandgap in graphene results in relatively high drain conductance, which limits the extrinsic f_T and f_{max} of the GFETs [6]. An approach has been proposed to realize the drain-current saturation in GFETs without a bandgap formation but via velocity saturation of charge

carriers at high fields [7]. This approach has recently been applied in the development of GFETs with a state-of-the-art high-frequency performance operating in the velocity saturation mode [4], [8]. Nevertheless, there is a need to improve material quality and fabrication processes to minimize the extrinsic factors to fully exploit graphene for high-frequency applications.

Extrinsic limitations of the f_T and f_{max} are associated with parasitic coupling and loss, in part affected by imperfections in the graphene, adjacent dielectrics and interfaces. The effects of imperfections on low-field dc graphene properties have been extensively studied experimentally [9]–[13] and theoretically [14]–[17] and are well understood. However, the carrier velocity at high field is a key parameter for the intrinsic performance at high frequencies. Theoretically, Monte Carlo simulations predict that the carrier velocity in graphene at high electric fields, i.e., up to 10^4 V/cm, should decrease with impurity concentration due to a decrease in the low-field mobility [18], [19]. In previous studies, it was shown that within a certain range of impurity concentrations, the charged impurities do not limit the saturation velocity directly by the phonon mechanism but act as traps emitting charge carriers at high fields, which prevents the current from saturation and thus potentially limits the extrinsic f_T and f_{max} [8]. Nevertheless, to the best of our knowledge, there are no published systematic studies on the dependencies between the quality of the graphene and adjacent dielectric materials and the high-frequency performance on the GFETs, which is important for further development of transistors for high-frequency applications.

In this work, we analyze the relationship between the graphene/dielectric material quality and the high-field high-frequency performance of GFETs, i.e., the extrinsic f_T and f_{max} at drain fields above 10^4 V/cm. The low field mobility is used as the most appropriate parameter to represent the material quality. We exploit the surface distribution of the graphene/dielectric material quality in terms of low field mobility caused by the lateral inhomogeneities and variations across the silicon chip surface. The dependencies are analyzed by combining models of the drain resistance, carrier velocity, saturation velocity and small-signal equivalent circuit. In addition, a sensitivity analysis is provided to clarify the relative significance of the equivalent-circuit parameters, hence, identifying a promising approach for improving GFET high-frequency performance.

II. METHOD

Fig. 1(a) shows an SEM image of a typical two-finger gate GFET fabricated and studied in this work. GFETs with a total gate width (W_g) of 30 μm and gate length (L_g) ranging from 0.5 μm to 2 μm were studied. Fig. 1(b) shows a 45° tilted SEM image of the gate area. The length of the ungated regions is 0.1 μm. Fig. 2 shows the main distinguishable stages (i-iv) of GFET fabrication. The GFETs are fabricated using high-quality chemical vapor deposition (CVD) graphene with measured Hall mobility up to 7000 cm^2/Vs.

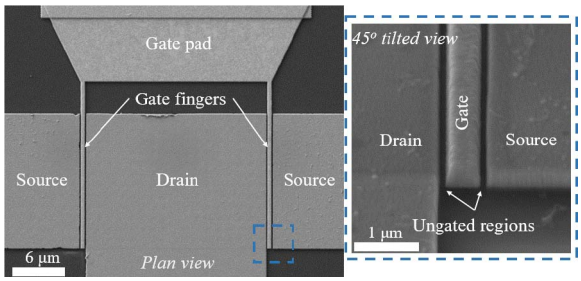

FIGURE 1. (a) SEM image of a GFET. (b) Magnified and 45° tilted view of the gate area in (a) corresponding to the dashed line box.

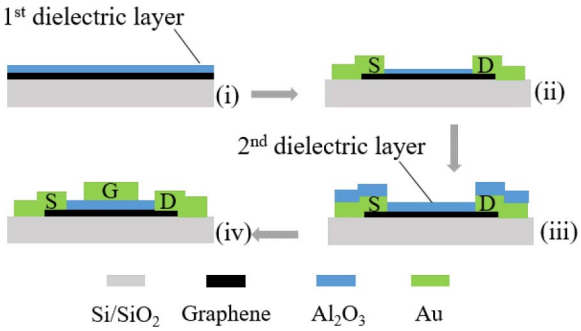

FIGURE 2. Main steps of the GFET fabrication. (i) Formation of the 1st dielectric layer, (ii) patterning of the dielectric/graphene mesa and formation of the source and drain contacts, (iii) deposition of the 2nd dielectric layer, and (iv) formation of the gate electrodes and source, along with the drain contact pads. Labels S, D and G indicate source, drain and gate electrodes, respectively.

The graphene film is transferred onto a high resistivity silicon/silicon oxide (Si/SiO_2) substrate with a SiO_2 thickness of 1 μm. A relatively thick oxide layer allows for the reduction of parasitic-pad capacitances. In stage (i), the transferred graphene film is covered with a 5 nm thick Al_2O_3 layer [4], as indicated by the 1st dielectric layer in Fig. 2. The 1st dielectric layer encapsulates graphene in the GFET channel and protects it from contamination during further processing, thereby reducing the concentration of impurities at the interface between the graphene and the gate dielectric [4]. In stage (ii), the graphene/dielectric mesa and, subsequently, the drain and source contacts are patterned. Notice that before metal deposition in the openings of the source and drain contact areas, the 1st dielectric layer, which separates the graphene from the lithographic resist, is etched off for metal/graphene ohmic contact formation. Apparently, this process allows for the effective removal of e-beam resist residues, providing a rather clean interface between the graphene and the metal and resulting in an extremely low specific-width contact resistivity of the graphene/metal junctions down to 15 Ω · μm. In stage (iii), the 2nd dielectric layer is formed by an atomic layer deposition of Al_2O_3 that is 17 nm thick with a total gate dielectric thickness of 22 nm. The 2nd dielectric layer covers the graphene edges exposed at the mesa sidewalls and, hence, prevents short circuiting by the overlapping gate fingers. In stage (iv), the gate electrodes,

source and drain contact pads are formed. All lithographic steps were performed using e-beam lithography, and e-beam evaporation was used for metallization. To verify the specific width contact resistivity of the graphene/metal junctions, typical transfer line method (TLM) test structures were designed and fabricated simultaneously with GFETs on the same Si chip. Similar GFET and TLM test structures were located at different positions on the Si chip within an area of approximately 10 mm × 5 mm. Not one of the fabricated GFETs was removed from the analysis as a random outlier. The surface distribution of the graphene/dielectric material quality over the Si chip surface allowed us to study the relationships between the material quality, dc and high-frequency performance of the GFETs via comparative analysis of the performance of transistors located at different positions on the chip.

The dc and ac performance of the GFETs and TLM test structures are characterized at room temperature using a Keithley 2612B dual-channel source meter and an Agilent N5230A network analyzer, respectively. The dc and ac measurement methods were followed as published in [4]. The biasing conditions, i.e., the combination of the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}), are optimized by the highest measured f_T and f_{max} for each GFET. The output characteristics were recorded during the S-parameters measurements with a holding time of 30 s. According to our previous studies, this holding time is sufficient for stabilizing the capture and emission of charges due to traps at high fields [20]. Typically, the optimal $V_{DS} \approx -1.1$ V corresponds to the intrinsic drain field $E_{int} \approx 1.5 \cdot 10^4 - 2 \cdot 10^4$ V/cm, at which the effective velocity of the charge carriers saturates [4], [8]. The optimal V_{GS} overdrive from the Dirac voltage ($V_{Dir} - V_{GS}$) varies in the range of approximately 0-4.5 V and is higher for the lower material quality.

III. RESULTS AND DISCUSSION

A. GRAPHENE QUALITY AND LOW-FIELD MOBILITY

Fig. 3(a) shows the measured drain resistance (R_{DS}) of two finger GFETs versus gate voltage. The drain resistance reveals a typical dependence with a maximum corresponding to the Dirac voltage (V_{Dir}). Therefore, we assume that Coulomb scattering dominates and that the mobility does not depend on the concentration of the charge carriers [12], [21]. This allows for finding the contact resistance (R_C), low-field mobility (μ_0) and residual concentration of charge carriers (n_0) as fitting parameters by applying the semi-empirical drain-resistance model [22]

$$R_{DS} = R_C + \frac{L_g}{W_g}\frac{1}{e\mu_0}\frac{1}{\sqrt{n_0^2 + \left((V_{GS} - V_{Dir})\frac{C_{ox}}{e}\right)^2}} \quad (1)$$

$$n = \sqrt{n_0^2 + \left((V_{GS} - V_{Dir})\frac{C_{ox}}{e}\right)^2} \quad (2)$$

where e is the elementary charge and C_{ox} is the gate capacitance per unit area. The C_{ox} is calculated assuming the dielectric constant of Al_2O_3 is equal to 7.5 [23]. n is the total charge carrier density. It can be shown that the graphene quantum capacitance can be ignored. The R_C includes the resistance of the ungated regions (R_{ung}), see Fig. 1, and the resistance of the graphene/metal junction (R_{mg}). As shown in Fig. 3(a), the R_{DS} dependence on V_{GS} is asymmetric. This can be explained by lower electron mobility and higher contact resistance due to the formation of the p-n barrier between the n-type gated channel and the p-type ungated region at a positive gate voltage overdrive [13], [24]. The solid line in the inset in Fig. 3(a) represents fitting by the drain-resistance model in the hole branch. Good agreement with the measured data confirms the assumption of Coulomb scattering and thus constant mobility. According to the self-consistent theory, the mobility limited by Coulomb scattering depends only on the charged impurity concentration and the dielectric constant of the substrate [14], [24]. The charged impurity concentration (n_{imp}) plainly defines the residual concentration of the charge carriers as $n_0 = 0.2 \times n_{imp}$ for graphene on SiO_2 [21], [25]. Therefore, n_0, found via the drain-resistance model, can be used as a material-quality parameter

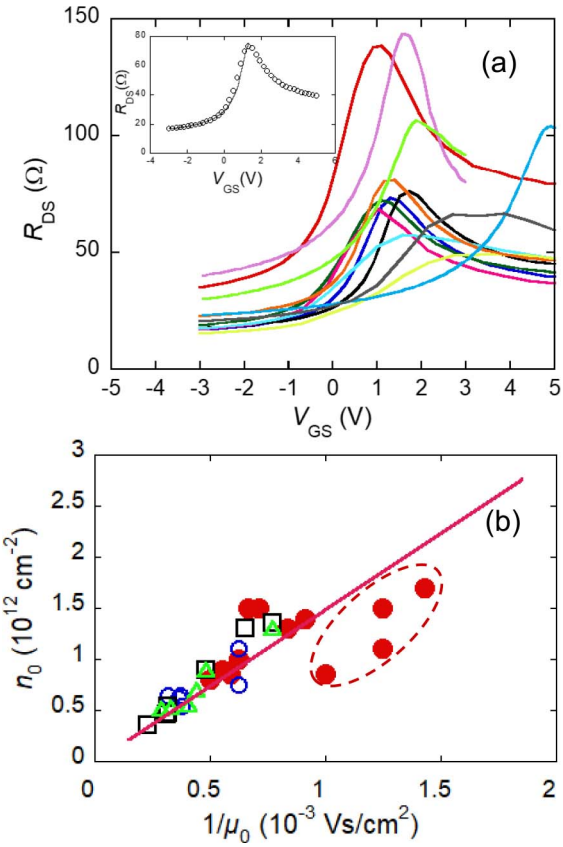

FIGURE 3. Different GFET channel transport properties across the silicon chip. (a) Drain resistance of the GFET's versus the gate voltage and inset shows the modelling results for the hole branch (line) of a GFET's. (b) Residual charge-carrier concentration versus inverse low-field mobility in the GFETs of gate lengths 0.5 μm (filled circles), 0.75 μm (open circles), 1 μm (squares), and 2 μm (triangles), located at different positions on the Si chip. The line corresponds to the product $n_0 \cdot \mu_0 = 1.5 \cdot 10^{15} V^{-1}s^{-1}$ [14], [21], [25].

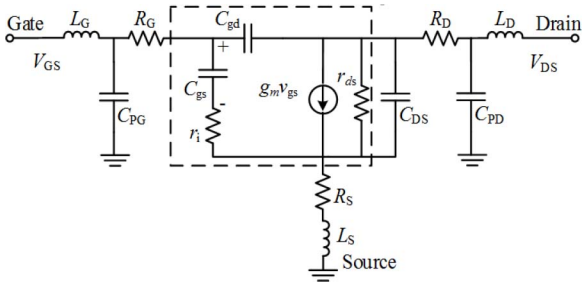

FIGURE 4. Small-signal equivalent circuit of a FET. The elements within the dashed line box represent the intrinsic part of the transistor [6].

when Coulomb scattering dominates [25]. The product of the low-field mobility and the residual-carrier concentration is constant, and for graphene on the SiO_2 substrate, it is $n_0.\mu_0 \approx 1.5 \cdot 10^{15}$ $V^{-1}s^{-1}$ [14]. Fig. 3(b) shows the residual charge-carrier concentration versus the inverse low-field mobility of the GFETs located at different positions on the Si chip for 4 different gate lengths. It can be seen that at mobilities above approximately 1000 cm^2/Vs, the product $n_0 \cdot \mu_0$ is close to the value of $1.5 \cdot 10^{15}$ $V^{-1}s^{-1}$. Hence, this indicates that the product $n_0 \cdot \mu_0$ can be assumed constant. The mobilities below approximately 1000 cm^2/Vs (data points within the dashed curve area) are reduced in comparison with those given by the product $n_0 \cdot \mu_0 = 1.5 \cdot 10^{15}$ $V^{-1}s^{-1}$, which was also observed previously [25]. This indicates additional contributions of the other charge-carrier scattering mechanisms, e.g., "short-range" or "resonant" scattering [12], [14]. The effective mobility, which includes all the scattering mechanisms, is given by Matthiessen's rule [26]. In this case, it is assumed that the more appropriate parameter for characterisation of the graphene and interfacial dielectric material quality is the low-field mobility derived from the drain-resistance model.

B. TRANSIT FREQUENCY AND MAXIMUM FREQUENCY OF OSCILLATION

In the analysis below, we establish correlations between the high-frequency performance of the GFETs and the graphene/dielectric-material quality using μ_0 as the overall quality indicator. The high-frequency performance of FETs is usually characterized by the transit frequency and the maximum frequency of oscillation, which are parameters closely related to the transistor current and power gains, respectively. Analytical approximations for the extrinsic f_T and f_{max} are derived from the FET small-signal equivalent circuit shown in Fig. 4. The elements within the dashed line box represent the intrinsic transistor [6]. g_m and r_{ds} are the intrinsic transconductance and differential drain resistance, respectively, C_{gs} and C_{gd} are the gate-source and gate-drain capacitances, respectively, C_{PG}, C_{PD} and C_{DS} are the external parasitic capacitances, respectively, R_G, R_S, R_D and r_i are the gate resistance, source series resistance, drain series resistance and charging resistance of the gate-source capacitance, respectively, and L_G, L_D and L_S are the lead inductances.

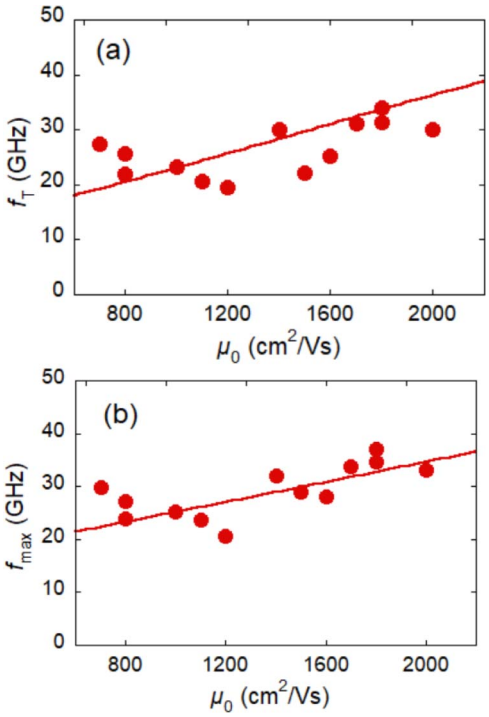

FIGURE 5. High frequency performance of different GFETs and the corresponding low field mobility. Extrinsic transit frequency (f_T) (a) and maximum frequency of oscillation (f_{max}) (b) of the GFETs located at different positions on the Si chip, versus the corresponding values of low-field mobility (μ_0). The solid lines are the models given by Eqs. (3)-(4) and corresponding polynomial fit dependences of the g_m, g_{ds}, and R_C, from Figs. 7-9. The dotted lines are a linear fit of the models.

The extrinsic f_T and f_{max} can be approximated as [4], [26]

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \frac{1}{1 + g_{ds}R_C + \frac{C_{gd}g_mR_C}{C_{gs}+C_{gd}} + \frac{C_{PG}}{C_{gs}+C_{gd}}}, \quad (3)$$

$$f_{max} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}(r_i + R_S + R_G) + g_m R_G \frac{C_{gd}}{C_{gs}}}}, \quad (4)$$

where $g_{ds} = 1/r_{ds}$ is the intrinsic differential-drain conductance. We estimated the capacitances as $C_{gs} = 0.5C_{ox}L_gW_g$ and $C_{gd} = kC_{gs}$, where $C_{ox} = 3$ fF $\cdot \mu m^{-2}$, W_g is the gate width and k is the fitting parameter, taking into account the decrease in charge-carrier concentration at the drain side [4], [26], [27]. The estimated capacitance values $C_{gs} = 0.47$ fF and $C_{gd} = 0.23$ fF differ less than 5% from those found using S-parameters measurements in our previous work [28]. The resistances are estimated as $R_S = R_C/2$, $r_i = 1/(2g_m)$, $R_G = R_{sh}W_g/(3L_g)$ and $R_{sh} = 0.08$ Ω for the gate electrode-sheet resistance [4], [26]. The parasitic gate-pad capacitance formed between the gate pad and the low-conductive surface of Si was found by delay-time analysis to be $C_{PG} \approx 8$ fF [4], [8]. Fig. 5 shows the extrinsic f_T and f_{max} of GFETs located at different positions on the Si chip versus the corresponding values of μ_0. There are dependencies between the graphene quality and the high-frequency performance of the GFETs. In general, f_T and f_{max} increase

in the range of approx. 20-40 GHz with μ_0 varying in the range of approx. 600-2000 cm^2/*Vs*, which is larger than the deviations from the corresponding modeled dependencies.

In the following sections, we analyze these relationships via the corresponding dependencies of the equivalent circuit and material parameters, i.e., g_m, g_{ds}, R_C, n and the effective velocity (υ) and saturation velocity (υ_{sat}) of the charge carriers on the low-field mobility. The analysis allows for evaluation of the relative effects of each parameter and thus clarifies the paths for further improvement of the GFET high-frequency performance. The experimental dependencies of f_T and f_{max} on μ_0 can be fully explained by the corresponding dependencies of g_m, g_{ds} and R_C found via semi-empirical models. In the analysis below, we assume that the intrinsic and extrinsic capacitances are constant.

C. VELOCITY, SATURATION VELOCITY AND TRANSCONDUCTANCE

The charge carrier velocity in the GFET channel starts to saturate around an intrinsic electric field (E_{int}) of 10^4 V/cm [8], [29]. We apply a model that assumes that the saturation velocity is limited by the inelastic emission of optical phonons (OPs) and can be approximated as [8], [29]

$$\upsilon_{sat} = \frac{2}{\pi}\frac{\omega_{OP}}{\sqrt{\pi n}}\sqrt{1-\frac{{\omega_{OP}}^2}{4\pi n \upsilon_F^2}}\frac{1}{N_{OP}+1} \tag{5}$$

where $\hbar\omega_{OP}$ is the OP energy, $N_{OP} = 1/[\exp(\hbar\omega_{OP}/k_BT) - 1]$ is the phonon occupation, $\upsilon_F \approx 10^8$ cm/s is the Fermi velocity and k_B is Boltzmann's constant. We ignore the effects of self-heating and assume a constant ambient temperature of 295 K. We verified the velocity saturation model in our previous work (Ref. 4) via simulations of the extrinsic f_T and f_{max} of GFETs with different gate lengths in the range of 0.5-2 μm, revealing good agreement with the experimental data.

Fig. 6(a) shows the saturation velocity of the charge carriers in the GFETs, located at different positions on the Si chip, versus corresponding values of the low-field mobility. The saturation velocity is calculated using Eq. (5) and the n calculated using Eq. (2). It can be seen that the υ_{sat} increases from approximately $1{\cdot}10^7$ cm/s to $2.5{\cdot}10^7$ cm/s in the studied μ_0 range. The dependencies between υ_{sat} and μ_0 are in agreement with our previous observations, indicating that the effective saturation velocity is not directly limited by the OPs of the impurities but rather reduced due to the increased residual concentration of the charge in the GFETs with a higher-impurity concentration [8]. The effective velocity of the charge carriers is calculated as [30]

$$\upsilon = \frac{\mu_0 E_{int}}{\left[1+(\mu_0 E_{int}/\upsilon_{sat})^\gamma\right]^{\frac{1}{\gamma}}} \tag{6}$$

where $E_{int} = (V_{DS} - I_{ds}R_C)/L_g$, I_{ds} is the drain-source current, and $\gamma = 3$ is the fitting parameter for the υ dependence on E_{int} found via delay-time analysis [8]. Fig. 6(a) shows the velocity of the charge carriers in the GFETs, calculated using Eq. (6), versus the corresponding values of the low-field mobility. It can be seen that the difference between the υ_{sat} and υ is less than 10% in the whole range of the low-field mobility. Therefore, one can assume that, in all the studied GFETs with different graphene quality and at a V_{DS} corresponding to the highest measured f_T and f_{max}, the effective velocity is relatively saturated.

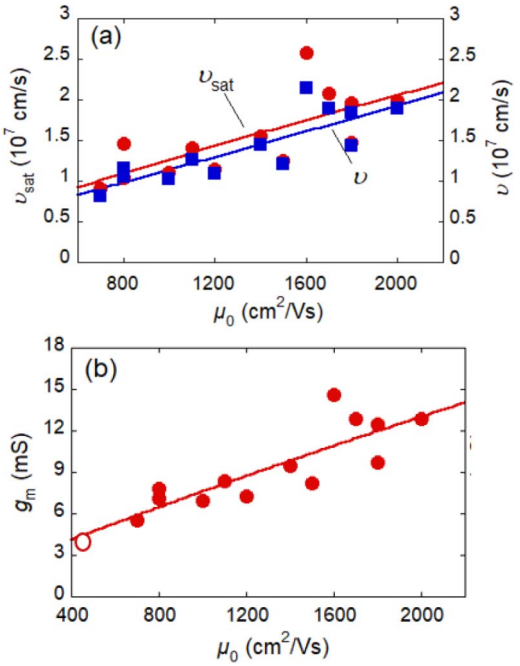

FIGURE 6. Higher saturation velocity and transconductance with improved lowfield mobility. (a) The saturation velocity (υ_{sat}) (circles), calculated using Eq. (5), and the carrier concentration calculated from Eq. (2) and the velocity (υ) (squares), calculated using Eq. (6), versus the low-field mobility in the GFETs located at different positions on the Si chip. The lines are the polynomial fitting curves. (b) The transconductance, calculated using Eq. (7), versus low field mobility in the GFETs, located at different positions on the Si chip. The line is a second order polynomial fitting curve. The open circle is from previous studies after de-embedding [28].

The intrinsic transconductance is calculated as [26]

$$g_m = \frac{\upsilon \cdot (C_{gs} + C_{gd})}{L_g} \tag{7}$$

Fig. 6(b) shows the transconductance, calculated using Eq. (7), versus low-field mobility in the GFETs located at different positions on the Si chip. g_m increases with μ_0, following the υ dependence, from approximately 6 mS to 14 mS. The solid line in Fig. 6(b) is the second-order polynomial fit of the calculated g_m on the μ_0 dependence and is applied in the further analysis for the models of f_T and f_{max} versus μ_0 using Eqs. (3)-(4). Fig. 6(b) includes also a g_m value found from S-parameters measurements scaled from our previous work using similar Theagreement with the dependence.

D. DRAIN CONDUCTANCE

Fig. 7(a) shows the drain-current density, calculated as $j_{ds} = I_{ds}/W_g$, versus the intrinsic-drain field measured at

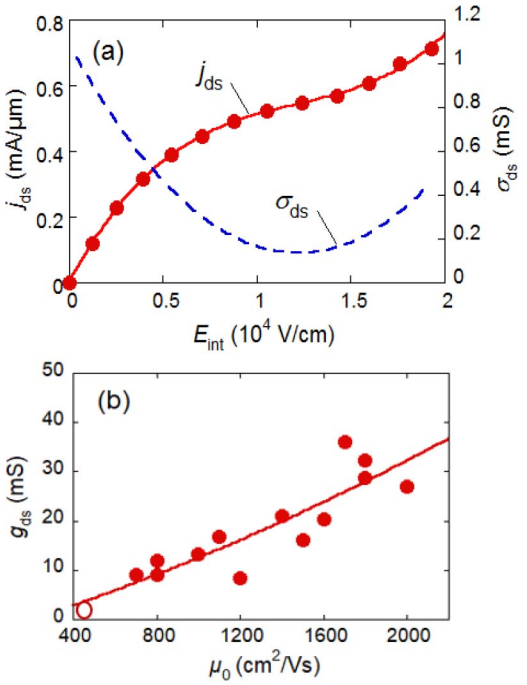

FIGURE 7. **(a) The drain-current density (jds) and differential-drain conductivity (υ_{sat}) versus the intrinsic-drain field measured at the GFET with $\mu 0 = 1800 cm^2/Vs$. The solid line is a third-order polynomial fitting curve. (b) The drain conductance versus the low-field mobility in the GFETs located at different positions on the Si chip. The line is a second-order polynomial fitting curve. The open circle is from previous studies after de-embedding [28].**

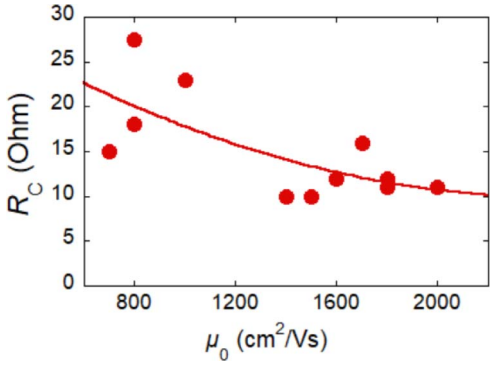

FIGURE 8. **Lower contact resistance with improved quality of the graphene channel. The contact resistance (R_C) (the sum of metal/graphene junction resistances and ungated region resistances) versus low-field mobility in the GFETs located at different positions on the Si chip. The lines are second-order polynomial fitting curves.**

the GFET with $\mu_0 = 1800$ cm^2/Vs and highest f_T and f_{max}; see Fig. 5. It can be seen that j_{ds} reveals a pronounced kink at the drain field of approximately 10^4 V/cm. We assume that the kink is associated with both the carrier velocity saturation, which typically occurs at the intrinsic drain fields of approximately 10^4 V/cm [8], [29], and the formation of a region with the residual concentration of the charge carriers at the drain side of the channel [6], [31], [32]. The field at the drain side corresponding to the kink voltage is large enough for velocity saturation [31]. Since the optimal field for the highest measured f_T and f_{max} is typically above that of the g_{ds} minimum, we assume that the velocity saturates at each point along the channel.

The complete drain-current saturation is prevented by channel ambipolarity due to a missing bandgap [6], [31]. The solid line in Fig. 7(a) is a third-order polynomial fitting curve, which is used to calculate the differential drain conductivity as $\sigma_{ds} = \partial j_{ds}/\partial E_{int}$. Fig. 7(a) shows the corresponding dependence of σ_{ds} on the intrinsic drain field. It can be seen that the σ_{ds} dependence reveals a minimum corresponding to the kink on the j_{ds} dependence. The optimal field for the highest measured f_T and f_{max} is typically above that of the σ_{ds} minima, which can be explained by counterbalancing contributions of the other equivalent circuit parameters; see Eqs. (3)-(4). Fig. 7(b) shows the drain conductance, calculated as $g_{ds} = \sigma_{ds} \cdot (W_g/L_g)$ corresponding to the drain fields of the highest measured f_T and f_{max}, versus the low-field mobility in the GFETs, located at different positions on the Si chip. As can be seen, the g_{ds} increases with μ_0 in the studied mobility range. The solid line in Fig. 7(b) is the second-order polynomial fit, which is applied in the further analysis for the models of the f_T and f_{max} versus μ_0 using Eqs. (3)-(4). Fig. 7 (b) also includes a g_{ds} value found from S-parameters measurements scaled from our previous work using similar technology and GFET design (Ref. 29). which is in very good agreement with the dependence.

E. CONTACT RESISTANCE

Fig. 8 shows the sum of the source and drain contact resistance, evaluated via fitting the drain-resistance model, see Eq. (1), to the GFET transfer characteristics versus the low-field mobility in the GFETs located at different positions on the Si chip. The R_C decreases with μ_0, from approx. 30 Ω down to 10 Ω, in the studied mobility range. The solid line in Fig. 8 is the second-order polynomial fit, which is applied in the further analysis for the models of the f_T and f_{max} versus μ_0 using Eqs. (3)-(4).

In this work, the lowest measured $R_C \approx 10\ \Omega$ corresponds to the specific width-contact resistivity $\rho_c = (R_C/2)\cdot(W_g) \approx 150\ \Omega \cdot \mu m$. In GFETs, the R_C is the combination of the contact-resistance parts associated with those of the ungated regions and the graphene/metal junctions and is defined as:

$$R_C = R_{mg} + R_{ung}, \tag{8}$$

where R_{mg} is the metal/graphene junctions' resistance and R_{ung} is the ungated region resistance. It can be shown, by separating the R_{ung}, that the values of R_{mg} are lower than those of the lowest previously published for both top and edge graphene/metal contacts, including perforated ones, which are typically above 100 $\Omega \cdot \mu m$ [33]–[36].

For comparison, the state-of-the-art silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) require a contact resistivity of 80 $\Omega \cdot \mu m$ per contact, which is approximately 10% of the on-state resistance of the

transistor [37], [38]. In our GFETs with the lowest R_C, the contact resistance per contact, i.e., R_S or R_D, is approximately 5 Ω. As shown in Fig. 3(a), it is less than 10% of the R_{DS} at approximately $V_{Dir} - 0.5$ V, which is the gate voltage typical for the highest measured f_T and f_{max}. We confirmed the extremely low contact resistance in our GFETs by using the transfer-length method (TLM) and specifically designed and fabricated TLM test structures on the same Si chip (see Section II). The average specific width-contact resistivity found by the TLM analysis is approximately 95 $\Omega \cdot \mu$m, which is in good agreement with that of the $\rho_{mg} = (R_{mg})\cdot(W_g) \approx 90\ \Omega \cdot \mu$m calculated by separating the R_{ung}.

So far, the increase in transconductance and differential-drain conductivity with mobility and a decrease in contact resistance with mobility have been observed. As shown in Fig. 5, an increase in f_T and f_{max} with mobility is observed owing to an increase in g_m and a decrease in R_C, but proportionate effects of these parameters on f_T and f_{max} are diminished owing to an increase in g_{ds} with mobility. The solid lines in Fig. 5 represent the f_T and f_{max} values modeled using Eqs. (3)-(4) versus μ_0 and the corresponding polynomial functions of g_m, g_{ds} and R_C found as fits to the experimental data shown in Figs. 7-9. The good agreement between the experimental trends and modeled dependencies of f_T and f_{max} verify the analytical approximations given by Eqs. (3)-(4), as well as the models used for calculations of g_m, g_{ds} and R_C.

F. GUIDELINES FOR IMPROVING THE HIGH FREQUENCY PERFORMANCE

Finally, a relative sensitivity analysis was performed to determine the most influential equivalent circuit parameters for improving the current state-of-the-art GFET technology. The partial effects of the equivalent-circuit parameters on f_T and f_{max} are analyzed. The relative sensitivity is defined as the ratio of the relative change in the function to the relative change in the variable [39]

$$S_f = \left(\frac{\partial f}{f}\right) \Big/ \left(\frac{\partial p}{p}\right) \tag{9}$$

where S_f denotes the relative sensitivity, f denotes the f_T or f_{max} and p denotes the parameters g_m, g_{ds} and R_C. The relative sensitivities are calculated using analytical expressions of partial derivatives of f_T and f_{max} given by Eqs. (3) and (4) and values of corresponding parameters given by fitting curves in Fig. 6-8. Fig. 9 shows a bar chart of the relative sensitivities of f_T and f_{max} to g_m, g_{ds} and R_C at a low-field mobility of 2000 cm^2/Vs. The variations in f_T and f_{max} are governed mainly by variations in g_m. The negative effects of g_{ds} and R_C on f_T are comparable and less than those of g_m. The effect of R_C on f_{max} is negligible. According to our analysis, the sensitivities show the same relationships in the whole studied mobility range and above the mobility of 2000 cm^2/Vs. It is clear that the most effective way of increasing f_T and f_{max} is by increasing the transconductance.

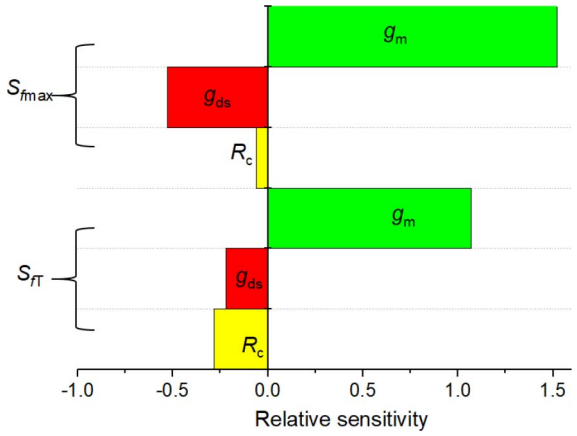

FIGURE 9. Most critical equivalent circuit parameters. A bar chart presenting the relative sensitivity of extrinsic transit frequency (f_T) and maximum frequency of oscillation (f_{max}) to the equivalent-circuit parameters g_m, g_{ds} and R_C at mobility of 2000 cm^2/Vs. The transconductance is the most important parameter in order to improve the f_T and f_{max}.

Since, according to our sensitivity analysis, the g_m is the most influencing parameter, an effective way of increasing f_T and f_{max} is by increasing the transconductance. An approach of increasing g_m in GFETs with the same design and dimensions is the selection of channel dielectric materials with higher optical phonon energies [7], [8], [31]. This will result in an increase in saturation velocity and thus g_m; see Eqs. (5)-(7). For example, the Al_2O_3 and hBN optical phonon energies are 87 meV and 100 meV, respectively [7], [18]. According to our calculations, replacing SiO_2 with Al_2O_3 or hBN will result in an increase in saturation velocities up to 3.10^7 cm/s and 5.10^7 cm/s and f_{max} of the GFETs up to 100 GHz and 150 GHz, respectively, at the same $L_g = 0.5\mu$m [7], [8]. According to our analysis, the differential drain conductivity g_{ds}, in the velocity saturation mode, should not increase much in the GFETs with higher saturation velocity.

IV. CONCLUSION

In conclusion, we have performed a comprehensive study of the relationship of the high-frequency performance of GFETs to the channel transport properties. The latter is to a large extent affected by the quality of the graphene and surrounding materials. An almost linear relationship between the high-frequency parameters of GFETs and low-field mobility was observed and is explained theoretically using a methodology based on the small-signal equivalent circuit model with parameters extracted from the low-field drain resistance model and the charge-carrier velocity saturation model. The relationship observed was governed mainly by the transconductance and the drain output conductance, while the contact resistance appeared to have a rather weak influence. The results indicate that the most promising approach for improving GFET high-frequency performance is by increasing the transconductance. In particular, the relatively high drain conductance in GFETs can be counterbalanced by achieving

high transconductance. In addition to scaling the gate length, an approach for increasing f_T and f_{max} is by encapsulating the graphene channel with dielectric material with reduced charged-impurity density and higher optical-phonon energy than that of SiO_2, resulting in higher saturation velocity and thus higher transconductance.

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