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**Abstract**. One of the biggest applications that are coming with the Internet of Things (IoT) are miniaturized sensor networks that connect wirelessly to each other and the internet. Microsupercapacitors (MSCs) are ideal to power these devices, with large cyclability and lifetime. Porous carbons are the material of choice for these devices, but their morphology and manufacturing are far from optimized. Vertically oriented graphene MSCs have shown great promise due to their high specific surface areas and conductivity. In this work, the growth of vertically aligned carbon nanosheets (CNS) on 2-inch wafers has been studied, and it has been used as active material to manufacture MSC and transmission line model (TLM) wafers. The fabricated CNS MSC devices show a capacitance of 7.4 µF (50.7 µF/cm$^2$, normalized to the area of the electrodes), a five-times increase from previous results obtained by the group.

## 1. Introduction

With the advent of Internet-of-things (IoT), wireless sensor networks can effectively be used in networks for condition monitoring in areas with low human interaction. For their effective deployment in such regions, it is imperative to have a power source that can be self-sustained without needing replacement. Microsupercapacitors (MSC) alongside energy harvesters can provide an integrated power unit that can work delivering and storing energy at high powers for an almost limitless lifetime. MSCs are miniaturized supercapacitors, energy storage devices that differ from batteries in its high power density and much improved cyclability. [1]

Vertical carbon nanosheets (CNS), interconnected porous 3D networks of vertically oriented graphite sheets, have been fabricated by several groups by plasma-enhanced chemical vapor deposition (PECVD) using different plasma sources. Microwave and RF plasma sources are the most used ones [2] as they produce thinner carbon walls, calling the material sometimes “vertical graphene” [3]. However, some papers have demonstrated that this structure is not ideal for supercapacitors, as the wide intersheet spacing yields lower surface area and poorer wettability [4][5].

In this work, vertically aligned carbon nanosheets (CNS) grown by DC-PECVD, also called carbon nanowalls, are grown following the work of prof. J. Sun [6], firstly on a silicon die, and later on a 2” silicon wafer. Moreover, satisfactory results have been found in growing CNS on an Au/Ti contact over an Si/$SiO_2$ substrate. The grown CNS is porous and conductive, with a relatively high surface area that yields good electrochemical properties. Later, CNS based MSCs were fabricated using the recipe and wettability was improved for enhanced electrode-electrolyte interaction. These devices were fabricated through a scalable process on a 2” Si wafer. The MSC design with an interdigitated pattern of 20 contact fingers with a spacing of 80 µm between them was electrochemically characterized. Furthermore, tests

regarding the contact resistance of the material, that will provide insights into the resistance of the device at the electrode-electrolyte interface and electrode-contacts interface, are under way.

## 2. Experimental

CNS has been used to fabricate two different kinds of devices, microsupercapacitors [7], and transmission line model (TLM) structures [8]. MSCs wafers consist on an array of different interdigitated MSC geometries with a different number of fingers and spacing between them, and TLM wafers consist of a series of Au lines separated at increasing distances below a stripe of the carbon material with four different widths. The first geometry allows for the electrochemical characterization of the devices, capacitance, ESR, energy and power density and other parameters, while TLM allows accurate measurement of the contact resistance of the material with the current collector.

### *2.1. Fabrication of MSCs and TLM structures. CNS growth.*

The fabrication process of all devices follows the steps shown in Fig. 1, developed initially for rGO [9]. Starting from a dry oxidized Si wafer, a lift-off process using a bi-layer resist masking technique, with LOR and S1813 positive resist on top, is used to pattern the metal into the interdigitated design (as seen in Fig. 1.) or the TLM structure (final devices shown in Fig. 3). 20 nm of titanium and 100 nm of gold were evaporated onto the resist to form the current collector, and then the carbon material was deposited. The patterned wafer was introduced on a cold wall, low-pressure PECVD reactor (BlackMagic, Aixtron). First, Ar and $H_2$ are introduced in the chamber with a constant flow, to create a protecting atmosphere and help initiate the plasma later. A current is passed through a graphite heater where the wafer stands, and once reached 775 °C, $C_2H_2$, the carbon precursor is introduced and the plasma is started and kept for 10 minutes. The complexity of the growth mechanism explained here has been studied by several groups [2], [10]–[12]. The plasma and the ionized molecules in it break down the $C_2H_2$ molecules transforming them into carbon dimers and other CH radicals. $H_2$ helps this process, and also etches amorphous carbon, while argon stabilizes the plasma. Initially, a buffer layer of nanographitic carbon gets deposited, followed by the formation of nanoislands. The material grows vertically by the effect of the electric field, that lifts the initial carbon nanoislands upwards at the grain boundaries. Once the carbon material is deposited, a layer of aluminum is evaporated and another

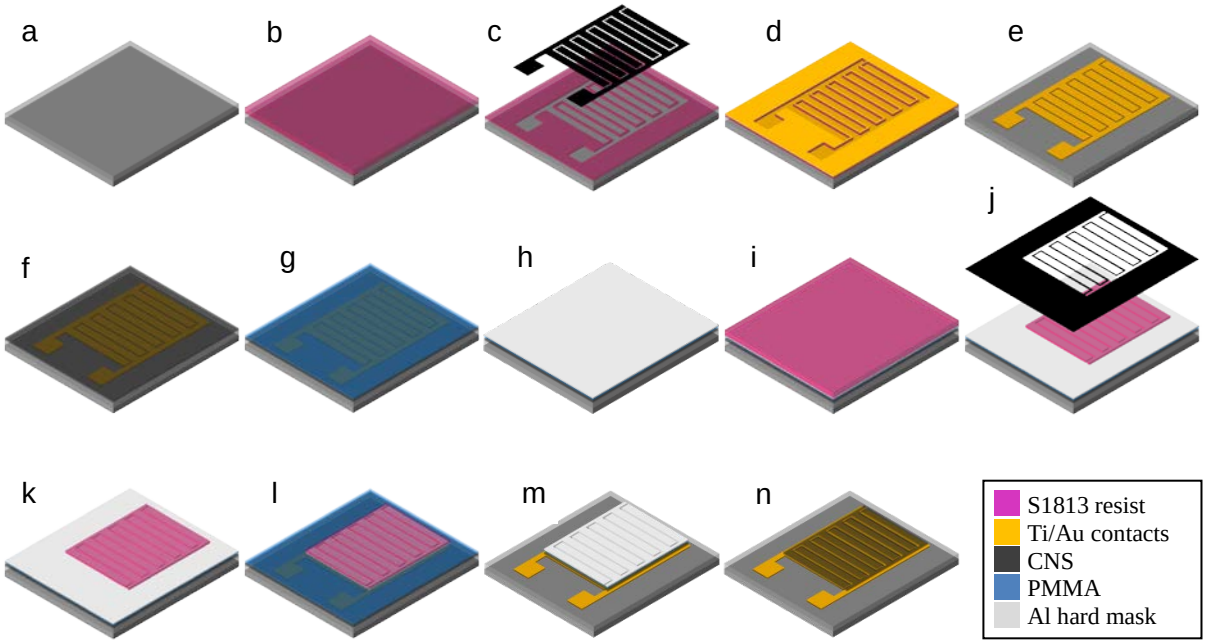


**Fig. 1.** Schematic drawings of microsupercapacitor fabrication process

lithography step is done to pattern it into a hard mask, etching the Al layer with a plasma of $SiCl_4$ and $Cl_2$. Through this hard mask, the carbon material is etched by an oxygen plasma and finally one last step etches the remaining Al mask.

*2.2. Material characterization.*
The material was characterized structurally using a JEOL Scanning Electron Microscope (Fig. 3), Dektak profiler was used to obtain the growth thickness and surface profile. Several micrographs were taken during the optimization of the growth process. Wettability studies were performed on the grown materials.

*2.3. Electrical characterization.*

*2.3.1. Electrochemical measurements.* The electrochemical tests were carried out using Gamry Reference 3000 potentiostat. Cyclic voltammetry (CV) applies a sweeping voltage at a constant rate between both electrodes, measuring the current. Galvanostatic charge discharge (GCD) measurements are done by applying a constant current and measuring the voltage. Electrochemical Impedance Spectroscopy (EIS) is also performed, by testing the impedance response at different frequencies. From these tests, the capacitance of the devices can be derived, as well as the energy and power densities, and the equivalent series resistance (ESR). The tests were done within a 1 V potential window using the ionic liquid EMIM-TFSI as electrolyte.

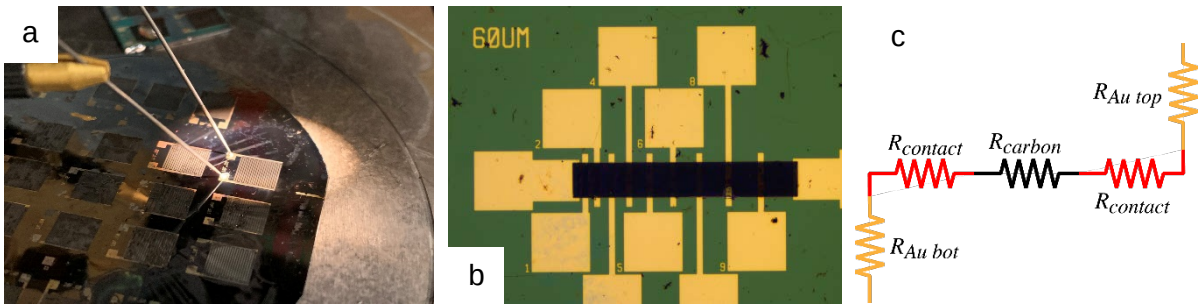


**Fig. 3.** (a) Measurement set up of CNS MSC, (b) Final TLM structures of CNS, (c) Resistance scheme

*2.3.2. TLM 2-point measurements.* TLM structures were designed and fabricated (Fig. 3) in order to allow measurements of the contact resistance between the electrode material and the contact pads. To do so, a stripe of carbon electrode was deposited on top of lines of gold with increasing distances between them. Using a probe station (Keithley 4200-SCS) inside the cleanroom, probes were connected to each pair of contact pads and resistance values were obtained. The measured resistance corresponds to the contributions in the equation below as indicated in Fig. 3(c):

$$R_{total} = 2R_{contact} + R_{Au\ top} + R_{Au\ bot} + R_{carbon}$$

## 3. Results and discussion

*3.1. CNS growth optimization.*
The first CNS growth in the PECVD system was made using a growth recipe provided by J. Sun [6]. Trying to obtain the same morphology in 2" wafers, the same conditions were tried, but the result was not adequate. For the good electrochemical performance of CNS, a large quantity of exposed edges - shown brighter in the SEM- should be present, as these store more charge than the basal planes [13]. When the growth was repeated in 1 $cm^2$ chips, with excellent results, it was surmised that the problem was the temperature homogeneity over the wafer. The temperature was then maintained for 150 s instead of 60 s, before starting the plasma and the precursor gas. The resulting material showed better structure than the initial growths.

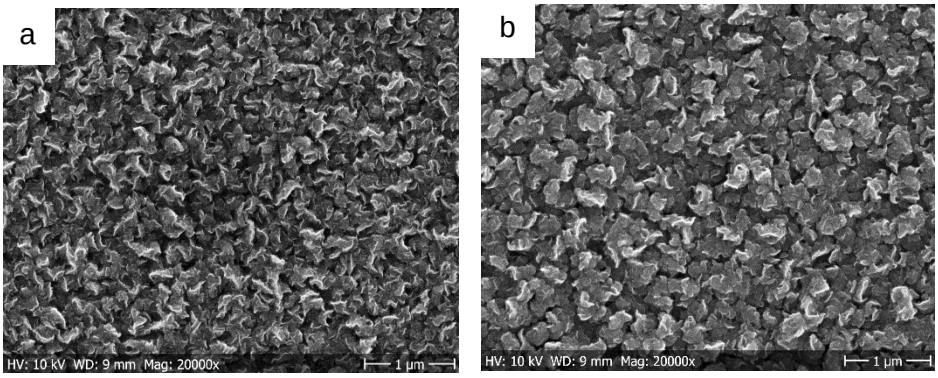


**Fig. 4.** SEM images showing the morphology of CNS: (a) First growth on a Si die, (b) Final growth with 150s wait, 2" Si wafer.

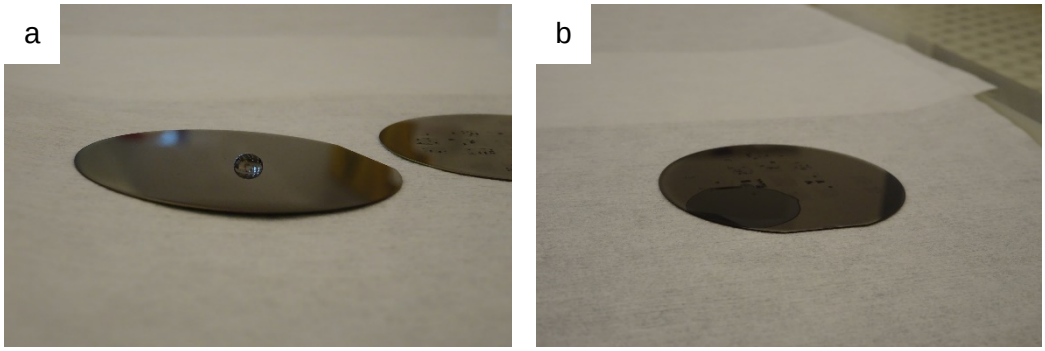


**Fig. 5.** (a) Wettability of CNS after growth, (b) Wettability after plasma treatment

An important parameter for the processing of the CNS wafers is its wettability, which depends on the morphology of the material and the intersheet distance [4], but also on the amount of defects and the chemistry of the nanosheets [14]. Oxygen and argon plasma treatments have been used in CNS samples to improve the wettability, being successful even at very low times (15 to 30 seconds) and powers (15W) (Fig. 5)

*3.2. MSC electrochemical results.*

From the electrochemical tests performed on CNS MSCs, the EIS show a capacitance of 7.4 µF, which translates to 50.7 µF/cm2 areal capacitance. For this device, the equivalent series resistance has also been calculated as 104 Ω, from the real part of the impedance.

From the CV measurements at different scan rates shown in Fig. 5a, the capacitance has also been calculated as the area under the curve – the total stored charge – over the voltage window, in Fig. 5b. The device, consisting of 20 fingers with 80 µm spacing, shows good capacitive behavior for the scan rates and within the voltage window tested, as can be derived from the quasi-rectangular shape of the CV graphs. The anodic current increase appearing at the 1V limit of the graph could be attributed to the splitting of absorbed water into the electrolyte, as the measurement set up, as seen in Fig. 3a, is open. The different curves yield areal capacitances between 40 and 23 µF/cm$^2$. This result can be compared with previous devices fabricated by the group. Vyas et al. [15] reported a vertical graphene-based MSC with 5.5 µF/cm$^2$ of total capacitance. This work improves that result, probably due to the plasma post-treatment that improved the wettability of the material, increasing the effective surface area and increasing the total capacitance. However, CNS-based MSC have lower performance than other materials such as thermally reduced graphene oxide, the smaller pores of which enable higher capacitances.

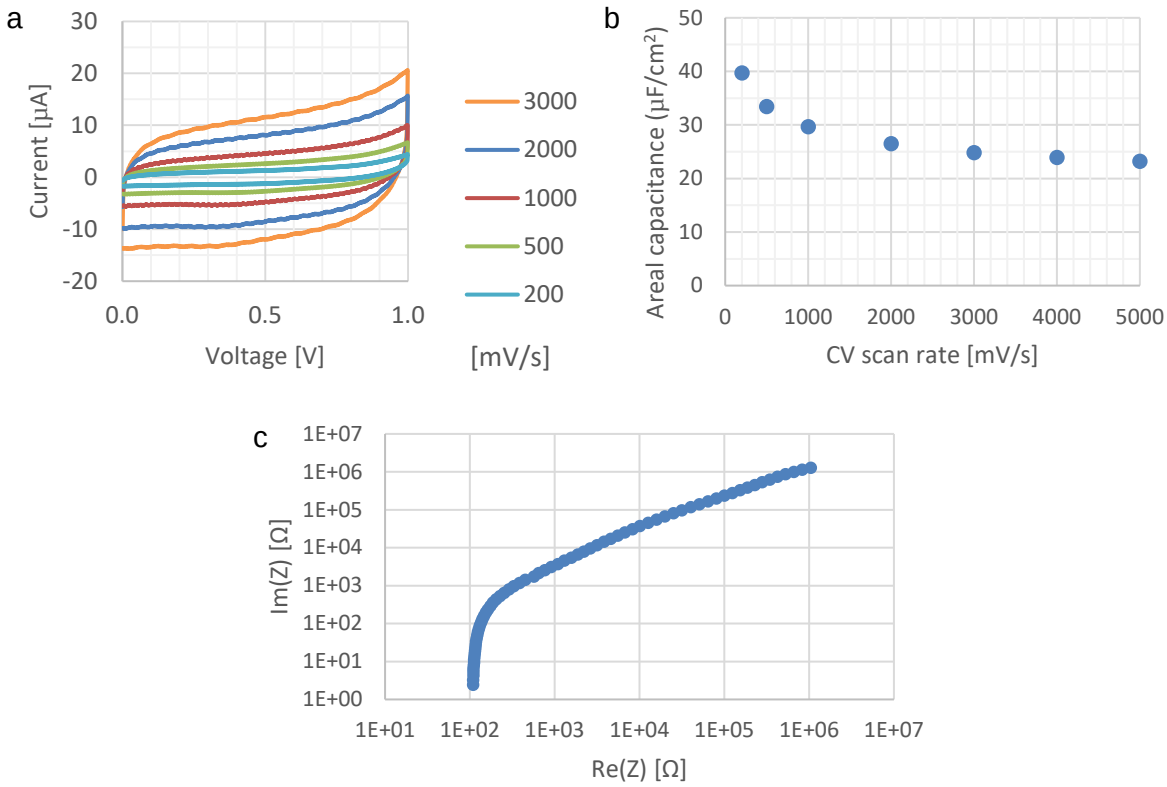


**Fig. 6.** (a) Areal capacitance from CV vs the scan rate. (b) Cyclic voltammetry measurements of a CNS MSC device at different scan rates (c) EIS test.

## 4. Conclusion

In this paper, the fabrication of CNS-based microsupercapacitors has been studied, as well as its electrochemical performance. The morphology of the vertical carbon nanosheets has been improved in 2" wafers, grown on Ti/Au contacts. The fabricated MSC devices showed an areal capacitance of 50.7 µF/cm$^2$, greatly improved from previous results using the same material. This previous device reported 5.5 µF/cm$^2$ of total capacitance, from the CV curve at 2000 mV/s. This work, compared with it, represents a fivefold increase in capacitance. Plasma treatment with argon and oxygen improved the wettability, probably accounting for this increase in performance. Future work will include measurement of the contact resistance of the carbon-metal interface by means of 2-point resistance measurements in the TLM structures.

## Acknowledgements

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