Thesis for the degree of Doctor of Philosophy

Wideband integrated circuits for optical communication systems

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Abstract

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The exponential growth of internet traffic drives data centers to constantly improve their capacity. Several research and industrial organizations are aiming towards Tbps Ethernet and beyond, which brings new challenges to the field of high-speed broadband electronic circuit design. With data centers rapidly becoming significant energy consumers on the global scale, the energy efficiency of the optical interconnect transceivers takes a primary role in the development of novel systems. Furthermore, wideband optical links are finding applications inside very high throughput satellite (V/HTS) payloads used in the ever-expanding cloud of telecommunication satellites. Their application being enabled by the maturity of the existing fiber based optical links and the high technology readiness level of radiation hardened integrated circuit processes. There are several additional challenges unique in the design of a wideband optical system. The overall system noise must be optimized for the specific application, modulation scheme, PD and laser characteristics. Most state-of-the-art wideband circuits are built on high-end semiconductor SiGe and InP technologies. However, each technology demands specific design decisions to be made in order to get low noise, high energy efficiency and adequate bandwidth. In order to overcome the frequency limitations of the optoelectronic components, bandwidth enhancement and channel equalization techniques are used. In this work various blocks of optical communication systems are designed attempting to tackle some of the aforementioned challenges. Two TIA front-end topologies with 133 GHz bandwidth, a CB and a CE with shunt-shunt feedback, are designed and measured, utilizing a state-of-the-art 130 nm InP DHBT technology. A modular equalizer block built in 130 nm SiGe HBT technology is presented. Three ultra-wideband traveling wave amplifiers, a 4-cell, a single-stage and a matrix single-stage, are designed in a 250 nm InP DHBT process to test the limits of distributed amplification. A differential VCSEL driver circuit is designed and integrated in a 4x 28 Gbps transceiver system for intra-satellite optical communications based in a rad-hard 130 nm SiGe process.

Keywords: TIA, data communication, VCSEL driver, optical interconnects, receiver front-end, SiGe HBT, InP DHBT, wideband amplifiers, distributed amplifiers.

Acknowledgment

Despite striving to express my appreciation towards colleagues, friends and family readily, I might have had varying levels of success. So let this section serve as a testament of how much their support meant to me during my studies. Dear reader, please forgive my literary verbosity while I express my due gratitude.

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Stavros Giannakopoulos

Göteborg, May 2021

List of Publications

This thesis is based on the following appended papers:

Letters and Journal papers

Paper A. Stavros Giannakopoulos, Zhongxia Simon He, Izzat Darwazeh, and Herbert Zirath. *Transimpedance Amplifiers with 133 GHz bandwidth on 130 nm InP DHBT.*, Electronics Letters 55, no. 9 (2019): p.521 – 523. IET, 2019.

Paper B. Temitope Odedeyi, **Stavros Giannakopoulos**, Zhongxia Simon He, Herbert Zirath, and Izzat Darwazeh. *InP DHBt Single-Stage and Multiplicative Distributed Amplifiers for Ultra-Wideband Amplification.*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I, Volume: 67, Issue: 11, Nov. 2020.

Paper C. Stavros Giannakopoulos, Ilias Sourikopoulos, Leontios Stampoulidis, Pylyp Ostrovskyy, Florian Teply, Klaus Tittelbach, Goran Panic, Gunter Fischer, Alexander Grabowski, Herbert Zirath, Philippe Ayzac, Norbert Venet, Anaëlle Maho, Michel Sotom, Shaun Jones, Grahame Wood and Ian Oxtoby. *A 112 Gb/s radiation-hard mid-board optical transceiver in 130 nm SiGe BiCMOS for intra-satellite links.*, Frontiers in Physics, 9 (2021).

Conference Proceedings

Paper D. Stavros Giannakopoulos, Klas Eriksson, Izzat Darwazeh, Zhongxia Simon He, and Herbert Zirath. *Ultra-Broadband Common Collector-Cascode 4-Cell Distributed Amplifier in 250nm InP HBT technology with over 200 GHz bandwidth.* In 2017 12th European Microwave Integrated Circuits Conference (EuMIC), pp. 142-145. IEEE, 2017.

Other publications

Other relevant publications co-authored by Stavros Giannakopoulos, the content of which partially overlaps with the appended paper or is out of the scope of the thesis:

[Oa] Stavros Giannakopoulos, Zhongxia Simon He, Izzat Darwazeh, and Herbert Zirath. *Differential common base TIA with 56 dB Ohm gain and 45 GHz bandwidth in 130 nm SiGe.* In 2017 IEEE Asia Pacific Microwave Conference (APMC), pp. 1107-1110. IEEE, 2017.

[**Ob**] **Stavros Giannakopoulos**, Zhongxia Simon He, and Herbert Zirath. *Tunable Equalizer for 64 Gbps Data Communication Systems in 130nm SiGe.* In 2018 Asia-Pacific Microwave Conference (APMC), pp. 627-629. IEEE, 2018.

[**Oc**] Temitope Odedeyi; **Stavros Giannakopoulos**; Herbert Zirath; Izzat Darwazeh. *Single-Stage and Multiplicative Distributed Amplifiers for 200 GHz+ Amplification.* IEEE APMC, (2019).

[**Od**] I. Sourikopoulos, L. Stampoulidis, **Stavros Giannakopoulos**, H. Zirath , P. Ostrovskyy, G. Fischer, M. Faugeron, A. Maho, L. Cyrille, G. Bouisset, N. Venet, M. Sotom, M. Irion, F. Schaub, J. Barbero, D. Lopez, R. G. Walker, Y. Zhou, I. Oxtoby, S. Duffy. *The H2020-SPACE-SIPHODIAS Project: Space-grade Opto-electronic Interfaces for Photonic Digital and Analogue Very-High-Throughput Satellite payloads.* International Conference of Space Optics-ICSO-2020 (2021).

Thesis

Some of the content presented in this thesis, including text, tables and figures may be partly or fully reused from the thesis below, which is part of the author's doctoral studies, without explicit mentioning

[**Oe**] S. Giannakopoulos, "Broadband Receiver Electronic Circuits for Fiber-Optical Communication Systems", Tekn. Lic. Thesis, Department of Microtechnology and Nanoscience, Chalmers University of Technology, 2019.

List of Acronyms

APD	–	Avalance Photodetector
BER	–	Bit Error Ratio
BEOL	–	Back End of Line
BW	–	Bandwidth
BiCMOS	–	Bipolar Junction Transistor - Complementary Metal Oxide Semiconductor
CB	–	Common Base
CC	–	Common Collector
CE	–	Common Emitter
CMOS	–	Complementary Metal Oxide Semiconductor
DA	–	Distributed Amplifier
DFE	–	Decision-Feedback Equalization
DHBT	–	Double Heterojunction Bipolar Transistor
EF	–	Emitter Follower
EQ	–	Equalizer
FEC	–	Forward Error Correction
FET	–	Field Effect Transistor
FFE	–	Feed-Forward Equalization
HBT	–	Heterojunction Bipolar Transistor
MMF	–	Multi-Mode Fiber
MMIC	–	Monolithic Microwave Integrated Circuit
MZM	–	Mach Zehnder Modulator
NRZ	–	Non-Return Zero
OOK	–	On-Off Keying
OI	–	Optical Interconnect(s)
PAM	–	Pulse Amplitude Modulation
PD	–	Photodetector/Photodiode
RT	–	Room Temperature
SSDA	–	Single Stage Distributed Amplifier
SNR	–	Signal-to-Noise Ratio
SOI	–	Silicon on Insulator
TIA	–	Transimpedance Amplifier
VCSEL	–	Vertical Cavity Surface Emitting Laser

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Part I

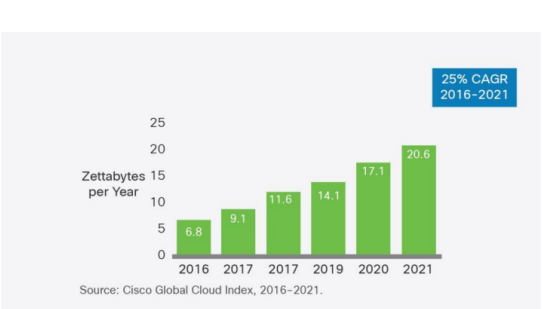
Introductory chapters

Chapter 1

Introduction

The global internet traffic has been steadily increasing, with current predictions calculating that the global traffic per year will reach 3.3 Zettabytes by 2021, as Fig. 1.1a indicates. The exponential increase on internet traffic, computing and network capacity is translated into higher demands on the interconnect infrastructure. Those demands impose requirements for increased interconnect bandwidth, bandwidth capacity, and higher energy efficiency on the existing networks. The Cisco Global Cloud index report states that approximately 71.5% of that traffic is restricted on interconnects within data centers [1]. With the continuous increase on the number of hyperscale data centers (Fig. 1.1b), in order to cover the traffic demands, the total energy consumption becomes significant.

The energy consumption of the data centers was 330 billion kWH in 2007 according to Greenpeace's Make IT green report [2]. The projected energy demand is expected to increase to 1000 billion kWh in 2020 [3]. The short-haul optical interconnects (OI) are an important contributor to the total energy demands of data centers, with the networking amounting up to 23% of the total power consumption [3]. However, by replacing copper interconnects with OIs the energy consumed per Gbps of transmission can drop from 25 mW per Gbps to 1 mW per Gbps as seen in Fig. 1.2 [4].



(a) Global data traffic statistics.

(b) Hyperscale data center numbers.

Figure 1.1: Global traffic and hyperscale data center number statistics and future predictions [1].

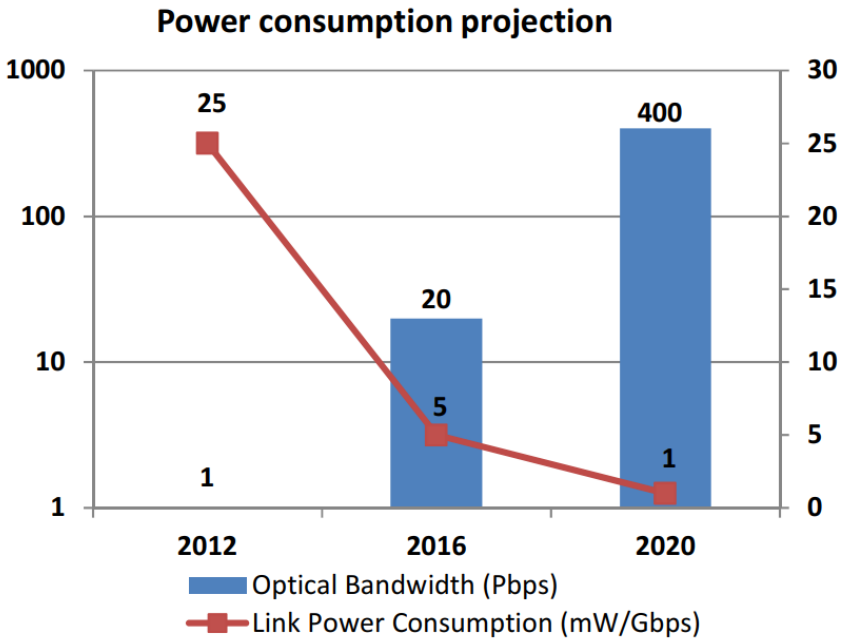


Figure 1.2: Estimated optical power consumption and bandwidth required by Internet data centers by 2020 [4].

1.1 Applications

The field of fiber-optical interconnects is quite mature with several commercially available interconnect solutions such as Thunderbolt [5], Infiniband [6] and the further development of the existing Ethernet standards [7]. Those technologies utilize optical interconnects over fiber to deliver gigabit datarates over hundreds of meters (Fig. 1.3). The transition from copper-based communications to OI brings multiple improvements [8], and is made possible thanks to state-of-the-art light emitters and detectors that can operate beyond 50 Gbps [9, 10]. Vertical Cavity Surface Emitting Lasers (VCSELs) have been on the forefront of research allowing the miniaturization of fiber-optical interconnect transceivers.

In addition to data center networks, energy efficient optical interconnects are utilized in a variety of fields. In automotive industry, they are used as intra-vehicle network buses using polymer fibers [11, 12]. In very high throughput satellites VCSEL based optical links are used to facilitate communications between different antennas and processing units within the payload [13]. In a similar fashion, free space optical communications are used in intra-aircraft and intra-satellite communication networks [14].

1.2 Thesis outline

This thesis explores the field of high speed electronics for optical interconnects suitable for data communication applications, aiming to achieve datarates of 100+

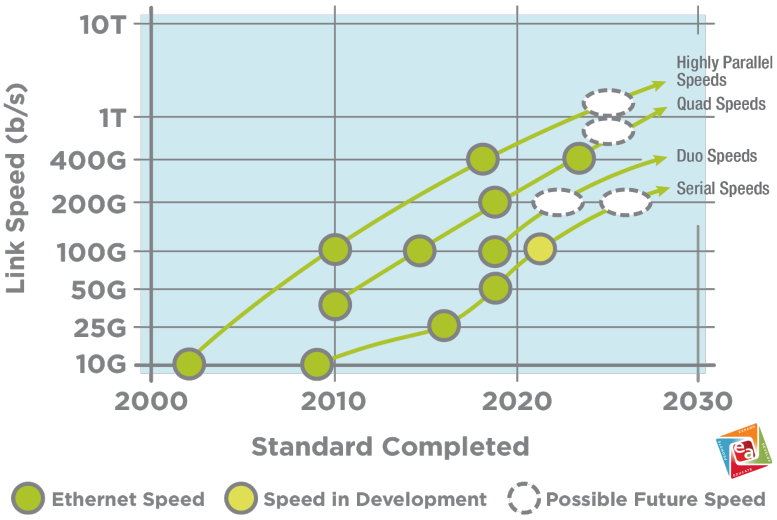


Figure 1.3: Existing and upcoming Ethernet standards [7].

Gbps with as low energy consumption as possible. This thesis consists of two parts. Part I is a general introduction to the field and puts the appended papers in context. In Chapter 2, we provide the background on optical interconnect systems as well as the limitation imposed by the optoelectronic components. In Chapter 3, we discuss relevant aspects of wideband amplifier design. In Chapter 4 we present the unique benefits of distributed amplification and discus the design of three such circuits. In Chapter 5 we review the literature in optical communication receiver systems, discuss the specific design trade-offs that each technology enables and present the design of two TIA front-ends and the characterization of an equalizer integrated circuit. In Chapter 6 we present the characterization of a VCSEL and the design of a VCSEL driver circuit as part of a space-grade optical communication module. Then in Chapter 7, we conclude the introductory part of this thesis.

Part II contains the appended papers. The contributed papers attempt to cover a wide array of topics revolving around wideband integrated circuits that find application in optical communication systems. In Paper D, we demonstrate a 250 nm InP Double Heterojunction Bipolar Transistor (DHBT) ultra-broadband distributed amplifier. In Paper B, we present the design challenges and characterization of two 250 nm InP double heterojunction bipolar transistor (DHBT) wideband distributed amplifiers (DA), a single stage distributed amplifer (SSDA), and a Matrix-cascaded single stage distributed amplifer (MSSDA). In Paper A, we propose two transimpedance amplifier topologies designed on a 130 nm InP DHBT process, achieving bandwidth higher than 133 GHz. In Paper C, we propose a 4 x 28 Gbps 130 nm SiGe HBT transceiver for space intra-satellite applications.

Chapter 2

Fiber-optical wideband communication system

A large portion of this thesis was part of the Multi-Terabit Optical Interconnects (MuTOI) project. As such, the discussion is focused on fiber-optical data communication systems suitable for short-range interconnects, which are commonly used within internet data centers and hyper-computing clusters. However, there is significant overlap between the limitations and basics of short-haul, long-haul, and intra-satellite OIs.

2.1 System overview

A fiber-optical data communication system follows the main design principles of typical communication systems: there is a transmitter, a transport medium, and a receiver. The transport medium is an optical fiber instead of a copper wire (as in typical wired communications); therefore, the signal changes from electrical to optical and then from optical back to electrical. In the transmitter, the electrical signals are converted to optical via a laser diode; then in the receiver they are captured by a photodector and converted to electrical form.

2.1.1 Top view

The top view of a typical fiber-optical system is presented in Fig. 2.1. In such a system, the transmitter and receiver subsystems are hybrid opto-electronic systems. More in-depth discussion on these hybrid systems is presented in Section 2.2. The figure assumes that a synchronous clock is provided both at the transmitter and at the receiver. In a real system, the receiver typically has to extract the clock and digital data from the received asynchronous analog signal. The subsystem that performs this function is called Clock and Data Recovery block (CDR) [15]. A further break-down of the system into its components is presented in Fig. 2.2, including the common blocks of the transmitter and receiver subsystems. The figure also indicates whether the data is represented as voltages, optical signals, or currents as

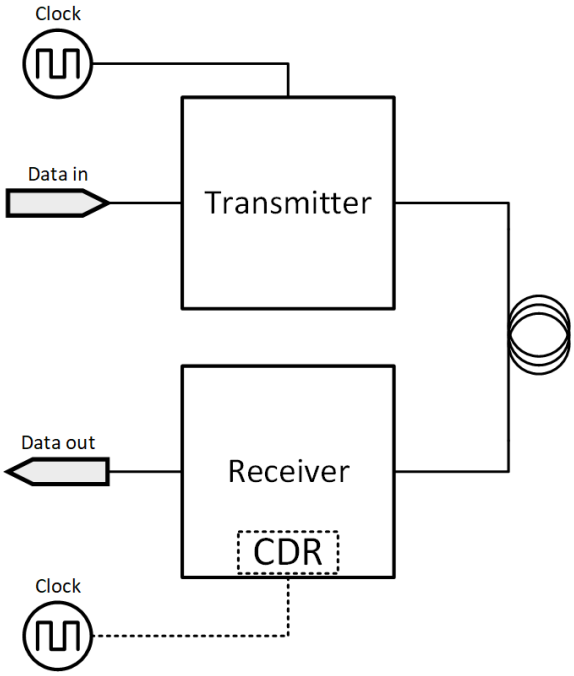


Figure 2.1: Fiber-optical system top view.

well as whether the data is in analog or digital format. The system in Fig. 2.2 is broken down into two subsystems in addition to the optical transport medium: the transmitter subsystem (TX) and the receiver subsystem (RX). The optical transport medium includes the optical fiber, the electrical-to-optical conversion block, and the optical-to-electrical conversion block. The typical lasers used in short-haul OIs are vertical cavity surface emitting Laser (VCSEL) as the electrical-to-optical conversion blocks and P-i-N photodiodes as the optical-to-electrical conversion blocks. Those components are then integrated with the electronics at a system level (heterogeneous integration).

2.1.2 Transmitter subsystem

A complete TX subsystem consists of one or multiple data inputs and a clock input if the clock is not generated in the transmitter. An encoding block after the data inputs might be used applying error redundancy algorithms such as forward error correction (FEC) which has been shown to improve performance of VCSEL based links [16]. Additionally, a variety of data encoding or modulation schemes (further discussed in Section 2.3) can be used in order to achieve trade-offs between the bandwidth utilisation, data throughput, and signal to noise ratio (SNR). Most state of the art TX subsystems also include a form of pre-emphasis or pre-distortion of the signal in order to compensate for the characteristics of the output amplifier and the transmission channel. The channel in this case is dominated by the laser-photodiode performance. An analog or digital-to-analog front-end amplification block is used last in the chain in order to amplify the data in the correct voltage-current swing

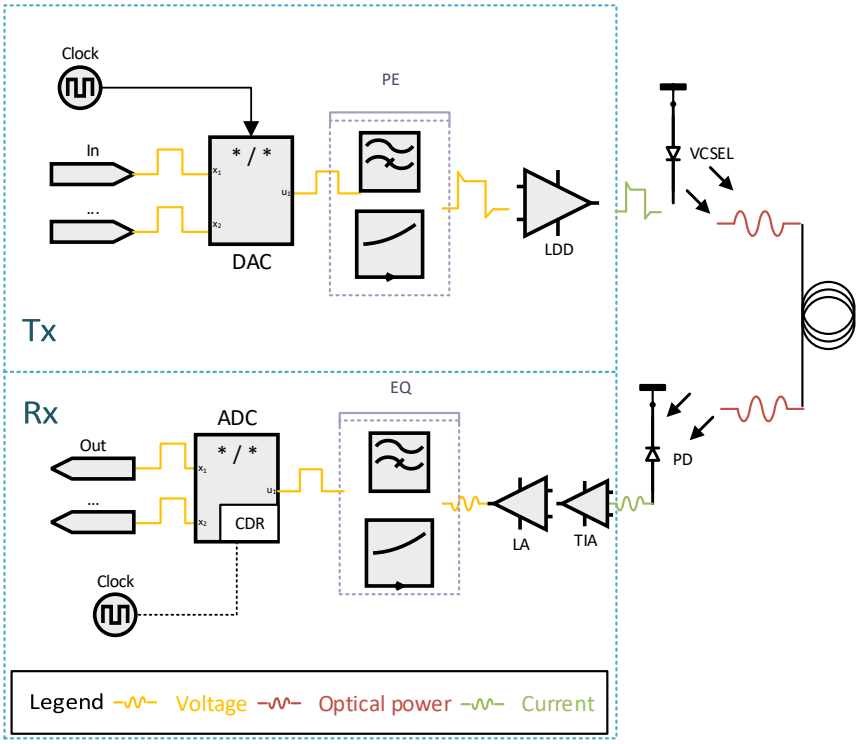


Figure 2.2: Optical link breakdown with the receiver (RX) and transmitter (TX) subsystems assuming heterogeneous integration.

required for the optimal operation of the laser.

2.1.3 Receiver subsystem

The RX subsystem consists of a front-end transimpedance amplifier (TIA) interfacing with the photodiode converting the photo-current generated into voltage signals. The TIA is usually followed by either a limiting amplifier or a linear amplifier depending on the complexity of the modulation scheme. Then an equalization block is used to further compensate for the channel and TIA bandwidth limitations. Additional blocks for correcting jitter and amplitude variations are also used in order to allow proper decoding and clock retrieval.

2.2 Optoelectronics

While several varieties of directly modulated lasers are used in short-haul optical data communication systems, the field is dominated by VCSELs and multi-mode fiber (MMF) links [17]. Continuous wave lasers modulated by Mach Zehnder modulators (MZM) are also utilized on long-haul high-capacity interconnect systems. For the receiver, p–i–n photodiodes are the most common photodetectors for such links due to their lower junction capacitance and higher bandwidth and lower bias voltage

compared to avalance photodiodes (APD) [18]. In high datarate long-haul optical links, wave-guide photodetectors are used which are limited by their parasitics [19].

2.2.1 VCSELs

VCSELs are one of the primary light sources used in datacom applications. The main structure of a laser diode is still present in a VCSEL; it consists of a light amplification structure between two mirrors with very high reflectivity. By increasing the bias current through the diode, as illustrated in Fig. 2.3, the rate of electrons passing through the gain medium increases. When the current increases past a minimum value called threshold current, the device starts lasing and further current increase causes an increase on the rate of photons generated and emitted. VCSELs, as opposed to typical light emitting diodes, use mirror structures called distributed Bragg reflectors (DBR) instead of simple mirrors. These structures are formed by alternating thin sheets of high and low refractive index to achieve near perfect reflectivity. A second significant difference is that VCSELs emit light vertically, as opposed to edge-emitting lasers, which allows multiple VCSELs to be fabricated and measured on a wafer without the need of dicing [18].

In terms of operation, the VCSEL is a nonlinear load whose frequency and transient behavior change based on the biasing conditions and temperature. The physical aspects of the VCSEL define most of its behavioral traits: the wavelength of emission, the jitter, the conversion efficiency, the linearity, the power consumption, the bandwidth and any oscillations on high frequency modulation, and the threshold current. VCSELs are typically biased and modulated by currents in the order of a few mA. The VCSEL must always be operating above threshold to avoid the turn on delay, in order to cope with high modulation frequencies, so typically a margin of about 1–2 mA above threshold is used [18].

In Fig. 2.4a, the I-V curve of a high speed VCSEL is shown for room temperature (RT) and at 85°C along with its corresponding I-P curve. The former can provide information about the device's dynamic resistance. The latter gives information regarding the threshold current, the thermal rollover, as well as the slope of the I-P

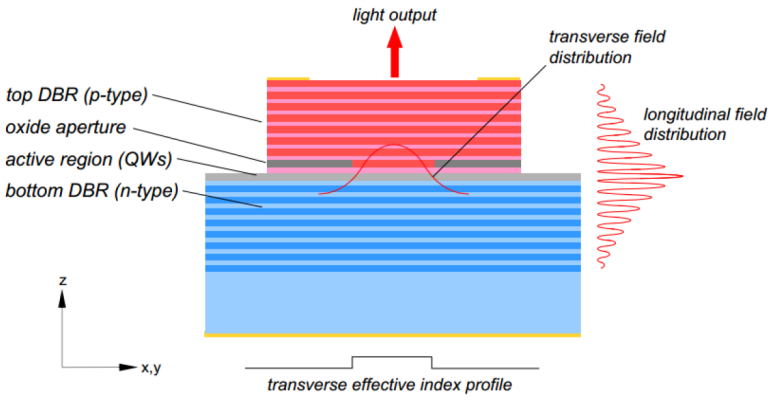
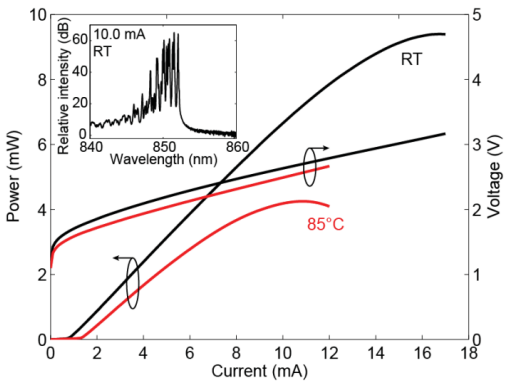
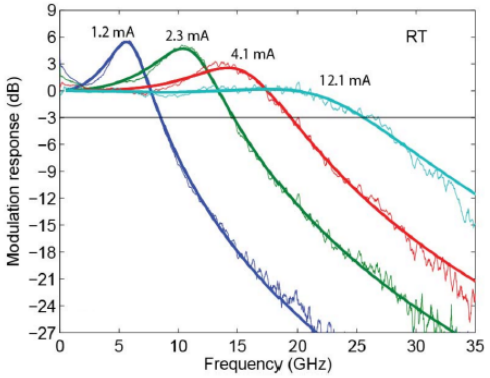


Figure 2.3: Cross-section of a typical VCSEL [18].



(a) VCSEL IPV curves at room temperature (RT) and 85°. Inlay: wavelength of emission.



(b) Modulation response of a VCSEL at room temperature (RT) for various bias currents.

Figure 2.4: IPV and modulation response of a state-of-the-art 850nm VCSEL [9].

curve. The slope efficiency given as $\frac{\Delta P}{\Delta I}$ is a measure of the VCSELs slope of output optical power to input current. The curve is an indication of the VCSEL's operating current range as well as the output power. The difference between the maximum optical power generated and the minimum optical power above threshold gives the optical power extinction ratio (ER) which is specified in dB. As shown in Fig. 2.4a, the optical power becomes non-linear at high operation currents (thermal rollover) and close to the threshold. Therefore, for large signal modulation suitable for high extinction ratio, the optimal bias point would be at the middle of the linear curve.

In Fig. 2.4b, the modulation response of a state-of-the-art 850nm VCSEL is given for various bias currents. The modulation bandwidth of the VCSEL evidently depends on the bias current. Therefore, the optimal bias point and optical modulation amplitude are dependent on the type of modulation used [20]. Additionally, in large signal modulation, the bandwidth of the VCSEL changes significantly between the high and low data bits.

2.2.2 Photodiodes

A photodiode is a diode that, under zero bias or reverse bias, generates a current proportional to the incident optical power. In short-reach optical links, two main varieties of Photodiodes are used, P-i-N or PIN photodetectors and Avalance Photodetectors (APD); both varieties have maximum bandwidth in the order of 30 GHz. PIN photodetectors are based on a P-i-N doped structure with an intrinsic region between the p and n doped regions. While this PD can be used in the so called photovoltaic mode (without any bias), generally a reverse bias is applied (photoconductive mode) in order to ensure that the intrinsic region is fully depleted. APD photodetectors are similar in design but typically larger and while they provide amplification of the incident light via avalance multiplication they have increased noise and larger capacitance. Additionally, they require higher reverse bias voltages to operate [21]. Receivers for long-haul optical communication links on the other hand, make use of wave-guide photodetectors with 80+ GHz bandwidth [19, 22, 23].

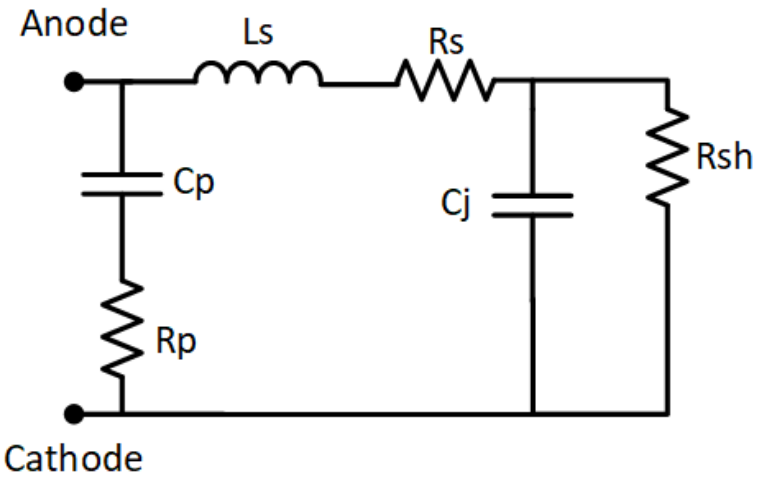


Figure 2.5: PD electrical parasitics model.

PD performance

Photodiodes used in high-speed optical interconnects have three main metrics of interest: their responsivity, bandwidth, and noise. The responsivity (R), measured in amperes per watt ($\frac{A}{W}$), gives the photocurrent generated as a response to optical power incident on the photodiode's aperture at a given wavelength. The current generated by the photodiode is called photocurrent (I_{ph}) and is given as:

$$I_{ph} = R \cdot P \tag{2.1}$$

R is the responsivity of the PD and P the received optical power.

The modulation bandwidth of operation (3-dB bandwidth) is dependent on the physical limitations of the photodiode. The parasitic components of a PIN photodiode are shown in Fig. 2.5. The parasitics include the bond-pad of the PD in the form of the pad capacitance C_p and resistance to ground R_p. A series inductance L_s and resistance R_s represent the traces from the pads to the junction as well as the junction series resistance. The main components are represented by the junction capacitance C_j and the shunt resistance R_{sh}. In photovoltaic mode, there is another term in addition to the junction capacitance, the diffusion capacitance, but when reverse bias is applied it becomes negligible.

When the PD is operated in photoconductive mode and is connected to an amplifier it becomes loaded by the amplifier's input impedance (R_L). While an ideal TIA should have zero input impedance, real systems have an impedance of typically up to 50 Ω. In that case, the overall frequency response of the PD-TIA system is that of an RC low-pass filter assuming that the PD is not limited by its transit time. The shunt resistance is generally very large compared to R_L so it can be neglected. The pad capacitance C_p can be combined with C_j, making it C_{PD}. The response of the PD-TIA system is therefore limited by R_L and C_{PD} [24].

Photodiode noise

The noise of the photodiode is a combination of shot noise, thermal noise, and $^1/_f$ noise [24]. In addition, a leakage current called dark current (I_{dark}) appears even in the absence of optical signal. This is a reverse current across the junction and stems from thermal generation of free carriers [18].

The $^1/_f$ or flicker noise becomes significant at lower frequencies, however in this work we assume a lowest frequency in the order of a few kHz; therefore, we can neglect this term. The dark current contribution is dependent on the reverse bias of the PD (V_A).

$$I_{dark} = I_{SAT}(e^{\frac{qV_A}{Nk_BT}} - 1) \tag{2.2}$$

Where q is the electron charge, K_B is the Boltzmann constant, N is the diode ideality factor, T the absolute temperature, and I_{SAT} the reverse saturation current. For the a typical PIN diode, the optimal bias for high speed operation is -5 V [10]. Under that condition the dark current is in the order of a few nA [21]; therefore, it becomes negligible compared to the other noise terms discussed below.

The thermal noise is given as:

$$\overline{i^2_{n,Th}} = \frac{4k_BT\Delta f}{R_{sh}} \tag{2.3}$$

Where q is the electron charge, Δ_f is the bandwidth over which the noise power is integrated, T the absolute temperature, and R_{sh} is the shunt resistance of the PD. For 30 Gbps+ PIN photodetectors this is in the order of 250 $k\Omega$ [10].

The diode shot noise is the most significant factor and is given as:

$$\overline{i^2_{n,sh}} = 2q \cdot (I_{ph} + I_{dark}) \cdot \Delta f \tag{2.4}$$

Where q is the electron charge, Δ_f is the bandwidth over which the noise power is integrated, and I_{ph} is the photocurrent given in equation 2.1. As shown in equations 2.4 and 2.3, the noise is dependent on the bandwidth of the receiver. For 50 GHz bandwidth, I_{ph} of 0.4 mA, R_{sh} of 250 $k\Omega$, and neglecting the dark current, equations 2.4 and 2.3 indicate that the shot noise contribution is $\approx$ 2000 times larger than that of the thermal noise. However, that does not take into consideration the noise contribution of the TIA, which will be discussed in the next chapter.

In Fig. 2.6 we can see the simplified equivalent model of the photodiode when used in combination with an amplifier. The model includes the photocurrent I_{ph}, the PD parasitics, the TIA's input impedance loading the PD R_L, the equivalent noise source of the PD $I_{n,pd}$, and the dark current of the PD I_{dark}.

Biasing and coupling

The biasing of the photodiode and the coupling with the amplifier can take two forms: AC and DC coupling. On DC coupling we can also further distinguish into: common anode, when the anode terminal is grounded for the AC signal, and common

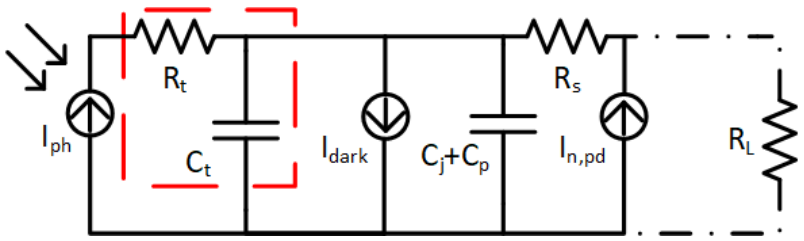
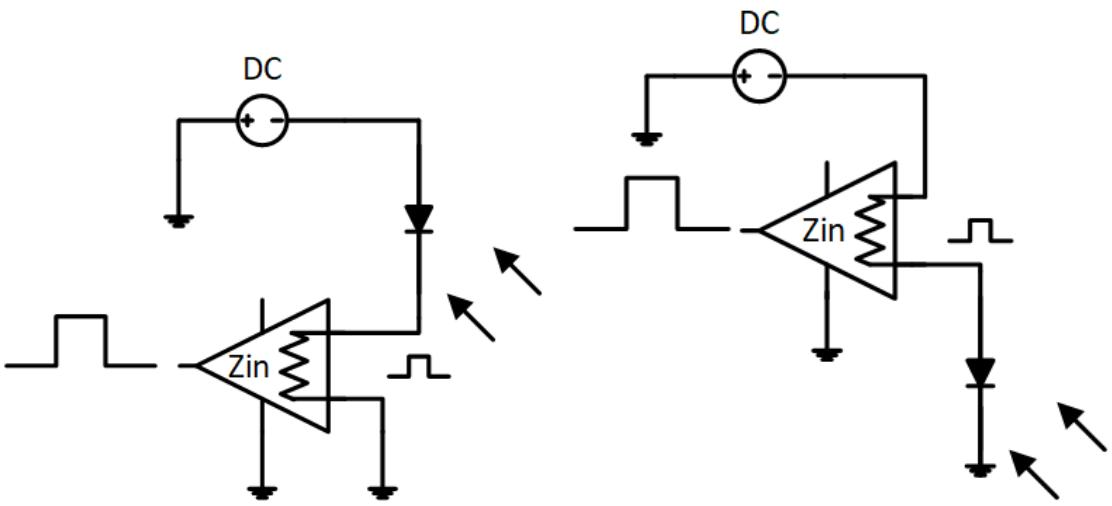


Figure 2.6: PD equivalent model.

cathode, when the cathode is grounded. The two alternative coupling modes can be seen in Fig. 2.7. The ideal TIA has zero input impedance (Z_{in}), however in practice the input impedance is typically 50 Ω.

The common-anode architecture is preferred when the voltage at the input of the transimpedance amplifier (V_{in}) can be kept stable by other circuit components despite the variations of the photo-current. The reverse bias of the photodiode must be typically at or above 2 V so the V_{in} of the circuit should provide that exact voltage while the photodiode anode would be grounded. This can be a challenge since it requires the design to be shifted +2 volts, which also calls for more careful design in order to not exceed the breakdown voltage of the transistors. As an example the fast HBT devices in 130 nm SiGe BiCMOS process have a $V_{B,CE}$ of approximately 1.5 V [25, 26]. Alternatively, if a negative voltage supply is available it should replace the ground in the anode, thus alleviating the aforementioned issues, at the expense of symmetric supply, which will increase the number of DC-pads required, thus increasing the chip size.

The common cathode is less challenging to realise with an additional external bias on the photodiode, thus eliminating the need for biasing through the input of the TIA. In this method the voltage across the diode will be $V_{bias} - V_{diode}$ where the later is the voltage drop across the diode junction. This voltage will be "seen" at the



(a) Common Anode. (b) Common cathode.

Figure 2.7: Different PD-TIA coupling topologies used in literature.

input of the TIA and should be taken into account when designing the input stage.

Even though in literature AC coupling of the input source is used in narrow-bandwidth tuned low noise amplifier design, it cannot be applied in the context of this project. NRZ data have a broadband spectrum that can span from kHz to GHz. Therefore, an AC coupled connection between the PD and the TIA would eliminate the low frequency components of the signal, and consequently introduce errors.

2.3 Modulation formats

Short-haul fiber-optical data communication systems are dominated by NRZ amplitude modulation formats. The simplest and most commonly used is the binary On-Off Keying (OOK) modulation. It is straightforward to realise and measure transceivers based on this modulation. Additionally, binary OOK modulation imposes less strict SNR-requirements than higher modulations, and therefore less strict noise requirements. Essentially it is simply a binary method of signaling, with '0' typically mapped to no signal or low optical power, and '1' to a signal pulse or high signal power. However, that means that the bit-rate is the same as the baud-rate. Therefore, for 100 Gbps data-rates a bandwidth of approximately 50 GHz is required, which can prove very challenging to realize due to the bandwidth limitations of the optoelectronic components mentioned above.

In order to transmit more data in a bandwidth-restricted channel, M-ary digital modulation schemes are utilized. The most common is 4-level Pulse Amplitude Modulation (PAM-4). In comparison with OOK, which can be considered PAM-2 modulation, PAM-4 transmits double amount of information for the same bandwidth, by sacrificing signal to noise ratio (SNR). Alternatively the bandwidth can be reduced to 50 GHz, which will allow a baudrate of 100 Gbps. The trade-offs in this case are: the SNR penalty imposed, which is at least -6 dB; the increased complexity of encoding and decoding blocks on the transceivers; and the increased complexity of characterization and measurement. The state-of-the-art in binary PAM-4 modulation VCSEL based links are 90+ Gbps [27, 28] and 110+ Gbps in duo-binary PAM-4 [29].

As mentioned earlier, an important metric in short haul fiber-optical interconnects is power consumption. However, the main goal of the field is to increase the datarate. Therefore, the energy consumed per bit of information sent is used as a means to measure the efficiency of datacom systems. This figure of merit is called energy efficiency (η_e) and is measured in $\frac{\text{pJ}}{\text{bit}}$ or $\frac{\text{mW}}{\text{Gbps}}$.

2.4 Transceiver electronics

As discussed above, the communication channel is heavily limited by the optoelectronic devices. However, even the simple modulation formats mentioned impose high requirements to the integrated electronic circuit design. Thankfully, due to the continuation of Moore's law on silicon devices and with the increasing maturity of III-V integrated devices, there are several processes suitable for the task.

Advanced deep sub-micron CMOS processes dominate on low-baud-rate high-energy-efficiency transceivers, especially with advanced silicon on insulator (SOI) and Fin-FET processes [30]. Additionally, they provide millimeter-wave components such as high frequency inductors and capacitors, and characterization tools suitable for RF applications driven by the 5G mobile network, datacom, and automotive industries. On the other end of the spectrum, Indium Phosphide (InP) double heterjunction bipolar transistors (DHBTs) and other III-V-material-based technologies that have traditionally been used for high-power or THz RF applications are becoming more common in the field. By reaching higher scales of integration and providing more interconnect layers, they enable transceiver circuit designs with unprecedented baud-rates. Lastly, the continuous advancement of Silicon Germanium heterostructure bipolar transistor (SiGe-HBT) and Bi-CMOS processes come to bridge the gap between the aforementioned processes both in performance and in production volume. In the core of this progress lies the added benefit of monolithically integrated photonic components; silicon photonics in CMOS processes, germanium photodetectors on SiGe, and lasers and photodetectors grown directly on InP transceivers. The specific merits of each process in receiver electronic circuit design will be further discussed in the following chapters.

2.5 Space environment challenges

VCSEL based optical links are considered for use in intra-satellite communication links in a variety of satellite payloads. In such environments, beside the extreme temperature ranges of operation the VCSELs and the electronics are constantly subjected to the space environment. The radiation of space typically introduces two different effects in analog linear circuits, cumulative effects caused by long term radiation, and Single Event effects (SEEs) or single event transients (SETs) which are essentially voltage surges that occur in integrated circuits in a radiation environment. SETs are typically caused by high energy particles passing through the substrate in the vicinity of sensitive active devices. There are several techniques to mitigate the effects of radiation which will be discussed in Chapter 6.

Chapter 3

Wideband Electronic Components

3.1 Wideband Amplifiers

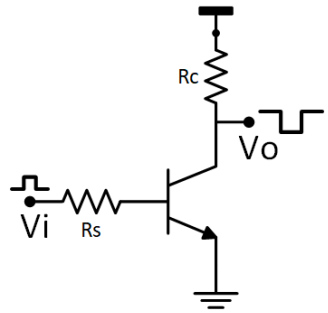
In order to achieve wideband communication while maintaining low power consumption, we need to utilize high-end semiconductor processes and clever design implementations. In order to do that, we choose to design in SiGe- and InP-based technologies since they represent the majority of the published work beyond 50 Gbps. By making this decision, we commit to HBT- and DHBT-based topologies and a relatively low degree of integration when compared with what is possible in CMOS processes. The most commonly used wideband amplifier topologies in literature are briefly presented in this section.

3.1.1 Single stage amplifiers

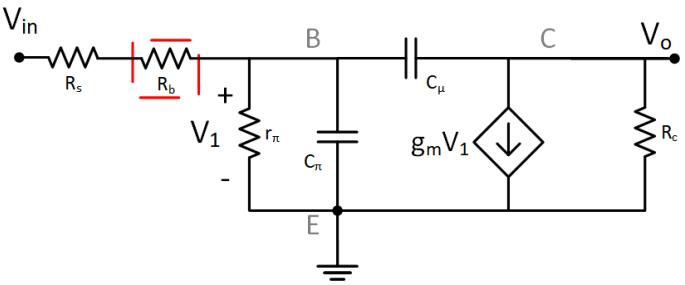
An abundance of different amplifier topologies are used in wideband designs. In this section, the most prominent wideband topologies in HBT and DHBT technologies will be presented and evaluated based on the amplifier criteria presented in the previous paragraph.

The common emitter amplifier is the most prolific amplifier topology in literature (Fig. 3.1a). It provides high current and voltage gain, adequate bandwidth (mainly limited by the Miller effect if not counteracted), but requires complex bias networks and emitter degeneration in order to maintain stable operation over temperature. The relatively high input impedance provided by CE can be very beneficial in OP-amp design where an ideally infinite input impedance is wanted. However, in TIA design, where a low input impedance is optimal, this is typically addressed with shunt-shunt feedback in order to lower the input impedance seen by the photodiode, while at the same time decreasing the noise. One additional downside, as mentioned, is the Miller effect which can degrade the bandwidth of the CE stage.

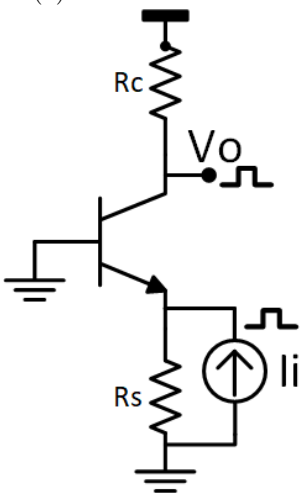
The small signal equivalent model of a CE amplifier seen in 3.1b is used to calculate the high frequency response of the circuit. The low frequency voltage gain



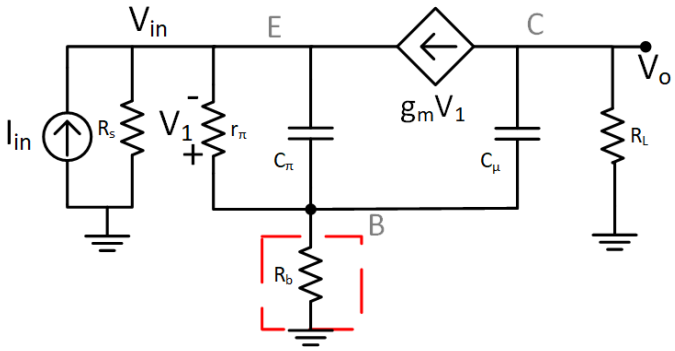
(a) Common Emitter.



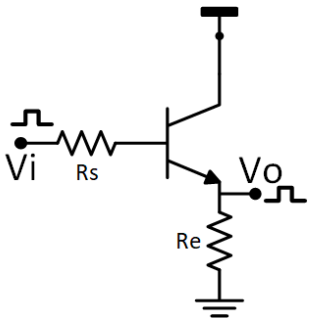
(b) CE small signal high frequency circuit.



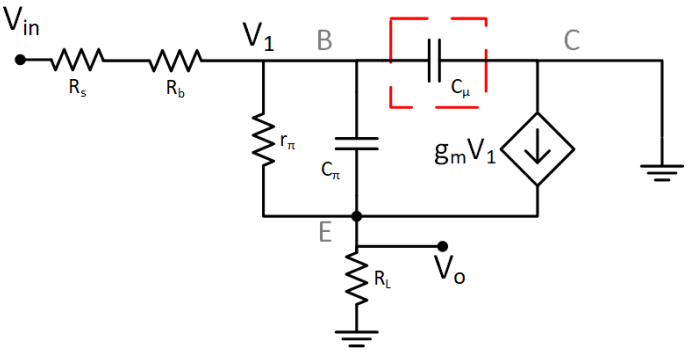
(c) Common Base.



(d) CB small signal high frequency circuit.



(e) Common Collector.



(f) CC small signal high frequency circuit.

Figure 3.1: Single ended amplifier topologies with high frequency small signal equivalent circuits ignoring R_o. Marked components are typically neglected to simplify the calculations.

of the circuit is equal to:

$$A_{v0} = g_m R_c \frac{r_\pi}{r_\pi + R_s + R_b} \tag{3.1}$$

Where g_m is the transistor transconductance, r_π is the base-emitter resistance, β is the transistor current gain, and R_b is the total resistance at the base of the transistor.

For processes with high β and $R_s + R_b << r_\pi$, the equation simplifies to:

$$A_{v0} = g_m R_c \tag{3.2}$$

Therefore, the gain of the amplifier can be increased by increasing either g_m which is a function of the collector current I_c or increasing R_c. With a dominant-pole approximation, at high frequencies the gain is limited by the time constants of the two capacitors present, the base emitter capacitor C_π and the base collector capacitor C_μ:

$$p_1 = -\frac{1}{C_\pi R_s + C_\mu(R_s + R_c + g_m R_s R_c)} \tag{3.3}$$

Additionally, the bandwidth further deteriorates with the presence of any capacitance at the collector terminal (load) by an additional time constant of $\tau_c = R_c C_l$. Since both C_π and g_m are dependent on I_c, there is a direct trade-off between gain and bandwidth.

The common base, seen in Fig. 3.1c, was used extensively in wideband optical communication systems since the 1980s [31] due to its very low input impedance, in combination with high bandwidth. In addition to those merits, it also provides high voltage gain and high output impedance, all of which are preferred in TIA design. However, CB input stages tend to be more noisy than other single-transistor architectures since the noise generated by the transistor is added directly to the input. CB stages can be used with or without feedback. The small signal equivalent model of a CB amplifier seen in 3.1d is used to calculate the high frequency response of the circuit. The low frequency current gain of the circuit, assuming R_b is very small and β is very large, is equal to:

$$A_{i0} = \frac{g_m r_\pi}{g_m r_\pi + 1} = \alpha \tag{3.4}$$

The transimpedance gain therefore becomes:

$$A_{t0} = \alpha R_c \tag{3.5}$$

The bandwidth is limited by two independent time constants relevant to C_π and C_μ such that:

$$\tau = C_\pi r_m + C_\mu R_c \tag{3.6}$$

It is evident that the time constant is significantly smaller, compared to the CE amplifier due to the small value of $r_m = 1/g_m$ which dominates the input impedance even at the presence of a source resistance R_s. Since C_π and r_m have an inverse relationship with I_c, the input time constant is independent of the biasing. At the output node, R_c coupled with the negligible C_μ and any load capacitance C_L form the main bandwidth limitation of the circuit. Thus, selecting R_c offers a direct trade-off between transimpedance gain and bandwidth.

The input impedance of the common base at low frequencies is:

$$Z_{i0} = -\frac{r_\pi + R_b}{1 + g_m r_\pi} = r_m + \frac{r_\pi + R_b}{1 + \beta} \tag{3.7}$$

Which for high values of β is dominated by the value of r_m, which can be controlled by the quiescent current. However the frequency response, is dependent on a single time constant:

$$\tau = C_\pi r_m \tag{3.8}$$

At high frequencies the value of the input impedance becomes $R_s//R_b$ since the capacitor C_π becomes a short circuit. Therefore, the input impedance of the common base appears inductive (increases with frequency) for $r_m < R_s//R_b$.

Common collector amplifier stages shown in Fig. 3.1e are a versatile tool in broadband amplifier design. With high input impedance, low output impedance, and near-unity voltage gain, and a very wide bandwidth, they serve as voltage buffers and DC-level shifters between other amplification stages. Due to their very high current gain, they are often used as output stages to drive the standard loads of 50 Ω. The small signal equivalent model of a CC amplifier seen in 3.1f is used to calculate the high frequency response of the circuit. The low frequency voltage gain of the circuit, assuming $R_b <<$ and $\beta >>$ is equal to:

$$A_{v0} = \frac{g_m R_L + \frac{R_L}{r_\pi}}{1 + g_m R_L + \frac{R_s + R_L}{r_\pi}} \tag{3.9}$$

Which is close to unity at low frequencies. At high frequencies the bandwidth is limited by a single dominant time constant:

$$\tau = C_\pi \frac{R_s + R_L}{1 + g_m (R_L + \frac{R_s + R_L}{\beta})} \tag{3.10}$$

And a zero is present at:

$$z_1 = \frac{g_m + \frac{1}{r_\pi}}{C_\pi} = \frac{1}{r_m C_\pi} \tag{3.11}$$

At frequencies below f_t the zero is located close to the pole, thus providing very high bandwidth. The output impedance of the CC topology follows a similar pattern with the input impedance of the common base. At low frequencies it is equal to:

$$Z_o = r_m + \frac{R_s + R_b}{\beta} \tag{3.12}$$

Which for high values of β becomes r_m, but at higher frequencies it becomes $R_s + R_b$ due to C_π shorting the input to the output. With careful control of r_m, R_s and R_b (wherever possible) one can achieve inductive output impedance or purely real output impedance, depending on the application. In a typical design scenario, R_b is device dependent, R_s depends on the previous driving stage, therefore only r_m can be controlled accurately via I_c.

The cascode circuit is a very common circuit topology originating from vacuum tube amplifier design [32]. It consists of the cascade of a common emitter stage feeding into a common base stage. The CB stage serves as a current buffer to the CE stage; therefore, the overall gain of the two stages is similar to that of the CE amplifier. The very low input impedance of the CB stage serves as the load

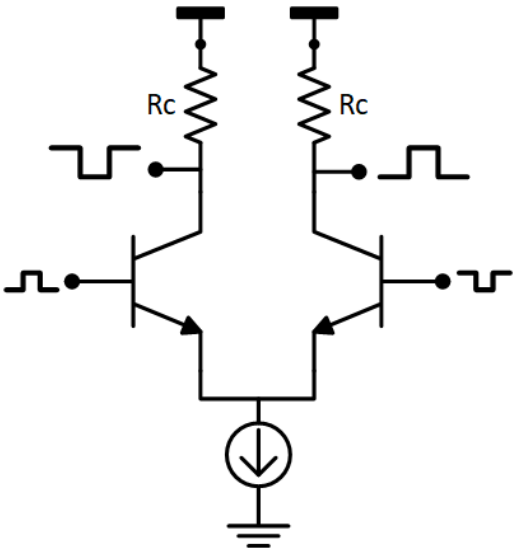


Figure 3.2: Differential CE amplifier.

impedance for the CE stage which diminishes the effects of the Miller capacitance. The cascade of these two stages provides a higher bandwidth than the CE stage due to the Miller effect being diminished, but it also requires higher voltage headroom and an additional bias supply for the CB stage.

3.1.2 Differential amplifiers

Differential amplifiers also originate from the era of vacuum tube designs [33]. They are amplifier stage pairs sensitive to differences between their two inputs. Using differential amplifiers offers plenty of benefits in the context of this wideband amplifier design (Fig. 3.2). The main benefit of such circuits is the common mode rejection. The circuits amplify differences between the inputs and dampen signals or noise which are common in both inputs [34]. Additionally, differential CE amplifiers, can be cascaded without the need of large inter-stage coupling capacitors which offers large savings in area. In wideband cascaded implementations, the bases of the next stage are biased via the collector of the previous stage which eliminates the need for biasing circuitry, however places a restriction to the voltage swing. Differential amplifiers can make use of positive or negative bias, and the tail current source can be made tunable in order to adjust the gain of the amplifier. The tail current is constant over time, which allows for simpler current source designs, but in turn increases the power consumption when compared with the single ended versions. At the same time, constant current means little to no variations on the voltage rails. The main issue in differential design is the added complexity due to the doubling of the components, as well as the challenge of achieving perfect symmetry.

3.2 State-of-the-art technologies

3.2.1 SiGe HBT

In high speed optical interconnect circuits, one can reach higher performance with BiCMOS, but if the same performance is reachable with CMOS, it is likely to consume less power. However the BiCMOS designs are still far better in terms of power consumption when compared with InP. In the case of circuits for high speed interconnects, BiCMOS provides an interesting trade-off between high performance, low noise, higher gain-bandwidth product; at the expense of higher energy dissipation and higher cost-to-manufacture.

The higher energy consumption of the BiCMOS can be attributed to the usage of bipolar transistors that require a constant collector current in order to remain operating at the optimal current density for highest bandwidth. In addition to that the state-of-the-art SiGe BiCMOS technologies have yet to reach the deep sub-micron feature sizes of modern Si-CMOS.

3.2.2 InP DHBT

InP and III-V based circuits are mainly designed for the highest performance possible. This can also be extrapolated by the f_t of such processes. Another interesting feature is the compatibility of such processes with modern monolithic photonic sub-assemblies. Circuits designed in an InP process have typically high energy consumption which is mainly attributed to the high supply voltage required as well to the essential current that the bipolar transistors require to operate in order to provide high gain and bandwidth. However, the high supply voltage required can provide a significant advantage in the linearity of amplifiers by providing additional voltage headroom.

3.2.3 Effects of Beta in wideband design

While SiGe based processes boast relatively high values for β [25], the opposite applies for state-of-the-art InP processes [35, 36]. In the latter case the β can be more than a order of magnitude smaller than the former, which negates most of the assumptions made in 3.1.1. Furthermore, non-linearities that appear at smaller device sizes for high current density skew the calculations even further.

Consider the small signal parameters of the aforementioned 130 nm SiGe HBT process with an f_t of 250 GHz and high β. The simulated small signal parameters deriving from β and I_c can be seen in Fig. 3.3, and are well within the assumptions made in the previous section. There is a visible but not substantial dependence on the device size, which can be attributed to smaller contacts giving rise to higher parasitic resistances, as well as the saturation of g_m at high current densities. With a β in the order of 400–600 in the optimum current density for max f_t, this process enables the design of wideband amplifiers that can be cascaded easily without loading due to the very high r_{pi}. Furthermore, using CC stages to buffer cascaded

amplification stages provide isolation since any impedance present at the emitter of a CC, appears at its base divided by $1 + \beta$.

Consider however the small signal parameters of a 130 nm InP process with f_t in the order of 520 GHz seen in Fig. 3.4. First, the reason for the g_m degradation at small device sizes is that the transistor is operated at high current density and base-collector depletion space-charge is neutralized by the electrons giving rise to 'base-pushout' i.e. Kirk effect [37]. The most important information in Fig. 3.4 are the low values of beta for all current densities. This is a well documented fact in high f_t processes but it has multiple ramifications in wideband design. As mentioned earlier in this chapter, wideband amplifiers are typically cascaded and make use of current or voltage buffers in order to avoid loading and improve the overall gain-bandwidth. However, with low r_π the input impedance of a typical CE or CC is severely decreased, effectively loading any previous gain stage. In the case of a CE amplifier, if high gain is required, then high current must then be used as per Eq. 3.1 in order to increase g_m. That in turn leads to a decrease of r_π limiting the gain increase, and increasing power consumption at the same time. A CC stage, which is commonly used to isolate two cascaded stages, suffers from the lower input impedance due to low r_π. Furthermore, due to the low β, a CC stage also provides significantly compromised isolation.

Despite all of the above downsides, high f_t processes see extensive use in both high frequency narrowband applications, as well as in wideband applications. One of the most prolific techniques that exploit the benefits of such processes while

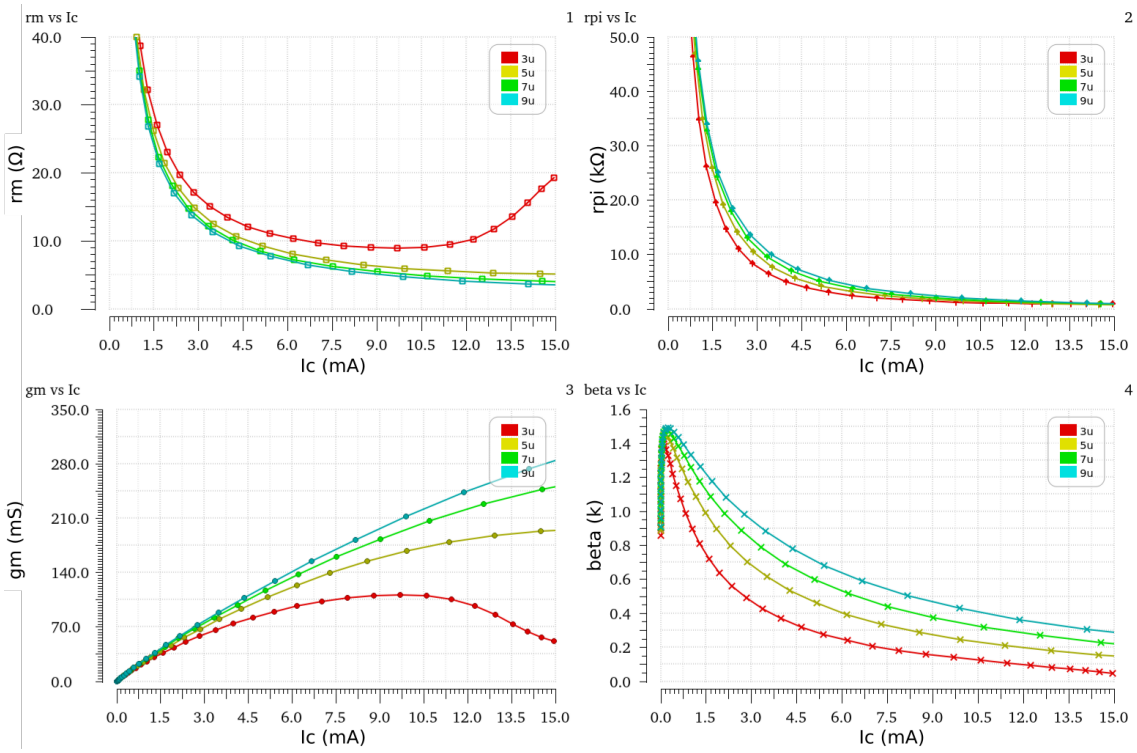


Figure 3.3: Simulated SiGe HBT small signal parameters vs collector current for various emitter sizes.

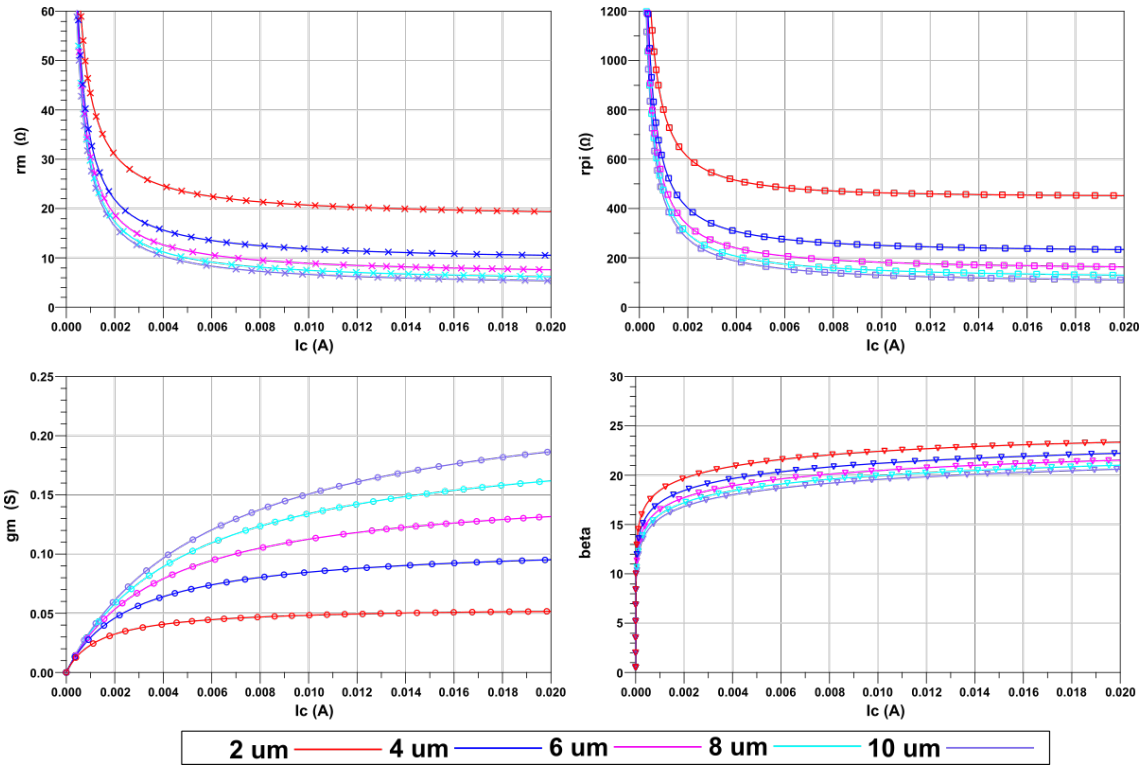


Figure 3.4: Simulated InP 130 nm DHBT small signal parameters vs collector current for various emitter sizes.

compensating for the shortfalls is distributed amplification, which will be discussed in the following Chapter.

Chapter 4

Ultra-Wideband Distributed Amplifiers

As mentioned on the previous Chapter, high f_t processes offer extremely high bandwidth but at the cost of limited β. That inherently limits the gains of cascaded amplification stages in baseband amplifiers. A potential work-around is offered when one considers distributed or travailing wave amplification, which can extend the bandwidth of such amplifiers to values close to f_t.

4.1 Distributed Amplifiers

The distributed amplifier consists of several amplifier cells connected in parallel with matched transmission lines at the input and output as shown in Fig. 4.1. The transmission lines are designed so that the signal that travels down the line of the amplifiers interferes constructively at each stage. This is accomplished by carefully designing the artificial transmission lines (ATL) for the appropriate phase delay, including the input and output parasitics of each cell in the design. Since the (terminated) transmission line serves as the load for the amplification cells, each individual cell does not offer very high gain, but since each cell contributes to the gain constructively, the total gain of the amplifier is high. Additionally, the output time constant of each cell is reduced, thus extending the bandwidth. Therefore the main benefit of this architecture is the ultra-wide bandwidth of such amplifiers, without sacrificing gain, but at the cost of power consumption and chip area. The state-of-the-art in distributed amplifiers is presented in Table. 4.1. Distributed amplifiers have been used in optical communication links as drivers for electro-optical Mach-Zehnder modulators [38–40], fiber-optic interleaved transmitters and receivers [41], and transimpedance amplifiers [42].

4.1.1 250 nm InP DHBT process

The wideband DA circuits in this chapter were designed using TSCs 250 nm InP DHBT process with an f_t and f_{max} of 520 GHz and 1.15 THz respectively [35]. The

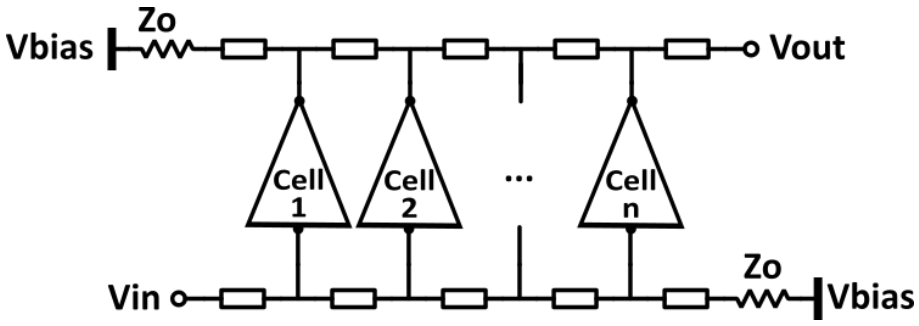


Figure 4.1: Typical topology of a distributed amplifier.

Table 4.1: State-of-the-art DAs in literature.

Technology	BW (GHz)	Gain (dB)	GBP (GHz)	P_{DC} (mW)	GBP/P_{DC} (GHz/mW)	Area (mm^2)	DA Topology	Ref.
250 nm InP DHBT	241	$10 \pm 2^*$	762	387	2.00	0.82	6-stage Cascode	[43]
250 nm **InP DHBT**	**207**	13.5 ± 2	**979**	**210**	**4.66**	**0.29**	**4-stage Cascode****	**D**
500 nm InP DHBT	175	$12 \pm 2^*$	697	180	3.87	0.975	5-stage tricode	[44]
250 nm InP DHBT	182	$10 \pm 2^*$	575	110	5.23	0.33	4-stage Cascode	[45]
250 nm InP DHBT	192	7.5 ± 1	455	40	11.38	0.24	SSDA	[46]
250 nm InP DHBT	235	16 ± 2	1480	117	12.65	0.41	2-Cascaded-SSDA	[46]
130 nm SiGe BiCMOS	170	$13 \pm 1^*$	759	74	10.26	0.22	4-Cascaded-SSDA	[47]
130 nm SiGe BiCMOS	175	16 ± 4	1102	360	3.06	0.38	2-Cascaded-SSDA	[48]
250 nm **InP DHBT**	**200**	**7.1 ± 3.5**	**455**	**67**	**6.79**	**0.28**	**SSDA**	**B**
800 nm InP dHBT	100	$10.6 \pm 1^*$	343	143	2.4	1	3-stacked	[49]
100 nm SiGe HBT	140	$11.7 \pm 3^*$	538	117	4.6	1.02	3-stacked	[49]
35 nm InGaAs mHEMT	335	$13 \pm 2^*$	1496	117	12.8	0.63	Cascode	[50]

* There were no comments on the gain ripple in these publications, so the gain ripple has been estimated from the s-parameter plot.
** CC: Common collector.

process Back End Of Line (BEOL) includes thin-film resistors, Metal Insulator Metal (MIM) capacitors and three gold interconnect metal layers, a thick top metal and a bond-pad metallization coating. A cross-section of the technology can be seen in Fig. 4.2.

4.2 DC to 200 GHz CC Cascode DA

4.2.1 Circuit topology

In Paper D, we presented the measurement and characterization of an ultra-broadband distributed amplifier designed in a 250 nm InP DHBT process provided by Teledyne Scientific Company (TSC) [35]. At the time of the publication, it was the widest bandwidth DA that could operate from DC frequencies. The DA made use of the Common Collector Cascode (CC-Cascode) topology which has been proposed by

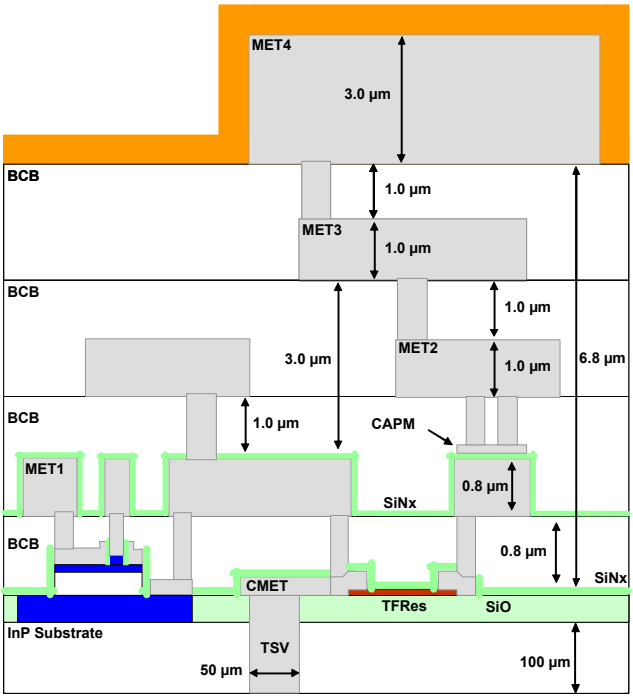


Figure 4.2: Cross-section of the 250 nm InP DHBT process by Teledyne.

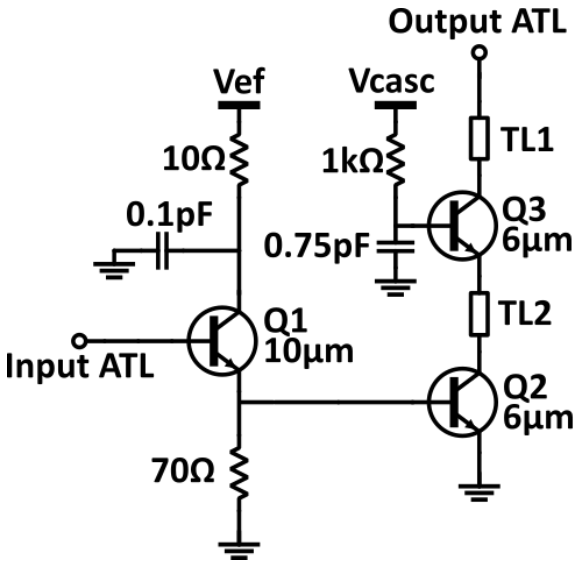


Figure 4.3: Circuit schematic of a single CC-Cascode cell.

Kobayashi et al [51] as an improvement to the common emitter or cascode distributed cells. A schematic of a single cell can be seen in Fig. 4.3. The bandwidth extending merits of a cascode have been extensively discussed in literature, however the presence of the CC in such a topology offers unique benefits. The first benefit is the increased isolation of the input from the output of the cell, which is important for a low β process. Additionally, the increase in the cell's input impedance reduces the loading of the input transmission line, allowing for more cells to be used. The obvious downside is the increased power consumed by each CC cell as well as the added

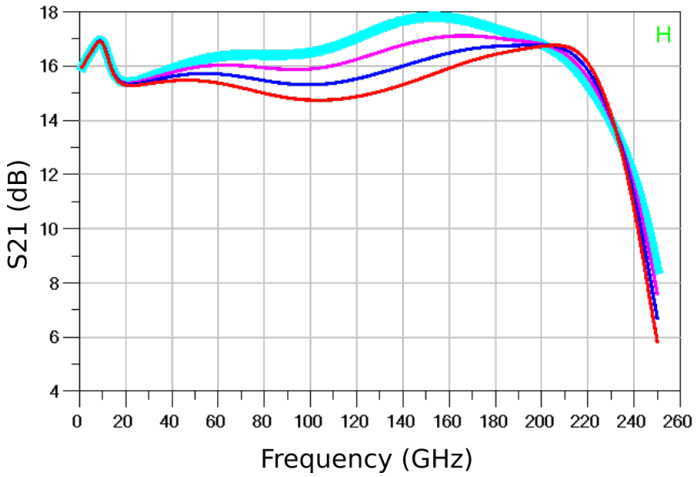


Figure 4.4: Effects of emitter inductance on gain of the DA. Cyan: 0 pH, purple: 2 pH, blue: 4 pH, red: 6 pH.

complexity of the interconnections between the transistors which can give rise to resonant effects.

The critical aspects of the design can be exemplified by how the added via inductance present on the emitter of the cascode amplifier manifest on the gain of the amplifier, as seen in Fig 4.4.

4.2.2 Measurement challenges

As made evident by the results presented in Paper D, the most challenging aspect of ultra-wideband DAs is how to fully characterize them.

The frequency measurement had to be divided to at least three separate measurement sweeps: a base-band to 67 GHz measurement using coaxial probes, a 70 GHz to 110 GHz measurement using WR-10 wave-guide probes, and a 140 GHz to 220 GHz measurement using WR-5.1 wave-guide probes. All probes had to be calibrated in a progressively demanding fashion and the bias point of the MMIC had to be restored after each break for calibration.

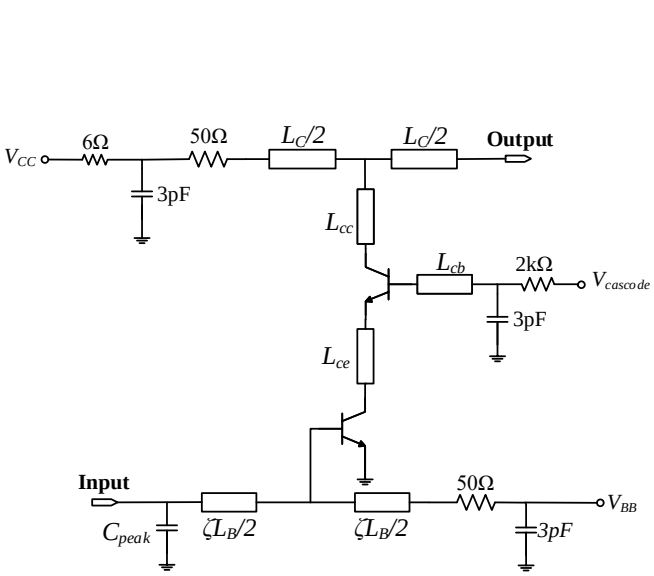
A characteristic of such amplifiers is the gain ripple which is prevalent in a significant part of the published literature (as seen in Table 4.1). The low frequency peaks on the gain response are caused by a combination of the on-chip ATL terminations and off-chip bias-probe inductance and capacitances. Novel approaches in literature, such as active ATL termination, are attempting to solve that issue [49].

4.3 Single cell and Multiplicative DAs

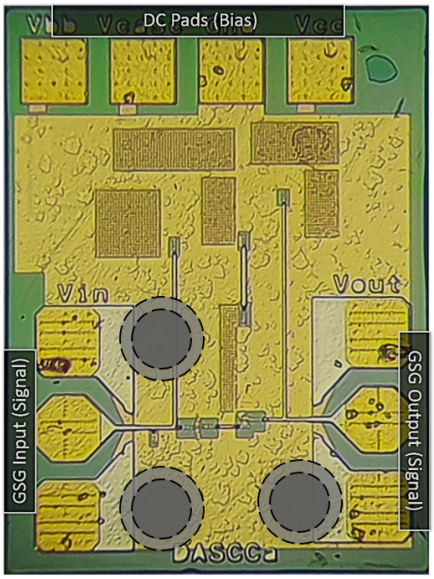
In Paper B we present the gain-bandwidth merit of the single stage distributed amplifier (SSDA) and its derivative multiplicative amplifier topologies (i.e. the cascaded SSDA (C-SSDA) and the matrix SSDA (M-SSDA)), for ultra-wideband amplification.

Two MMIC were designed in Teledyne Scientific Company's (TSC) 250 nm InP DHBT process mentioned in the beginning of this chapter. The MMICs were measured and characterized and post measurement simulations were performed to understand their limitations. At the time of publication, the SSDA had the widest bandwidth for any single stage amplifier reported in literature. Furthermore, the three tier M-SSDA demonstrated the highest bandwidth and gain-bandwidth product for any matrix amplifier presented in literature.

4.3.1 Single Stage DA



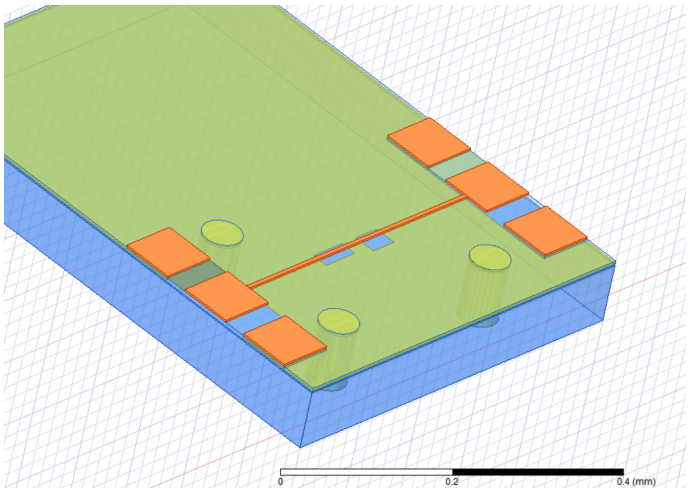
(a) Schematic circuit of SSDA with scaled input line, shunt capacitance and adapted loss compensation.



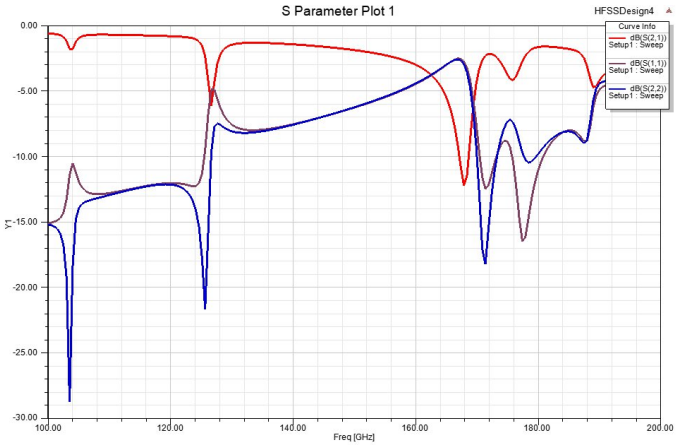
(b) Microphoto of SSDA. Footprint: 460 µm x 620 µm. Dashed circles indicate location of through-substrate vias.

Figure 4.5: SSDA: Circuit diagram and MMIC microphotograph

A critical observer would point out the gain ripple in the results of the frequency domain measurement of the SSDA. This is partly attributed to the ground inductance as discussed in Paper B (in Fig. 9), but also attributed to the way the ground plane is interrupted in order to couple the signal to the SSDA. In order to connect the transmission line metal (MET4 in Fig.6) to the capacitors (CAPM, between MET2 and MET1), and the HBTs and Thin Film resistors (connected via MET1) slots are required in the ground plane (MET2) as shown in Fig. 4.6a. The substrate modes are excited through the slots in accordance to [46], however in that work there were no



(a) Simplified SSDA model with through transmission line for substrate mode simulation.



(b) Results of the substrate mode EM simulation.

Figure 4.6: Substrate mode EM simulation and effects.

substrate vias, therefore the calculation of the mode indices was straightforward. In our case through-substrate vias are used in order to adequately ground the substrate near the active components and signal transmission lines. However, due to the low density of the through-substrate vias, resonant modes could be sustained in the space between, as indicated by HFSS E/M simulations. A through transmission line with accurate TSV and slot model was created and simulated. The results have verified that the large gain variation observed in our SSDA design corresponds to resonant modes at 160 GHz and 190 GHz, which is reflected in the S22 (dB) plot in Fig. 4.6b.

4.3.2 Matrix-SSDA

Since the basic cell topology of the SSDA was used in order to implement the M-SSDA (see Fig. 11 in Paper B), it was expected to be more severely affected by substrate resonant modes due to the much larger chip area, in addition to the existence of large slots for the C_{BLOCK} capacitors marked as structure 1 in Fig. 4.7. The 3-dimensional view of the structures 1 and 2 is shown in Fig. 4.8, which includes the transmission lines feeding in the capacitor as well as the transmission lines in between the cascoded DHBTs. Significant cross-talk is expected between the two C_{BLOCK} capacitors through the substrate, which has been explored in [52].

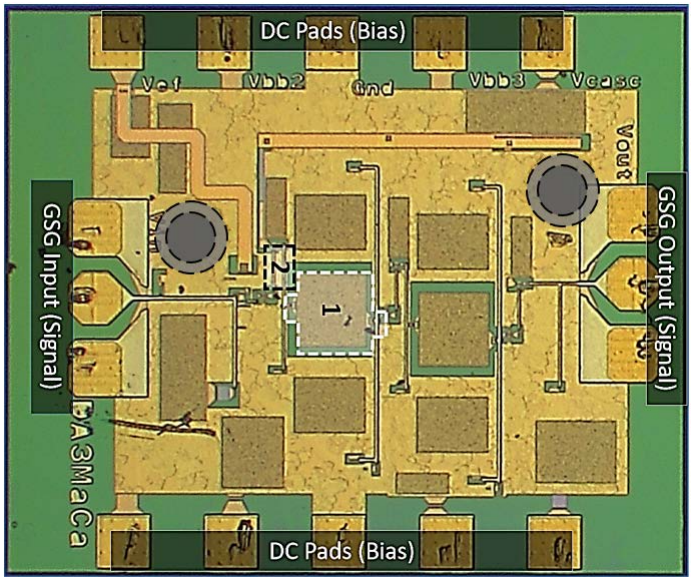


Figure 4.7: Microphoto of the M-SSDA. Region 1 (enclosed by white dashed lines) marks the location of the inter-stage capacitor C_{BLOCK} between tier 1 and tier 2, and the associated vias and metal connections; region 2 (enclosed by black dashed lines) marks the location of peaking inductances L_{ce} and L_{cc}. Dashed circles indicate location of through-substrate vias.

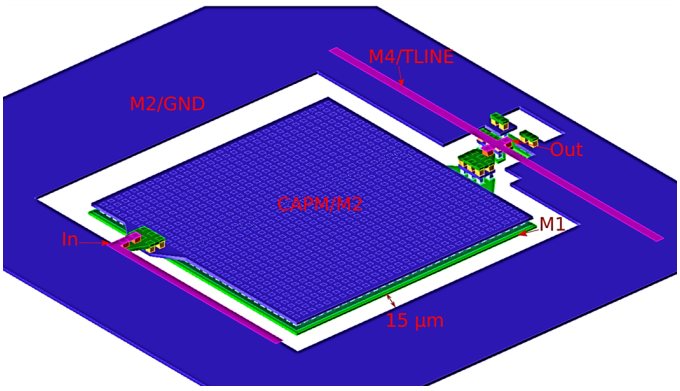
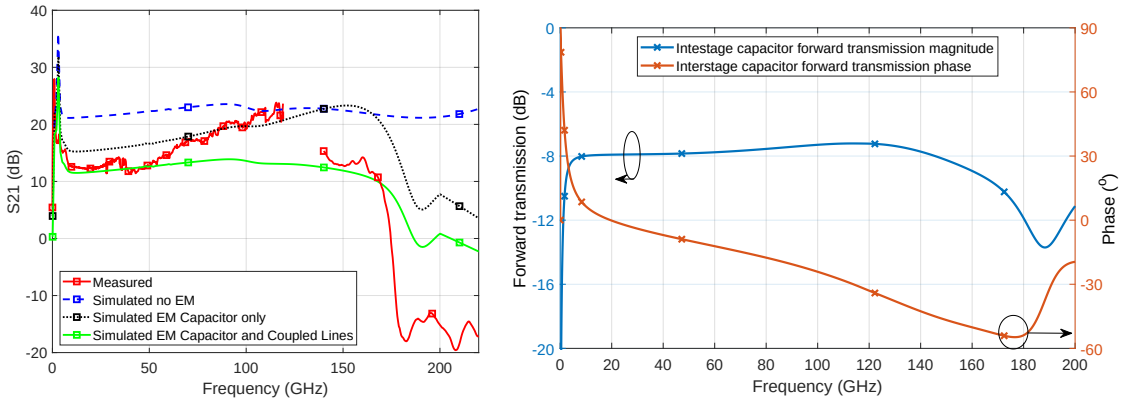


Figure 4.8: Structure and interconnects of the inter-stage ac-coupling capacitors together with the input and output matching transmission lines, used in the E/M simulations.



(a) Bandwidth- and gain-limiting effect of inter-stage capacitors and transmission line coupling.

(b) Forward transmission simulation of inter-stage Capacitor.

Figure 4.9: Results of E/M simulation.

E/M simulations of the cross-talk between the capacitor structures show a cross-talk of approximately -14 dB at 80 GHz that peaks at around -7 dB at 110 GHz, which accounts for the gain variation seen in the S21. The inclusion of the E/M simulated structure models affects the bandwidth of the DA as shown in Fig. 4.9a.

A significant factor is the self resonant frequency of capacitor C_{BLOCK}. According to E/M simulations of the forward transmission of the capacitor structure (shown in Fig. 4.9b) the capacitor introduces significant losses on the signal, and limits the bandwidth at around 170 GHz. Thus, future improvements in the low frequency coupling between the matrix stages, would require alternative techniques or significant improvements on MIM capacitor fabrication.

Chapter 5

Wideband Optical Receivers

In this chapter, we discuss the basic building blocks of a broadband electronic fiber-optical receiver system. We begin with a review of the most prominent receiver front-ends and complete receiver systems in literature, broken down the semiconductor technology used and rated in regards of power consumption and bitrate. Then we analyze the basics for the transimpedance amplifier and present our contribution to the field.

5.1 Literature review on receiver systems

In order to establish the current state of the field, a thorough but not exhaustive literature review was performed; the results are presented in Fig. 5.1. The focus of the review was on fiber-optical interconnect receiver systems and receiver system blocks, and they were evaluated in terms of two important performance metrics: power consumption and bitrate. The combination of those two values provides the figure of merit for such systems: the energy efficiency, as defined in the previous chapters. The reviewed works were classified based on the technology used in order to further illustrated the pros and cons of each technology.

Several trends are clearly visible in Fig. 5.1. Silicon-based CMOS systems offer the lowest power consumption but fall behind in terms of bitrate. The highest-performing CMOS-based receiver is designed and fabricated in deep sub-micron state-of-the-art FinFET technology [30], in order to benefit from high unity-gain frequency. However, some of the most prominent designs are achieved with more conventional 65 nm CMOS [66, 72], 90 nm CMOS [58] and even 180 nm CMOS [57]. The main benefit of CMOS-based processes, aside from their compatibility with the contemporary switching and network equipment, is the high degree of integration and digital logic that can be implemented monolithically. Therefore, most CMOS-based systems also include a variety of additional subsystems: bias-generation blocks, DC-offset cancellation, automatic feedback/gain control, digital equalization etc. Those subsystems are non-trivial to realise in HBT-only technologies.

Systems designed in InP processes typically are the most power-consuming, but also provide some of the highest bit- and baud-rate receivers. Due to their high

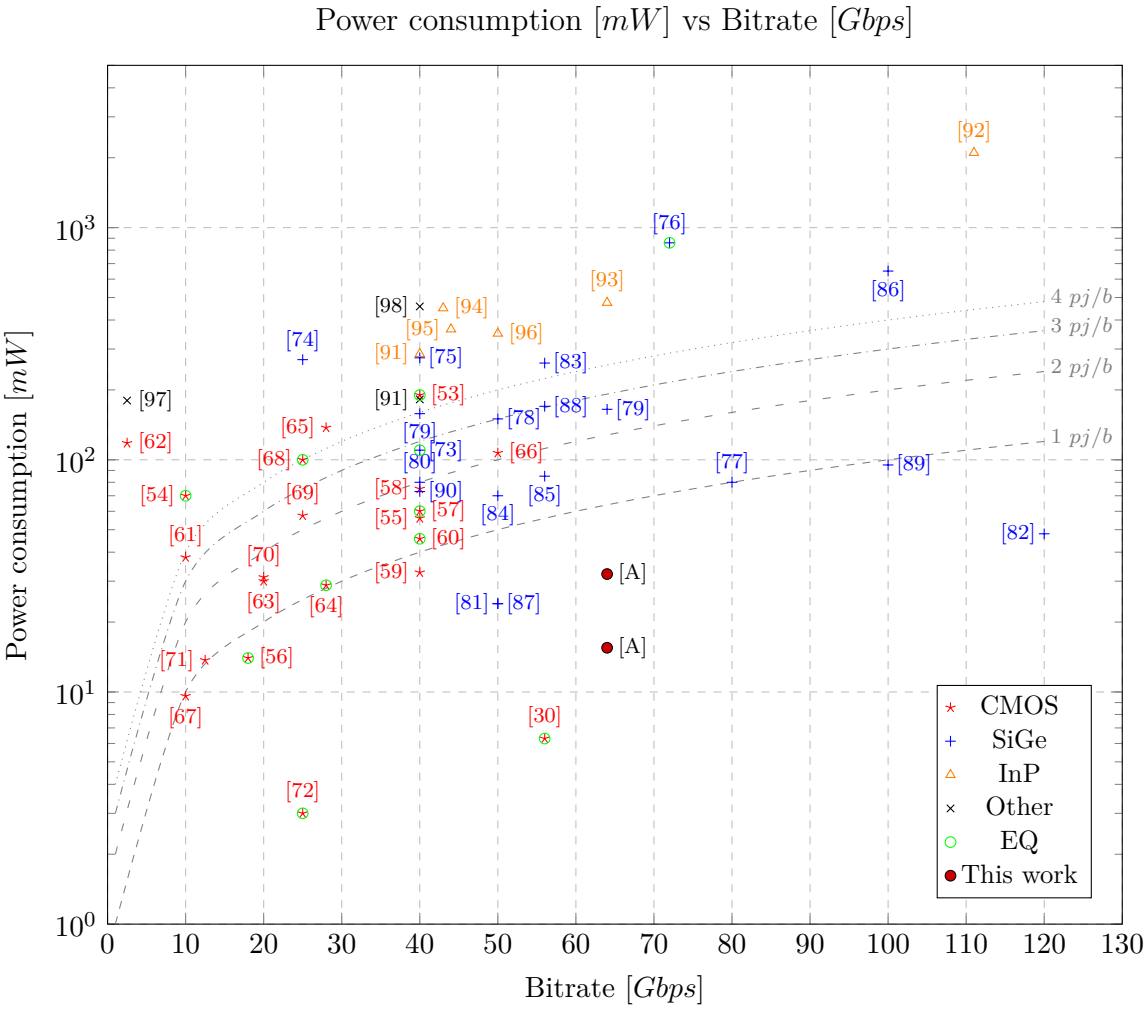


Figure 5.1: Prominent receiver system publications based on reported measured bitrate and power consumption.

gain and very high f_t and f_{max}, InP based systems have demonstrated the highest performing TIA-Demultiplexer system [92]. It is evident however, that the power consumption, and consequently the energy efficiency of such systems is relatively low.

SiGe-based systems fall in the middle between the two aforementioned technologies. This is partly due to the increased frequency of operation compared to Si-CMOS. Additionally, most SiGe technologies offer high-performing HBTs built on top of an existing and mature CMOS process with high-density metal system. In that way, the SiGe BiCMOS processes get the best of both worlds: high CMOS integration for digital control blocks, and higher f_t and f_{max} due to the high-speed HBTs provided. One of the limitations of SiGe processes is that they have not achieved the maturity and miniaturization that silicon-based CMOS have. During the later half of this decade, several state-of-the-art receivers have been published [76, 79, 85, 89, 90], demonstrating the growing maturity of SiGe-based processes.

State-of-the-art systems until 2015 used OOK to achieve competitive results [76, 90], with the exception of CMOS based designs. After that point in time however, higher modulation schemes became more prominent (PAM-4, duo-binary, PAM-8) even on the faster SiGe and InP based processes [79, 86].

As discussed in the previous chapters, the optoelectronic components used in short-haul optical communication links have typically modulation bandwidths in the range of 25 GHz - 30 GHz. Therefore the electronic circuits must employ an array of bandwidth extension or equalization methods in order to receive 50+ Gbps datarates. The most common bandwidth extension methods used are: inductive peaking [89], staggered gain peaking [90], continuous-time linear equalization (CTLE) [99], and decision-feedback equalization (DFE) [100].

In long-haul optical communication links however, and in wireless optical links, the photodetectors used are mainly limited by their parasitic capacitance. In those cases, a TIA with low input impedance is preferable as it can extend the bandwidth of operation. The case for such an application becomes more appealing since most wave-guide photodetectors are integrated on InP substrates, which are compatible with the InP DHBT process used in this work.

5.2 TIA

The transimpedance amplifier (TIA) is a core component to any system that amplifies current with low input impedance. This is important for fiber-optical communications in the receiver design, where a photodetector converts incident light into a small photocurrent. That photocurrent (in the order of a few hundred μA) is in turn converted into a voltage by the TIA. The voltage output of the TIA is in the order of a few mV and requires further amplification to be quantized and converted into digital-logic values.

The main figure of merit for a current-to-voltage amplifier is the transimpedance gain which is typically given as V_{out}/I_{in} or Ω of transimpedance, or dBΩ through equation 5.1.

$$A_{TI}[\text{dB}\Omega] = 20 \times \log(\frac{V_{out}}{I_{in}}) \tag{5.1}$$

Noise is a very important measure of TIA performance. Since TIAs are used as the first stage of the receiver system, they are the main contributors of the system's entire noise performance. The noise of the TIA is given as a noise spectrum, which by integrating over the bandwidth and dividing by the TIA gain at the mid-band point R_{TIA}, gives us the input-referred rms noise current ($i^{rms}_{n,TIA}$) as seen in equation 5.2 [101].

$$i^{rms}_{n,TIA} = \frac{1}{|R_{TIA}|}\sqrt{\int_0^\infty |Z_{TIA}(f)|^2 \times I^2_{n,TIA}(f)df} \tag{5.2}$$

Where $Z_{TIA}(f)$ is the frequency response of the TIA, and $i^2_{n,TIA}(f)$ is the output-referred noise spectrum of the TIA.

While gain and noise are important for receiver circuits, power consumption is always relevant in any circuit design. As mentioned in Chapter 2.3, there is an evident need to maintain as high energy efficiency as possible.

An additional limitation in TIA design is the maximum optical current that can be tolerated (I_{max}). This is the maximum current that the TIA input stage can tolerate before going into compression, which would affect the jitter and bit error rate (BER). In order to optimize the design for I_{max} we can find the maximum photocurrent that the given PD can generate. This is limited by the maximum optical power that the PD can receive multiplied by its responsivity as shown in equation 2.1. Additionally, the receiver's sensitivity is defined by the ability to detect very small currents, which is in turn limited by noise. The smallest detectable current typically is orders of magnitude smaller than the I_{max}, therefore the receiver needs to have a very large dynamic range.

Bandwidth is the frequency range at which the amplifier provides adequate amplification and is defined up to the frequency where the gain of the receiver drops by 3 dB. In TIA and receiver design, there are several bandwidth-limiting factors. The photodetector capacitance seems to be an important limitation in state of the art technology. The intrinsic junction capacitance is on the order of 20–100 fF for the 30 GHz bandwidth photodetectors [10]. That parasitic capacitance is also approaching the value of the bond-pad capacitance which is typically $\approx$ 10–60 fF on either side of the wire-bond. Additionally, depending on the topology of the first amplification stage, the TIA input capacitance must also be taken into account. The total capacitance of the PD (including the parasitic and pad capacitances), the TIA input impedance, and the feedback resistor (if any) define the frequency performance of the system in terms of an R-C response as shown in equation 5.3.

$$BW_{PD-TIA} = \frac{1}{2\pi R_{in}(C_{PD} + C_{TIA})} \tag{5.3}$$

By reducing the input resistance of the TIA (R_{in}), we can improve the receiver bandwidth [31, 102]. However, the noise of the system would increase proportionally. Therefore, while designing for very low input impedance is beneficial for bandwidth-limited systems, it will affect the noise performance. Additionally, any stage after the input stage affects the total Gain-Bandwidth product of the system and typically extra measures are taken in order to keep a large bandwidth together with adequate gain. It is natural that the performance is also limited by the transit or current gain unity frequency (f_t), and the maximum frequency of oscillation (f_{max}) of the transistors in any given process.

A figure of merit seen in equation 5.4, as given by Voinigescu [101], combines most of the aforementioned design goals of a broadband transimpedance amplifier:

$$FoM = \frac{Z_{TIA} \times I_{max} \times BW_{3dB}}{i_{n,TIA}^{rms} \times P_{DC}} \tag{5.4}$$

Another consideration in addition to the bandwidth and gain of the amplifier is its linearity. In this context, linearity refers to the transient behavior of the TIA

in respect to gain compression; sufficient linearity can be achieved by biasing the amplifier within its linear region of operation. If a TIA-PD receiver is meant to be used not only for OOK, but also PAM-4 modulation, a linear response is required in order for all three levels in an eye-diagram to be sufficiently open. In order to maintain linearity on the receiver system level, a typical design practice is to include a variable gain amplifier after the TIA stage in order to tune the overall TI-gain of the receiver. Additionally, the input stage of the TIA must have sufficiently high I_{max} as mentioned earlier. Alternatively, tunable feedback can be used on the TIA to adjust the transimpedance gain. Most TIAs in literature are linear and use gain tuning in order to adjust to different input signal amplitude scenarios. However OOK-optimized designs use limiting amplifiers, cascaded after the TIA stage in order to improve the eye opening and reduce the requirements on the analog-to-digital conversion and clock retrieval blocks [15].

5.3 133 GHz TIA front-ends in 130 nm InP

As mentioned in Chapter 2.2, PIN and APD photodetectors achieve limited bandwidth in the order of 30 GHz. However, long-haul optical communication receivers use waveguide photodetectors with 80+ GHz bandwidth, which are limited by the parasitic capacitance and loading impedance [19]. Similarly, one-sided junction photodiodes presented in [23] achieved more than 60 GHz bandwidth without considering the loading resistance of the TIA. Lastly, PIN traveling wave photodetectors integrated on InP substrate, with bandwidth larger than 120 GHz were proposed, with extensive steps made in order to improve the output matching to 50 Ω [22].

Since all of the above photodetectors are limited by the bandwidth and loading of the electronics, new TIA circuits that take advantage of that were designed. The prime design directive was to reduce the loading of the photodetectors and extending the overal receiver bandwidth.

In Paper A, we present the design and fabrication of two receiver front-end circuits using TSC 130 nm InP DHBT process [36]. The process boasts an f_t and f_{max} of 520 GHz and 1.15 THz respectively. The process Back End Of Line (BEOL) includes thin-film resistors, Metal Insulator Metal (MIM) capacitors and three gold interconnect metal layers and a top bond-pad metallization. A cross-section of the technology can be seen in Fig. 5.2.

5.3.1 Process enabled trade-offs

As seen in 3.2.3 the β of an 130 nm InP process is quite low which in turn voids the assumptions made in that chapter. Additionally, the g_m is saturated quite quickly for smaller devices. However by increasing the transistor area we can decrease the current density to the same current level, and consequently get a higher g_m which would give lower input resistance in a CB-stage. A larger device however has more parasitics, therefore lower bandwidth. In order to chose the device size for a CB TIA

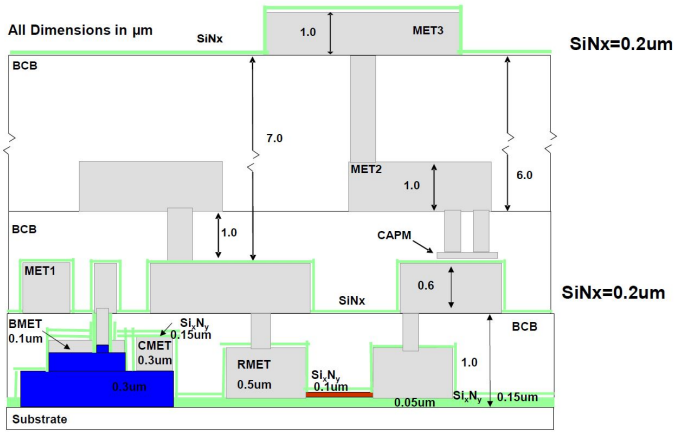


Figure 5.2: Cross-section of the 130 nm InP DHBT process.

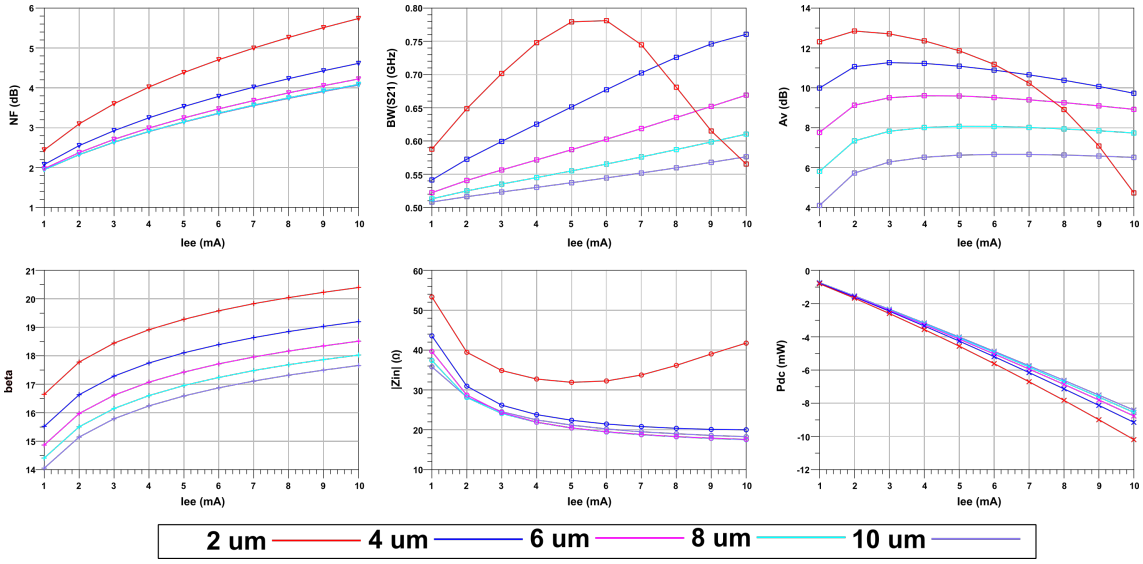
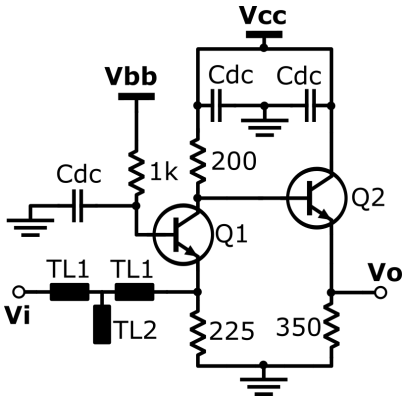


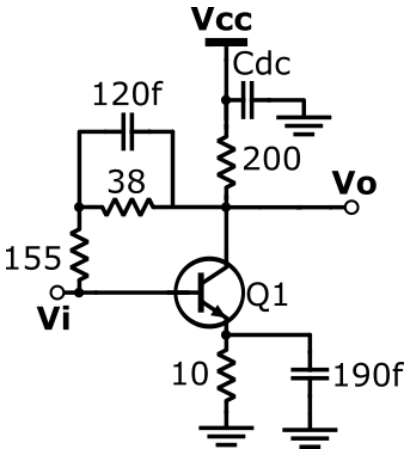
Figure 5.3: Ideal CB amplifier parameters for various emitter sizes as a function of emitter current.

the design space of the possible device sizes was explored as a function of emitter current. The resulting trade-offs are seen in Fig. 5.3.

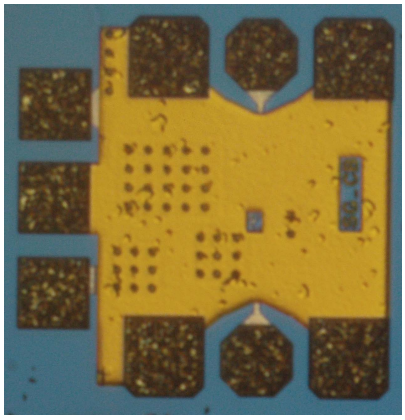
The main outcomes of this examination are that a smaller device has significant benefits including: higher β, higher bandwidth, higher dc gain (Av), and it will consume the least power. The drawbacks of such a device are a substantially increased noise figure (NF) and a higher input impedance. In order to achieve the highest bandwidth and gain, the smallest device was selected for the CB stage.



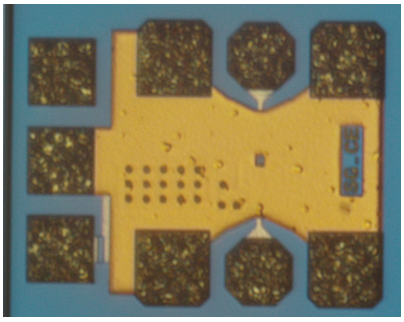
(a) Schematics of the CB TIA.



(b) Schematics of the CE TIA.



(c) Micrograph of the CB TIA.



(d) Micrograph of the CE TIA.

Figure 5.4: Schematics and micrographs of the two TIA MMICs.

5.3.2 Circuit design

In order to avoid loading the CB stage a CC stage was used at the output in order to isolate the 50 Ohm output from the resistor R_c (Fig. 5.4a). While a CC would ideally not load the CB stage in normal circumstances, that is not true for a low-β process, therefore an amount of loading was expected. In addition to the CB TIA stage, a more traditional CE with shunt-shunt feedback TIA was also designed as a comparison (Fig. 5.4b). The CE was designed for the same bandwidth as the CB TIA and for similar total power consumption. The designed CB and CE MMICs can be seen in Fig. 5.4c and Fig. 5.4d respectively. The two MMICs were reported in Paper A.

A measurement campaign including frequency and time domain characterization was carried out. The frequency domain results of the two TIAs are presented in Paper A. Both measured devices showed good matching with the simulation, had more than 133 GHz bandwidth, minimal group delay variation and more than 42 dBΩ TI gain.

Electrical time domain measurements carried out up to 64 Gbps provided eye

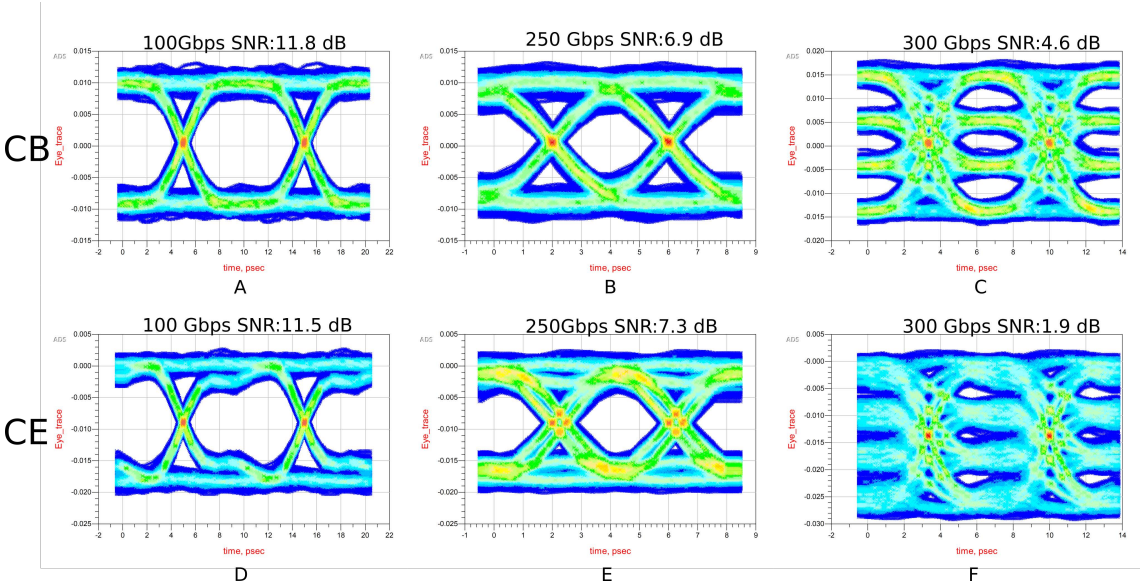


Figure 5.5: Simulated electrical time domain eye diagrams for the two TIAs.

Table 5.1: Test scenarios for the TIA-PD simulations.

Scenario	**BR (Gbps)**	f_t **(GHz)**	C_{pd} **(fF)**
T1	50	40	250
T2	100	40	30
T3	50	150	50

diagram and noise histogram measurements for the two TIAs (as seen in Paper A). The two TIAs had a measured averaged input-referred noise current density of 30.2 $pA/\sqrt{Hz}$ for the CB and 13.9 $pA/\sqrt{Hz}$ for the CE. The energy efficiency of the two circuits at 64 Gbps was 0.5 pJ/bit for the CB and 0.4 pJ/bit for the CE. Since there was no possibility to perform time domain measurements with datarates higher than 64 Gbps an extended simulation campaign was carried out in order to evaluate the highest possible performance of the TIAs. Eye diagram simulations $>$ 100 Gbps were done to complement the measured eye diagrams. The high data-rate eye diagram simulation results can be seen in Fig. 5.5. The simulations indicate that both TIAs can be used for $>$ 250 Gbps OOK communication, and the CB could also be used for 150 Gsps PAM-4 for a total of $>$ 300 Gbps, albeit with a limited SNR. The energy efficiency of the TIAs therefore is adjusted to 0.13 pJ/bit for the CB and 0.10 pJ/bit for the CE while maintaining an SNR 6 dB.

5.3.3 Optical link simulations

Furthermore, in order to explore the interactions between the TIA and a potential PD an optical link simulation was done. In 5.1 we present the three PD scenarios that were considered for the optical simulation. In scenario T1 we consider a PD which is limited by both transit time and high parasitic capacitance, which is typically

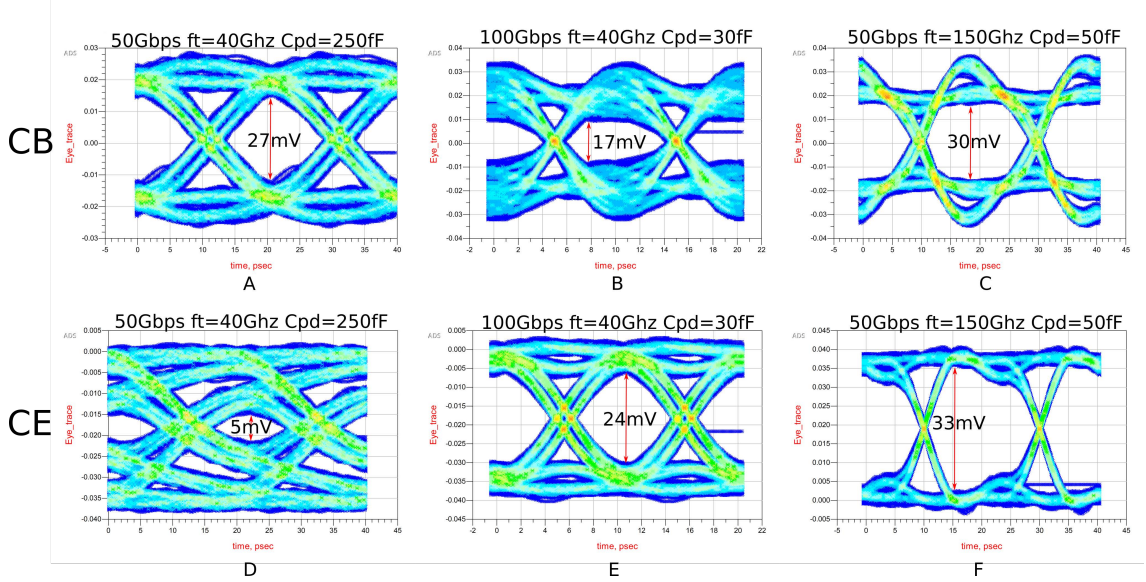


Figure 5.6: Simulated optical time domain eye diagrams for the two TIAs for three photodiode scenarios.

used in free space optical communication links [103]. In scenario T2, a photodetector that is limited by transit time, such as the one discussed earlier [10]. In scenario T3, we consider a photodetector that is not limited by transit time, but is somewhat limited by the parasitic capacitance, corresponding to a wave-guide photodetector [19]. The results of the simulated optical eye diagrams can be seen in Fig. 5.6. As expected the CB TIA performs significantly better than the CE on heavily bandwidth limited photodetectors in T1; in T2 the CB eyes are closed due to its inductive input reactance, which causes ripple; in T3 the CB and CE perform equally well.

An additional investigation on the frequency response in terms of transimpedance gain (including the PD responsivity of 0.4 A/W) and input impedance is presented in Fig. 5.7. The plots were extracted with the photodetector of T1 connected to the CB TIA, CE TIA and a 50 Ω load. When compared to the 9 GHz bandwidth of the PD, the CB TIA extends the bandwidth to 31.5 GHz, and the CE TIA extends the bandwidth to 15.5 GHz. The bandwidth extension is partly due to the inductive input reactance of the CB (as discussed in 3.1.1) and partly due to the lower resistance seen by the PD capacitance.

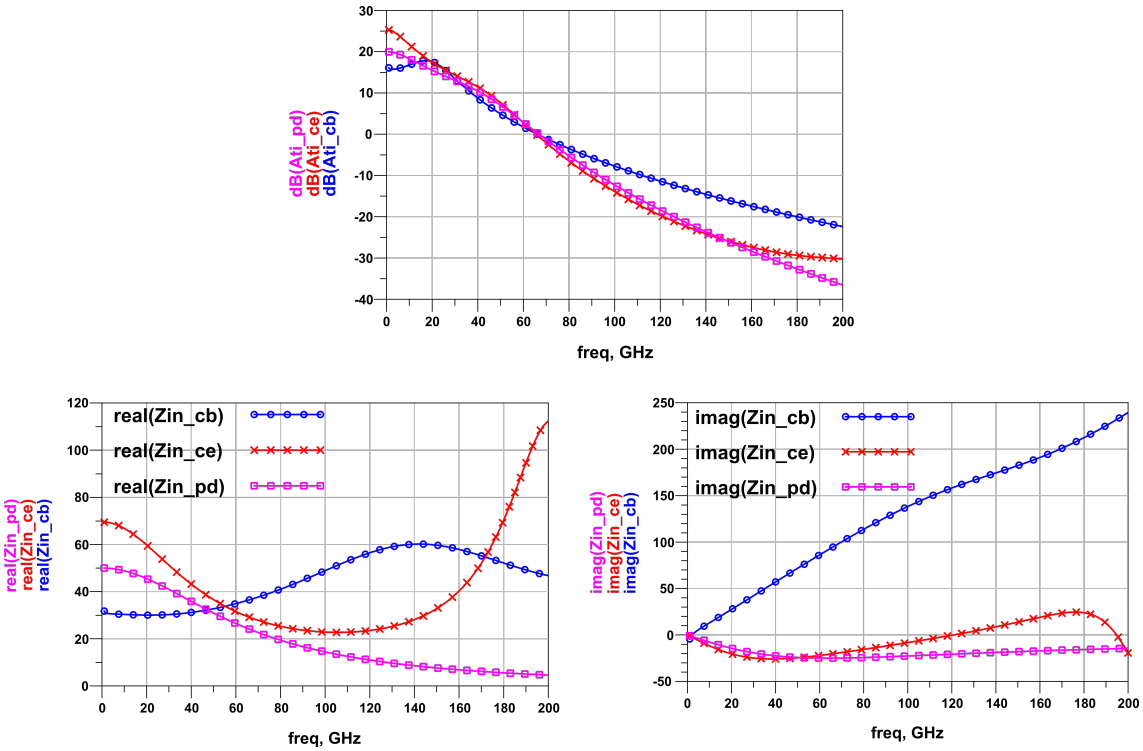


Figure 5.7: Simulated Ti-bandwidth and input impedance of the scenario T1 PD, connected to the CB, CE or a 50 Ohm load.

5.4 Bandwidth Enhancement and Equalization

As mentioned earlier in this Chapter, a significant portion of the relevant research utilizes some form of bandwidth extension or equalization. There are several techniques to increase the bandwidth of a TIA, however each one has a trade-off. The most common way to extend the bandwidth of a TIA, and maintain a low input impedance is to use feedback. The most common type of feedback used is negative shunt-shunt feedback, comprising of a simple resistor between the output and the input of the TIA. Inductive feedback is also used to achieve peaking and improve the total bandwidth [82]. However, large inductors (in the order of a few nH) are bulky and do not work for very high frequencies, due to their self-resonance, thus are avoided in monolithic microwave integrated circuit (MMIC) design.

Inductive peaking and capacitive degeneration are two very common ways to extend the bandwidth of an amplifier stage. In the former case the inductor connected in series with the load of the amplifier increases the load impedance at a certain frequency based on the inductance, subsequently increasing the overall gain of the amplifier (peaking) around that frequency [60]. Capacitive degeneration is most commonly used with CE and differential CE amplifiers in combination with resistive degeneration. The resistive degeneration reduces the amplifier gain, thus expanding the bandwidth; while the capacitive feedback peaks the gain (bypassing the resistor) at a certain frequency close to the 3 dB cut-off region. Additionally, series inductors at the input and sometimes at the output of the receiver are used to improve the matching [104].

Another method of improving bandwidth is by cascading many small-gain, high-bandwidth amplification stages after the TIA but at the expense of energy efficiency and chip area. Those amplification stages can utilize peaking at higher frequencies in order to compensate for the drop of gain in the main TIA stage. An additional benefit becomes apparent if those stages have tunable gain or tunable

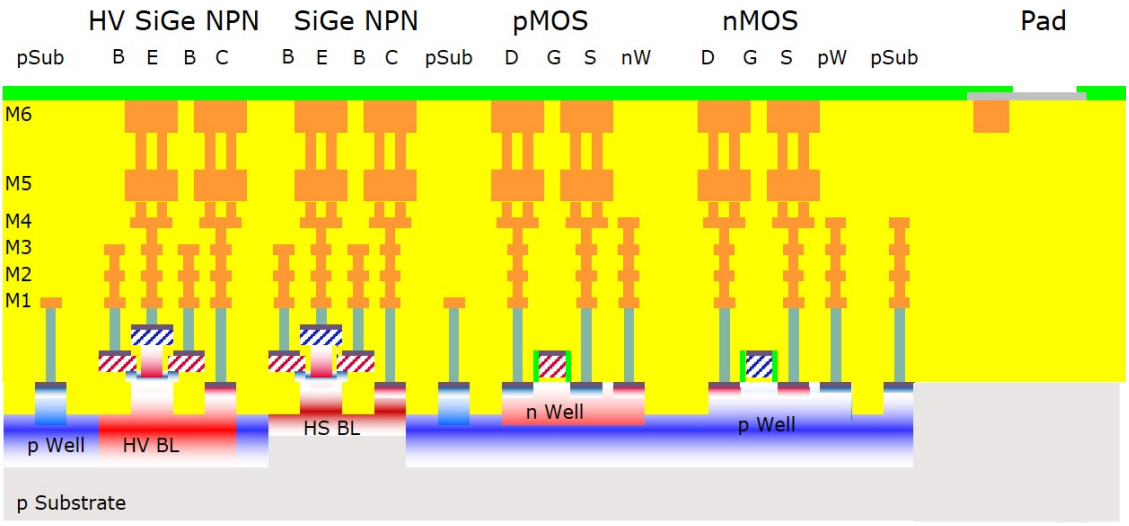


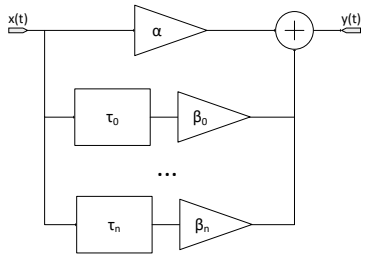
Figure 5.8: Cross-section of the 130 nm SiGe HBT process by Infineon.

frequency of peaking, in which case the overall bandwidth response of the receiver can be controlled and adapted on demand.

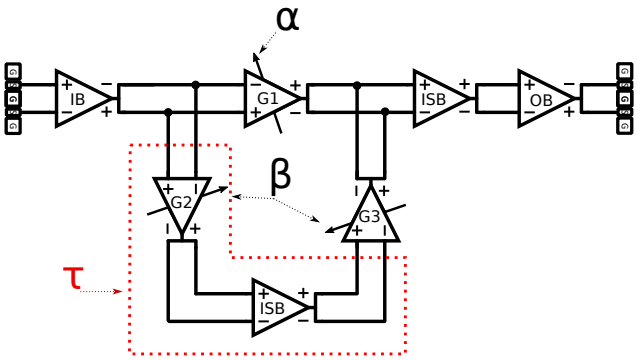
Lastly, dedicated equalization circuitry can be used after the TIA stage similar to what is typically used in cable and backplane equalization systems [105].

5.4.1 Modular FFE Equalizer in 130 nm SiGe

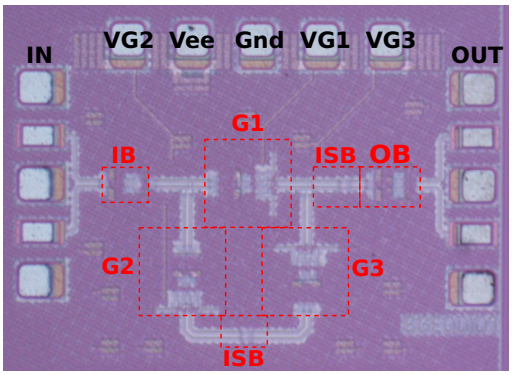
In this as yet unpublished work, we present the design and fabrication a differential, feed-forward equalizer (FFE) with adjustable equalization and modular implementation. The design is suitable for receiver or transmitter equalization and was intended as a demonstrator module, with intentions to integrate with the TIA designed in Paper [Oa]. It was designed using Infineon's 130 nm SiGe BiCMOS process [25]. The fully commercial process uses SiGe HBTs with f_t and f_{max} of 250 GHz and 370 GHz respectively, coupled with a fully developed CMOS process. The process BEOL offers 4 interconnect metal layers, 2 thick copper RF metals and aluminum bond-pad metallization. A cross-section of the technology can be seen in Fig. 5.8.



(a) Block diagram of FFE topology.



(b) Top schematic of the designed equalizer.



(c) Chip micrograph of the designed equalizer MMIC.

Figure 5.9: Implementation of the FFE Equalizer from block diagram to MMIC.

5.4.2 IC design

One of the most common ways to design an equalizer is to use feed-forward equalization. The block diagram of a typical FFE system with n-taps is shown in Fig. 5.9a. The principle of FFE is that the input signal $x(t)$ is delayed by a time τ and amplified by β_n for each tap, then all the tap outputs are summed with the original signal which was amplified by α to give us the equalized signal $y(t)$. The analytical description of the output signal $y(t)$ for an n-tap equalizer is described in Eq. 5.5.

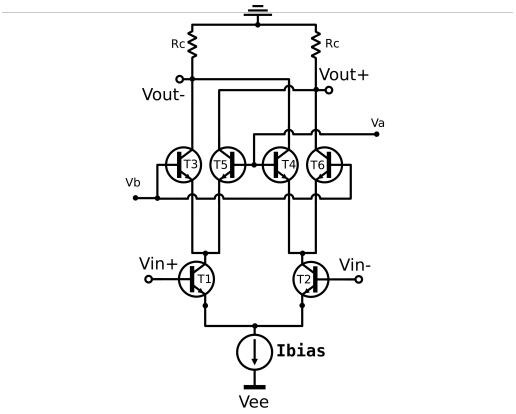
$$y(t) = \alpha \cdot x(t) + \beta_0 \cdot x(t - \tau_0) + \cdots + \beta_n \cdot x(t - \tau_n) \tag{5.5}$$

The tap delays τ_n and the tap gain coefficients β_n are the equalizer coefficients that define the response of the equalizer. The proposed 1-tap FFE is based in an earlier implementation presented in [106]. The block diagram of the proposed equalizer is shown in Fig. 5.9b. The coefficients α and β are represented by the gain of three identical gain cells: G1 provides the forward path gain, G2 and G3 provide the tap gain. All three gain cells are implemented as tunable Gilbert cell amplifiers. The delay τ is not tunable in this implementation, rather it includes the delay of cell G2 and inter-stage buffer (ISB) between G2 and G3, as well as the added delay of the transmission lines present in the delayed path as shown in Eq. 5.6. The transmission line delay is insignificant in the frequency range of interest, so the dominating factor comes from the time delay introduced by the two cells G2 and ISB.

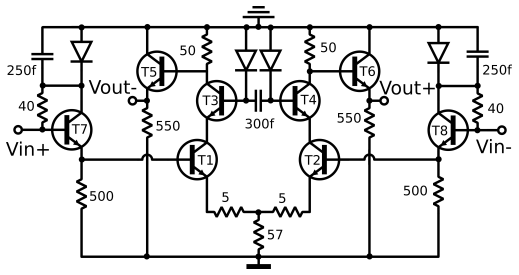
$$\tau = \tau_{G2} + \tau_{ISB} + \tau_{TL} \tag{5.6}$$

The main gain cell of the proposed equalizer is a Gilbert cell as opposed to a conventional differential common emitter (CE) amplifier cell. In a differential CE gain cell the gain control is achieved through tuning the tail current of the CE-pair. While this implementation is very simple and elegant, it also implies that the current and subsequently the power consumption of each gain cell increases as the gain increases. That leads to higher power consumption at higher gain. Additionally, as mentioned in Chapter 3, HBTs have their optimum f_t at a specific current density, so the CE-pair bias current cannot deviate much from the optimum current without affecting the bandwidth of the amplifier. The most significant drawback is that due to the increased current through the collector resistor R_c, the dc voltage at the collector of the CE-pair changes accordingly, which affects the dc-biasing of the subsequent stage or gain cell. While differential CE amplifiers are very robust in regards to drifts of the dc-bias, large drifts limit the dynamic range of following stages and of the whole equalizer in regards to tunability.

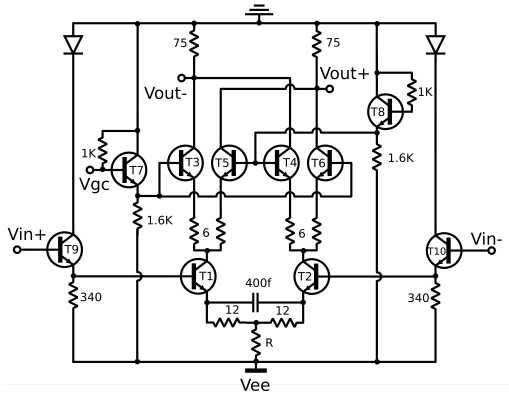
In contrast, in a simple Gilbert cell, (as shown in Fig. 5.10a) the gain control is achieved via the difference between voltages V_a and V_b and the sign of their difference controls whether the amplifier is inverting or not. At the same time, the current I_{bias} and the current through the two R_c resistors remains the same at all bias control settings. With that advantage in mind, we can essentially replicate the gain cell for all taps without having to optimize the biasing, making the topology reusable. Furthermore, since the current remains constant throughout the gain tuning range,



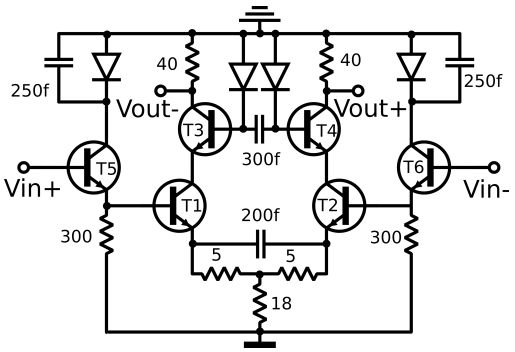
(a) Basic implementation of a Gilbert Cell.



(b) Schematic of the 50 Ω Input buffer.



(c) Schematic of Gilbert variable gain cell.



(d) Schematic of the 50 Ω Output buffer.

Figure 5.10: Circuit schematics of the a typical Gilbert cell, input buffer, variable gain cell, and output buffer.

the bandwidth remains unchanged as well and the common mode voltage at the collector remains constant at different gain settings. The main drawbacks of using Gilbert gain cells are the larger number of transistor devices which increases both the complexity and the area. In addition to that, a more complex biasing network is required to support the Gilbert gain cells which leads to an increase in power consumption compared to the CE topology.

As shown in Fig. 5.9c, the equalizer consists of six discrete blocks. An input buffer (IB), shown in Fig. 5.10b, that provides matching to 100 Ω differential input and includes a differential cascode amplifier that contributes with a gain of 6 dB in order to offset the signal splitting in the two paths. The cascode amplifier uses 50 Ω resistors as loads to maintain wide bandwidth. Two inter-stage buffers (ISB) that consist of a single emitter follower stage provide isolation and dc level shift between the gain cells. The design includes also a differential cascode output buffer (seen in Fig. 5.10d) which uses 40 Ω resistors as loads which in addition to the output transmission lines provide output matching to the 50 Ω measurement environment. The output cascode amplifier utilizes two 5 Ω resistors and a 200 fF capacitor as

degeneration in order to compensate for the high frequency gain roll-off and to maintain the equalized signal.

Three variable gain Gilbert cells (G1, G2, and G3) shown in Fig. 5.10c control the tap coefficients. Each gain cell includes its biasing network and emitter follower input buffers. Transistors T_4 and T_5 are biased via transistor T_8 and provide the base gain of the cell through 75 Ω resistors. The gain control is achieved via the voltage V_{gc} which turns the transistors T_3 and T_6 on or off, canceling the gain at nodes V_{out+} and V_{out-}. At the collectors of T_1 and T_2, 6 Ω degeneration resistors are used in order to improve the linearity of the gain control. The voltage V_{gc} can be tuned between 0 V and −0.25 V in order to control the gain; when V_{gc} is set to 0 V then T_3 and T_6 are biased at the same level as T_4 and T_5 effectively canceling the gain at the output; when V_{gc} is set to −0.25 V, T_3 and T_6 are turned off, allowing the maximum current through T_4 and T_5, thus providing the maximum gain. The cells use 12 Ω degeneration resistors and a 200 fF peaking capacitor at the emitters of T_1 and T_2 in order to provide a measure of peaking to offset bandwidth losses.

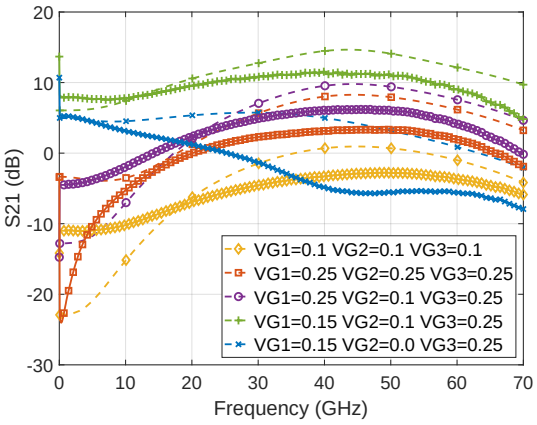
5.4.3 Frequency characterization

The equalizer chip was characterized in the 10 MHz to 70 GHz band on a VectorStar ME7838A series broadband vector network analyzer (VNA) by Anritsu via 75 μm 145 GHz Infinity probes. Due to equipment limitations the equalizer was measured on single- ended configuration. The three control voltages: VG1, VG2 and VG3 (corresponding to the Vgc voltages of cells G1, G2 and G3 respectively) were adjusted in order to obtain various equalization settings. Additionally, the power of the input signal was varied between −25 dBm to −10 dBm in order to extrapolate the 1-dB power compression point of the equalizer for various frequency points.

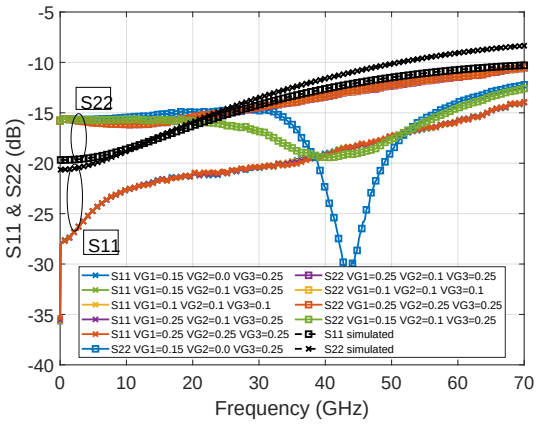
The S-parameter measurement results are shown in Fig. 5.11a; the peaking control of the device is demonstrated for various equalization settings, achieving a maximum of 27 dB of single-ended peaking and a bandwidth higher than 70 GHz on the minimum peaking setting. Since there are 3 possible control voltages, the possibilities for equalization can accommodate for a wide range of channel responses. In Fig. 5.11b the S11 and S22 parameters of the equalizer are shown, where is evident that the broadband matching input and output buffers maintain good matching throughout the bandwidth, despite the gain variations. The group delay variation for the same settings is presented in Fig. 5.11c where we can see close matching between the simulated (dashed) and measured (solid with markers) response. The group delay variation is minimal for frequencies higher than 20 GHz. The results of the input power sweep between −25 dBm and −10 dBm are shown in Fig. 5.11d.

5.4.4 VCSEL receiver equalization

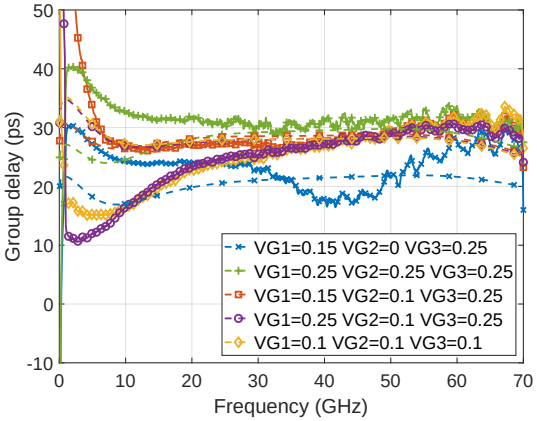
In order to evaluate the equalizer in a receiver equalization scenario, an experimental setup including a 1060 nm VCSEL, a variable optical attenuator and a commercial



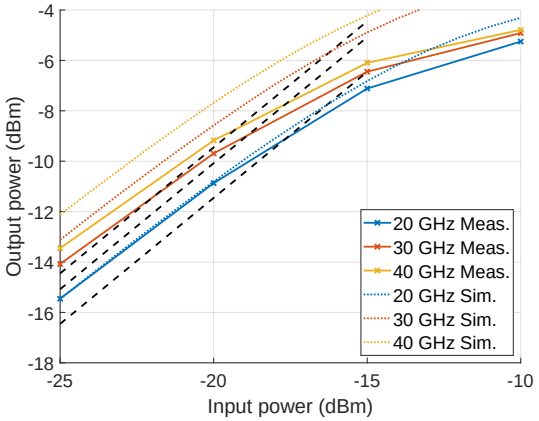
(a) S21 results vs simulation for various gain control settings.



(b) Input and output reflection for various gain control settings.



(c) Group delay variation for various gain control settings.

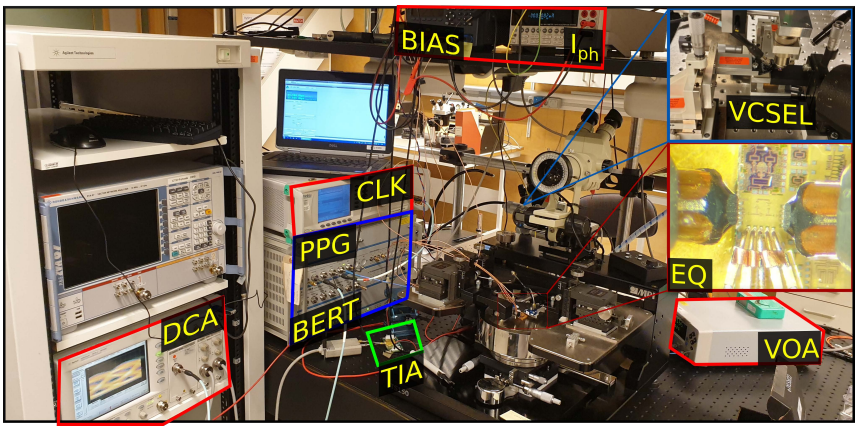


(d) 1dB compression curves for various frequencies.

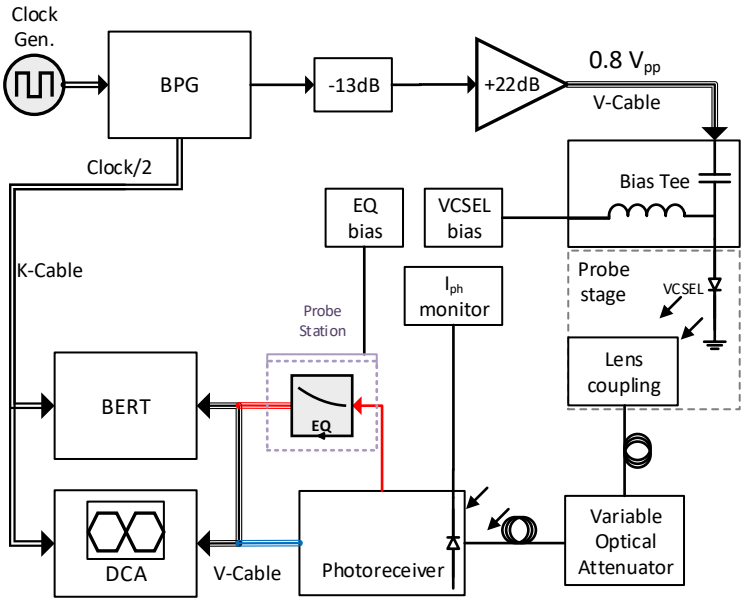
Figure 5.11: Frequency domain measurements of the equalizer MMIC. Tap coefficients VG1, VG2, and VG3 refer to negative voltages.

photo-receiver module was built. Eye diagram and bit error ratio (BER) measurements were carried out; then, without any changes in the setup, the output of the receiver was connected to the equalizer's input to measure the improvement in BER. The 1060 nm VCSEL has a 7 μm aperture and it is suitable for short- to medium-reach interconnects [107].

In Fig. 5.12, we show the test-bench which consists of 3 sub-assemblies : the signal generation setup, the optical setup, and the signal characterization setup. For the signal generation we used an HP 83712B CW clock generator to provide the clock signal to an SHF 12103A binary pattern generator (BPG) which generated the NRZ, PRBS-15 data-stream with 0.38 V_{pp} amplitude. Since a modulation signal larger than 0.6 V_{pp} was required to operate the VCSEL with adequate eye opening, an SHF 804TZ 22 dB broadband amplifier and a -13 dB attenuator were used to set the modulated signal to approximately 0.8 V_{pp}. The signal generated by the amplifier is fed through a 64 GHz bias tee to the probed 18 GHz 1060 nm VCSEL. The optical



(a) Experimental setup.

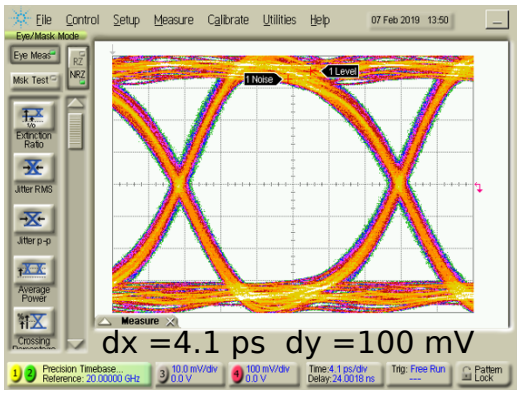


(b) Experimental setup schematics.

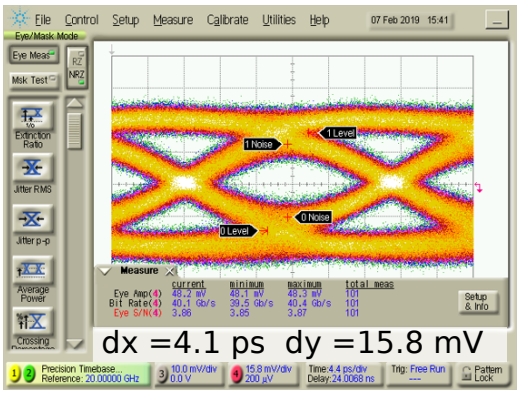
Figure 5.12: Experimental test bench used for the time domain optical measurements.

signal is captured through a lens coupling setup into a 1 m long multi-mode optical fiber; then an EXFO FVA-3150 variable optical attenuator (VOA) is used to adjust the optical power to avoid saturating or damaging the receiver. The optical signal is received by a Picometrix commercial 35 GHz photo-receiver with integrated TIA. The average optical power of the receiver is monitored via its photocurrent. The electrical signal of the TIA is then fed to either an Agilent Infinium DCA-J 86100C Digital communications analyzer for eye diagram inspection or to an SHF 11100B Bit Error Rate Tester (BERT) using V-band coaxial cables.

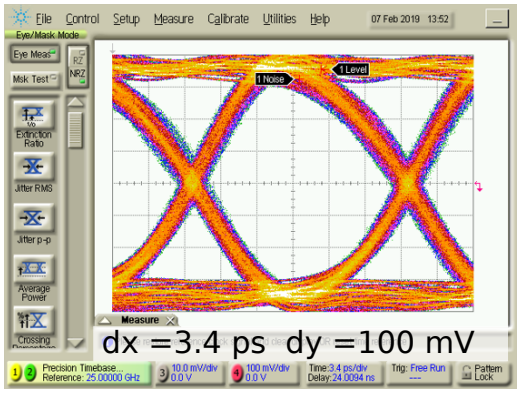
The electrical input and electrical output of the complete VCSEL-receiver



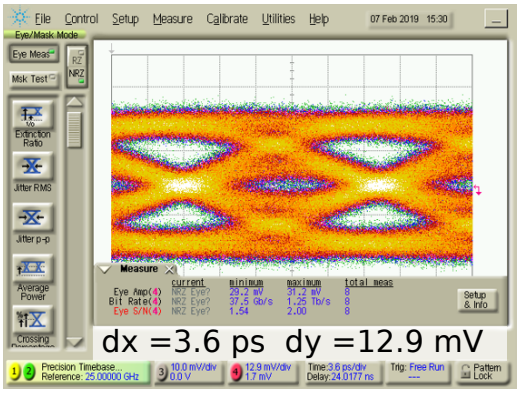
(a) VCSEL input at 40 Gbps.



(b) TIA output at 40 Gbps.



(c) Group delay variation for various gain control settings.



(d) VCSEL input at 50 Gbps.

Figure 5.13: Frequency domain measurements of the equalizer MMIC.

experimental setup is shown in Fig. 5.13 for two different bitrates. As evident from the figures, the vertical eye opening of the VCSEL-receiver test setup is reduced from 16 mV at 40 Gbps to practically 0 at 50 Gbps.

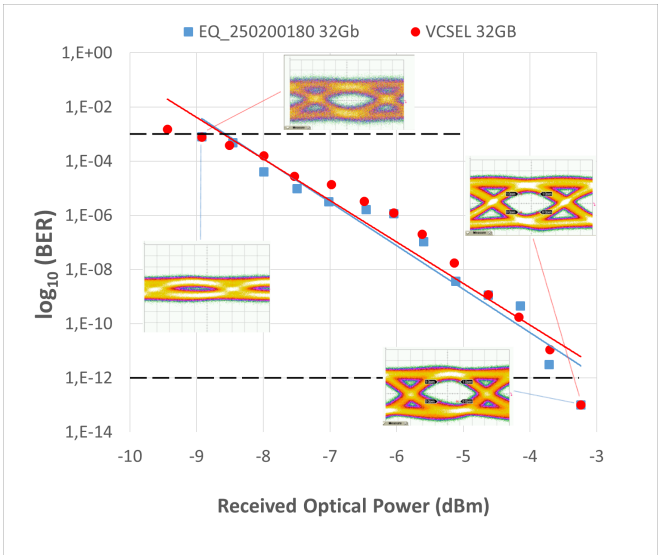
After inspecting the eye diagrams and optimizing the bias of the VCSEL at 11 mA and the attenuation of the optical signal at -3 dB to avoid saturating the receiver, we obtain eye diagram and BER measurements for the experimental setup by varying the optical attenuation and monitoring the photodiode current of the receiver to infer to the received optical power. We then proceed to repeat the BER measurements with the equalizer chip connected at the output of the receiver. The equalizer was probed and connected as single ended with the unused ports terminated to 50 Ω through 60 GHz dc-block adapters. Two equalization settings were optimized experimentally in order to produce the best possible eye diagrams: setting 250200180 which corresponds to $VG1 = -0.250$ V, $VG2 = -0.200$ V, and $VG3 = -0.180$ V; and setting 200115250 corresponding to $VG1 = -0.200$ V, $VG2 = -0.115$ V, and $VG3 = -0.250$ V.

The first experiment was carried out at 32 Gbps, where error free operation

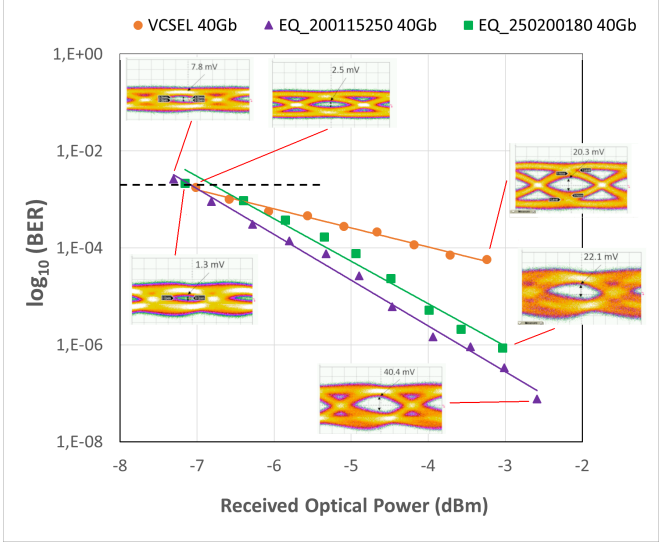
was achieved. As seen in Fig. 5.14a, there is only a slight improvement in the BER by using the equalizer. The second experiment was carried out at 40 Gbps. Two different equalization settings were used for significant improvements in the BER as shown in Fig. 5.14b. At the maximum optical power, the VCSEL-receiver test had a BER of 5.8E–5, and with the two different equalization settings the BER improved to 8.7E–7 and 3.38E–7, resulting in an improvement of more than two orders of magnitude. On the third experiment, the optical power was set to the maximum value of −3 dBm and the bitrate was increased. The starting value was 32 Gbps, where we observed error free operation with BER less than 1E–12. Similarly, the maximum bitrate when a BER of 1E–3 was reached, is presented. The results, found on Fig. 5.15, show a 6 Gbps increase on the maximum BR from 44 Gbps to 50 Gbps.

5.4.5 Summary

We presented an analog fully differential 1-tap FFE suitable for fiber optical data communication receivers with a maximum tunable single-ended peaking of 27 dB, a power consumption of 370 mW from a −3.3 V power supply, measuring an area of 0.94×0.76 mm^2. The tap design of the equalizer follows a modular architecture and it can be scaled to a large number of taps. Due to the non-peaked bandwidth of 60 GHz it can also be used as a VGA with a gain tuning range of 10 dB. The fabricated equalizer module's functionality was verified by performing receiver equalization on a 18 GHz bandwidth 1060 nm VCSEL communication link. The equalized performance exceeded the baseline un-equalized one by more than 2 orders of magnintude improvement on the BER and an increased FEC-enabled bitrate of 50 Gbps.



(a) BER at 32 Gbps with equalization setting 250200180.



(b) at 40 Gbps for two different equalization settings: 250200180, and 200115250.

Figure 5.14: BER measurements of the VCSEL-TIA test-bench with and without receiver equalization. Dashed lines indicate the Error free (1E–12) and FEC limit (1E–3).

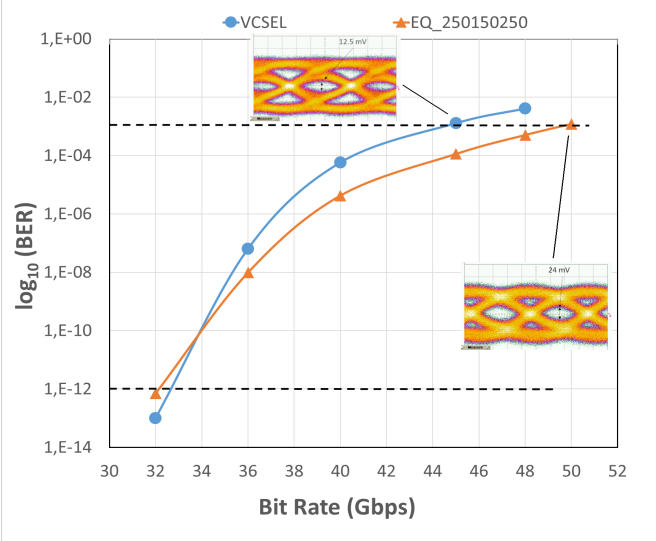


Figure 5.15: BER measurements with and without the equalizer over data-rates between 32 GHz to 50 GHz. Dashed lines indicate the Error free (1E–12) and FEC limit (1E–3).

Chapter 6

VCSEL driver for Space applications

In Paper C, we presented a VCSEL based optical transceiver MMIC with 4 x 28 Gbps datarate, implemented in IHPs SG13RH 130 nm SiGe BiCMOS with f_t and f_{max} of 250 GHz and 350 GHz. The process is radiation hardened (RH) and is currently under qualification by ESA standards. The transceiver was aimed at short-reach optical interconnect links within very high throughput satellites (V/HTS), therefore special considerations appropriate for the space environment had to be met.

6.1 VCSEL characterization and modeling

The VCSEL driver design process was mainly driven by the system specification and the characteristics of the VCSEL load. The overall system specification, as elaborated in Paper C, set strict performance requirements for the VCSEL-Driver sub-module. So, a measurement and modeling campaign of the VCSEL was deemed necessary to enable an educated IC design process. The output of this process was a netlist model for the VCSEL that enabled co-simulation with the driver circuit, in order to achieve optimized system performance.

6.1.1 VCSEL measurements

As mentioned in Section 2.2.1, VCSELs are typically the performance bottleneck in short reach optical interconnect systems. To that end, two different test setups were used in order to characterize the VCSELs over the full temperature range of operation of the final module. The first test setup was used for DC IPV measurements and can be seen in Fig. 6.1. The second setup which was used for the VCSEL S-parameter measurements is shown Fig. 6.2. The results of the measurements are compared with the VCSEL model later in this chapter.

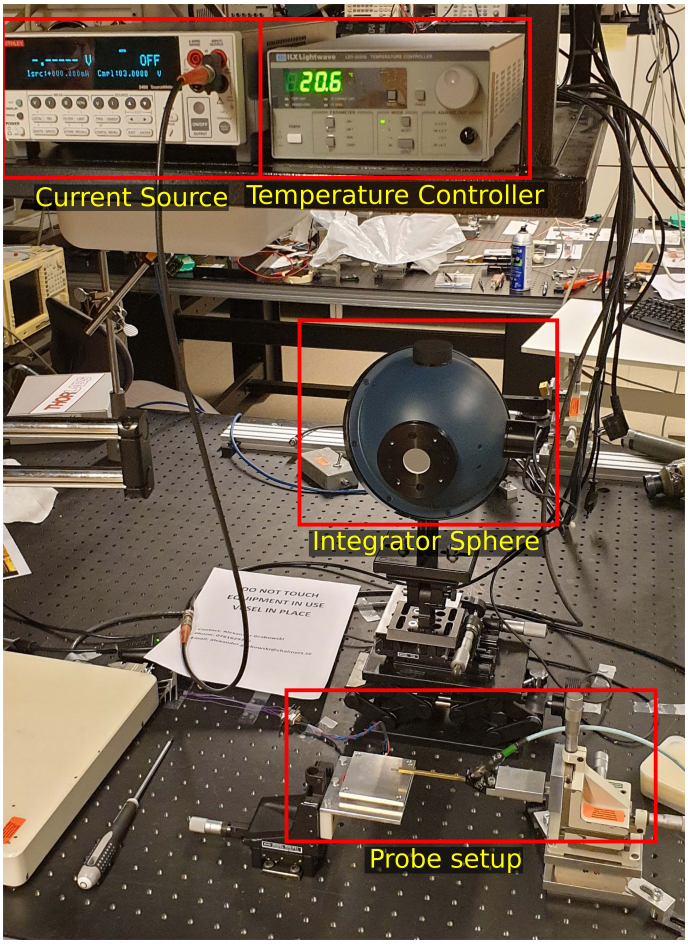
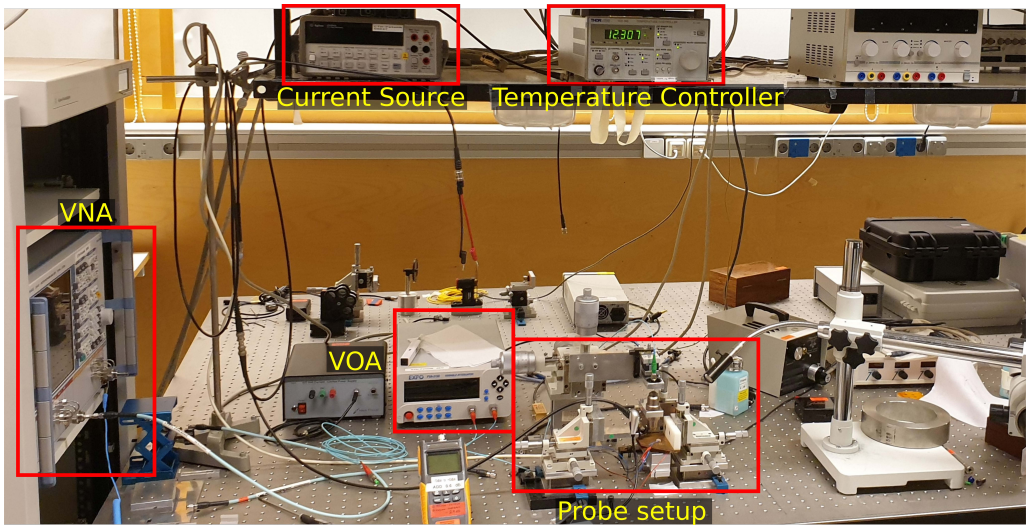
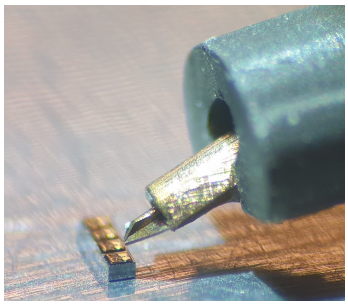


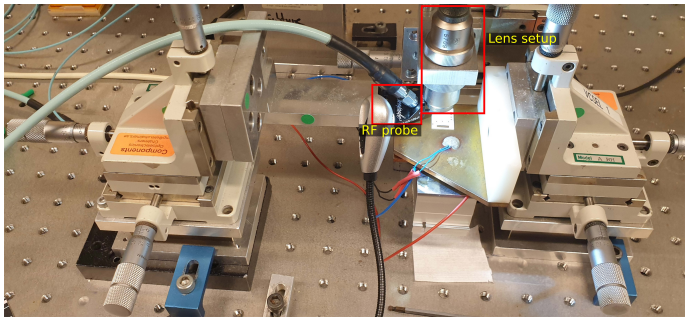
Figure 6.1: Experimental setup for the IPV VCSEL measurements.



(a) S-parameter measurement setup photo.



(b) VCSEL array under the probe.



(c) S-parameter probe and lens-coupling setup.

Figure 6.2: Experimental setup for the S-parameter VCSEL measurements.

6.1.2 VCSEL modeling

Several different approaches have been used in literature in VCSEL modeling ranging from the conventional rate equation model, to large signal physical VCSEL model [108], behavioral modeling using Volterra series or artificial neural networks (ANN) [109]. The basic equivalent circuit model works only for small signal modulation of the VCSEL. The main issue is that as discussed in Section 2.2.1, the VCSEL is a non-linear device both in terms of biasing, as well as temperature. Therefore the small signal model parameters (seen in Fig. 6.3) Pad capacitance, C_p, and mirror resistance, R_m, are typically constant over bias current, while junction resistance (R_j) and mirror capacitance (C_m) are not. Furthermore those parameters depend on the ambient temperature.

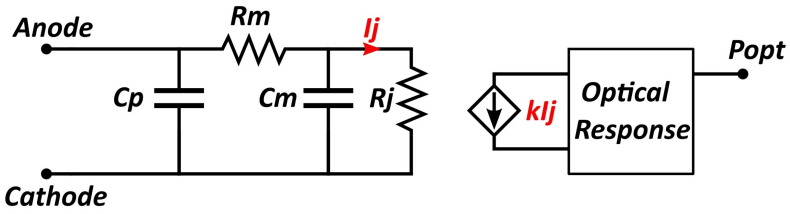


Figure 6.3: VCSEL parasitic model used for fitting.

In order to address those issues in a fashion to enable the design of the driver, we pursued the development of a behavioral polynomial model of the VCSEL based on measured dc and transient characteristics. The two part model was written in Spectre language which enabled us to co-simulate it with the driver electronics. The two parts of the model account for the electrical front-end which interfaces with the driver, and the optical back-end which deals with the VCSELs dynamics. The former is important in optimizing the Driver-Load interface, while the latter becomes exceedingly important in the characterization of the transmitter's optical output. The model took into account the impact of the bias current and temperature, as well as the dynamic characteristics of optical generation. The results of the modeled vs the measured VCSEL response were presented in Paper C in Fig. 8.

6.2 Driver design

The unique challenges of the application (space environment on low earth orbit) dictate specific trade-offs that go against typical VCSEL driver design. The trade-offs revolve around robustness, performance, power consumption, programmability, and predictability. The recommendations for designing electronics for space typically increase complexity or power in order to alleviate the magnitude of the different effects [110].

The VCSEL model in conjunction with the models of the packaging and interconnect layers of the Optical Sub-Assembly (OSA) module (seen in Paper C Fig. 3B) were used to optimize the design of the driver circuit. The test-bench for the driver optimization can be seen on Fig. 6.4.

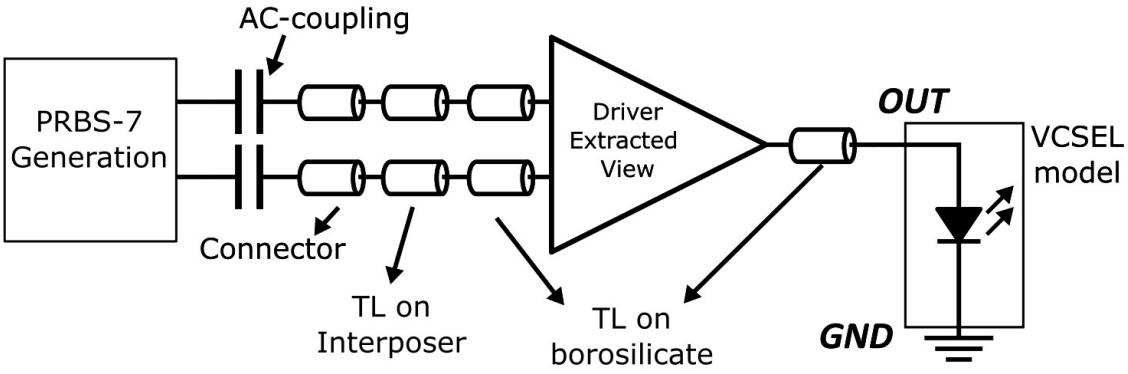


Figure 6.4: Block diagram of the test bench used for the design of the driver.

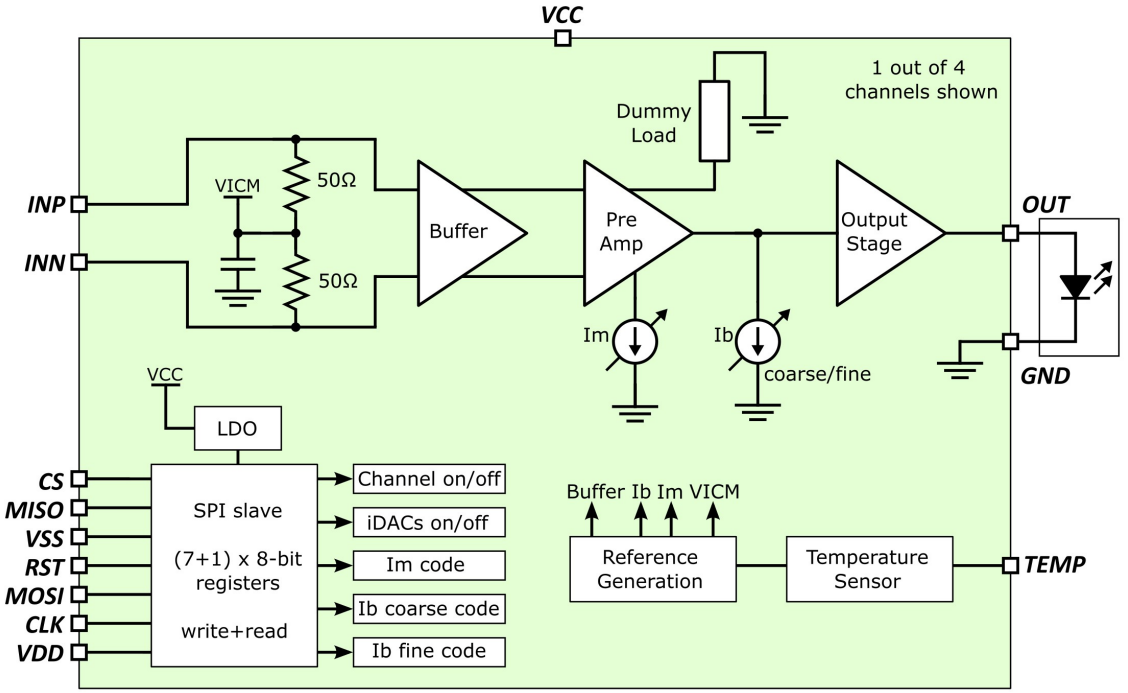


Figure 6.5: Schematic block diagram of a single channel of the VCSEL Driver.

The Driver, as shown in Fig. 6.5 was implemented using differential topology with full-centroid symmetry and double or triple redundancy wherever possible. In addition to reducing the effects of component miss-match, this implementation provides a means of averaging in order mitigate the RF path from single event transient induced charges.

The bias currents of the RF stages and any current mirror were increased in the order of a few mA in order to reduce the impact of SETs [111]. Transistor sizes in the RF path were increased in order to shield the sensitive signal path from low energy SETs [112]. This is contrary to the design goal of low power consumption, however it is demanded by the harsh space environment. All transistors made use of guard rings and extended number of well contacts in order to reduce the substrate impedance [113]. Additionally the tunability of the Driver was designed with plenty of margin in

order to accommodate for fabrication corners and device aging. The programmability of the Driver was implemented via an on-chip Serial-Parallel Interface (SPI) in order to avoid unnecessary bias and control interconnects through the module. The extracted simulated results of the Driver with the VCSEL and the module packaging were presented in Paper C in Fig.11B.

Chapter 7

Conclusion

Optical interconnects are becoming a staple of data center networks by offering high datarates at decreasing cost and energy. High-speed, wideband electronic circuits were designed in state-of-the-art semiconductor technologies with the goal to overcome the unique challenges posed by the optoelectronic short- or long-haul communication channel. In addition to the specific field, there is a plethora of other applications for such systems: intra- and inter-vehicle optical communication, intra- and inter-satellite optical communication, and radio-over-fiber, to name a few. While those fields are in various datarates and stages of maturity, they call for original topologies and interdisciplinary application of existing circuits.

7.1 Future outlook

In this work we presented some of the building blocks of receiver and transmitter optoelectronic systems for a variety of optical link scenarios. However an abundance of engineering challenges still remains regarding packaging and optimizing the electronics with regard to the optoelectronics.

Tackling different application environments (space, vehicles) imposes a whole new array of considerations that do not exist in the temperature controlled data-center environment. Temperature, radiation, vibrations, long term reliability, and configurability, are a few of the challenges demanding novel electronic solutions. Further research could also focus on the threshold between the analog data covered in this work and the digital data upon which the communication fabric is built, with emphasis on digital to analog and analog-to-digital converters, as well as clock generation and recovery blocks. Additionally, several secondary circuit blocks are required in order to satisfy the long term stability and quality requirements of the industry. Typical examples are: on chip bias generation networks (with band-gap references, noise rejection etc.), DC offset cancellation loops, feedback control circuits, serial to parallel interface (SPI) and memory blocks to allow programming of tunable circuits without the need for additional bias connections.

Lastly, while the designed receiver electronics presented on this work were aimed at OOK and to an extend at PAM-4 baseband communication, that does not

necessarily limit their usability with other modulation schemes. That opens up the potential to use existing circuits for transmission of Phase Shift Keying (PSK), or quadrature PSK (QPSK) which are popular in radio-over-fiber applications.

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