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Mobility degradation and series resistance in graphene field-effect transistors

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***Abstract* — Accurate device models and parameter extraction methods are of utmost importance for characterizing graphene field-effect transistors (GFETs) and for predicting their performance in circuit applications. For DC characterization, accurate extraction of mobility and series resistance is of particular concern. In this paper, we show how a first-order mobility degradation model can be used to separate information about mobility degradation and series resistance for a set of GFETs of different channel lengths. Data from a large set of top-gated GFETs based on chemical vapor deposited (CVD) graphene was analyzed to validate the proposed model and extraction procedures. For removing any uncertainties caused by observed device-to-device data variations due to the uneven quality of CVD graphene, the same methods were applied to a set of closely located bottom-gated GFETs found in literature. Those GFETs were designed for transfer length methods and fabricated on exfoliated graphene of homogenous quality. Similar mobility degradation behavior was observed for both sets of devices with the mobility being reduced to half for a voltage-induced charge carrier density of 10^{13} cm^{-2}.**

***Index Terms*— charge carrier mobility, graphene field-effect transistors, mobility degradation, series resistance.**

I. Introduction

Graphene, a two-dimensional carbon material organized in a hexagonal pattern, holds a lot of promise for becoming the channel material of future field-effect transistors due to its high low-field mobility and extremely high charge-carrier saturation velocity [1]. For graphene field-effect transistors (GFETs) the low-field mobility is an important parameter for monitoring the quality of the channel material, and for predicting the GFET performance in circuit applications [2]. Accurate modeling of the current–voltage (I/V) characteristics is important for device design optimization, projection of performances, and exploration of analog/RF circuits providing new or improved functionalities [3].

The low-field mobility of a GFET is usually determined from drain current versus gate voltage measurements at low drain voltages, typically 10-100 mV, using a resistance model referred to as the Kim model [4]. This model, sometimes referred to as a "constant mobility model", assumes a constant mobility due to long-range impurity scattering, and a charge model including both impurity-induced residual carriers and gate voltage-induced carriers. However, it is generally expected that the mobility would decrease as the number of gate-índuced carriers increases.

For MOSFETs, mobility degradation is a well-known phenomenon thoroughly investigated already in the mid-1960´s. Of special relevance to this work is a remark made early on by Crawford who showed that mobility degradation had the same effect on the MOSFET I/V characteristics as the series resistance [5].

The analogy between GFETs and MOSFETs was discussed by Das Sarma et al. [6] who made comparisons between short-range scattering in GFETs and surface-roughness scattering in MOSFETs - two scattering mechanisms of increasing importance as the number of field-induced carriers increases.

For monolayer graphene, Zhu et al. found already in 2009, albeit in a low temperature context, that while mobility limited by Coulomb scattering was independent of carrier density, the mobility limited by short-range scattering was inversely proportional to carrier density [7].

By 2010 Dorgan et al. [8] had observed that for bottom-gated GFETs the charge carrier mobility was decreasing for carrier densities above $2{\cdot}10^{12}$ cm^{-2} also in the 300-500 K temperature range. Their observations of mobility degradation was later supported by observations made by Zhong et al. who found similar mobility degradation behavior both at 77 K and 300 K in their work on mobility extraction methods based on field-effect measurements [9, 10]. They also noted in passing that the fitting method developed by Kim et al. uses a higher contact resistance to compensate for the mobility degradation.

In this article we will show how the series resistance extracted using the Kim model contains information about mobility degradation. Leaving further discussions of the scattering mechanisms in graphene to others, we propose a first-order mobility model based on two dominant scattering mechanisms similar to what has been used for MOSFET modeling for over fifty years. For this work we adopt an engineering approach; an approach from the parameter extraction and device modeling point of view that allows us to explain the experimental observation of why the series resistance, albeit designed to be constant from device-to-device, appears to depend on the gate length of the device. By showing how to separate information about mobility degradation from the series resistance, we hope to provide

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new insights into GFET operation and modeling most helpful for device characterization engineers and circuit designers.

In the following sections we will discuss i) the proposed mobility model, ii) the two different sets of GFETs used to validate the model (one set being top-gated GFETs based on CVD graphene and the other set being bottom-gated GFETs on exfoliated graphene), iii) the parameter extraction methods used, iv) the experimental results found, and finally v) the validation of the mobility degradation model.

II. Theory

Our intention with this section is to show that the Kim model [4] contains information about the mobility dependence on the charge carrier density. This information can be obtained by assuming the following first-order mobility model,

$$\mu = \frac{\mu_0}{1+\theta\sqrt{V_0^2+V_{GSO}^2}}, \tag{1}$$

a model similar to the one successfully used for silicon MOSFETs for more than fifty years [6] [11] [12] [13]. The MOSFET model has been adapted for GFETs by using the transversal field model introduced by Kim et al. resulting in a carrier density

$$n = \frac{C_{ox}}{q}\sqrt{V_0^2+V_{GSO}^2}\,. \tag{2}$$

In these equations, μ_0 is the long-range Coulomb scattering mobility, θ the mobility degradation parameter, C_{ox} the gate oxide capacitance per unit area, q the electron charge, and $V_0=qn_0/C_{ox}$ the residual voltage determined by the density of residual carriers n_0 at the minimum conductivity Dirac point, [14]. Finally, $V_{GSO}=V_{GS}-V_{Dirac}$ is the gate-to-source voltage overdrive of the Dirac voltage V_{Dirac}.

By inserting (2) into (1) we obtain

$$\mu = \frac{\mu_0}{1+n/n_{ref}}, \tag{3}$$

where $n_{ref} = C_{ox}/(q\theta)$ is the carrier density for which the mobility is reduced to half. This mobility model is the result of two scattering rates being added using Mathiesen´s rule, one being proportional to $1/\mu_0$ and one being proportional to the carrier concentration, n.

Inserting the mobility degradation model into the linear region field-effect transistor equation upon which the Kim resistance model rests [15], yields

$$I_D = \frac{k\sqrt{V_0^2+V_{GSO}^2}}{1+\theta\sqrt{V_0^2+V_{GSO}^2}}\left(V_{DS}-R_{C0}\times I_D\right), \tag{4}$$

where the transconductance parameter $k=(W/L)\mu_0 C_{ox}$ is determined by the product of the geometry related width-to-length aspect ratio W/L of the channel, and the technology related parameter $k'=\mu_0 C_{ox}$, V_{DS} is the applied drain to source voltage, and $R_{C0}=R_D+R_S$ is the sum of the drain and source series resistances to the external drain/source terminals including the resistances of the metal/graphene junctions and the access areas between the metal contacts and the channel.

Solving for I_D we obtain

$$I_D = \frac{kV_{DS}\sqrt{V_0^2+V_{GSO}^2}}{1+\underbrace{(\theta+kR_{C0})}_{\theta_{eff}}\times\sqrt{V_0^2+V_{GSO}^2}}. \tag{5}$$

This model equation has four model parameters, k, θ_{eff}, V_0, and V_{Dirac}, and is similar to the well-known models used for MOSFET parameter extraction [16, 17].

The modified Kim GFET resistance model now becomes

$$R_{DS} = \underbrace{\frac{1}{k\sqrt{V_0^2+V_{GSO}^2}}}_{R_{channel}} + \frac{\theta}{k} + R_{C0}\,. \tag{6}$$

As shown in (6) the channel resistance consists of two parts, both proportional to $1/k$, where the second part (θ/k) is due to the mobility degradation effect. Under the assumption of a constant series resistance R_{C0}, the "effective" series resistance $R_C=R_{C0}+\theta/k$ can be extracted by means of the gate voltage dependence of the total resistance R_{DS}. However, for separating the channel resistance part θ/k from the contact/series resistance R_{C0}, measurement data are needed from devices of different gate lengths since θ/k is proportional to the channel length L while the contact resistance R_{C0} is not. This will be explored in a following section based on measurement data from two sets of GFET devices, one set of bottom-gated GFETs on exfoliated graphene, and one set of top-gated GFETs on chemical vapor deposited (CVD) graphene.

(*Eq.* (6) *above has been corrected and hence this paragraph differs somewhat from the paragraph in the published article.*)

III. Device Fabrication

For validating the proposed mobility model, data from experimental I_D vs V_{GS} GFET transfer curves were obtained from two sets of graphene field-effect transistors of different channel lengths. For this purpose, a test chip containing a large set of GFETs was fabricated using chemical vapor deposited (CVD) graphene transferred to the surface of a 1 µm SiO_2 layer grown by wet oxidation on a high-resistivity silicon substrate. Top-gated GFETs were fabricated using the same methods as described in detail in previous papers [2]. This includes the use of electron-beam lithography and reactive ion etching to shape the individual GFET active areas. Using an oxidized aluminum nucleation layer, a multi-stage atomic layer deposition process was used to form a 22 nm top-gate Al_2O_3 dielectric (corresponding to C_{ox}=300 nF/cm^2). Gate fingers 300 nm thick were formed by e-beam lithography using a 10 nm titanium adhesion layer. Finally, the source and drain microprobe pads were formed. All GFETs are 15 µm wide while gate lengths vary from 0.5 to 10 µm (0.5, 0.75, 1, 2, 4, 6, 8 and 10 µm). The use of e-beam lithography and reactive ion etching infers minimal deviations from the nominal gate dimensions. Transfer current/voltage (I/V) characteristics were obtained using Keithley 2612B dual-channel SourceMeter SMU and Cascade probe station using a drain voltage of 100 mV.

For comparison, data from a second set of GFETs were obtained from an article by Zhong et al. [9, 10]. They used a

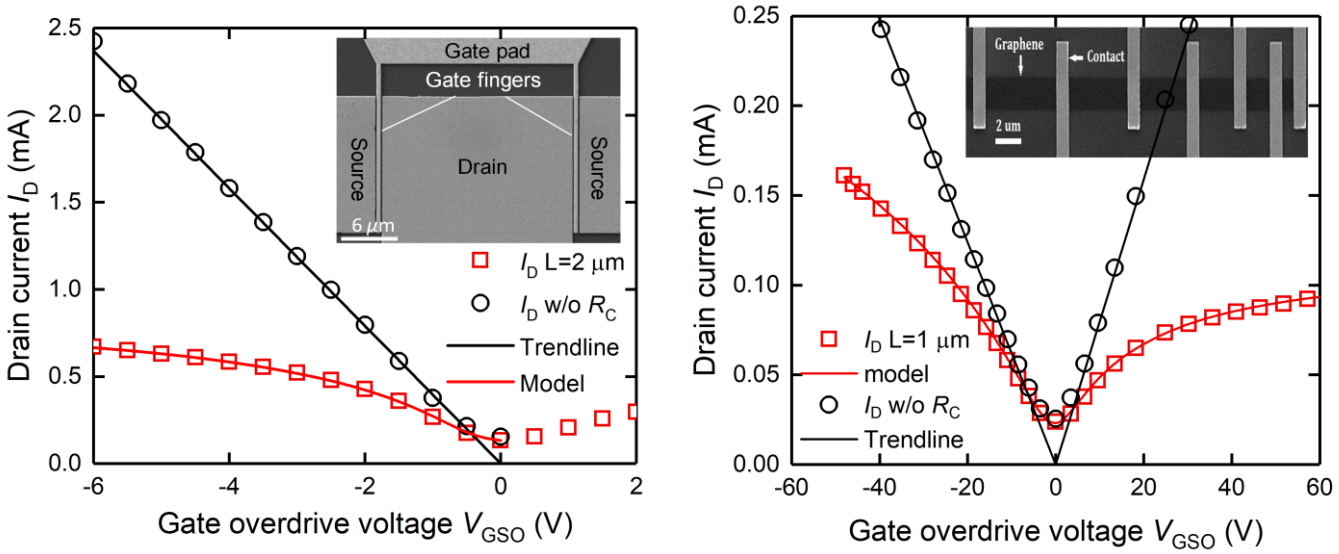

Fig. 1. The parameter extraction process includes finding and subtracting from the measured I_D vs. V_{GSO} data the series resistance R_C that gives the best straight line approximation for V_{GSO} >> V_0. Left-hand figure shows data for one example device from the set of top-gated GFETs from our laboratory, while the right-hand figure shows similar data for one of the TLM GFETs in [9]. Insets show SEM images of the GFETs - TLM structure inset courtesy of Zhiyong Zhang [9].

compact test structure designed for the transfer length method (TLM) with back-gated GFETs of six different channel lengths ranging from 1 to 6 μm. As described in their paper, these GFETs were fabricated on mechanically exfoliated single-layer graphene placed on a heavily p-doped silicon substrate covered with 285 nm silicon oxide. The graphene sample was patterned into a 2.2 μm wide strip using electron-beam lithography and reactive ion etching. Low resistance Pd/Au contacts were deposited by electron-beam evaporation and formed using lift-off technology.

IV. Experimental

Careful parameter extraction methods based on the Kim model were applied for extracting the transconductance parameter k and the "series resistance" R_C in regions where the influence of the residual carriers and the quantum capacitance was negligible, i.e. for V_{GSO}>>V_0. Figure 1 shows the transfer characteristics for one GFET of each set of devices. Also shown are the straight lines typical of field-effect transistors in their linear region obtained after subtraction of the "series resistance" R_C. Based on an intelligent guess for the initial R_C value, the extraction process was fine-tuned to minimize the error yielding contact resistance values accurate within a few per cent. Inserted into the model, the extracted model parameters yielded excellent model fit to experimental data. We can also observe that while the narrow back-gated GFETs fabricated on high-quality graphene have well-defined Dirac points, the wide top-gated GFETs on CVD graphene seem to suffer from spatial variations of the Dirac point along the 15 μm width of the GFETs. However, the excellent linearity[1] of the I/V characteristics obtained after subtraction of the series resistance is a strong indication of the validity of the proposed mobility model.

Figure 2 shows the results of the parameter extraction process for a set of twelve top-gated CVD GFETs and for the six bottom-gated GFETs of the TLM structure. The average mobility for the set of bottom-gated GFETs is 4990 cm^2/Vs, while for the set of top-gated CVD GFETs it is 3300 cm^2/Vs. The extracted resistance R_C was found to increase with increasing gate length as shown in figure 2b. For the bottom-gated GFETs, the same excellent linear relationship of R_C vs. L from [10] could be repeated, while for the top-gated CVD GFETs variations in the graphene quality reflected in device-to-device variations of the contact resistance causes some uncertainties concerning the exact slope. Nevertheless, the extrapolated (L=0) contact resistance R_{C0} is well defined for both sets of devices. The extracted contact resistances are 190 and 400 Ωμm, respectively, for the bottom- and top-gated GFETs, where one reason for the difference could be due to the series resistance of the access areas of the top-gated GFETs.

Since the GFETs are designed for equal contact and access areas independent of channel length, we were rather confident at this point that mobility degradation was the reason for the series resistance varying with the gate length.

Figure 2c shows a plot of the extracted values for θ_{eff}=kR_C vs. 1/L, where for comparison the values obtained for the bottom-gated GFETs have been rescaled to the same gate oxide thickness as that of the top-gated GFETs. A mobility roll-off parameter θ=0.2 V^{-1} was obtained, corresponding to a reference concentration n_{ref} of 10^{13} cm^{-2}, a value in excellent agreement with previous observations [8].

V. Model Validation

Finally, it remains to validate the proposed model by comparing the results obtained here with previously published observations. In their paper, Zhong *et al.* used their six GFET

[1] Data points from the overdrive voltage range 3V_0<V_{GSO}<14V_0 with negligible influence of residual carriers were used to find the contact resistance R_C. For almost all devices the linear fit resulted in R^2>0.9985 - a strong indication of the validity of the proposed mobility model.

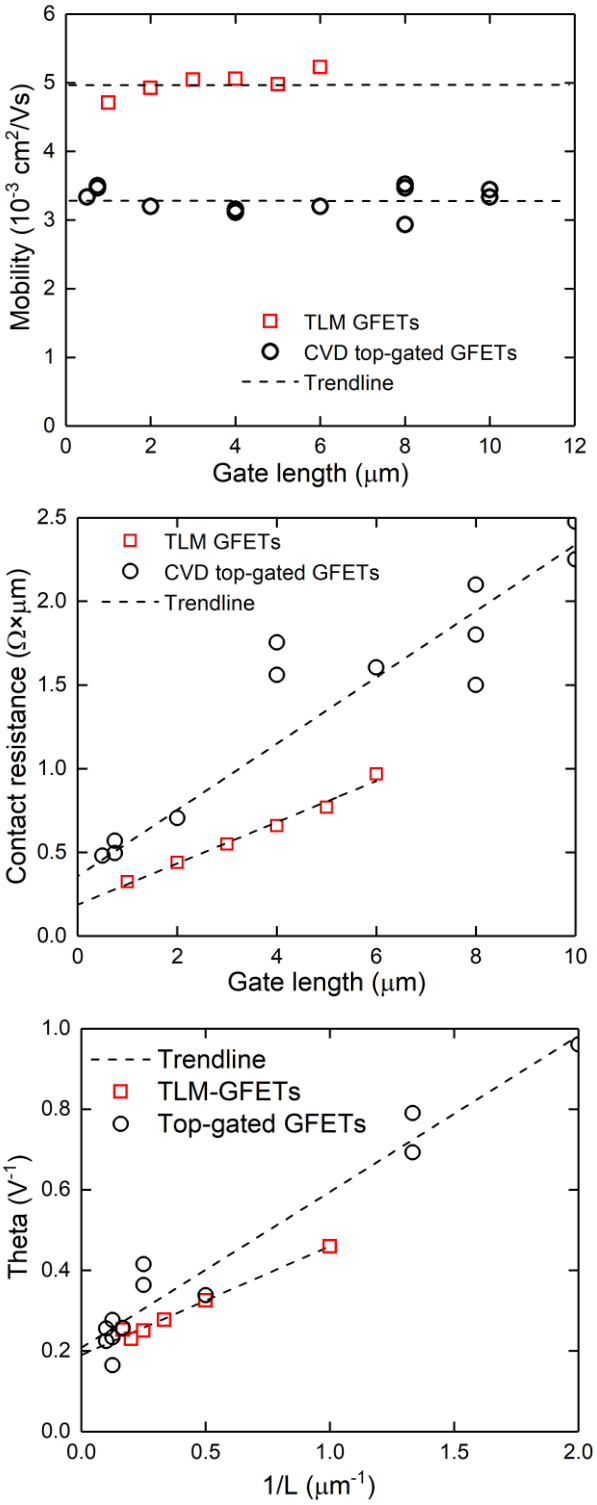

Fig. 2. Graphs showing the relationships between extracted model parameters and channel length for both sets of GFETs: a) mobility vs. L, b) resistance R_C vs. L, and c) θ_{eff} vs. $1/L$.

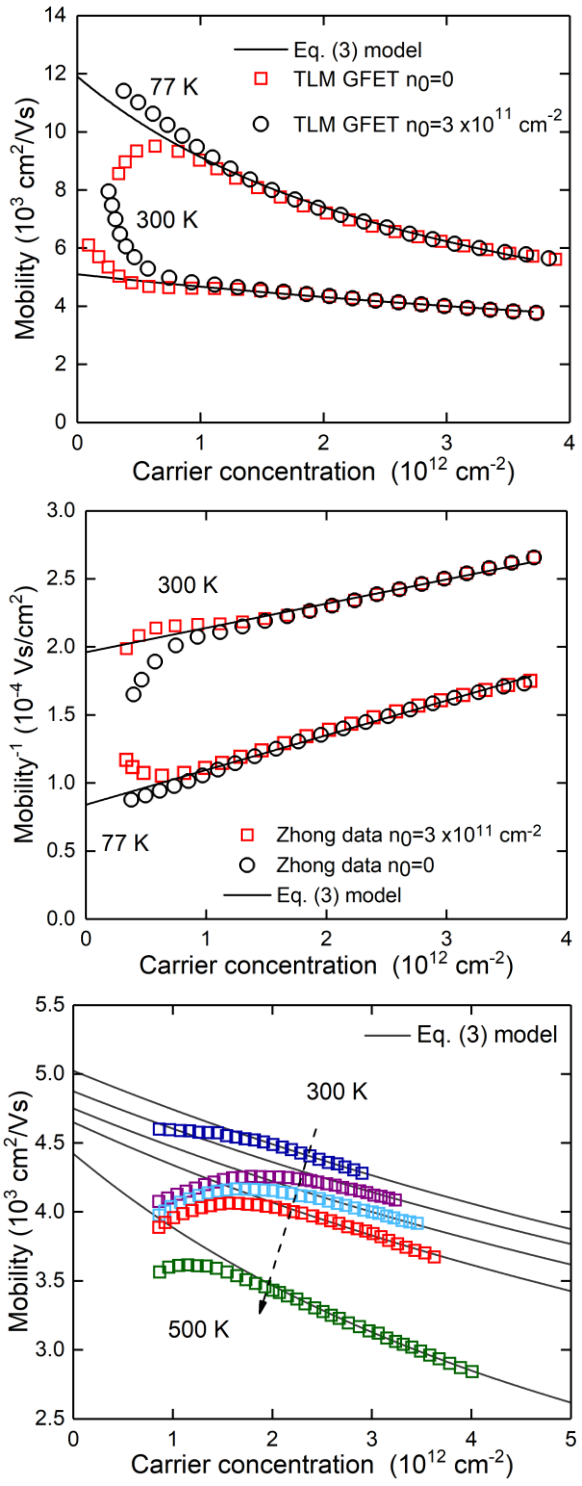

Fig. 3. Mobility vs. carrier density graphs. a) eq. (3) mobility model fitted to 300 K and 77 K data published by Zhong et al. [9] showing excellent model fit for carrier densities n>10^{12} cm^{-2}, b) inverse of same mobility data plotted vs. carrier density showing excellent linearity for n>10^{12} cm^{-2}, and c) eq. (3) mobility model fitted to data published by Dorgan et al. [8] at five different temperatures in the range from 300 K to 500 K in steps of 50 K.

TLM structure for extracting the mobility as a function of the gate-overdrive voltage, or equivalently as a function of the density of carriers, both at room temperature (300 K) and at 77 K. Figure 3a shows their extracted hole mobilities together with our model from (3). Good agreement between their data and our model is shown for carrier densities much larger than the residual carrier density n_0, i.e. in the region used for extracting the mobility and contact resistance. However, as we approach the Dirac point, the hole mobility extracted strongly depends on the density of residual carriers used in the charge model needed.

In further support of the mobility degradation model proposed in (3), figure 3b shows the inverse of the same hole mobilities versus carrier density. The excellent linearity shown strongly supports the proposed mobility model since the existence of other scattering mechanisms should have manifested themselves in the form of nonlinearities.

Figure 3c shows similar results published by Dorgan et al. showing the dependence of the mobility on the number of carriers using bottom-gated GFETs [8]. This graph shows our model fitted to their data at five different temperatures ranging from 300 to 500 K. Again, good agreement is shown for carrier densities in the region used for extracting the mobility and contact resistance. Whether the discrepancies close to the Dirac point between our model and their work solely depends on uncertainties in the charge model or on less efficient screening must be left for future investigations. Here, it is important to remember that Dorgan et al. noted that not all their samples displayed the dip in mobility at low charge density. In their attempt to study the transition from hole mobility to electron mobility at the Dirac point, they found uncertainties on the order of ±2000 cm^2/Vs.

From the point-of-view of the circuit designer, we have to accept the fact that while the current at the Dirac point is given by the product of mobility and residual carrier density, it is difficult to separate the two. The use of a certain mobility model reduces the residual carrier density to the role of a fitting parameter compensating for possible errors.

VI. Conclusions

In conclusion, we believe that the low-field mobility model proposed in this paper will pave way for a better understanding, and more accurate modeling, of graphene field-effect transistors. After having reviewed the relationship between mobility degradation and series resistance, we have shown how to separate the two effects yielding an average mobility degradation parameter and a correct series resistance for a set of GFETs of different channel lengths. Moreover, we hope this work will serve to remove the misconception of the Kim model being a "constant mobility model" only, since it actually contains first-order information about mobility degradation due to an increasing number of charge carriers induced by the transversal field.

VII. Acknowledgement

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