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Performance of Deep Neural Networks on Low-Power IoT Devices

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Abstract

Advances in deep learning have revolutionized machine learning by solving complex tasks such as image, speech, and text recognition. However, training and inference of deep neural networks are resource-intensive. Recently, researchers made efforts to bring inference to IoT edge and sensor devices which have become the prime data sources nowadays. However, running deep neural networks on low-power IoT devices is challenging due to their resource-constraints in memory, compute power, and energy. This paper presents a benchmark to grasp these trade-offs by evaluating three representative deep learning frameworks: uTensor, TF-Lite-Micro, and CMSIS-NN. Our benchmark reveals significant differences and trade-offs for each framework and its tool-chain: (1) We find that uTensor is the most straightforward framework to use, followed by TF-Micro, and then CMSIS-NN. (2) Our evaluation shows large differences in energy, RAM, and Flash footprints. For example, in terms of energy, CMSIS-NN is the most efficient, followed by TF-Micro and then uTensor, each with a significant gap.

CCS Concepts: • Computer systems organization → Embedded systems; • Computing methodologies → Neural networks.

Keywords: IoT, Deep Neural Networks, Low-Power

1 Introduction

In recent years, Deep Neural Networks (DNNs) have outperformed other algorithms to solve complex problems in computer vision [10], Natural Language Processing (NLP) [5], and Human Activity Recognition (HAR) [15]. Similarly, novel IoT applications utilize DNNs to recognize and categorize sophisticated sensor data [7]. Typically, the resource-intensive tasks of training and inference are offloaded to cloud providers. With the Internet of Things, billions of devices produce massive volumes of data to be analyzed, raising two primary concerns. First, IoT devices collecting sensitive sensor data from users and storing them in cloud services poses privacy issues. Second, processing extensive amounts of sensor data may overwhelm infrastructure in terms of bandwidth and available computation. To address these concerns, researchers bring inference to edge and sensor devices [13, 16].

In particular, DNN inference on low-power IoT devices brings new challenges due to their resource-constraints. We recognize three main challenges. First, IoT devices have a small memory-size, typically in the range of KBs, where an average DNN requires MBs of storage. Second, DNN inference demands significant energy, but IoT devices require power duty cycling to preserve energy. Third, DNNs are designed using GPU/CPU optimization libraries (e.g., CUDA/Intel DL Boost), unavailable on low-power IoT devices.

The development process of DNNs on low-power IoT devices is a tedious task, where devices are manually managing memory and computation resources. There is a diversity of languages and frameworks, for example, for training DNNs in the cloud or for converting them for IoT devices, and each framework has different tool-chains. Moreover, when designing and training a DNN, it is unknown how efficient it will be on an embedded device. In this paper, we argue that it is essential to evaluate and reveal trade-offs of common frameworks, including the complexity of the development process and the resource-efficiency of their IoT run-time environments.

This paper focuses on the inference part of Deep Neural Networks (DNNs) on low-power IoT devices, assuming the training is done off-line on more powerful devices. We present a benchmark for evaluating three deep learning frameworks for IoT devices: TensorFlow-lite-Micro[2],
The CNN consists of several layers stacking together: convolution kernels, max pooling, and fully connected layer. The final layer is the output number of classes.

The code generator is different across the platforms. The dependency refers to other libraries needed to run inference. The usability reflects the end-to-end development process (from training to on-device inference).

Table 1. High-level comparison of deep learning frameworks. The code generator is different across the platforms. The dependency refers to other libraries needed to run inference. The usability reflects the end-to-end development process (from training to on-device inference).

<table>
<thead>
<tr>
<th>Framework</th>
<th>Code</th>
<th>Generator</th>
<th>Dependency</th>
<th>Usability</th>
</tr>
</thead>
<tbody>
<tr>
<td>uTensor</td>
<td>C++</td>
<td>Auto</td>
<td>Mbed OS</td>
<td>Easy</td>
</tr>
<tr>
<td>TF-Micro</td>
<td>C++</td>
<td>Auto</td>
<td>None</td>
<td>Medium</td>
</tr>
<tr>
<td>CMSIS-NN</td>
<td>C</td>
<td>Manual</td>
<td>None</td>
<td>Hard</td>
</tr>
</tbody>
</table>

2.3 IoT Deep Learning Frameworks

The frameworks used in our benchmark are the following.

- **uTensor**. An open-source framework [12] for deep learning inference on Mbed-OS enabled IoT devices. uTensor focuses on rapid-prototyping from TensorFlow-trained neural networks to convert them for IoT devices. uTensor is written in C++ and provides built-in functions for quantization.

- **TensorFlow Lite Micro (TF-Micro)**. An open-source framework [2] for supporting machine learning inference on micro-controllers. The library is written in C++ as part of the TensorFlow ecosystem. TF-Micro uses TensorFlow to write and train a neural network. TF-Micro provides a wide range of options to optimize and quantize a neural network using the TensorFlow Lite Converter. TF-Micro can run as stand-alone or using an operating system like Zephyr OS.

- **CMSIS-NN**. Cortex Microcontroller Software Interface Standard for Neural Networks is an open-source library [6] for ARM devices. It is written in C and provides several quantized functions like Convolution, Pooling, Softmax, and Fully-Connected layers. CMSIS-NN does not provide training tools or generators for the C code. The developer needs to use another library to train, quantize, and convert the network’s weights in C code. CMSIS-NN is designed to maximize neural networks’ performance on the Cortex-M series by employing the on-board DSP accelerator (CMSIS-DSP) [6].

3 Benchmark Design

In this section, we introduce the design goals of our benchmark and then present the actual benchmark.

3.1 Overview and Evaluation Goals

Our benchmark evaluates three deep-learning platforms: CMSIS-NN, uTensor, and TF-Micro (see Table 1). Their toolchains are similar in training a network but differ significantly on the code generation and quantization methods. Our goal is to evaluate trade-offs between the development process and their run-time environment’s efficiency on low-power IoT devices. For the run-time environment, we focus on the efficiency of running inference on low-power devices in terms of: a) memory footprint, b) inference execution time, and c) energy consumption.
3.2 Benchmark Process

We present the process of our benchmark in Figure 2. We color the automated steps in green and user-defined steps in blue. There are four steps to generate a neural network and execute it on an IoT device. First, we define and train the neural networks and report the accuracy in Keras\(^2\) (see Table 2). Keras is an intuitive API wrapper on top of TensorFlow to help define and train machine learning models. All the networks are based on the same architecture (see Figure 1), data-set, and hyper-parameters. Second, we quantize the same network for each tool-chain based on each framework’s method. Third, we link the network, the evaluation code, and the framework library to produce the executable file. Fourth, we run inference on the same low-power IoT device for each framework to evaluate its performance.

4 Performance Evaluation

This section presents our evaluation results on low-power IoT devices. The evaluation answers the following questions: (a) To what extent is inference technically feasible on IoT devices? (b) What is the overhead of neural networks on IoT devices in terms of computation, memory, and energy consumption? (c) What is the trade-off between automation in the development process and performance of inference on IoT devices?

4.1 Experimental Setup

Software implementation. We define and train the neural networks listed in Table 2 using Python 3.8.6 and Keras 2.4.0. For generating the object code, we have three cases:

- **CMSIS-NN.** We use the ARM GCC toolchain to build and link the C code.
- **uTensor.** We use utensor-cgen to generate the C++ code and mbed-cli to build and link C++ code, including Mbed OS.
- **TF micro.** We use the TF-Lite-Converter to export the network. We use West toolkit from Zephyr OS to build and link the TF-Micro C++ code.

Hardware Setup. We use the nRF-52840-DK board that features a 32-bit ARM Cortex-M4 at 64 MHz supporting DSP instruction set (CMSIS-DSP), 256 KB of RAM, and 1 MB of flash memory. We use the Nordic-Semiconductors Power Profiler Kit v1.1.0\(^3\) to measure power consumption.

Data & Code Availability. We provide the data and code of the benchmark in a public repository.\(^4\)

4.2 Data-sets

We train the neural networks with two standard data-sets.

**MNIST.** The Modified National Institute of Standards and Technology (MNIST) data-set for hand-written numbers. The data-set consists of 70,000 black and white 28x28 pixel hand-written numbers, where 60,000 are for training and 10,000 for testing. There are ten classes, one for each digit.

**CIFAR-10.** The Canadian Institute For Advanced Research (CIFAR) data-set for image classification. The data-set consists of 60,000 32 x 32 color images, where 50,000 are for training and 10,000 for testing.

Table 2. Convolutional Neural Networks trained on MNIST & CIFAR-10. The first column is the number of convolution kernels. For example, Conv-16 means the second layer (see Figure 1) and fourth layer have 16 kernels respectively. \(\text{Param.}\) is the number of trainable parameters.

<table>
<thead>
<tr>
<th>Convolution - Kernels</th>
<th>MNIST</th>
<th>CIFAR-10</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Param.</td>
<td>Accuracy</td>
</tr>
<tr>
<td>Conv-16</td>
<td>6,490</td>
<td>0.97</td>
</tr>
<tr>
<td>Conv-32</td>
<td>17,578</td>
<td>0.98</td>
</tr>
<tr>
<td>Conv-64</td>
<td>53,578</td>
<td>0.98</td>
</tr>
<tr>
<td>Conv-96</td>
<td>108,010</td>
<td>0.99</td>
</tr>
<tr>
<td>Conv-128</td>
<td>180,874</td>
<td>0.99</td>
</tr>
</tbody>
</table>

\(^2\)https://keras.io/
\(^3\)https://www.nordicsemi.com/Software-and-tools/Development-Tools/Power-Profiler-Kit
\(^4\)https://github.com/chrpro/TinyML-Evaluation/
We repeat each experiment 20 times. We report the maximum memory for the network and dynamically allocates the all the necessary data in the RAM. TF-Micro statically allocates (253 KB). The reason is that CMSIS-NN statically allocates 123 KB compared to uTensor and TF-Micro (28 KB & 60 KB). As we increase the number of kernels to 128, we notice CMSIS-NN has the largest footprint (22 KB) similar to uTensor and TF-Micro (28 KB & 60 KB). For demonstration purposes, a real-world application using these network will not leave any memory for the applications themselves.

In Figure 4, we present the flash footprints for each framework. For CMSIS-NN and TF-Micro, the flash footprint increases proportionally with the number of static variables. The reason is that the linker allocates static variables into the flash to be copied to RAM during the start-up phase. For uTensor, the flash footprint is the same for all experiments as it counts only for program code and input vectors. Finally, we notice that the larger neural network (with 128 kernels) consumes less than 37% (367 KB) of available flash (1MB). However, we consider these networks only for demonstration purposes. A real-world application using these network will not leave any memory for the applications themselves.

Inference Execution Time. We continue with the average inference execution time for each network. In Table 3, we report the results for the MNIST data-set. We notice that CMSIS-NN outperforms all other frameworks, as it is specialized for the on-board DSP accelerator available on Cortex-M devices. For example, the smallest network with 16 kernels and CMSIS-NN runs on average in 0.2 s (see Table 2), with TF-Micro in 1.0 s, and with uTensor in 3.0 s. The largest network with 128 kernels and CMSIS-NN runs on average in 8.45 s, with TF-Micro in 43.4 s, and with uTensor in 139 s. In Table 4 we report the results for CIFAR-10 data-set. We notice a similar behavior with CMSIS-NN outperforming the others, following by TF-Micro, and uTensor. We have not noticed any significant time deviation among the experiments.

Energy Consumption. In this part, we present the energy consumption based on the average electric current drawn in mA by utilizing Mbed OS. We notice similar behavior when using the CIFAR-10 data-set (see Figure 3b). However, a network with 128 kernels consumes almost all the available RAM, and with CMSIS-NN (265 KB), it exceeds the device capacity (256KB). However, we consider these networks only for demonstration purposes. A real-world application using these network will not leave any memory for the applications themselves.
We now discuss our results and remaining challenges. Framework automation. We observe that defining and training a deep neural network follows a similar process among all frameworks. However, they differ significantly in development process automation and especially in the quantization method. uTensor offers an easy-to-use toolchain where built-in functions are handling the quantization and code generation. TF-Micro offers more sophisticated quantization methods, but the user needs to configure them manually. CMSIS-NN gives programmers full-control over every aspect, leading to very efficient code, but the networks need to be converted and defined manually in C code. The result is a trade-off between the complexity of the development process and the efficiency of the resulting code-base: Code in CMSIS-NN has a higher efficiency but is more complex to implement when compared to simpler and versatile approaches (TensorFlow ecosystem) with less focus on performance.

**Memory Management.** We observe that memory management plays a crucial role in the performance of low-power IoT devices. CMSIS-NN benefits from static allocation of memory regions and definition of specialized 8-bit and 16-bit DSP data-types. In addition, CMSIS-NN boosts performance on the Cortex-M series by employing the on-board DSP accelerator (CMSIS-DSP). On the other hand, uTensor and TF-Micro use generic 32-bit data types and dynamic memory allocation. The generic data type allows multiple platform support, but it comes with a cost on low-power IoT devices.

**Concluding Remarks.** We conclude the discussion with two remarks. First, there is no framework to fit both the rigorous development process of deep neural networks and the low-power devices’ performance. Second, wide networks consume significant memory and energy of devices across all frameworks. Low-power IoT devices cannot utilize well-established pre-trained networks available on cloud services. There is a need for ultra-lightweight neural network architectures for low-power devices.

## 5 Related Work

**Compression.** The frameworks of our evaluation supports only quantization to reduce the size of the networks. Other unsupported methods include weight pruning [4], and network compression [4].

**ML Frameworks.** In this paper, we use three popular frameworks for low-power devices. Next to these, other framework exist: **STM32 Cube.AI [11]** is a proprietary machine learning framework by STMicroelectronics. This framework has a limited scope and is tied to STM MCUs. **Glow [9]** is an open-source machine learning graph optimizer created by Facebook. Glow does not support low-power devices yet, but it is an on-going work.

**ML Benchmarks.** Our benchmark is not the first one to evaluate the performance of machine learning platforms. **MLPERF [8]** is a large-scale benchmark suite for Machine Learning inference across different platforms and hardware. **DAWNBench [1]** is a deep learning benchmark focusing mostly on GPU performance. In contrast, our paper focuses on the applicability of DNN inference on low-power IoT devices.

## 6 Conclusion

This paper shows the trade-offs between the development process automation of Deep Neural Networks (DNNs) and
the low-power devices’ performance. We present a benchmark to evaluate three representative frameworks for DNNs inference on low-power IoT devices. Our benchmark reveals significant differences and trade-offs for each framework and its tool-chain: (1) We find that uTensor is the easiest framework to use, followed by TF-Micro, and then CMSIS-NN. (2) Our evaluation shows large differences in energy, RAM, Flash footprints. In terms of energy, CMSIS-NN is the most efficient, followed by TF-Micro and then uTensor, each with a significant gap.

7 Acknowledgments
This work was supported by the Swedish Research Council (VR) through the project “AgreeOnIT”, and the Vinnova-funded project “KIDSAM”. The complete evaluation using MNIST. The RAM and flash footprints are the maximum memory allocation. Time refers to the average inference execution time. The energy consumption is based on the average electric current draw.

Table 4.

<table>
<thead>
<tr>
<th>Conv. -Ker.</th>
<th>RAM (byte)</th>
<th>Flash (byte)</th>
<th>Time (ms)</th>
<th>Energy (mJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>22,788</td>
<td>29,724</td>
<td>188</td>
<td>5±0.1</td>
</tr>
<tr>
<td>32</td>
<td>47,396</td>
<td>40,828</td>
<td>597</td>
<td>16±0.1</td>
</tr>
<tr>
<td>64</td>
<td>110,436</td>
<td>76,828</td>
<td>2,091</td>
<td>57±0.1</td>
</tr>
<tr>
<td>96</td>
<td>191,908</td>
<td>105,336</td>
<td>4,495</td>
<td>122±0.1</td>
</tr>
<tr>
<td>128</td>
<td>253,042</td>
<td>166,470</td>
<td>8,445</td>
<td>230±0.1</td>
</tr>
</tbody>
</table>

Table 3. The complete evaluation using CIFAR-10. The RAM and flash footprints are the maximum memory allocation. Time refers to the average inference execution time. The energy consumption is based on the average electric current draw.

Table 4. The complete evaluation using CIFAR-10. The RAM and flash footprints are the maximum memory allocation. Time refers to the average inference execution time. The energy consumption is based on the average electric current draw.

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References