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Sensorless Capacitor Voltage Balancing of a Grid-Tied, Single-Phase Hybrid Multilevel Converter with Asymmetric Capacitor Voltages using Dynamic Programming

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***Abstract*—This paper shows a sensorless capacitor voltage balancing control approach for a grid-connected, single-phase hybrid multilevel inverter based on an NPC main stage with a voltage stiff DC-link and an arbitrary number of H-Bridge modules (capacitor modules) with asymmetric capacitor voltages. Using nearest-level control, a model predictive control (MPC) approach with a prediction horizon of one time step is chosen to find an optimal switching-state combination among the redundant switching combinations to balance the capacitor voltages as quick as possible. Using the Lyapunov stability criterion, it is shown that an offline calculated optimal switching-state sequence for each discrete output voltage level can be used to operate the inverter without using any voltage sensors for the capacitor voltages. To validate the stability of the approach, a laboratory inverter with a resistive load is operated with the offline calculated optimal switching-state sequences and it is shown that the capacitor voltages converge to their desired reference voltages.**

***Index Terms*—Modular multilevel converters, Multilevel systems.**

I. Introduction

Multilevel converters are commonly used for high voltage applications for power systems [1]–[3] or, sometimes, these are even suggested for large electric drives [4]–[6]. Lately, multilevel inverters are gaining in interest for low voltage applications ($V < 1\,\mathrm{kV}$) due to their advantages in comparison to two-level converters, for example fault-tolerant operation [7], [8], reduced common mode noise emissions [9] and the application of cheap low voltage MOSFETs [10]–[12]. Nonetheless, a major drawback is that the DC-sources are typically exposed to low order harmonics, which can be mitigated by different approaches [13]–[15].

In [16], the authors have presented a hybrid multilevel converter, similar as described in [17]. The additional series connected H-bridges, containing capacitor modules, should help to reduce the grid-filter size, when operated at the grid. The authors have presented a model predictive control approach, using a prediction horizon of one time step, for a hybrid multilevel converter. The presented approach determines the optimal switching-state combination among all redundant combinations to balance all capacitor voltages as fast as possible. However, as described in [16], all capacitor voltages are constantly measured.

In extension to [16], this paper shows that a series of offline calculated optimal switching-state sequences can be used to operate a hybrid converter with an arbitrary number of switched capacitor modules without actually measuring the capacitors' voltages. This kind of approach is commonly referred to as dynamic programming. The stability of the proposed approach is assessed using Lyapunov's stability criterion and a laboratory converter setup is operated with resistive load to demonstrate the control concept's validity.

II. Exponential Modular Multilevel Converter Basics

The topology of a grid-connected asymmetric hybrid multilevel converter based on an NPC main stage and n H-bridges, can be seen in Fig. 1. This topology is referred to as exponential modular multilevel converter (EMMC) [16]. For simplicity, a lossy L-filter with an inductance L_{filter} and a series resistance R_{filter} is chosen as a grid-filter within the scope of this paper's analysis. Besides a pure inductive filter, an LCL-filter, as for example described in [18], [19], could be chosen. To ensure not only the proper control of the active power flow, the DC link voltage V_{DC} must be larger than the peak value of the grid voltage ($V_{\mathrm{AC,pk}} = \sqrt{2} \cdot 230\,\mathrm{V}$) to control also the reactive power flow. For example, considering a sufficient control margin, it might be suitable to chose a DC link voltage of $V_{\mathrm{DC}} = 350\,\mathrm{V}$. The semiconductor switches of the main stage (NPC module) are operated in pairs and only adjacent switches should be activated at a time. If three switches in series are activated, as for example $S_{1,\mathrm{NPC}}$,$S_{2,\mathrm{NPC}}$ and $S_{3,\mathrm{NPC}}$, one DC

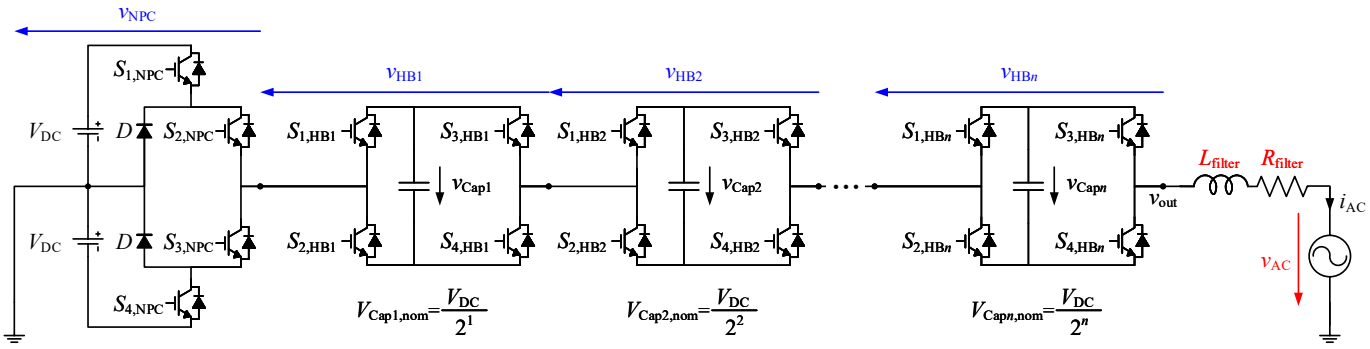

Fig. 1: Grid-connected, single-phase EMMC arrangement using an NPC module as the main stage.

source is short-circuited. Therefore, the switching-state of the NPC main stage relative to the individuals switches' states can be expressed as

$$S_{\mathrm{NPC}} = \{1, 0, -1\} = S_{1,\mathrm{NPC}} S_{2,\mathrm{NPC}} - S_{3,\mathrm{NPC}} S_{4,\mathrm{NPC}} \quad (1)$$

and, thus, the output voltage of the NPC stage becomes

$$v_{\mathrm{NPC}} = V_{\mathrm{DC}} S_{\mathrm{NPC}} \quad . \quad (2)$$

The nominal reference voltages of the series connected H-bridges are graded by a factor of 2. Similar to the NPC module, the switches of each H-bridge are operated in pairs. If the two upper ($S_{1,\mathrm{HB}i}$ and $S_{3,\mathrm{HB}i}$) or the two lower switches ($S_{2,\mathrm{HB}i}$ and $S_{4,\mathrm{HB}i}$) are activated, the voltage source (capacitor module) is bypassed. If the switches are operated diagonally, the corresponding voltage source (capacitor module) is inserted in forward ($S_{2,\mathrm{HB}i}$ and $S_{3,\mathrm{HB}i}$) and reverse ($S_{1,\mathrm{HB}i}$ and $S_{4,\mathrm{HB}i}$) direction into the phase strand, respectively. Consequently, the switching-state of each H-bridge relative to the individuals switches' states, can be expressed as

$$S_{\mathrm{HBi}} = \{1, 0, -1\} = S_{2,\mathrm{HB}i} S_{3,\mathrm{HB}i} - S_{1,\mathrm{HB}i} S_{4,\mathrm{HB}i} \quad , \quad (3)$$

which can be used to express the output voltage of each H-bridge according to

$$v_{\mathrm{HB}i} = \frac{V_{\mathrm{DC}}}{2^i} S_{\mathrm{HB}i} \quad (4)$$

with $i = 1, 2, ..., n$. Using (2) and (4) the output voltage of the EMMC can be expressed as

$$v_{\mathrm{out}} = V_{\mathrm{DC}} S_{\mathrm{NPC}} + \sum_{i=1}^{n} S_{\mathrm{HB}i} \frac{V_{\mathrm{DC}}}{2^i} \quad , \quad (5)$$

while the switching-state vector can be defined as

$$S_{\mathrm{EMMC}} = \begin{bmatrix} S_{\mathrm{NPC}} \\ S_{\mathrm{HB1}} \\ \vdots \\ S_{\mathrm{HB}n} \end{bmatrix}' \quad . \quad (6)$$

The modulation index can be calculated according to

$$M = \frac{v_{\mathrm{out}}}{V_{\mathrm{DC}}} \quad (7)$$

and it should be limited to a maximum of 1. With n H-bridge modules, the number of output voltage levels L can be expressed as

$$L = 2^{n+1} + 1 \quad . \quad (8)$$

Due to the fairly high number of output voltage levels, the desired sinusoidal output voltage shape can be easily generated using a fundamental frequency switching technique, for example nearest-level control [20].

III. Control of the EMMC

The current control scheme of the EMMC is depicted in Fig. 2. A detailed description about the current control and the sensorless capacitor balancing technique, using an offline calculated optimal switching-sequence, is given in the following section.

A. Current Control using a Proportional-Resonant Controller

The derivative of the output current i_{AC} can be expressed as

$$\frac{di_{\mathrm{AC}}}{dt} = -\frac{R_{\mathrm{filter}}}{L_{\mathrm{filter}}} i_{\mathrm{AC}} - \frac{1}{L_{\mathrm{filter}}} (v_{\mathrm{out}} - v_{\mathrm{AC}}) \quad (9)$$

with v_{out} as described in (6). Using the Laplace transform of (9), the current i_{AC} in relation to the output voltage v_{out} can be expressed in transfer-function form as

$$G_{\mathrm{p}}(s) = \frac{i_{\mathrm{AC}}}{v_{\mathrm{out}} - v_{\mathrm{AC}}} = \frac{1}{sL_{\mathrm{filter}} + R_{\mathrm{filter}}} \quad . \quad (10)$$

To control a sinusoidal single-phase current through the grid filter, a Proportional-Resonant (PR) controller, as described in [21], can be used. Its gain can be mathematically expressed as

$$G_{\mathrm{c}}(s) = K_{\mathrm{p}} + \frac{K_{\mathrm{i}} s}{s^2 + \omega_0} \quad . \quad (11)$$

Using the forward Euler method as described in [22],

$$\frac{1}{s} \rightarrow T_{\mathrm{s}} \frac{z^{-1}}{1 - z^{-1}} \quad , \quad (12)$$

the controller gain $G_{\mathrm{c}}(s)$ can be transformed into the z-domain, which results in

$$G_{\mathrm{c}}(z^{-1}) = K_{\mathrm{p}} + T_{\mathrm{s}} \frac{K_{\mathrm{i}} z^{-1}}{T_{\mathrm{s}}^2 \frac{z^{-2}}{1 - z^{-1}} - \omega_0 - \omega_0 z^{-1}} \quad . \quad (13)$$

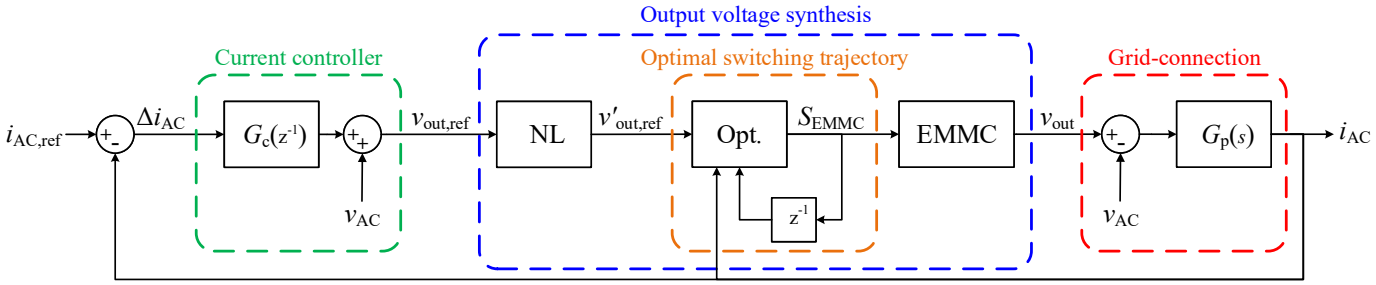

Fig. 2: Current control scheme of the EMMC.

The sample time T_s is the inverse of the switching frequency f_{sw} at which the entire converter leg is operated. The controller parameters K_i and K_p can be parametrized in a similar manner as for a PI-controller, for example as described in [20], [23]. To improve the performance of the current controller, the measured grid voltage v_{AC} can be used as feedforward term, as can be seen in Fig. 2. Hence, the current controller determines the required output voltage $v_{out,ref}$, which should be synthesized by the nearest discrete output voltage level $v'_{out,ref}$. Then a switching-state combination should be chosen and applied to actually output the required voltage.

B. Sensorless Capacitor Voltage Balancing using Dynamic Programming Approach

To properly control the current, the capacitor voltages must be balanced according to their nominal rating by the alternately selection of optimal switching-state combinations, as highlighted in orange in Fig. 2. In the following, a model predictive control approach with a prediction horizon of one time step is introduced to find the optimal switching-state vector to mitigate the capacitors' voltages imbalance within the next switching interval as much as possible.

The dynamics of the capacitors' voltages, according to Fig. 1, can be described as

$$\frac{dv_{Capi}}{dt} = -\frac{1}{C_i} S_{HBi} i_{AC} \tag{14}$$

with $i = 1, 2, ..., n$. The deviation of the capacitors' voltages relative to their nominal reference voltages can be expressed as

$$\Delta v_{Cap} = \begin{bmatrix} v_{Cap1} \\ v_{Cap2} \\ \vdots \\ v_{Capn} \end{bmatrix} - \begin{bmatrix} V_{Cap1,ref} \\ V_{Cap2,ref} \\ \vdots \\ V_{Capn,ref} \end{bmatrix} . \tag{15}$$

For each output voltage level of the EMMC, there are m switching-state combinations according to

$$S_{EMMCm} = \begin{bmatrix} S_{NPC,1} & S_{HB1,1} & \cdots & S_{HBn,1} \\ \vdots & \vdots & \ddots & \vdots \\ S_{NPC,m} & S_{HB1,m} & \cdots & S_{HBn,m} \end{bmatrix} . \tag{16}$$

TABLE I: Switching sate combinations for $v_{out} = \frac{V_{DC}}{2^4}$ and $n = 4$, which gives $m = 5$ possible combinations

$S_{NPC}\left(\frac{V_{DC}}{2^0}\right)$	$S_{HB1}\left(\frac{V_{DC}}{2^1}\right)$	$S_{HB2}\left(\frac{V_{DC}}{2^2}\right)$	$S_{HB3}\left(\frac{V_{DC}}{2^3}\right)$	$S_{HB4}\left(\frac{V_{DC}}{2^4}\right)$
1	-1	-1	-1	-1
0	1	-1	-1	-1
0	0	1	-1	-1
0	0	0	1	-1
0	0	0	0	1

Thus, considering just the switching-states of the H-bridges comprising the capacitor modules, S_{EMMCm} can be reduced to

$$S_{HBm} = \begin{bmatrix} S_{HB1,1} & \cdots & S_{HBn,1} \\ \vdots & \ddots & \vdots \\ S_{HB1,m} & \cdots & S_{HBn,m} \end{bmatrix} . \tag{17}$$

Consequently, the weighting vector W, relative to the direction of the current, to asses the effectiveness of each individual switching-state combination can be calculated as

$$W = \begin{cases} +S_{HBm} \cdot \Delta v_{Cap} & \text{for } i_{AC} \geq 0 \\ -S_{HBm} \cdot \Delta v_{Cap} & \text{for } i_{AC} < 0 \end{cases} . \tag{18}$$

Thus, the switching combination achieving the maximum value of W yields the optimal switching-state combination according to

$$\max(W) \rightarrow S_{opt} . \tag{19}$$

To understand the suggested approach better, a short example is given. The output voltage v_{out} should be $\frac{V_{DC}}{2^4}$ and the current is positive according to $i_{AC} \geq 0$. The number of H-bridge modules is $n = 4$. This results in $m = 5$ possible switching-state combinations as stated in TABLE I. Presumably, the first two capacitor modules are balanced, whereas the third and fourth show a deviation of $-1\,\mathrm{V}$ and $2\,\mathrm{V}$, respectively. Thus, the weighting vector can be calculated as

$$W = \begin{bmatrix} -1 & -1 & -1 & -1 \\ 1 & -1 & -1 & -1 \\ 0 & 1 & -1 & -1 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0\,\mathrm{V} \\ 0\,\mathrm{V} \\ -1\,\mathrm{V} \\ 2\,\mathrm{V} \end{bmatrix} , \tag{20}$$

which results in

$$W = \begin{bmatrix} -1\,\mathrm{V} \\ -1\,\mathrm{V} \\ 1\,\mathrm{V} \\ -3\,\mathrm{V} \\ 2\,\mathrm{V} \end{bmatrix} \quad . \tag{21}$$

Finally, the optimal switching-state combination becomes

$$S_{\mathrm{opt}} = [0\ 0\ 0\ 0\ 1] \quad . \tag{22}$$

The suggested approach can be used for each discrete output voltage level and a corresponding sequence of optimal switching-state combinations can be calculated offline and only the stored sequences can be used online without measuring the capacitor voltages, as shown in Fig. 2. This approach is referred to as dynamic programming.

IV. Stability of Dynamic Programming Approach

It is assumed that for some desired steady state current trajectory $i_{\mathrm{AC,ref}}$ the required optimal switching sequences S'_{NPC} and $S'_{\mathrm{HB}i}$, for achieving the necessary output voltage $v_{\mathrm{out}} = V_{\mathrm{DC}}\, S'_{\mathrm{NPC}} + \sum_{i=1}^{n} S'_{\mathrm{HB}i}\, v_{\mathrm{Cap}i}$, can be accurately generated. The developed converter system displays experimentally the following behavior: when driven by such optimal switching sequence, independent of the initial state, the system eventually reaches the desired current trajectory. This section is aimed in proving this behavior.

The considered system is described by the current i_{AC} and n capacitor voltages $v_{\mathrm{Cap}i}$, which represent together the state vector. The deviation between the actual state and the desired reference trajectory is described by

$$\Delta i_{\mathrm{AC}} = i_{\mathrm{AC}} - i_{\mathrm{AC,ref}} \tag{23}$$

and

$$\Delta v_{\mathrm{Cap}i} = v_{\mathrm{Cap}i} - v_{\mathrm{Cap}i,\mathrm{ref}} \quad . \tag{24}$$

The dynamics of the actual and the reference current, both driven by the same optimal switching sequences S'_{NPC} and $S'_{\mathrm{HB}i}$, are given by

$$\frac{di_{\mathrm{AC}}}{dt} = -\frac{R_{\mathrm{filter}}}{L_{\mathrm{filter}}} i_{\mathrm{AC}} - \frac{1}{L_{\mathrm{filter}}}(V_{\mathrm{DC}} S'_{\mathrm{NPC}} + \sum\nolimits_{i=1}^{n} S'_{\mathrm{HB}i} v_{\mathrm{Cap}i} - v_{\mathrm{AC}}) \tag{25}$$

and

$$\frac{di_{\mathrm{AC,ref}}}{dt} = -\frac{R_{\mathrm{filter}}}{L_{\mathrm{filter}}} i_{\mathrm{AC,ref}} - \frac{1}{L_{\mathrm{filter}}}(V_{\mathrm{DC}} S'_{\mathrm{NPC}} + \sum\nolimits_{i=1}^{n} S'_{\mathrm{HB}i} v_{\mathrm{Cap}i,\mathrm{ref}} - v_{\mathrm{AC}}) \quad , \tag{26}$$

respectively, such that the current error's dynamic becomes

$$\frac{d\Delta i_{\mathrm{AC}}}{dt} = -\frac{R_{\mathrm{filter}}}{L_{\mathrm{filter}}} \Delta i_{\mathrm{AC}} - \frac{1}{L_{\mathrm{filter}}} \sum\nolimits_{i=1}^{n} S'_{\mathrm{HB}i} \Delta v_{\mathrm{Cap}i} \quad . \tag{27}$$

Analogously, the dynamics of the actual and the reference capacitor voltages, both again driven by the same optimal switching sequences S'_{NPC} and $S'_{\mathrm{HB}i}$, are given by

$$\frac{dv_{\mathrm{Cap}i}}{dt} = -\frac{1}{C_i} S'_{\mathrm{HBi}} i_{\mathrm{AC}} \tag{28}$$

and

$$\frac{dv_{\mathrm{Cap}i,\mathrm{ref}}}{dt} = -\frac{1}{C_i} S'_{\mathrm{HBi}} i_{\mathrm{AC,ref}} \quad , \tag{29}$$

leading to the following dynamics for the capacitors' voltage errors

$$\frac{d\Delta v_{\mathrm{Cap}i}}{dt} = -\frac{1}{C_i} S'_{\mathrm{HBi}} \Delta i_{\mathrm{AC}} \quad . \tag{30}$$

The proof of the behavior mentioned at the beginning of this section is easily shown by introducing the following Lyapunov function $V = V(\Delta i_{\mathrm{AC}}, \Delta v_{\mathrm{Cap}i})$ according to

$$V = \frac{L_{\mathrm{filter}}}{2} (\Delta i_{\mathrm{AC}})^2 + \sum\nolimits_{i=1}^{n} \frac{C_i}{2} (\Delta v_{\mathrm{Cap}i})^2 \quad , \tag{31}$$

analogous in form to the total energy stored in the inductance and capacitances of the system. This function V is strictly positive as soon as some of the errors Δi_{AC} and/or $\Delta v_{\mathrm{Cap}i}$ do not vanish. According to (27) and (30) the time derivative of V shows that V is a non-increasing function

$$\frac{dV}{dt} = -R_{\mathrm{filter}} \Delta i_{\mathrm{AC}}^2 \quad . \tag{32}$$

Therefore, the system dynamics drive the Lyapunov function to lower values, decreasing all along Δi_{AC} and $\Delta v_{\mathrm{Cap}i}$, until reaching $\Delta i_{\mathrm{AC}} = 0$ which also yields $\sum_{i=1}^{n} S'_{\mathrm{HB}i}\, \Delta v_{\mathrm{Cap}i} = 0$. At this point $\Delta v_{\mathrm{Cap}i}$ also stops being reduced, according to (30), without necessarily implying $\Delta v_{\mathrm{Cap}i} = 0$. Nevertheless, since the switching sequence values $S'_{\mathrm{HB}i}$ change the whole time, the only way to satisfy $\sum_{i=1}^{n} S'_{\mathrm{HB}i}\, \Delta v_{\mathrm{Cap}i} = 0$ under these conditions at any time after reaching $\Delta i_{\mathrm{AC}} = 0$ is $\Delta v_{\mathrm{Cap}i} = 0$. In other words, the Lyapunov function (31) shows that when driving the converter system with the optimal switching sequence corresponding to some desired reference trajectory, such trajectory is achieved asymptotically

$$i_{\mathrm{AC}} \xrightarrow{t\to\infty} i_{\mathrm{AC,ref}} \quad \text{and} \quad v_{\mathrm{Cap}i} \xrightarrow{t\to\infty} v_{\mathrm{Cap}i,\mathrm{ref}} \quad . \tag{33}$$

This is the Lyapunov theorem ([24], chapter 3) applied to the considered converter dynamics. It is worth noting (although quite trivial) that the main ingredient in the previous proof is the existence of a nonvanishing (positive) resistance R_{AC}, which constantly dissipates power and thus ensures the Lyapunov function decrease.

V. Measurements

To validate the effectiveness of the introduced control approach, a laboratory converter setup, based on the power module demonstrators from Imperix Ltd., was used. All of the power modules' switches are IGBTs. The laboratory converter consists of an NPC main-stage, connected to two DC-sources, and four H-bridge modules. The DC-link voltages of the main stage were chosen to be $V_{\mathrm{DC}} = 350\,\mathrm{V}$. The converter was operated only with a resistive load ($L_{\mathrm{filter}} \approx 0$ and $V_{\mathrm{AC}} = 0$).

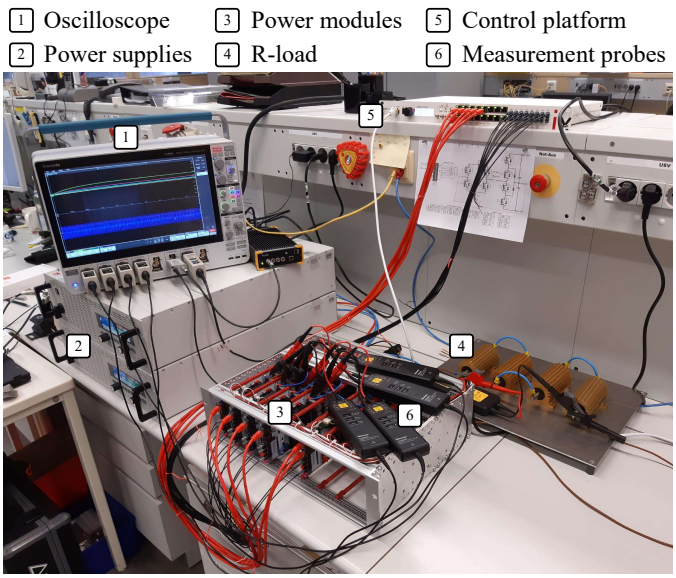

Fig. 3: Laboratory setup of the EMMC with one NPC main-stage and four H-bridge modules.

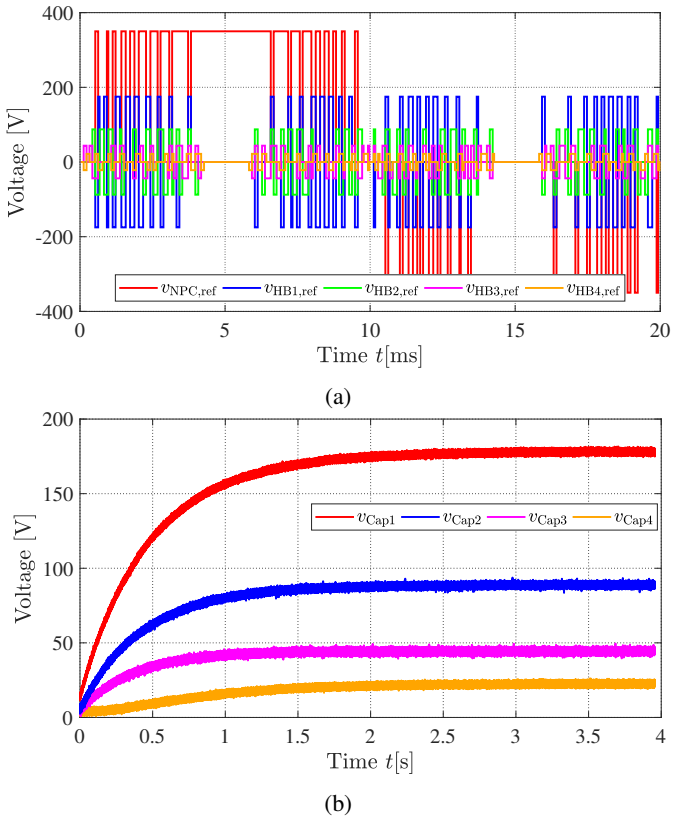

Fig. 4: (a) Ideal output voltages of the individual converter stages for one fundamental period based on the offline calculated optimal switching-state sequences and (b) measured charging process of the individual capacitor voltages.

The laboratory setup can be seen in Fig. 3. The current was controlled to about 8.5 A with a fundamental frequency of 50 Hz to reach a modulation index of one, achieving an output power of about 1.5 kW. Figure 4(a) shows the ideal output voltage waveforms (assuming $\Delta v_{\mathrm{Cap}i} = 0$) of the single stages of the converter to illustrate the applied switching sequence for the time duration of one electrical period. Initially, the capacitors were discharged. As can be seen from Fig. 4(b), within about 4 s the measured capacitor voltages converge to their required reference voltages, graded with a factor of two relative to the adjacent converter modules. The actual average switching frequencies of the individual converter stages for the switching sequence illustrated in Fig. 4(a) are listed in TABLE II. The NPC module is operated with about 1.85 kHz, while the H-bridges' switching frequency is doubled to about $\overline{f}_{\mathrm{sw,HB}i} \approx 3.9\,\mathrm{kHz}$. The measured output voltage v_{out} and current i_{AC} can be seen in Fig. 5. As depicted in the figure, the measured voltage distortion $THD_{\mathrm{v,meas}}$ is 6.48 %, which is higher than the ideal voltage distortion $THD_{\mathrm{v,ref}}$ of 2.52 %. The reason for this deviation is that the ideal voltage

TABLE II: Average switching frequency of the individual converter stages corresponding to the switching sequence illustrated in Fig. 4(a)

$\overline{f}_{\mathrm{sw,NPC}}$	$\overline{f}_{\mathrm{sw,HB1}}$	$\overline{f}_{\mathrm{sw,HB2}}$	$\overline{f}_{\mathrm{sw,HB3}}$	$\overline{f}_{\mathrm{sw,HB4}}$
1.85 kHz	3.75 kHz	3.80 kHz	4.05 kHz	4.00 kHz

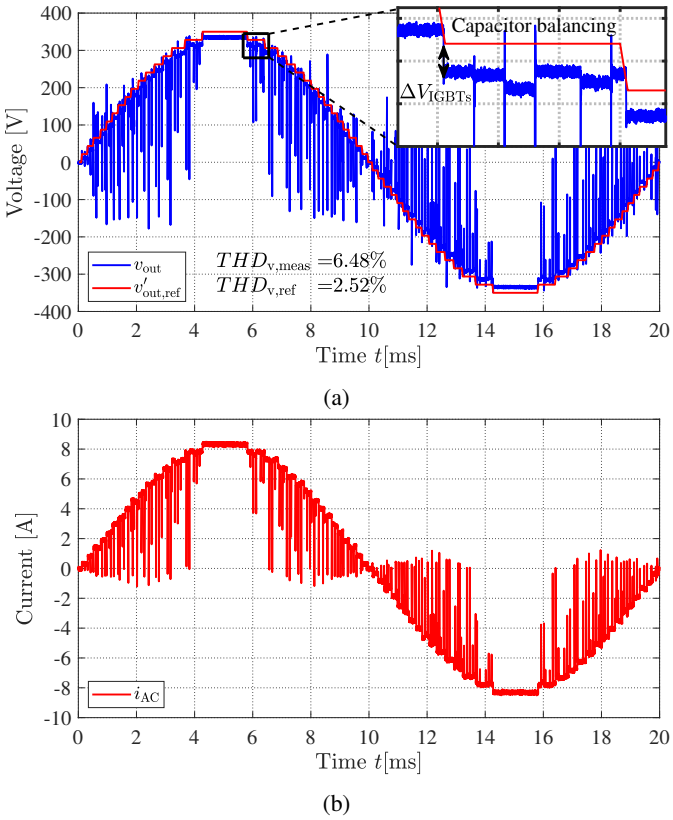

Fig. 5: (a) Measured output voltage v_{out} and (b) current i_{AC} with balanced capacitor voltages.

waveform does not consider the voltage drop across the IGBT switches and the occurring voltage dips, caused by the slight asynchronous executing of the switching-states of the NPC and H-bridge modules due to the usage of different gate-drive circuitries. Furthermore, the inset in Fig. 5(a) shows that the switching-state combination is constantly changing, even if the reference voltage level is the same, depending on the selected update time T_s. In this manner, the capacitors' are constantly being balanced. Since an almost pure resistive load is chosen, the current waveform, shown in Fig. 5(b), looks quite similar to the voltage waveform.

VI. Conclusion

This paper has presented a control approach for a single-phase, grid-tied hybrid multilevel converter with asymmetric capacitor voltages. A simple PR-controller is used for the current control and the output voltage is generated using nearest-level control. To ensure a proper current control, the capacitor voltages are balanced using dynamic programming. Meaning, an optimal sequence of switching-state sequences, based on a model predictive control approach with a prediction horizon of one time step, for each voltage level is calculated offline and applied online without measuring the capacitors' voltages. Using the Lyapunov stability criterion, it has been shown that the proposed control approach is asymptotically stable. To experimentally validate the derived stability of the control approach, a laboratory converter has been operated using a resistive load. It has been seen that the control approach charged all capacitors from zero to their set reference voltages and the desired output voltage waveform was properly generated.

Acknowledgment

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