



Artem Roey



Whether you realize it or not, we have witnessed the evolution of wireless communication technologies taking place in the last few decades. Services such as real-time video calls, which were originally accessible to TV reporters only, are now available for everyone. The tons of equipment previously required for establishing a video connection is now converged to a smartphone easily fitting our pocket. Moreover, the continuously developing high speed and low latency wireless networks enable new services such as self-driving cars and the internet of things, which would be integrated into our daily lives in the nearest future.

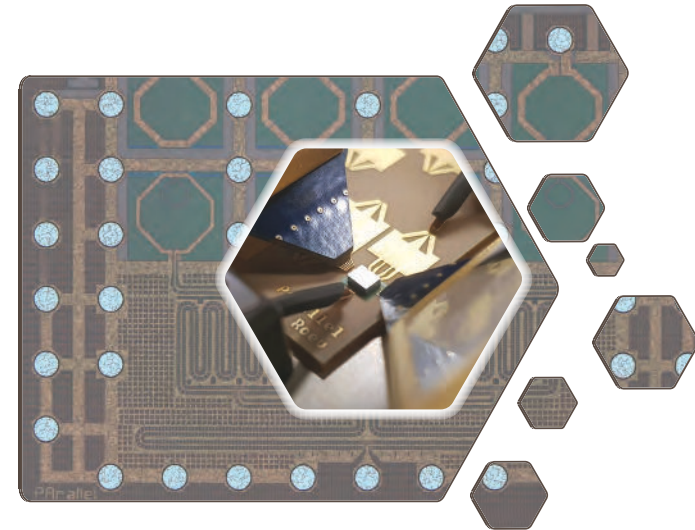
The evolution of wireless communications is driven by advances in radio hardware technologies, which need to offer us high-performance, energy-efficient, compact, and cost-effective solutions. The above targets are feasible at an individual metric level but are very challenging in combination. This thesis presents a non-conventional design approach for efficient and high-performance millimeter-wave power amplifiers (PAs), which are critical components of modern wireless systems. The focus of this work is on silicon-based technologies allowing a high level of integration at a reasonable cost but traditionally providing insufficient output power and energy efficiency limited by conventional power-combining approaches. The latter problems have been partly overcome by the proposed PA architecture based on a new efficient power-combining solution. The work evaluates the performance and scalability bounds of the architecture as well as presents its optimization flow for achieving optimal system-level performance by accounting for various multiphysics effects. Moreover, the proposed architecture has been demonstrated through an example of the combined PA implemented in an advanced high-speed SiGe process from NXP Semiconductors, which is one of the main industrial partners of this work. The developed PA has a wideband performance with both high efficiency and high output power, which outperforms the state-of-the-art silicon-based PAs.

I believe that the techniques and ideas proposed in this thesis will play an important role in sustainable wireless systems where high-performance, low energy consumption, and cost efficiency are important requirements.

ARTEM ROEY

Wideband Watt-Level Spatial Power-Combined Power Amplifier  
in SiGe BiCMOS Technology for Efficient mm-Wave Array Transmitters

2021



# Wideband Watt-Level Spatial Power-Combined Power Amplifier in SiGe BiCMOS Technology for Efficient mm-Wave Array Transmitters

ARTEM ROEY

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THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

# Wideband Watt-Level Spatial Power-Combined Power Amplifier in SiGe BiCMOS Technology for Efficient mm-Wave Array Transmitters

ARTEM ROEV



**CHALMERS**

Department of Electrical Engineering  
Antenna Group  
CHALMERS UNIVERSITY OF TECHNOLOGY

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*Front Cover:* The figure on the front cover illustrates the developed Watt-Level spatial power-combined power amplifier in SiGe BiCMOS technology.

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# Wideband Watt-Level Spatial Power-Combined Power Amplifier in SiGe BiCMOS Technology for Efficient mm-Wave Array Transmitters

## PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven,  
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door

ARTEM ROEV

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*Het onderzoek of ontwerp dat in dit proefschrift wordt beschreven is uitgevoerd in overeenstemming met de TU/e Gedragscode Wetenschapsbeoefening.*

Всей семье



# Abstract

The continued demand for high-speed wireless communications is driving the development of integrated high-power transmitters at millimeter wave (mm-Wave) frequencies. Si-based technologies allow achieving a high level of integration, but usually provide insufficient generated RF power to compensate for the increased propagation and material losses at mm-Wave bands due to the relatively low breakdown voltage of their devices. This problem can be reduced significantly if one could combine the power of multiple active devices on each antenna element. However, conventional on-chip power combining networks have inherently high insertion losses reducing transmitter efficiency and limiting its maximum achievable output power.

This work presents a non-conventional design approach for mm-Wave Si-based Watt-level power amplifiers that is based on novel power-combining architecture, where an array of parallel custom PA-cells suited on the same chip is interfaced to a single substrate integrated waveguide (to be a part of an antenna element). This allows one to directly excite  $TE_{m0}$  waveguide modes with high power through spatial power combining functionality, obviating the need for intermediate and potentially lossy on-chip power combiners. The proposed solution offers wide impedance bandwidth (50%) and low insertion losses (0.4 dB), which are virtually independent from the number of interfaced PA-cells. The work evaluates the scalability bounds of the architecture as well as discusses the critical effects of coupled non-identical PA-cells, which are efficiently reduced by employing on-chip isolation load resistors.

The proposed architecture has been demonstrated through an example of the combined PA with four differential cascode PA-cells suited on the same chip, which is flip-chip interconnected to the combiner placed on a laminate. This design is implemented in a 0.25  $\mu\text{m}$  SiGe BiCMOS technology. The PA-cell has a wideband performance (38.6%) with both high peak efficiency (30%) and high saturated output power (24.9 dBm), which is the highest reported output power level obtained without the use of circuit-level power combining in Si-based technologies at Ka-band. In order to achieve the optimal system-level performance of the combined PA, an EM-circuit-thermal optimization flow has been proposed, which accounts for various multiphysics effects occurring in the joint structure. The final PA achieves the peak PAE of 26.7% in combination with 30.8 dBm maximum saturated output power, which is the highest achievable output power in practical applications, where the 50- $\Omega$  load is placed on a laminate. The high efficiency ( $\geq 20\%$ ) and output power ( $\geq 29.8$  dBm) over a wide frequency range (30%) exceed the state-of-the-art in Si-based PAs.



**Keywords:** spatial power combining, array amplifiers, integration, RFIC, substrate integrated waveguide.

# Preface

This thesis is in partial fulfillment for the degree of Doctor of Philosophy at Chalmers University of Technology and Eindhoven University of Technology (TU/e).

The work resulting in this thesis was carried out between December 2016 and August 2021 at the Antenna Group, Department of Electrical Engineering, Chalmers and Integrated Circuits Group, Department of Electrical Engineering, TU/e. The doctoral program involved the industrial internships at SAAB AB (Gothenburg, Sweden) and NXP Semiconductors (Nijmegen, The Netherlands) - in a total duration of 21 months. Professor Marianna Ivashina of Chalmers is the main supervisor and examiner. Associate Professor Rob Maaskant of Chalmers is the co-supervisor. Professor Marion Matters-Kammerer of TU/e is the dual-degree promoter.

The work is a part of the Silicon-based Ka-band massive MIMO antenna systems for new telecommunication services (SILIKA) project, funded by the European Union's Horizon 2020 research and innovation program under the Marie Skłodowska Curie grant agreement №721732.



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My sincere gratitude goes to all the current and former members of the BL Smart Antenna Solutions group (NXP Semiconductors) I had the honor to work with during my more than 1.5-year industrial internship. In particular, I would thank Ir. Marcel Geurts for his support in problem-solving, responsiveness, and priceless lessons extending beyond the internship realms. I also wish to especially thank Dr. Jawad Qureshi for his expert advice, constructive feedback, and valuable time he spent teaching me. Successful development of the custom power amplifier in such a short period of time has not been possible without his technical insights and extensive experience. Furthermore, I would like to acknowledge Ir. Louis Praamsma, Dr. Xin Yang, Dr. Mustafa Acar, Ir. Jan Willem Bergman, Carlota Salamat and Alexander Simin, whose expertise and encouragement allowed me quickly learn Qubic process and prepare three successful designs for a single tape-out. In addition, I wish to thank Marcel Webers for supporting with the measurements and Ir. Arjen van der Helm from TCE-N Sample Services for assisting with the prototype assembly. Moreover, I will always be thankful to Parastoo Taghikhani, Marzieh SalarRahimi, Mohammad Hossein Moghaddam, and Dr. Eduardo Vilela Pinto dos Anjos for their kind friendship and invaluable help in many practical aspects during my stay in the Netherlands.

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Last but not least, I would like to express my deepest gratitude to my family for always being there for me, supporting me at every step I take.

# List of Publications

This thesis is based on the work contained in the following appended papers:

## Paper A

A. Roev, R. Maaskant, M. Ivashina, and A. Höök, “Wide-band spatially distributed TE<sub>10</sub> substrate integrated waveguide transition for high-power generation at mm-Wave frequencies,” in *Proceedings of the 2017 International Symposium on Antennas and Propagation (ISAP)*, Phuket, 2017, pp. 1-2.

## Paper B

A. Roev, R. Maaskant, A. Höök, and M. Ivashina, “Efficient millimeter-wave high power generation with spatial power-combined feeding element,” in *Proceedings of the 12th European Conference on Antennas and Propagation (EuCAP 2018)*, London, 2018, pp. 1-4.

## Paper C

A. Roev, R. Maaskant, A. Höök, and M. Ivashina, “Wideband mm-Wave transition between a coupled microstrip line array and SIW for high-power generation MMICs,” in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 10, pp. 867-869, Oct. 2018.

## Paper D

A. Roev, M. V. Ivashina, R. Maaskant, and M. K. Matters-Kammerer, “*N*-way spatial power combining in SIW for high power generation MMICs – scalability bounds,” in *Proceedings of the 2019 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Atlanta, GA, USA, 2019, pp. 1789-1790.

## Paper E

A. Roev, R. Maaskant, M. K. Matters-Kammerer, and M. V. Ivashina “High power mm-Wave spatial power combiner employing on-chip isolation resistors,” in *Proceedings of the 14th European Conference on Antennas and Propagation (EuCAP 2020)*, Copenhagen, 2020, pp. 1-5.



**Paper F**

A. Roev, P. Taghikhani, R. Maaskant, C. Fager, and M. Ivashina, “A wideband and low-loss spatial power combining module for mm-Wave high-power amplifiers,” in *IEEE Access*, vol. 8, pp. 194858-194867, 2020.

**Paper G**

A. Roev, J. Qureshi, M. Geurts, R. Maaskant, M. Matters-Kammerer, and M. Ivashina, “A wideband mm-Wave Watt-level spatial power-combined power amplifier with 26% PAE in SiGe BiCMOS technology,” in preparation for submission to *IEEE Transactions on Microwave Theory and Techniques*, vol. X, pp. XX-XX, 2021.

**Paper H**

A. Roev, R. Maaskant, M. Ivashina, “Transition arrangement between an SIW structure and a transmission line arrangement,” Swedish Patent application M1 P2SE00 AB/ab. Filled on: October 27, 2017.

*Other related publications of the Author not included in this thesis:*

- O. A. Iupikov, A. A. Roev and M. V. Ivashina, “Prediction of far-field pattern characteristics of phased array fed reflector antennas by modeling only a small part of the array – case study of spaceborne radiometer antennas,” in *Proceedings of the 2017 11th European Conference on Antennas and Propagation (EuCAP)*, Paris, 2017, pp. 2636-2639.

### **Thesis**

Some of the work presented in this thesis, such as text, figures, and tables may partly or fully be reused from [★], which is a part of the author’s doctoral studies.

- [★] A. Roev, “Compact and wideband spatial power combining module for mm-Wave high-power amplifiers,” Thesis for the Degree of Licentiate of Engineering, Department of Electrical Engineering, Antenna Group, Chalmers University of Technology, Gothenburg, 2020.



# Acronyms

3G	Third Generation
4G	Fourth Generation
5G	Fifth Generation
AG	Array Gain
B2B	Back-to-Back
BEOL	Back End of Line
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BW	Bandwidth
CB	Common Base
CE	Common Emitter
CPW	Coplanar Waveguide
CW	Continuous Wave
DC	Direct Current
DTI	Deep Trench Isolation
DUT	Device under Test
EIRP	Equivalent Isotropically Radiated Power
EM	Electromagnetic
ESD	Electrostatic Discharge
ETSI	European Telecommunications Standards Institute
FLA	Focal Line Array
FSPL	Free Space Path Loss
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GPPG	Ground-Power-Power-Ground
GSG	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor
HV	High Voltage
InP	Indium Phosphide
ISA	Irregular Sparse Array
JFOM	Johnson's Figure of Merit

LNA	Low Noise Amplifier
LTCC	Low Temperature Co-fired Ceramic
LV	Low Voltage
MIM	Metal-Insulator-Metal
MIMO	Multiple Input Multiple Output
ML	Microstrip Line
mm-Wave	Millimeter Wave
OSP	Organic Solderability Preservative
P1dB	1-dB Compression Point
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMS	Root Mean Square
Rx	Receive
SiGe	Silicon-Germanium
SIW	Substrate Integrated Waveguide
SNR	Signal to Noise Ratio
SOA	Safe Operating Area
SoC	System-on-Chip
SOLT	Short-Open-Load-Through
TE	Transverse Electric
TEM	Transverse Electromagnetic
TL	Transmission Line
TRL	Thru-Reflect-Line
Tx	Transmit
VNA	Vector Network Analyzer
WG	Waveguide

# Contents

<b>Abstract</b>	<b>i</b>
<b>Preface</b>	<b>iii</b>
<b>Acknowledgments</b>	<b>v</b>
<b>List of Publications</b>	<b>vii</b>
<b>Acronyms</b>	<b>xi</b>
<b>Contents</b>	<b>xiii</b>

## I Introductory Chapters

<b>1 Introduction</b>	<b>1</b>
1.1 Active Antenna Array Challenges at mm-Wave Frequencies . . . . .	2
1.1.1 Conventional Power Combining . . . . .	6
1.1.2 Integration with Antenna Elements . . . . .	9
1.2 Goal and Objectives . . . . .	10
<b>2 Spatial Power Combining in Substrate Integrated Waveguide</b>	<b>13</b>
2.1 Spatial Power Combining Techniques . . . . .	13
2.2 Substrate Integrated Waveguide . . . . .	15
2.2.1 Fundamental Characteristics . . . . .	16
2.2.2 Integration with Active Components . . . . .	18
2.2.3 Practical Implementation . . . . .	19
2.3 Transition between a Coupled Microstrip Line Array and Substrate Integrated Waveguide . . . . .	21
2.3.1 Scalability Bounds . . . . .	22



## CONTENTS

2.3.2	Numerical Validation . . . . .	23
2.3.3	Isolation Enhancement Technique . . . . .	26
2.3.4	Experimental Demonstration . . . . .	29
2.4	Conclusion . . . . .	32
<b>3</b>	<b>Spatial Power-Combining Module</b>	<b>33</b>
3.1	Design Description . . . . .	33
3.2	Critical Effects of Coupled Power Amplifiers . . . . .	35
3.3	Experimental Validation . . . . .	38
3.3.1	Fabricated Prototype . . . . .	38
3.3.2	Measurement Results . . . . .	39
3.4	Summary . . . . .	43
<b>4</b>	<b>Watt-Level mm-Wave SiGe Power Amplifier</b>	<b>45</b>
4.1	Power Amplifier Architecture . . . . .	46
4.2	Power Amplifier Cell . . . . .	47
4.2.1	Overall Design Description . . . . .	47
4.2.2	Active Circuitry . . . . .	50
4.2.3	Passive Circuitry . . . . .	52
4.2.4	ESD Protection Circuit . . . . .	55
4.2.5	Experimental Setup . . . . .	56
4.2.6	Measurement Results . . . . .	59
4.2.7	Summary . . . . .	63
4.3	Combined Power Amplifier . . . . .	65
4.3.1	Multiphysics Design Flow . . . . .	65
4.3.2	Fabrication and Assembly Considerations . . . . .	70
4.3.3	Experimental Setup . . . . .	74
4.3.4	Performance Evaluation . . . . .	77
4.4	Summary . . . . .	83
<b>5</b>	<b>Conclusions</b>	<b>89</b>
5.1	Summary and Achievements . . . . .	89
5.2	Future Perspectives . . . . .	91

## II Included Papers

<b>Paper A</b>	<b>Wide-Band Spatially Distributed TE<sub>10</sub> Substrate Integrated Waveguide Transition for High-Power Generation at mm-Wave Frequencies</b>	<b>113</b>
1	Introduction . . . . .	113
2	Design Details . . . . .	114

3	Numerical Results . . . . .	114
4	Conclusions . . . . .	116
5	Acknowledgment . . . . .	117
	References . . . . .	117
<b>Paper B Efficient Millimeter-Wave High Power Generation with Spatial Power-Combined Feeding Element</b>		<b>121</b>
1	Introduction . . . . .	121
2	Numerical Results . . . . .	122
3	Design of the Prototype . . . . .	127
4	Conclusion . . . . .	128
5	Acknowledgment . . . . .	128
	References . . . . .	128
<b>Paper C Wideband mm-Wave Transition between a Coupled Microstrip Line Array and SIW for High Power Generation MMICs</b>		<b>133</b>
1	Introduction . . . . .	133
2	Numerical Results . . . . .	135
3	Prototype and Measurement Results . . . . .	136
4	Conclusions . . . . .	138
	References . . . . .	139
<b>Paper D N-Way Spatial Power Combining in SIW for High Power Generation MMICs – Scalability Bounds</b>		<b>143</b>
1	Introduction . . . . .	143
2	Scalability Study . . . . .	143
3	Numerical Results . . . . .	145
	References . . . . .	147
<b>Paper E High Power mm-Wave Spatial Power Combiner Employing On-Chip Isolation Resistors</b>		<b>151</b>
1	Introduction . . . . .	151
2	Concept and Operation Principle . . . . .	152
3	Numerical Validation Results . . . . .	153
	3.1 Scattering Parameters . . . . .	154
	3.2 Total Performance in Presence of PAs . . . . .	155
4	Conclusion . . . . .	158
	References . . . . .	158
<b>Paper F A Wideband and Low-Loss Spatial Power Combining Module for mm-Wave High-Power Amplifiers</b>		<b>163</b>
1	Introduction . . . . .	163

## CONTENTS

2	Design of the Power Combining Module Including the Effects of PAs .	165
3	Measurement Results . . . . .	173
3.1	Input Impedance Matching . . . . .	173
3.2	Radiation Pattern . . . . .	175
3.3	Power Combining . . . . .	175
4	Conclusion . . . . .	178
	References . . . . .	178
 <b>Paper G A wideband mm-Wave Watt-level spatial power-combined power amplifier with 26% PAE in SiGe BiCMOS technology 185</b>		
1	Introduction . . . . .	185
2	Design Flow . . . . .	187
3	Power Amplifier Unit Cell . . . . .	188
3.1	Circuit Design . . . . .	189
3.2	Measurement Results . . . . .	191
4	Combined Power Amplifier . . . . .	192
4.1	Description of the Architecture . . . . .	192
4.2	Joint EM-Circuit-Thermal Optimization . . . . .	193
4.3	Spatial Power Combiner . . . . .	196
4.4	Measurement Results of the Combined Power Amplifier . . . .	199
5	Discussion . . . . .	203
6	Conclusion . . . . .	204
	References . . . . .	205
 <b>Paper H Transition Arrangement between an SIW Structure and a Transmission Line Arrangement 211</b>		
1	Technical Field . . . . .	211
2	Background . . . . .	211
3	Summary . . . . .	212
4	Brief Description of the Drawings . . . . .	213
5	Detailed Description . . . . .	213
6	Claims . . . . .	217
	References . . . . .	218
 <b>Curriculum Vitae</b>		<b>219</b>

# Part I

## Introductory Chapters



# Introduction

Historically, the millimeter wave (mm-Wave) spectrum has been mostly allocated for radar applications, however, the increasing demand in high speed and low latency wireless data channels has led to the exploitation of the possibilities of launching communication services at Ka-band (26–40 GHz) and beyond [1]. The achievable data rate over a wireless channel is mostly determined by four factors: bandwidth, signal-to-noise ratio (SNR), modulation scheme, and whether spatially separated data paths are exploited. These fundamental relations are expressed in the Shannon-Hartley theorem [2]:

$$C_{\max} = N_p B \log_2(1 + \text{SNR}). \quad (1.1)$$

This theorem establishes the maximum data rate ( $C_{\max}$ ) at which error-free information can be transmitted over the channel with a certain bandwidth ( $B$ ) and SNR. Factor  $N_p$  represents the number of independent data paths. In order to compensate for the limited channel bandwidth of the third generation (3G) and its successor – the fourth generation (4G) communication systems – the wireless industry has started to explore more advanced methods and new technologies. In particular, the multiple-input multiple-output (MIMO) technique allows us to increase the data rate of a wireless link using multiple transmitting and receiving antennas to exploit multipath effects of the channel efficiently [3]. The performance of such MIMO systems is critically dependent on the availability of uncorrelated paths. In practice, for a limited array antenna area, continuous increase in the number of antennas and, hence, spatial channels, does not necessarily lead to significantly higher data rates. This is the consequence of the spatial correlation between multiple paths as well as increased antenna mutual coupling effects [4]. Furthermore, improvement of SNR in 3G/4G communication systems by increased transmitter output power is restricted according to applicable electromagnetic (EM) fields exposure limits [5]. Therefore, to further increase the data rate, a wider frequency bandwidth is required [6]. However, such a wide bandwidth is not available at existing sub-6 GHz communication bands.

As a result, mm-Waves is a key enabler for high data rate fifth-generation (5G)



communication networks by providing a wide frequency spectrum [7]. Despite the obvious advantage of a large available spectrum, using mm-Wave bands are accompanied by many technological challenges. Mainly, this is due to the increased propagation and material loss, as well as limitations of existing semiconductor processes [8].

## 1.1 Active Antenna Array Challenges at mm-Wave Frequencies

In order to indicate the main technological challenges in wireless networks at mm-Wave frequencies and to explore possible solutions, a basic link budget analysis is essential. For this purpose a downlink scenario assuming a base station with 1000 m reach in a suburban deployment at 28 GHz is examined. The block diagram of a wireless link system example is shown in Figure 1.1 [9]. The chosen 100 MHz

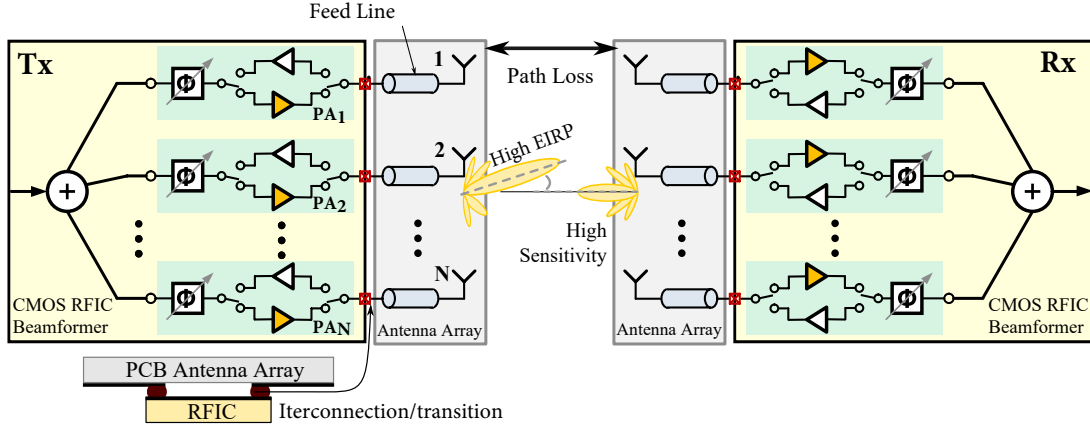


Figure 1.1: Block diagram of a mm-Wave wireless link system employing  $N$ -channel beamforming RFIC in downlink scenario.

bandwidth results in  $-84$  dBm receiver sensitivity [10, 11]. The required SNR for quadrature amplitude modulation with 16 points in the grid (16-QAM) is 8 dB [10, 12]. The receiver antenna gain is 17 dB. The required total equivalent isotropic radiated power (EIRP) can be determined as:

$$\text{EIRP}_{\text{dBm}} = \text{Receiver Sensitivity} + \text{SNR} - \text{Rx Antenna Gain} + \text{Path Loss}. \quad (1.2)$$

The path loss in the idealistic case (lossless medium) might be represented by free-space path loss (FSPL), caused by the spherical expansion of the wavefront in free space [13]:

$$\text{FSPL}_{\text{dB}} = 20 \log_{10} \left( \frac{\lambda}{4\pi R} \right), \quad (1.3)$$

where  $\lambda$  is the wavelength in free space, and  $R$  is the distance between the transmitting and the receiving antennas. The shift from conventional 3G/4G operation bands

### 1.1. ACTIVE ANTENNA ARRAY CHALLENGES AT MM-WAVE FREQUENCIES

towards mm-Wave implies more than  $10\times$  wavelength reduction, which leads to more than 20 dB higher FSPL. Moreover, absorption losses in different mediums are increased at mm-Wave frequencies. Rain, fog, and water vapor exacerbate this loss [14]. In the present scenario, the estimated path loss is in the order of 133–156 dB [10,15]. Given the calculations above, the required total EIRP for the transmit side is between 40 and 63 dBm (see Table 1.1) [16].

Table 1.1: Downlink link budget at 28 GHz

Parameter	Assumptions	Value
Receiver Sensitivity Limit	100 MHz	−84 dBm
Required SNR	16-QAM	8 dB
Total Array Gain	16 Elements	17 dB
Estimated Path Loss	1000 m	133–156 dB
Required Transmitted EIRP	-	40–63 dBm

The next question is how to realize the required EIRP by the transmitter? From the transmitter perspective, EIRP is defined as:

$$\text{EIRP}_{\text{dBm}} = P_t + G_A - L, \quad (1.4)$$

where  $P_t$  is the RF power supplied to transmitting antenna in dBm,  $G_A$  is the antenna gain in a given direction relative to an isotropic antenna in dBi, the term  $L$  represents losses at the interconnections and feeding lines in dB. In order to realize the required EIRP in specific directions corresponding to the positions of users, mm-Wave transmitters exploit a phased-array architecture [17]. Figure 1.1 shows an RF integrated circuit (RFIC) containing  $N$  independent RF branches each of which is interfaced with the corresponding antenna element. In the transmit mode, each RF branch is formed by a tunable phase shifter and power amplifier (PA). The beam steering functionality is realized by setting corresponding phase coefficients in each RF branch.

The gain of an antenna array  $G_A$  is produced by its individual element gain  $G_{\text{el}}$  and the array gain AG, representing the array configuration effects. There are different promising unconventional antenna array architectures, such as irregular sparse arrays (ISAs) [18,19] and focal line arrays (FLAs) [20,21]. The unconventional array architectures allow for more degrees of freedom in the design, but are not established technologies yet. In the present analysis a conventional uniform array architecture is employed. The array gain of the antenna array with uniformly-spaced identical elements is defined by element spacing  $d$  [22]. The individual element gain in an idealistic case is dependent on the effective aperture area  $A_{\text{eff}}$  only [22]. The above relations are summarized in (1.5).

$$G_{\text{el}} = 10 \log_{10} \left( \frac{4\pi A_{\text{eff}}}{\lambda^2} \right)$$

$$G_A = G_{\text{el}} + \text{AG} , \text{ where} \quad (1.5)$$

$$\text{AG} = 10 \log_{10} \left( \frac{2Nd}{\lambda} \right) \Big|_{d < \lambda \ll Nd}$$

However, to prevent unwanted grating lobes in wide-scan antenna arrays ( $\pm 45^\circ$  or larger), element spacing  $d$  must not exceed  $\lambda/2$ . Taking that into account, array gain becomes  $\text{AG}|_{d=\lambda/2} = 10 \log_{10}(N)$ . The half-wavelength spacing also limits the aperture size of antenna elements and, hence, individual gain  $G_{\text{el}} \leq 5$  dBi. Increasing the number of antenna elements  $N$  requires more PAs. Assuming each individual PA operates at an output power of  $P_{\text{out}}$ , the total power accepted by the transmitting antenna can be expressed as:

$$P_t = P_{\text{out}} + 10 \log_{10}(N). \quad (1.6)$$

Therefore, for the assumed scenario the transmitter EIRP can be written as:

$$\text{EIRP}_{\text{dBm}} = P_{\text{out}} - L + G_{\text{el}} + 20 \log_{10}(N), \text{ where } G_{\text{el}} \leq 5 \text{ dBi}. \quad (1.7)$$

As one can see from Equation 1.7, there are three intuitive ways to improve EIRP:

1. Increase the number of antenna elements ( $N$ );
2. Employ high-power PAs;
3. Reduce interconnection losses ( $L$ ).

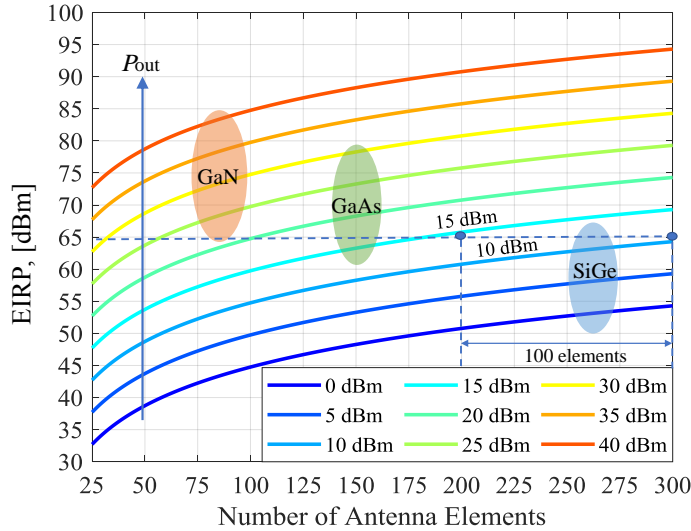


Figure 1.2: EIRP as a function of the number of antenna elements ( $N$ ) in the uniform array. The set of curves corresponds to different  $P_{\text{out}}$ . The colored regions indicate the typical  $P_{\text{out}}$  at Ka-band for different semiconductor technologies.

### 1.1. ACTIVE ANTENNA ARRAY CHALLENGES AT MM-WAVE FREQUENCIES

Figure 1.2 shows the EIRP as a function of the number of antenna elements for different PA output power levels. At the desired EIRP levels, increasing the individual PA output power by 5 dBm is equivalent to adding 100 extra antenna elements in a large-scale antenna array ( $N \geq 150$ ). The latter is not practical since it occupies more area and requires a lot of additional beamforming branches. Hence, the system becomes more expensive and less reliable.

Therefore, using a high-power PA ( $P_{\text{out}} \geq 25\text{--}30$  dBm) per single antenna element and minimizing interconnection losses between them allows one to efficiently generate the desired EIRP, and hence, to compensate for the increased path loss at higher frequencies. However, existing loss minimization techniques demonstrate a trade-off between their power enhancement and relative bandwidth [23]. In particular, a direct matching approach in [24] obviates the need for a potentially lossy impedance matching network and demonstrates 20% higher output power but offers 5% bandwidth only.

Although the continued growth of new applications drives the semiconductor industry towards more cost-effective solutions for mm-Wave, an efficient generation of high-power is still challenging at these frequencies [25–29]. In order to characterize and compare the performance of semiconductor materials for high-power applications at mm-Wave frequencies, Johnson’s figure of merit (JFoM) can be used [30]. It includes the most critical parameters of materials: the charge carrier saturation

Table 1.2: Properties of the typical semiconductor materials

Material	Saturation velocity, [ $\times 10^4$ m/s]	Breakdown field, [MV/cm]	JFoM normalized to Si
Si	1.0	0.3	1.0
GaAs	1.5	0.4	2.7
InP	0.7	0.5	20
GaN	2.5	3.3	27

velocity in the material and the electric breakdown field. The latter directly defines the amount of power, which a semiconductor device could bring to the load. As is clear from Table 1.2, III-V compound semiconductors (GaN, GaAs, InP) can potentially generate more power at mm-Wave frequencies in comparison with silicon (Si) [31–34]. However, their relatively low thermal conductivity (compared to Si) restricts the maximum power density, which results in devices with larger areas. The relatively lower level of integration for III-V compound devices has limited their mainstream use. From a cost perspective, GaAs and GaN technologies are more expensive for high volumes, mainly due to their smaller wafer size.

In cellular communications, where compactness and cost-effectiveness are important, silicon technologies are becoming attractive alternatives [35, 36]. The high integration capability of Si technologies allows designing multi-functional chips con-

taining independent Tx/Rx beamforming branches as well as a digital control interface [37–41]. However, due to the fundamental material properties (See Table 1.2), the generation of 25 – 30 dBm output powers is very challenging for silicon technologies and requires non-conventional design solutions.

### 1.1.1 Conventional Power Combining

The maximum output power limitation of a single Si transistor might be overcome by combining the power of multiple active devices on each antenna array element [42–46]. Traditionally, on-chip power combining is categorized by the scale of integration. It might be device-level or circuit-level [47].

The device-level power combining is based on parallelization or stacking (and sometimes both) identical transistors in a region whose extent is small compared to one wavelength, and is generally limited to the number of devices that can be combined efficiently. Placing multiple transistors in parallel (See Figure 1.3) allows one to increase the output current, but it is also accompanied by a proportional reduction of the output load impedance [48–50]. It means that an additional matching circuit with a high transformation ratio is needed. Stacking multiple transistors leads

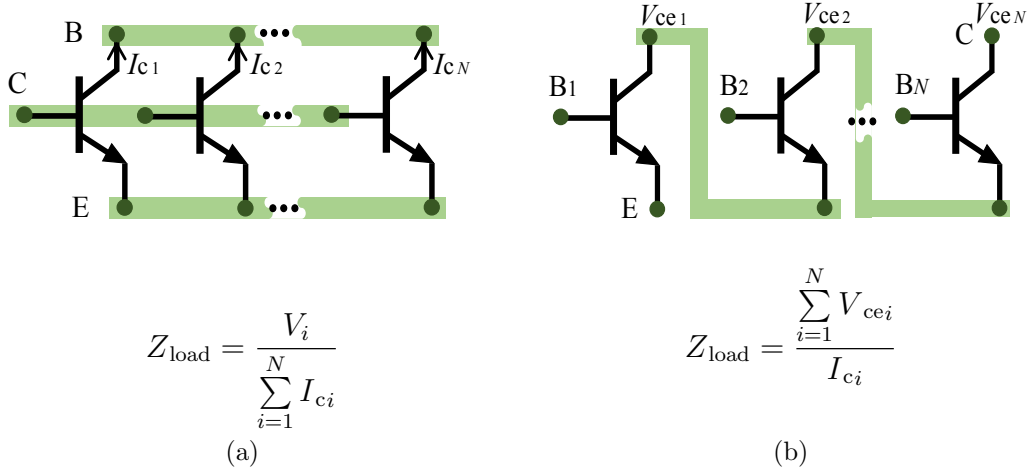


Figure 1.3: Device-level power combining: (a) Parallelization; (b) Stacking.

to the output voltage and optimal load impedance increasing. The latter is usually desired since individual high-power devices have intrinsically low optimal impedance. However, in practice, the number of stacked transistors is limited due to the increasing complexity of interconnection topology and difficulty to minimize parasitic effects [51–53]. The device-level power combining is efficient at sub-6 GHz frequencies. At mm-Wave frequencies, spatially distributed effects in the interconnecting and routing lines become significant. This causes the transistors to operate differently from each other, which leads to the reduction of output power, efficiency, and gain. Moreover, when

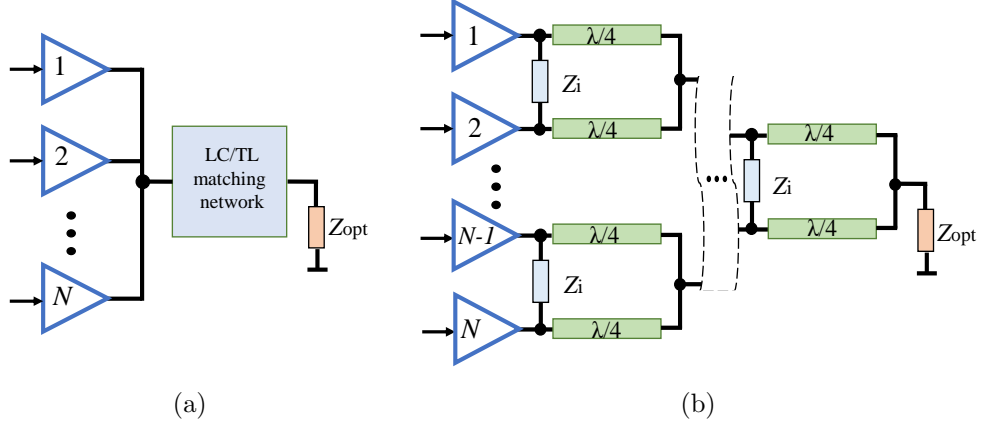


Figure 1.4: Conventional circuit-level power combiners: (a) Non-Isolated current combiner; (b) Wilkinson combiner based on transmission lines.

the devices are closely spaced, mutual thermal coupling between them increases, which might cause a thermal breakdown [54]. Thereby, the number of the combined devices ( $N$ ) usually does not exceed 5, which corresponds to  $\leq 6.9$  dB relative power increase [49, 51, 52].

To overcome the above interconnect and thermal issues, circuit-level power combining is based on combining multiple smaller independent PA-cells. Figure 1.4 (a) shows a non-isolated current combiner, where the outputs of the  $N$  individual PA-cells are simply connected to a single point. This approach is similar to the device-level parallelization (Fig. 1.3 (a)) and also requires an additional matching circuit. Increasing the number of interfaced PAs results in the higher impedance transformation ratio, and hence the output matching circuit becomes more complex, especially if a wide bandwidth is required [55]. Wideband operation is usually achieved by using multi-stage matching networks, which intrinsically occupy more areas and have higher losses. Another challenge is the mutual coupling between the combiner input ports, which might negatively affect the individual PA-cell behavior. The latter is addressed in Wilkinson power combiners with isolation load resistors [56–58]. Figure 1.4 (b) shows an example of a planar Wilkinson combiner using traditionally  $\lambda/4$  transmission lines (TLs). The cascade connection of two-way Wilkinson power combiners can provide an  $N$ -way combining; however, increasing the number of inputs is accompanied by higher losses in the series-connected  $\lambda/4$  TLs. This fact constrains the relative increase of power after combining, which is expressed as:

$$\text{Relative Power Increase}_{\text{dB}} = 10 \log_{10}(N) - L_{\lambda/4} \log_2(N), \quad (1.8)$$

where  $L_{\lambda/4}$  represents insertion losses in a single TL with electrical length  $\lambda/4$ . Figure 1.5 shows the relative increase of output power as a function of the number of interfaced PAs. The set of curves correspond to different insertion losses of the  $\lambda/4$  TLs. In the lossless case (blue line), the output power is proportional to the number

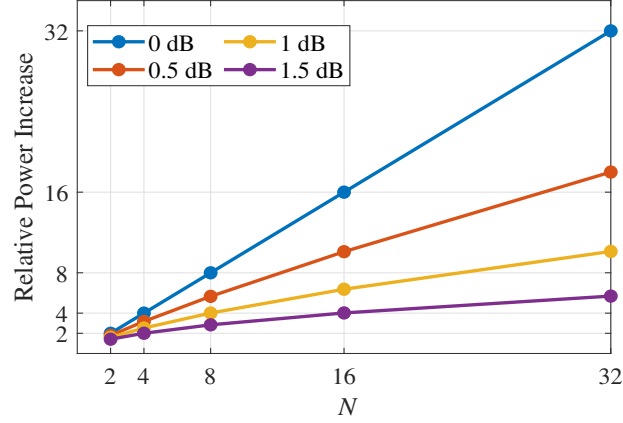


Figure 1.5: Relative power increase as a function of number of interconnecting PA-cells ( $N$ ). The set of curves correspond to different losses of the  $\lambda/4$  TLs.

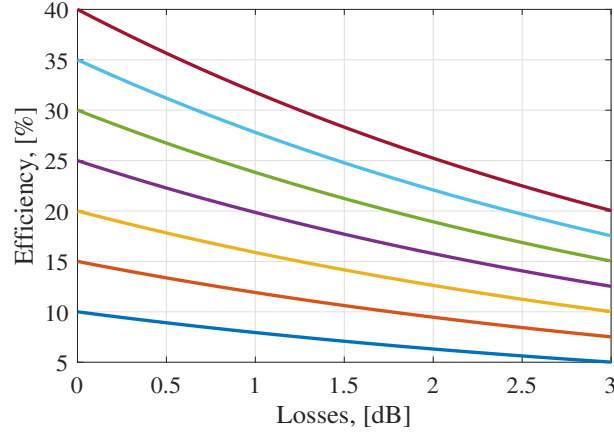


Figure 1.6: Efficiency as a function of insertion losses in the output power combiner. The set of curves corresponds to the efficiency of an individual PA-cell (lossless combining).

of PA-cells. However, in the presence of losses, increasing of the number of PAs does not help to significant increase the output power [59, 60].

Besides the maximum output power limitation, the combiner losses cause a significant reduction of the combined PA efficiency, which is a ratio between the output RF power and the total DC power taken from a supply source. This effect is exemplified in Figure 1.6, showing the combined PA efficiency as a function of insertion losses in the output power combiner. In the case of an ideal (lossless) power combiner, the efficiency of the combined PA is equal to the efficiency of its individual PA-cell, which corresponds to the points on the y-axis. Increasing the combiner insertion losses leads to the output power reduction while the DC power consumption remains the same. As a result, a significant efficiency degradation is observed, especially for the PA-cell with initially high efficiency (dark red curve). For example, the insertion losses of

### 1.1. ACTIVE ANTENNA ARRAY CHALLENGES AT MM-WAVE FREQUENCIES

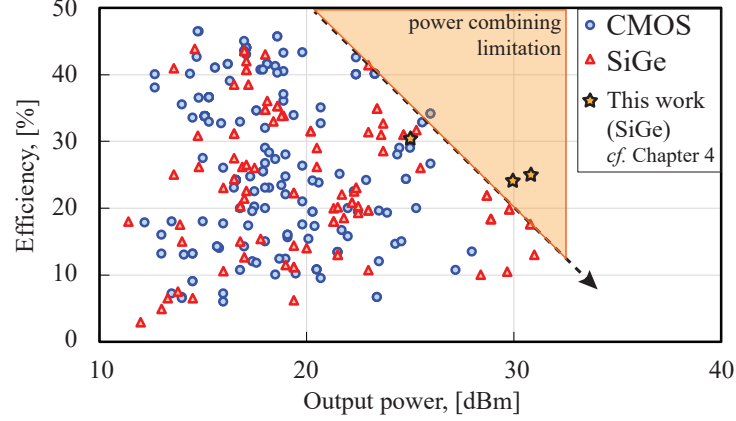


Figure 1.7: Performance of the reported state-of-the-art Si-based PAs at Ka/V-band: efficiency versus saturated output power [61].

2 dB lead to the efficiency drop from 40% to 25% for the PA-cell with initially high efficiency, whereas the PA-cell with initially low efficiency (light red curve) demonstrates the efficiency reduction from 15% to 10% only. Since conventional circuit-level on-chip power combiners are intrinsically lossy due to the Si substrate [60, 62, 63], the existing combined PAs demonstrate a trade-off between the output power and efficiency. Figure 1.7 shows the performance of the reported state-of-the-art Si-based PAs at Ka/V-band in the efficiency-power coordinate plane. Although the reported PAs with output power less than 24 dBm demonstrate relatively high efficiency, the Watt-level PAs have very limited efficiency ( $\leq 18\%$ ) caused by the lossy power combiners. Therefore, new power-combining solutions and PA architectures are required for facilitating efficient high-power generation at mm-Wave frequencies.

#### 1.1.2 Integration with Antenna Elements

Besides the employment of high-power PAs, reaching the desired EIRP level requires minimization of interconnection losses between active devices and antenna elements. In the perspective of integration with active components, planar TL structures such as microstrip line (ML), coplanar waveguide (CPW), and stripline offer a compact and cost-efficient solution (See Figure 1.8 (a)). However, these TLs suffer from high dielectric and ohmic losses as well as radiation leakage, especially at mm-Wave frequencies [64].

Moreover, parasitic field radiation by bent planar TLs might cause undesired coupling between adjacent RF branches, and hence, affect the performance of active components [65]. In contrast, conventional hollow metal waveguides (WGs) have intrinsically low insertion losses and perfect isolation, however it is difficult to combine with active components (See Figure 1.8 (b)). It also requires a good electrical contact between metal blocks. The latter might be partly overcome by using the gap wave-



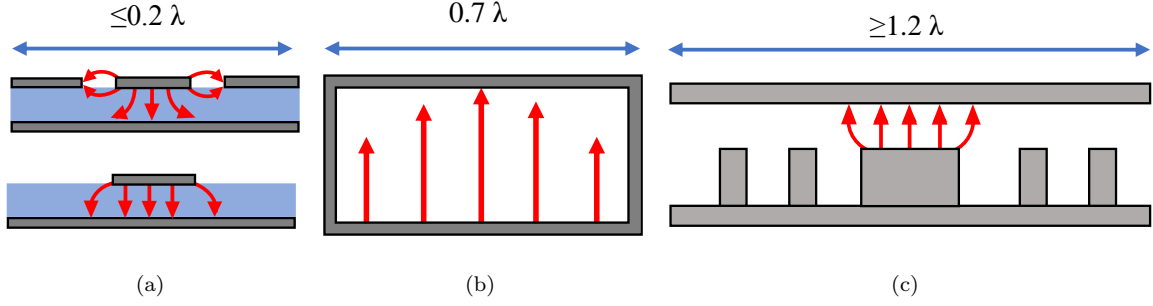


Figure 1.8: Transmission lines and fundamental E-field mode distribution: (a) CPW and ML planar TLs; (b) Hollow metal rectangular WG; (c) Ridge gap WG.

uide technology [66], but it has limited application in dense beam-steering antenna arrays since it requires more space in order to realize artificial magnetic conductors as shown in Figure 1.8 (c).

Despite the huge amount of challenges, mm-Wave offers a wide variety of integration options in comparison with conventional sub-6 GHz bands. At mm-Wave frequencies the size of antennas becomes compatible with RFICs size. This fact allows to make an antenna as a part of a package or even integrate it into an RFIC back-end [67–69].

## 1.2 Goal and Objectives

In view of the aforementioned motivation, this work aims to develop and experimentally demonstrate new power combining and integration solutions for efficient Watt-level mm-Wave transmitters in Si-based technologies. Several objectives are established to achieve this aim:

**Objective 1.** Develop a new power combining architecture eliminating the need for the intermediate and potentially lossy on-chip combiners by directly interfacing an array of PAs to a single radiation element;

- Investigate architecture constraints and scalability bounds;
- Analyze the critical effects of interconnected PAs in different operating regimes (linear and non-linear regimes);
- Explore possibilities of integration with existing antenna elements, in particular elements in SIW technology.

**Objective 2.** Design a combined Watt-level PA using a new architecture, demonstrating both high output power and high efficiency over a wide frequency bandwidth. The focus of the design is on an advanced high-speed SiGe process from NXP Semiconductors, which is one of the main industrial partners of the Silika project [70].

- Design a custom PA-cell suitable for the new PA architecture;
- Develop a new EM-circuit-thermal design flow capable of taking account of various multiphysics effects occurring in the joint structure containing multiple PA-cells;
- Develop a combined PA prototype to evaluate its performance as well as to explore the architecture sensitivity to assembly and fabrication imperfections.

Throughout this work, the main performance targets are high output power and energy efficiency in combination with a wide operation bandwidth and a compact size for potential applications in dense antenna arrays with electrically small inter-element distance.



# Spatial Power Combining in Substrate Integrated Waveguide

This chapter outlines the principle of operation and the design methodology of the proposed compact spatial power combining transition between an array of amplifiers and a single substrate integrated waveguide (SIW). This concept is validated through measurements of the fabricated passive back-to-back transition.

## 2.1 Spatial Power Combining Techniques

As an alternative to the conventional device-level and circuit-level power combining, quasi-optical or spatial power combining techniques are becoming more and more attractive as the interest in mm-Wave frequency applications is growing. [47, 59, 71–74]. Spatial power combining is an essential part of quasi-optical amplifiers, as for example shown in Figure 2.1 (a), where the spatially distributed electromagnetic wave is coupled to the space-fed array of PAs, amplified, and transmitted directly to the radiating element.

Spatial power combiners have a number of advantages over conventional circuit-level solutions [47]:

- *Intrinsically low insertion losses*, which do not increase significantly when increasing the number of combined PAs.
- *High maximum achievable output power* (as a result of the constant insertion losses). The maximum number of interfaced PAs is constrained by the physical limitations of the architecture only.
- *Direct integration with an antenna element*. A spatially distributed output wave can be directly fed to the radiation element without using any intermediate transitions that are potentially bulky and lossy.

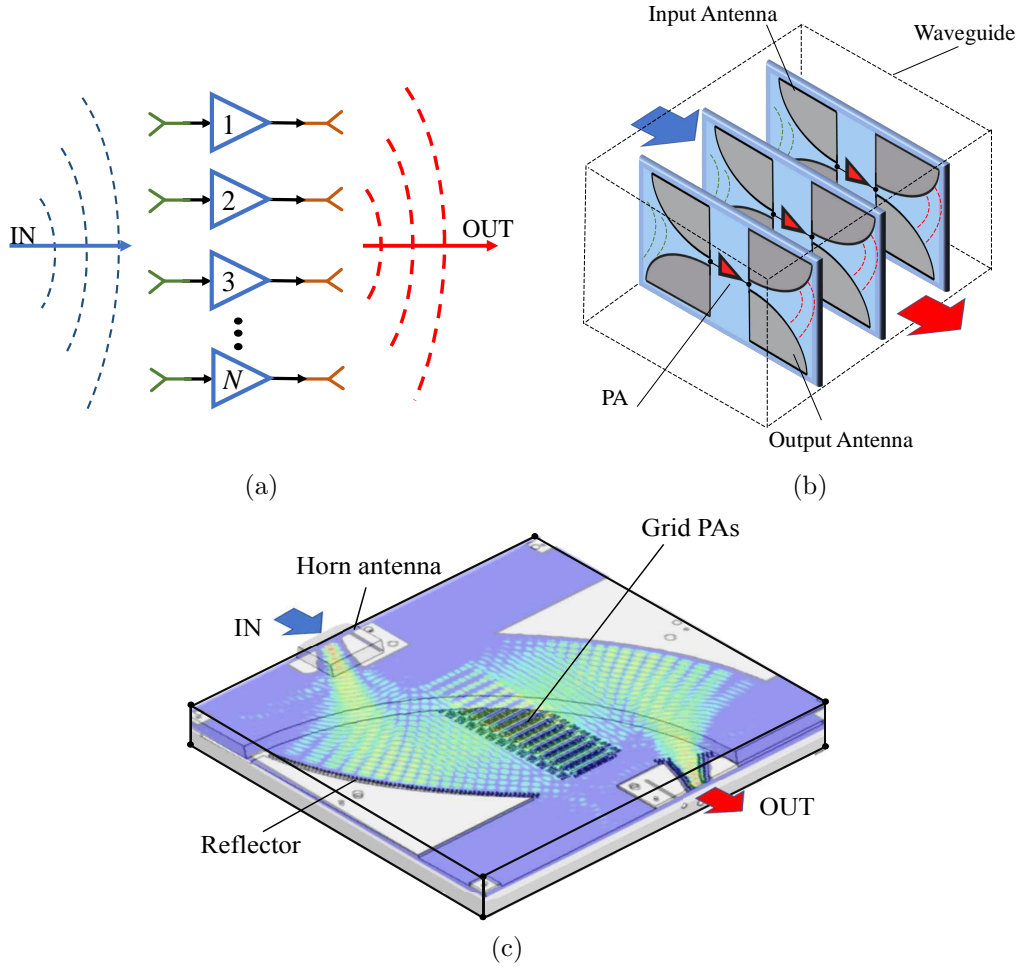


Figure 2.1: Spatial power combining: (a) Quasi-optical beam amplifier concept; (b) Fundamental WG mode amplification using insert longitudinal active trays [75, 76]; (c) Spatial power combining in gap WG technology [71].

In practice, spatial power combiners are usually realized inside hollow metal WGs [74–76], as shown in Figure 2.1 (b). The coming waves are sampled by an array of receiving probe antennas, amplified by multiple PAs, and radiated into a WG by an array of output antennas. The PAs and antenna probes can be placed on multiple planar longitudinal trays inside the WG. This arrangement allows us to accommodate broadband traveling-wave antennas and improve performance by using multi-stage active components placed along the direction of propagation. Nevertheless, this structure also has technological and implementation problems including complex packaging for performing high isolation between the inputs and outputs of active components and high sensitivity to assembling tolerances. The latter is partly addressed by a spatial power combiner packaged in the gap WG technology, where a parallel-plate WG mode can be potentially amplified by a grid of PAs (See Figure 2.1 (c)). However, in order to create the distributed WG mode, a bulky

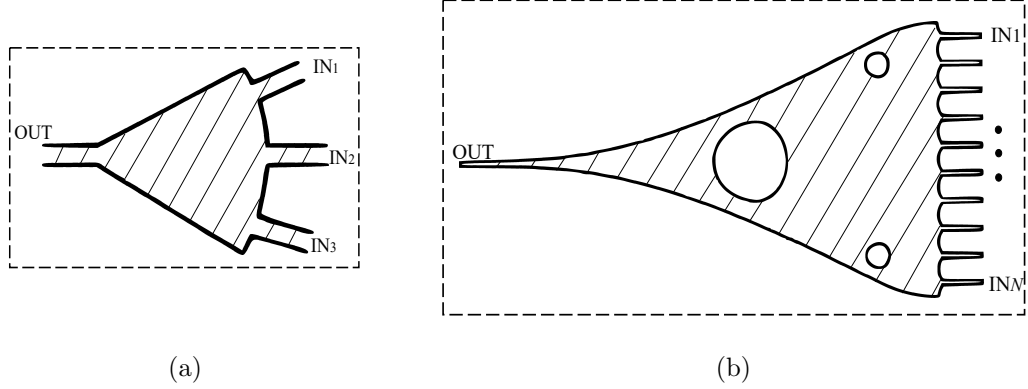


Figure 2.2: Planar spatial power dividers/combiners: (a) Sectorial 1:3 power divider [77]; (b) Tapered microstrip power divider [78].

parallel-plate reflector illuminated by a (horn) antenna is required. The latter limits applications of such combiners in dense antenna arrays with electrically small inter-element distance. In addition, despite a potentially high scalability of the structure, the edge PAs cannot be efficiently utilized due to the tapered field distribution [71].

Planar spatial power combiners are more suitable for the integration with active components since a combiner and amplifier modules can be placed on the same substrate. However, the existing solutions of planar dividers/combiners are based on the generation of a distributed quasi-TEM mode in over-sized MLs [79]. Over-sized MLs have intrinsically low impedance, which is challenging for their direct integration with conventional planar antennas. As a consequence, an impedance transformer formed by a long tapered ML section is an essential part of such combiners. Figure 2.2 (a) shows a sectorial power divider as an example [77]. Besides the lossy tapered ML section, an additional drawback of this solution is that the input ports are located on an arc to ensure that the input signals combined constructively. The latter has been addressed in [78], where etched holes in the middle of the conductor pattern are used to equalize the signal path lengths from the input port to the output port, as shown in Figure 2.2 (b). However, this structure is long and has a narrow-band performance.

## 2.2 Substrate Integrated Waveguide

Substrate integrated waveguide (SIW) technology plays an important role in the realization of active antenna arrays at mm-Wave frequencies. It combines functionalities and performance of conventional WGs as well as supports an efficient integration with active components due to its compact and planar structure. SIW is a particular case of a conventional rectangular metal WG shrunk in height that is embedded into a printed circuit board (PCB), as shown in Figure 2.3. The top and bottom metal

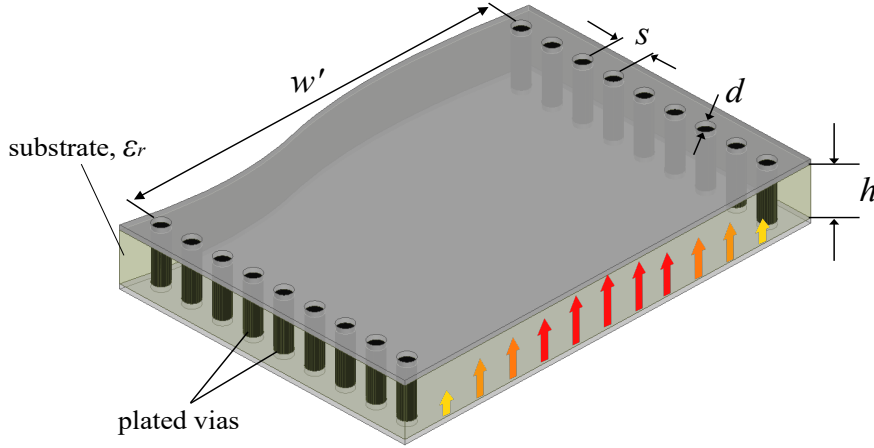


Figure 2.3: Substrate integrated waveguide (SIW) and its fundamental  $TE_{10}$  mode E-field distribution.

walls are directly represented by two PCB metal layers, whereas side walls are formed by rows of plated vias between the corresponding metal layers [80].

### 2.2.1 Fundamental Characteristics

Due to the same topology, SIWs are similar to the conventional rectangular WGs in terms of their propagation and dispersion characteristics [81]. For a rectangular WG, the longitudinal wave vector component ( $k_z$ ) of arbitrary  $TE_{mn}$  mode is given by:

$$k_z = \sqrt{k^2 - \left(\frac{m\pi}{w}\right)^2 - \left(\frac{n\pi}{h}\right)^2}, \quad (2.1)$$

where  $w$  is the WG width;  $h$  is the WG height;  $k = 2\pi/\lambda$ ;  $n, m \in \mathbb{N}_0$ . Each WG mode is mainly characterized by its cut-off frequency; it is the lowest frequency for which a mode will propagate. The WG cut-off frequency corresponds to  $k_z = 0$ . Therefore, the cut-off frequency for an arbitrary  $TE_{mn}$  mode can be defined as:

$$f_{c\ mn} = \frac{c}{2\pi\sqrt{\varepsilon_r}} \sqrt{\left(\frac{m\pi}{w}\right)^2 + \left(\frac{n\pi}{h}\right)^2}, \quad (2.2)$$

where  $\varepsilon_r$  is the relative permittivity of the medium inside the WG. Since the height of the SIW ( $h$ ) is very small, the  $TE_{mn}$  modes with  $n \geq 1$  propagate at extremely high frequencies only and usually are not taken into consideration. As one can see, for any  $TE_{m0}$  mode the cut-off frequency is defined by the WG width ( $w$ ) only. Therefore, SIW and conventional waveguide with the same electrical width have identical propagating  $TE_{m0}$  modes. Figure 2.4 shows the magnitude of the E-field distributions for the  $TE_{10}$  and  $TE_{20}$  modes propagating in the SIW with  $w' = 7.11$  mm,

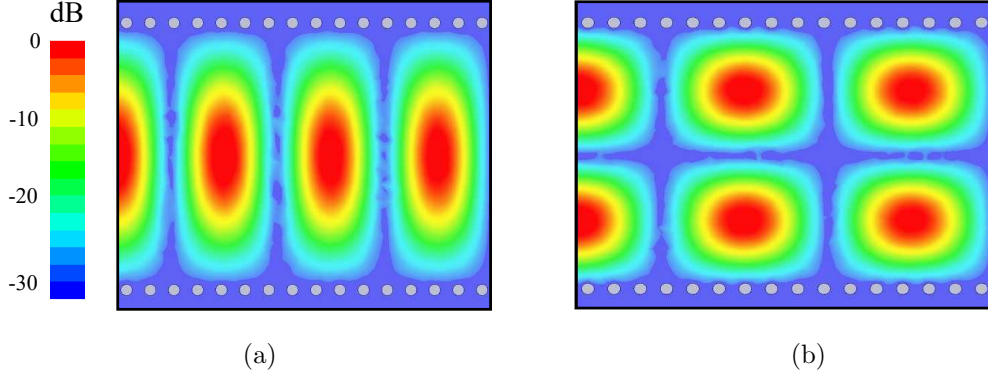


Figure 2.4: Magnitude of the real part of the E-field distribution at 30 GHz: (a) TE<sub>10</sub> mode; (b) TE<sub>20</sub> mode.

$h = 0.254$  mm,  $\epsilon_r = 3.6$ . The fundamental mode of a WG is the mode that has the lowest cut-off frequency, in the presented case, it is the TE<sub>10</sub> mode. The cut-off frequency of TE<sub>10</sub> is defined as:

$$f_{10c} = \frac{c}{2w\sqrt{\epsilon_r}}. \quad (2.3)$$

However, it is worth noting that in order to take into account a finite size of the vias forming the side walls, the width of the SIW can be expressed as:

$$w = w' - \frac{d^2}{0.95s}, \quad (2.4)$$

where  $w'$  corresponds to the center-to-center distance between the vias in the transverse direction,  $d$  is the diameter of the vias,  $s$  is the spacing among them in the longitudinal direction [81].

Another important characteristic of the SIW as a TL is its characteristic impedance. The impedance concept plays a fundamental role in transmission theory. There are several definitions of the TL characteristic impedance: voltage-current, power-voltage, and power-current [82]. For the TEM mode all definitions converge to the same characteristic impedance, i.e., one that is solely a function of the geometry and is frequency independent [82, 83]. Conversely, the characteristic impedance of the fundamental TE<sub>10</sub> mode propagating in the SIW is not uniquely defined and depends on frequency:

$$Z_{\text{TE10}} = k \frac{h}{w} \sqrt{\frac{\mu}{\epsilon}} \left(1 - \frac{\lambda^2}{4w^2}\right)^{-1/2} \quad \text{where} \quad \begin{cases} k = \frac{\pi}{2}, & \text{if V-I def.} \\ k = 2, & \text{if P-V def.} \\ k = \frac{\pi^2}{8}, & \text{if P-I def.} \end{cases} \quad (2.5)$$

According to the voltage-current approach, the characteristic impedance of the SIW is defined as the ratio of the maximum transverse voltage across the top and bottom



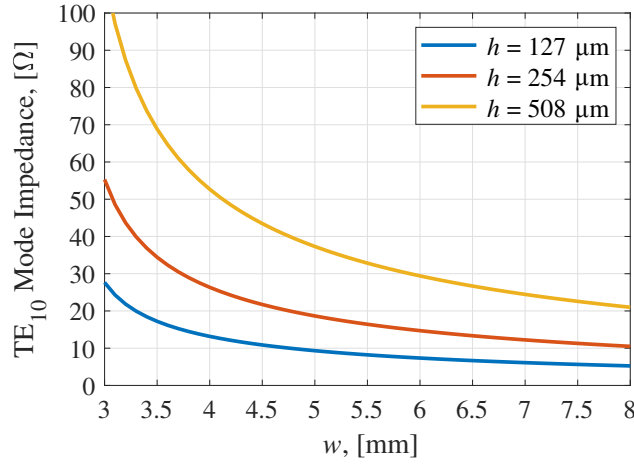


Figure 2.5: Characteristic impedance of the SIW as a function of the width. The set of curves corresponds to different substrate thicknesses.

to the total longitudinal current. Whereas the power-voltage and power-current definitions are based on the power propagating through the WG cross-section. However, the definitions differ by a scaling factor ( $k$ ) only. Figure 2.5 shows the characteristic impedance of the fundamental SIW  $TE_{10}$  mode (V-I def.) as a function of the SIW width ( $w$ ) for different substrate height values ( $h$ ). By analogy with a ML, employing a thinner substrate and increasing the SIW width allows reducing the characteristic impedance. The latter conclusion is important for future integration with active components, as it is discussed in the next section.

### 2.2.2 Integration with Active Components

As shown in Figure 2.5, the characteristic impedance of the SIW is in practice significantly lower than the typical 50-Ω interface impedance of the (PA) chip. Therefore,

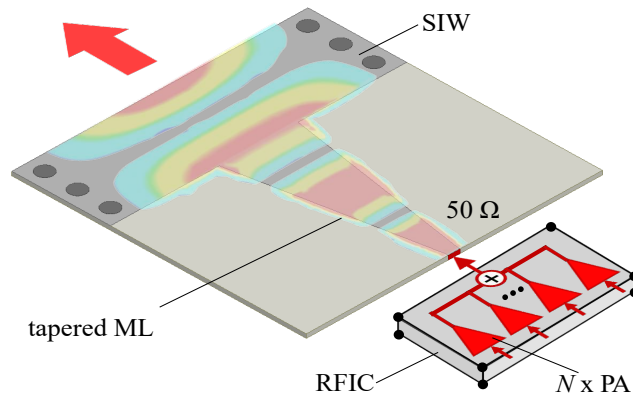


Figure 2.6: Classical transition interfacing an array of PAs with a single SIW.

in order to realize optimal impedance matching a transition between the SIW and the ML/CPW should have an impedance-transforming functionality. A straightforward way of doing this is to employ a tapered TL section.

Figure 2.6 exemplifies a conventional ML to SIW transition concept [80, 84]. As illustrated, the chip with multiple PAs delivers high power to the input port of the transition which is then transferred to the SIW. Achieving an optimal impedance match renders the transition long and therefore lossy, especially if a wide frequency bandwidth (BW) is required (See [80, 84], and Table 2.1).

Table 2.1: Comparison between state-of-the-art solutions and the proposed designs

Reference	Frequency, [GHz]	Bandwidth, [%]	Losses (b2b), [dB]	SIW width, [ $\lambda$ ]
1 $\times$ , TE10 [80]	25-31	12	0.15	0.50-0.62
1 $\times$ , TE10 [84]	17.5-30	50	1	0.44-0.76
2 $\times$ , TE20 [85]	20-40	50	2	0.57-1.14
4 $\times$ , TE10 [this work]	22-36	48	0.3	0.51-0.84
8 $\times$ , TE10 [this work]	25-36	42	0.4	0.62-1.06
10 $\times$ , TE10 [this work]	25-35	30	0.4	0.65-1.10

This fundamental trade-off between BW and power losses limits the applicability of conventional transitions in high-power mm-Wave transmitters. Moreover, as discussed in Section 1.1.1, on-chip power combiners are inherently lossy, and thus, constrain the maximum output power generated by the PAs.

### 2.2.3 Practical Implementation

The SIW technology permits the implementation of conventional rectangular WG components and antennas in a planar form, as well as enables their integration with active devices [86]. SIW-based structures preserve most of the advantages of conventional metallic WGs, such as high quality-factor, self-consistent electrical shielding, and high power-handling capabilities. This fact results in the great acceptance of SIW-based components, including iris and cavity filters [87], directional couplers [88], circulators [89], slot array [90], and leaky-wave antennas.

In terms of practical implementation, SIW-based structures could be fabricated using standard PCB processes or low-temperature co-fired ceramic (LTCC) technology, which makes them lighter and less expensive in comparison with metal WGs. However, the presence of a dielectric inside the structures increases its losses. Dielectric losses can be minimized by using substrates with low loss tangent.

Figure 2.7 shows an example of an SIW-based slot array antenna [90]. It consists of 16 SIW columns each of which has 22 longitudinal slots. The columns are fed through the incorporated 1-to-16 alternating phase power divider. In order to synthesize an

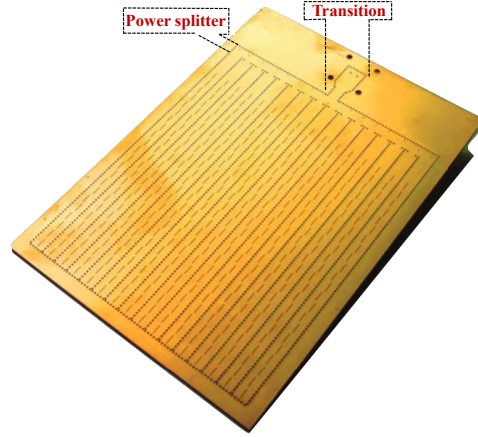


Figure 2.7: A K-band  $16 \times 22$  SIW-based slot array antenna. The radiation pattern shape complies with ETSI class 3, the antenna gain is  $\geq 26$  dBi over 20–24 GHz [90].

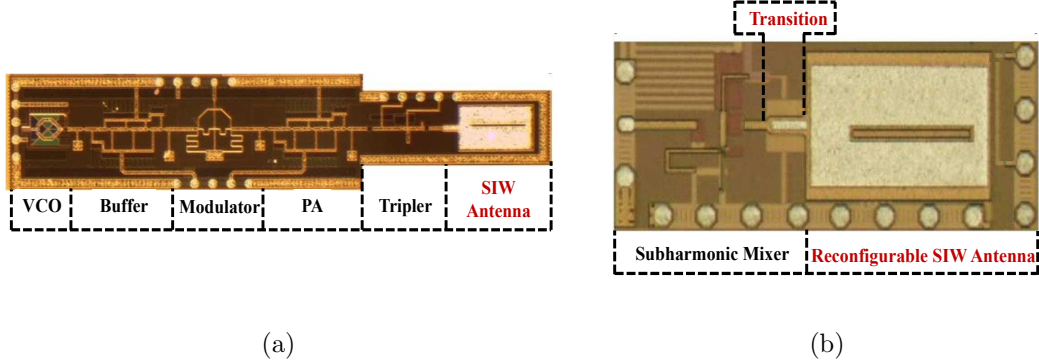


Figure 2.8: A SiGe BiCMOS transmitter/receiver chipset with on-chip SIW antennas at THz frequencies [91]: (a) Integrated transmitter chip; (b) Receiver chip.

antenna array with the desired radiation pattern envelope and gain, a well-established approach for conventional metal WG array antennas has been implemented. The measured antenna gain is  $\geq 26.0$  dBi within the operation band 20–24 GHz, the radiation pattern shape complies with the European Telecommunications Standards Institute (ETSI) class 3 requirements. The radiation efficiency is 74.3 % at the center frequency. The antenna has a simple planar structure allowing its fabrication using a conventional low-cost PCB technology.

At THz frequencies, SIW-based structures become more compact and could be directly implemented on-chip. Figure 2.8 shows a SiGe BiCMOS transmitter/receiver chipset with on-chip SIW-based antennas [91]. Despite the intrinsically high silicon substrate losses, system-on-chip (SoC) architectures become more efficient at these frequencies compared to conventional approaches where discrete antennas are used that suffer from extremely high interconnection losses. THz transmitters are usually based on frequency multiplication using non-linear active components. In the present case, the frequency tripler is directly connected to the antenna, as shown in

Figure 2.8 (a). Therefore, an antenna should have a high-pass filtering functionality to suppress unwanted fundamental and second harmonic signals. An SIW-based antenna is a good candidate to realize the desired functionality due to its intrinsic high-pass filtering property (See Equation (2.1)). Figure 2.8 (b) shows the microphotograph of the THz receiver with the on-chip SIW-based slot antenna. The interconnecting transition between the 50- $\Omega$  subharmonic mixer and the SIW is formed by a conventional tapered ML section. However, this solution has several limitations as discussed in the above subsection.

## 2.3 Transition between a Coupled Microstrip Line Array and Substrate Integrated Waveguide

In order to overcome the limitations of the conventional power combining approaches, minimize interconnection losses, and enable direct integration between active components and antenna elements in mm-Wave dense antenna arrays, a new transmitter architecture has been proposed. It is based on a multi-channel transition [Paper A], which directly interfaces an array of PAs to an SIW via multiple spatially distributed MLs, as shown in Figure 2.9. This allows one to directly excite spatially distributed SIW modes with high power. Figure 2.9 visualizes the transfer from the ML mode(s) to the fundamental  $TE_{10}$  SIW mode. The input ports are coupled through the spatially distributed SIW modes, which causes mutual coupling effects to play a critical role in the proposed transition performance and its design process. In order to take into account mutual coupling effects, the design approach is based on ‘active’

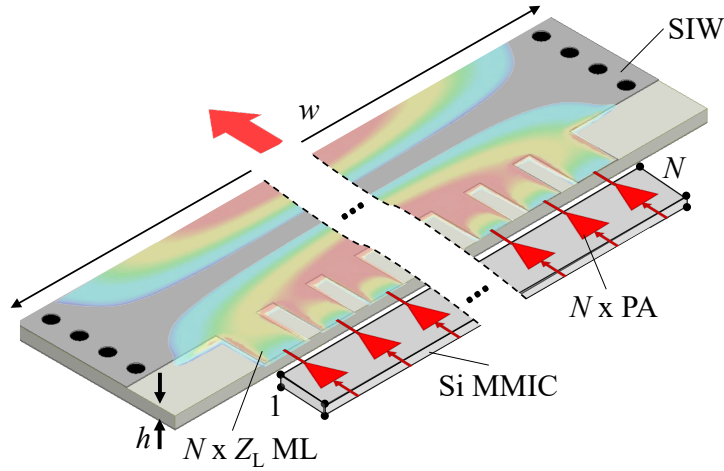


Figure 2.9: Compact transition interfacing  $N$  power amplifiers (possibly embedded in a single MMIC) to a single SIW.

impedance matching, a technique known from antenna array network theory. It allows the reflection coefficient of each ML mode to be analyzed in the presence of the ML array excitation and ML array mutual coupling effects, with the ultimate goal to maximize the overall power transfer to the SIW. The active reflection coefficients at the transition input ports are defined as

$$\Gamma_n = \frac{1}{A_n} \sum_{m=1}^N A_m S_{nm} \quad n \in \{1, \dots, N\}, \quad (2.6)$$

where  $S_{nm}$  is the 50- $\Omega$  S-parameter from ML port  $m$  to  $n$ ,  $A_m$  is the complex excitation coefficient of port  $m$ . In the case of uniform excitation  $\{A_n\}_{n=1}^N = 1$ .

The proposed transmitter architecture has a number of advantages over the conventional approach as shown in Figure 2.6:

- *Output power is no longer limited* by lossy on-chip power combiners.
- *Spatial power-combining functionality* resulting in low insertion losses, which are virtually constant relative to the number of interfaced PAs.
- *Wide bandwidth in combination with compact size*, since the tapered ML section is not required.
- *Generation of the desired higher-order modes* ( $\text{TE}_{m0}$ ) by applying corresponding excitation coefficients  $\{A_n\}_{n=1}^N$ .

### 2.3.1 Scalability Bounds

In the proposed architecture, the power accepted by the antenna element is proportional to the number of interfaced PAs. Therefore, it is important to investigate the scalability of the multi-channel transition. According to the voltage-current approach, the characteristic impedance of the SIW is defined as a ratio of the maximum transverse voltage across the top and bottom to the total longitudinal current (See Equation (2.5)). Assuming that the total (integrated) SIW longitudinal current is a sum of  $N$  ML currents, an impedance matching model could be represented as a parallel connection of  $N$  MLs (each with an equal input impedance  $Z_L$  in active mode) to a common port. The common port impedance should be approximately equal to the characteristic impedance of the SIW  $\text{TE}_{10}$  mode ( $Z_{\text{TE}_{10}}$ ) to realize a good impedance match:

$$Z_{\text{TE}_{10}} \approx Z_L/N. \quad (2.7)$$

Thus, increasing the number of channels demands decreasing the SIW characteristic impedance ( $Z_{\text{TE}_{10}}$ ). This could be done by increasing the width ( $w$ ) or decreasing the height ( $h$ ) (See Equation (2.5)). Figure 2.10 shows the estimated number of connected PAs ( $N$ ) as a function of the ML impedance for different substrate thickness

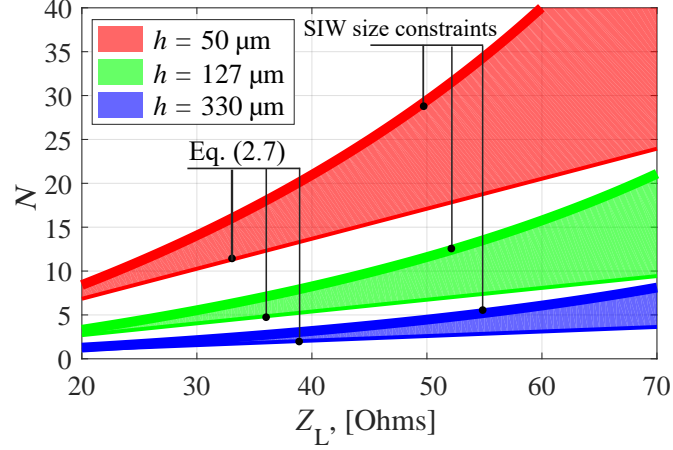


Figure 2.10: Estimated number of the connected PAs as a function of their optimal impedance for different substrate height values  $h$ . Results correspond to a single mode SIW at Ka-band.

values ( $h$ ). The upper bound of the filled areas corresponds to the maximum number of channels, geometrically limited by the SIW width (the spacing between the lines is assumed to be equal to the line width). The lower bounds are set by the optimal impedance matching criteria. As one can see, employment of a thin substrate and high ML impedance channels allow for interfacing more amplifiers to a single SIW, and hence significantly increase the output power as compared to a single channel transition (See Figure 2.6).

For example, employing a substrate with  $h = 50 \mu\text{m}$  allows to interface up to  $N = 30$  PAs with  $50\text{-}\Omega$  optimal load impedance into a single mode SIW at Ka-band. In an ideal case, it results in 14.7 dB relative power increase. A small substrate thickness of the proposed solution enables its future in-package and on-chip realization.

### 2.3.2 Numerical Validation

The proposed spatial power-combining transition has been tested in a 4:1 configuration, as shown in Figure 2.11. It includes four input ML ports with  $50\text{-}\Omega$  reference impedance and a single matched SIW port as an output. The SIW width has been chosen in such a way that both the  $\text{TE}_{10}$  and  $\text{TE}_{20}$  modes can propagate.

The critical design parameters are the positions of MLs, the distances between MLs, their lengths and widths. The transition has been optimized to realize an optimal active impedance matching under the condition of uniform excitation ( $\{A_n\}_{n=1}^4 = 1$ ). The optimal design parameters are presented in [Paper B]. Figure 2.12 (a) illustrates the field coupling from multiple quasi-TEM modes to the  $\text{TE}_{10}$  mode and its subsequent propagation inside the SIW when the input ports are uniformly excited. In spite of the fact that the transition has been optimized to maximize power transfer into the fundamental  $\text{TE}_{10}$  mode, higher-order modes could also be generated by ap-

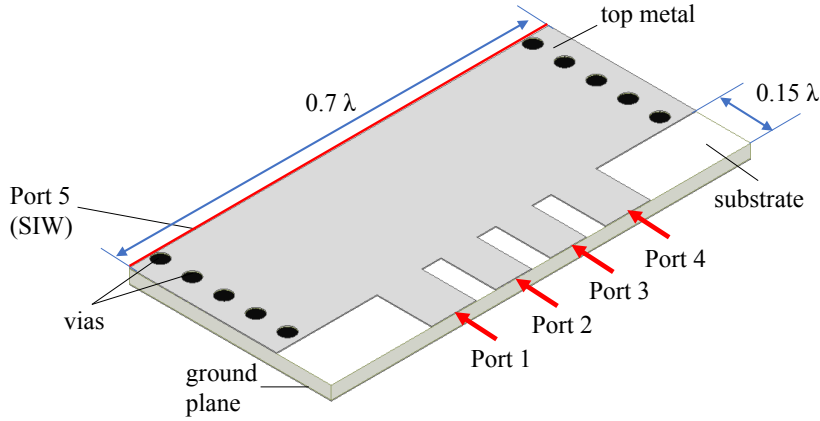


Figure 2.11: EM model of the proposed power-combining transition in a 4:1 configuration.

plying different excitation scenarios. Figure 2.12 (b) exemplifies a generation of the  $TE_{20}$  mode by the same arrangement; corresponding excitation coefficients are defined as:  $A_n = e^{-j\phi_n}$ , where  $\phi_n = \{0, 0, \pi, \pi\}$ . The higher modes ( $TE_{30}$ ,  $TE_{40}$ ) might be obtained by increasing the SIW width and interfacing more input ports, which gives extra degrees of freedom for implementing more complex excitation scenarios. Due to the flexibility of the proposed transition, it is expected to play an essential role in multi-mode antennas, where multiple modes are usually employed to increase the operation bandwidth [92]. The simulated passive and active reflection coefficients ( $|S_{11}|$ ,  $|S_{22}|$  and  $|\Gamma_1|$ ,  $|\Gamma_2|$ ) of the 50- $\Omega$  ports of the 4:1 transition over the 25–35 GHz frequency range are shown in Figures 2.13 (a) and (b) respectively. Although the passive reflection coefficients of the individual ports reach  $-5$  dB level, their active reflection coefficients (when all input ports are excited simultaneously) remain below  $-25$  dB over 30% bandwidth and  $\leq -15$  dB over 50% bandwidth. The latter is a result of efficiently utilizing mutual couplings between the ports. Figure 2.13 (c) shows the couplings between the 50- $\Omega$  input ports. As one can see, the coupling between the edge ports ( $|S_{14}|$ ) reaches  $-4$  dB level, whereas the coupling between port 1 and port 3 ( $|S_{13}|$ ) is below  $-12$  dB over the 25–35 GHz frequency range. The relatively high  $|S_{14}|$  mainly attributes to the coupling between the ports within SIW modes. This effect might be critical for some applications, where active components require a good isolation between channels. A method of isolation enhancement is discussed in the next subsection.

Figure 2.13 (d) shows transmission coefficients between the symmetric 50- $\Omega$  input ports and the output SIW port ( $|S_{15}|$ ,  $|S_{25}|$ ). In case of an ideal 4:1 power combiner/divider:  $|S_{15}| = |S_{25}| = -6$  dB. However, the average level of the simulated transmission coefficients is  $\geq -6.25$  dB, which results in approximately 0.25 dB incertion losses. The relative difference between  $|S_{15}|$  and  $|S_{25}|$  does not exceed 0.2 dB, implying that the power amplifiers in the array are utilized effectively.

### 2.3. TRANSITION BETWEEN A COUPLED MICROSTRIP LINE ARRAY AND...

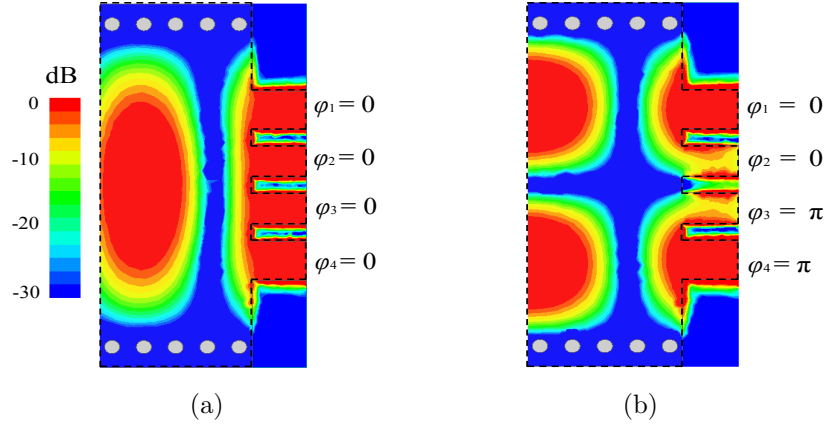


Figure 2.12: Magnitude of the real part of the E-field distribution at 30 GHz: (a)  $TE_{10}$  mode; (b)  $TE_{20}$  mode.

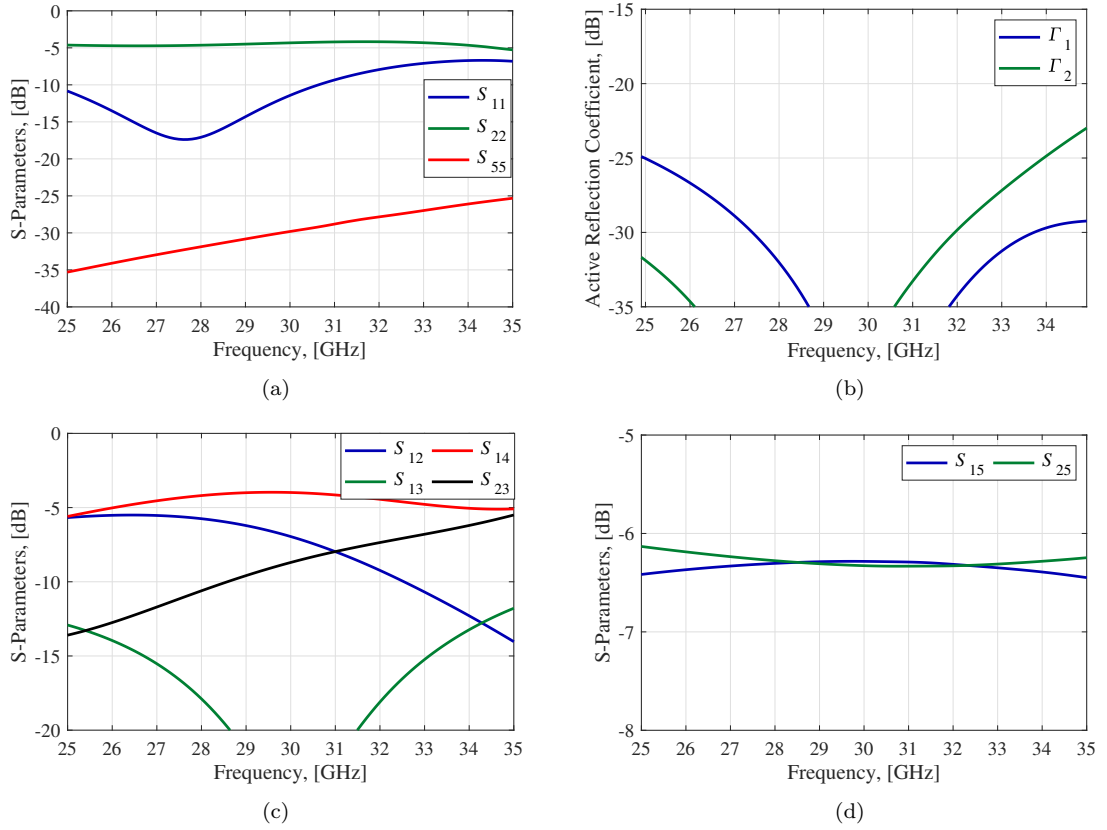


Figure 2.13: Simulated (a) Passive reflection coefficients; (b) Active reflection coefficients of the input ports, as shown in Figure 2.11; (c) Coupling between the input ports; (d) Combiner insertion losses. The results for symmetric ports are omitted.



The special case of a 10-way power combiner with 50- $\Omega$  CPW input ports has been presented in [Paper D]. The simulated active reflection coefficients of the CPW-ports and passive reflection coefficient at the wave port of the structure are better than  $-10$  dB over more than 30% relative bandwidth (25–35 GHz). Numerical results validate the model and show that this configuration allows for efficient power combining from multiple amplifiers, and hence can generate  $10\times$  more power while maintaining a constant loss of almost 0.3 dB.

Summarizing the above, the proposed transition overcomes fundamental limitations of single-channel SIW transitions and simultaneously achieves a wide bandwidth and low power loss, and also outperforms the state-of-the-art multi-channel multi-mode transitions in terms of its compactness and power transfer/combining efficiency (See Table 2.1).

### 2.3.3 Isolation Enhancement Technique

An essential factor worth taking into account in the transition design procedure is the mutual coupling between PAs. The transition is designed under the condition of a uniform excitation assuming identical PAs ( $\{A_n\}_{n=1}^4 = 1$ ). However, realistic PAs might be slightly different in their amplitude-phase characteristics due to dif-

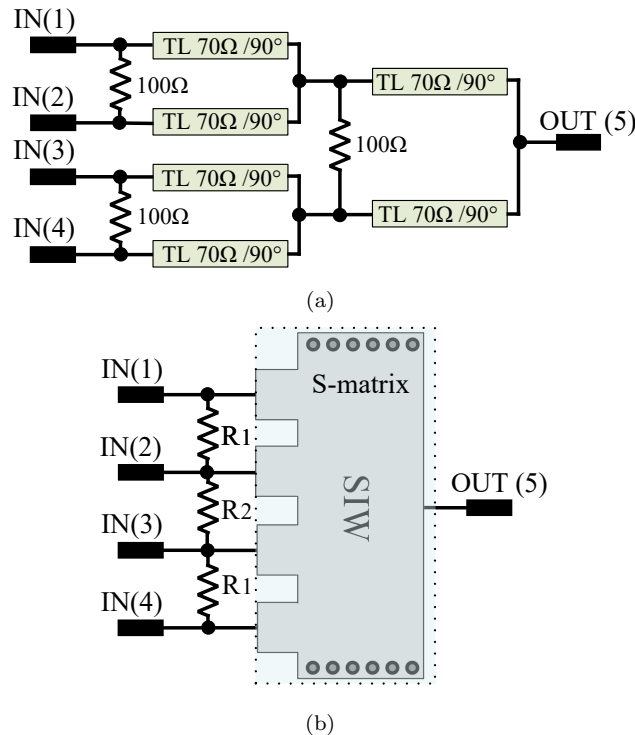


Figure 2.14: Simulation models of the 4-way power combiners: (a) Ideal Wilkinson power combiner; (b) Spatial power combiner with and without isolation load resistors.

ferent thermal regimes, semiconductor process variations and fabrication tolerances. This effect could be introduced into the design procedure by varying complex excitation coefficients  $\{A_m\}_{m=1}^4$  in Equation 2.6. Generally, in order to reduce the effect of  $\{A_m\}_{m=1}^4$  on the active reflections  $\{\Gamma_n\}_{n=1}^4$ , the magnitudes of  $S_{nm}$  have to be minimized.

This minimization problem has been addressed in [Paper E]. In a similar manner as in the Wilkinson power combiner (See Figure 2.14 (a)), isolation resistors ( $R_1, R_2$ ) are introduced in-between the PA outputs, as shown in Figure 2.14 (b). In the case of ideal uniform excitation, the voltage difference between the input ports will be zero implying that no current will flow into the isolation resistors, and hence, there is no power dissipation. For a non-uniform excitation, the differential-mode power will be dissipated in the resistors. This enhanced isolation between the channels results in a smaller variation of the input port active reflection coefficients  $\Gamma_n$ . Despite the power dissipation in the isolation resistors, the combined output power is expected to be higher (compared to non-isolated scenario). This is due to the behaviour of the individual PAs, which deliver less power if the output is mismatched [93]. The optimal resistor values could be found in [Paper E]. Figure 2.15 shows the mutual

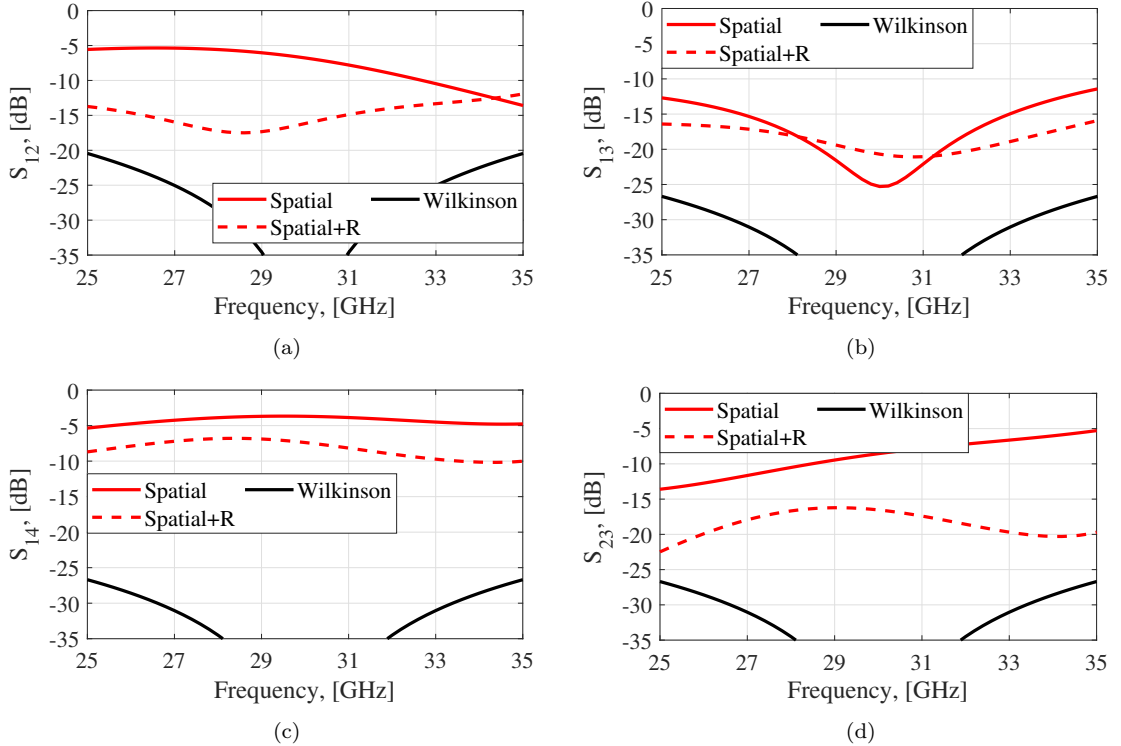


Figure 2.15: Simulated mutual coupling between the input ports of the spatial power combiner with and without isolation resistors (dashed and solid lines, respectively) and an ideal Wilkinson power combiner (black line). The results for symmetric ports are omitted.

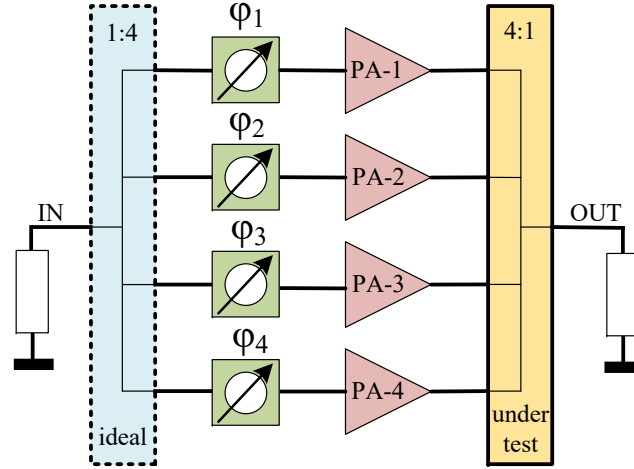


Figure 2.16: The simulation test-bench for the evaluation of the combined PA performance in the presence of normally distributed phase errors, used for the ideal Wilkinson power combiner and the spatial power combiners with and without isolation resistors.

coupling between input ports. As one can see, isolation resistors allow to significantly reduce the coupling compared to the original design with no isolation resistors. In particular, the  $|S_{23}|$  and  $|S_{13}|$  remain below  $-15$  dB, and  $|S_{12}|$  and  $|S_{14}|$  remain below  $-12$  dB and  $-7$  dB, respectively, over the 25–35 GHz band. The relatively high level of  $|S_{14}|$  could be reduced by introducing another resistor between the edge ports. The latter is not practical since it requires long interconnecting lines. The ideal Wilkinson combiner intrinsically has good input matching and exhibits excellent isolation properties.

In order to evaluate the sensitivity of the power combiners to non-identical PAs, a simulation test-bench has been proposed (See Figure 2.16). It has a single 50- $\Omega$  input port interfaced to an ideal 1:4 power splitter. The power splitter feeds an array of identical common-base PA-modules in SiGe Heterojunction Bipolar Transistor (HBT) technology [94]. The power amplifiers are power-matched to a 50- $\Omega$  load impedance. In practice, phase variations of the PA complex gain dominate over amplitude drifts. This effect is emulated by four independent phase shifters with normally distributed phase values  $\{\phi_n\}_{n=1}^4$ . The outputs of the PAs are interfaced to the matched 4:1 power combiners under test. The performance of such a joined active structure has been investigated in terms of PA metrics: forward transfer gain, output power, and efficiency.

The performed statistical analysis shows that introducing isolation resistors allows one to significantly reduce the negative impact of a non-uniform excitation on the overall output power, gain, and power efficiency. The proposed power combining transition with the isolation resistors is comparable with the classic Wilkinson power combiner in terms of sensitivity to a non-uniform excitation, while it has both a significantly lower insertion loss and a more compact size.

### 2.3.4 Experimental Demonstration

In order to experimentally demonstrate the concept of the spatial power combining transition, a passive prototype (without isolation resistors) in back-to-back (B2B) configuration has been designed, as shown in Figure 2.17. It is an 8 ports structure, which has 4 input and 4 output 50- $\Omega$  coaxial ports to allow for calibration and testing with a standard vector network analyzer (VNA). However, coaxial connectors are bulky compared to the transition size and, as a consequence, additional divergent routing lines are required. The effect of those need to be de-embedded from the measurement results. The routing lines are closely spaced in the SIW region, and hence, might cause additional undesired coupling effects. The latter significantly complicates calibration and de-embedding procedures. To avoid these problems, the device under test (DUT) includes divergent lines to make the routing lines to the connectors (shown in Figure 2.17 by light gray color) virtually independent. In this case, 2-port

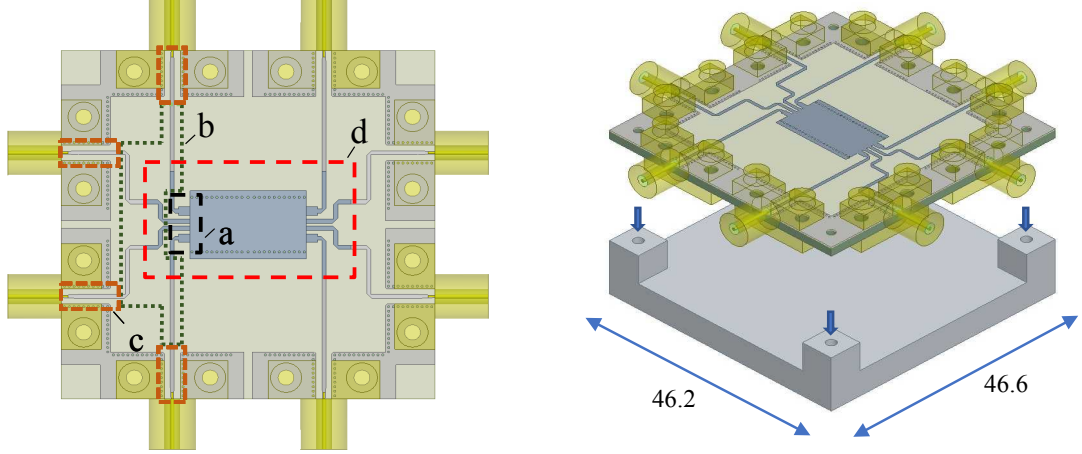


Figure 2.17: A mechanical model of the 8-port B2B prototype: (a) The entire B2B structure including two connected transitions; (b) The proposed transition between SIW and four short and strongly-coupled TLs; (c) 50- $\Omega$  routing MLs that decouple the TLs at the ports of the B2B for the purpose of testing; (d) Connector interface regions.

only thru-reflect-load (TRL) calibration kit could be used to remove the effect of the routing lines and connectors from the measured results. It is important to note that the electrical length of the routing lines should be the same. Figure 2.18 shows the fabricated prototype and its corresponding TRL calibration kit. The structure is built on a hybrid multilayer PCB with edge metallization, which is formed by stacking two dielectric material layers. The top substrate is a RO4350 laminate with a relatively low loss tangent, whereas the bottom hardback substrate is FR4, which makes the structure more rigid. The PCB has an overall size of approximately  $46 \times 46$  mm and is bolted to an aluminum support frame. The optimum design parameters of the DUT and interconnection MLs are provided in [Paper C].

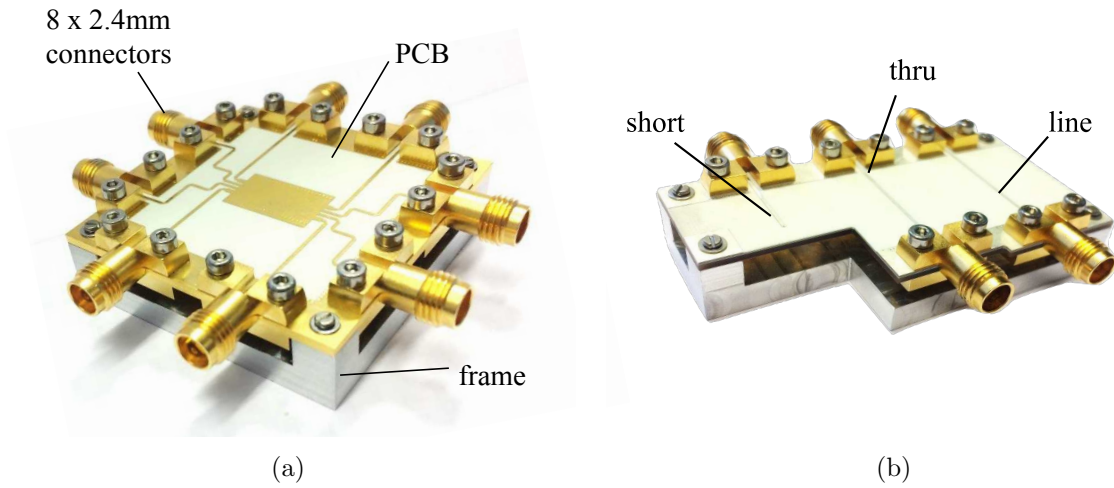


Figure 2.18: (a) Fabricated spatial power-combining transition in a back-to-back configuration; (b) Designed thru-reflect-line (TRL) calibration kit.

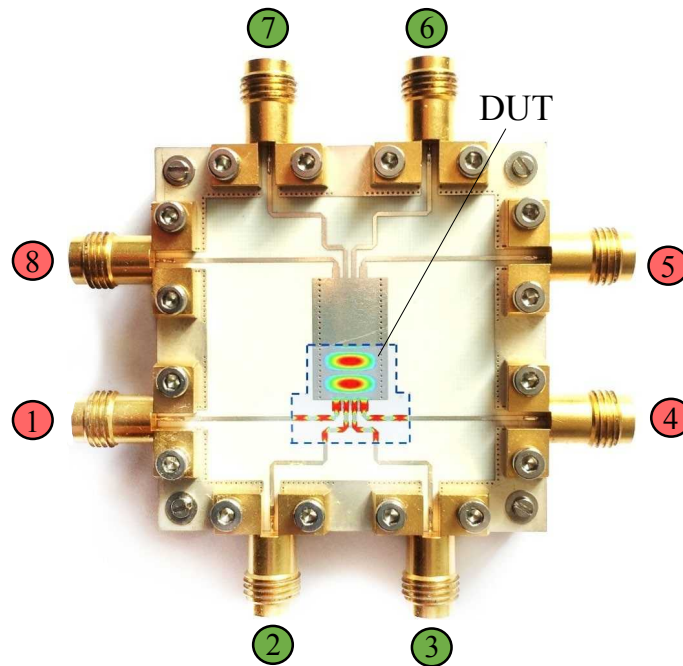
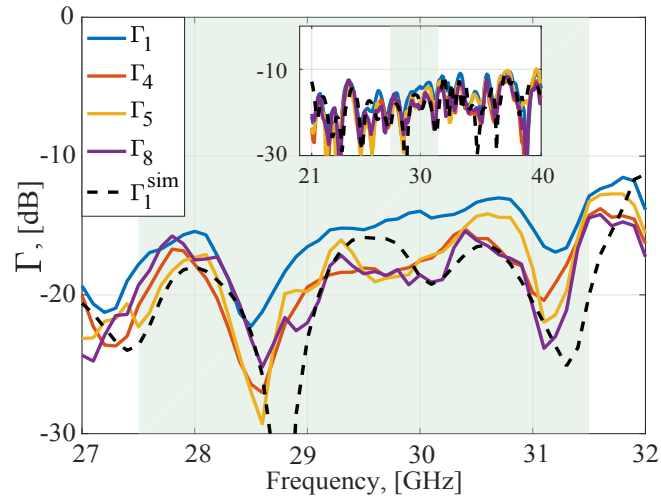
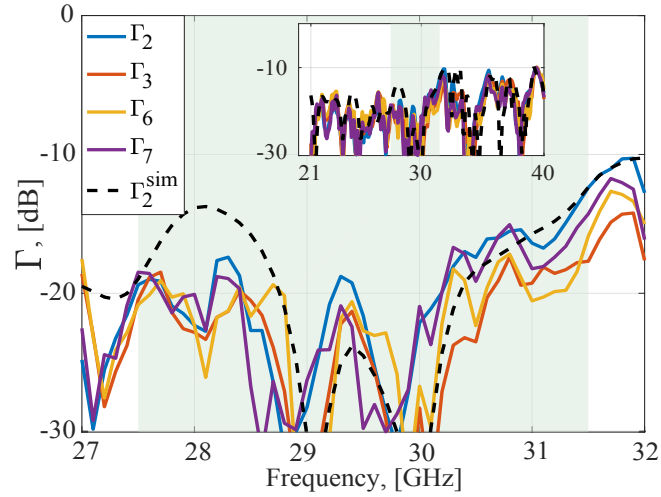


Figure 2.19: Measured DUT in a back-to-back configuration. The symmetric ports are marked by the same colors. The shown E-field magnitude distribution corresponds to simultaneous excitation of the input ports at 30 GHz.

Results of multiple single-ended measurements performed by a 4-port VNA have been combined to construct the full  $8 \times 8$  scattering matrix; the corresponding port numbers are shown in Figure 2.19. The magnitude of the measured active reflection coefficients ( $|\Gamma_n|, n \in \{1 \dots 8\}$ ) of the symmetric  $50\text{-}\Omega$  ports are shown in Figure 2.20. The curves are close to each other and in good agreement with the simulations shown by black dashed lines. However, ripples on the measured curves are visible that are mainly attributed to connector interfaces whose negative effects cannot be entirely removed by the designed 2-port TRL calibration kit since, in practice, these interconnections are slightly different due to the fabrication and measurement uncertainties.



(a)



(b)

Figure 2.20: Measured (solid) and simulated (dashed) active reflection coefficient of the symmetric  $50\text{-}\Omega$  ports of the B2B prototype (including effect of connectors), as shown in Figure 2.19.

In spite of this, the measured  $|\Gamma_1|$  and  $|\Gamma_2| < -13$  dB in the desired frequency range and  $< -10$  dB over the whole range (20–40 GHz). Insertion losses of the DUT are shown in Figure 2.21. The measured losses were de-embedded using the thru-standard of the designed calibration kit. Contributions of the dielectric and radiation losses have been estimated using simulation data. At 30 GHz the total losses of the DUT are 0.73 dB, where the contribution of the dielectric and radiation losses are 0.28 dB and 0.45 dB, respectively. Radiation losses are dominant and attributed to the bent MLs in the DUT. The overall expected losses of the proposed transition without routing lines are estimated to be less than 0.3 dB.

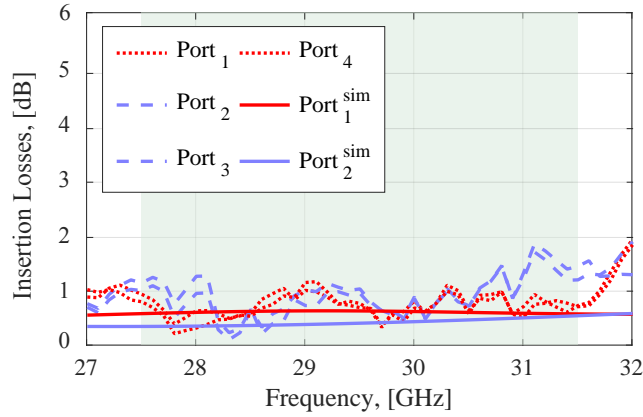


Figure 2.21: Measured (dashed) and simulated (solid) insertion losses of proposed DUT.

## 2.4 Conclusion

A novel transition concept based on the direct excitation of the SIW modes by an array of coupled MLs has been proposed. Its spatial power combining functionality obviates the need for potentially lossy on-chip power combiners. The passive transition examined in a B2B configuration shows that the proposed solution overcomes the fundamental limitations of the conventional power combining architectures. It allows us to simultaneously achieve wide BW (50%) and low insertion losses (0.4 dB) while it offers a compact planar form-factor. The proposed concept has a wide range of possible applications, e.g. in mm-Wave antenna arrays, where each element is interfaced with an inexpensive grid amplifier RFIC, or as a fully on-chip integrated antenna solution at sub-THz frequencies.

## Spatial Power-Combining Module

This chapter describes the active performance of the designed low-loss power combining module, providing an interface between an array of PAs to a single standard rectangular WG. The active performance of the module in the presence of critical effects of coupled PAs is tested in combination with a commercial multichannel transmitter.

### 3.1 Design Description

A detailed model of the designed power-combining module, which employs the spatially distributed excitation of the SIW-based cavity modes by an array of four MLs is shown in Figure 3.1. A conventional rectangular WG interface has been chosen as an output port to demonstrate the power combining and radiation performance in the presence of critical effects of realistic PAs. In order to integrate a WG interface, the design concept of the  $90^\circ$  bent interface between an SIW-based cavity with etched aperture and a stepped ridge WG has been employed [95]. However, instead of using the relatively bulky and long multi-section SIW in [95], the desired multi-mode field distribution in the relatively wide SIW-based cavity is directly created by an array of MLs [Paper C]. The direct multi-mode excitation allows to reduce the size of the transition and hence the losses in comparison with [95]. The consequence is that the array of MLs, the SIW-based cavity, the coupling aperture, and the ridge metal WG cannot be analyzed independently from one another and have to be considered as a single module. In contrast to the previous B2B design, where four quasi-TEM modes are matched to a single  $TE_{10}$  mode (See Figure 3.2 (a)), the present structure performs a direct matching of the over-moded cavity with open aperture, as shown in Figure 3.2 (b). The electric field of the resonant cavity mode is concentrated near the bottom orthogonal ridge and is coupled through the etched rectangular aperture into the metal WR-28 flange with stepped ridges. The latter is very challenging due to the low substrate height as well as because of different medium rendering this



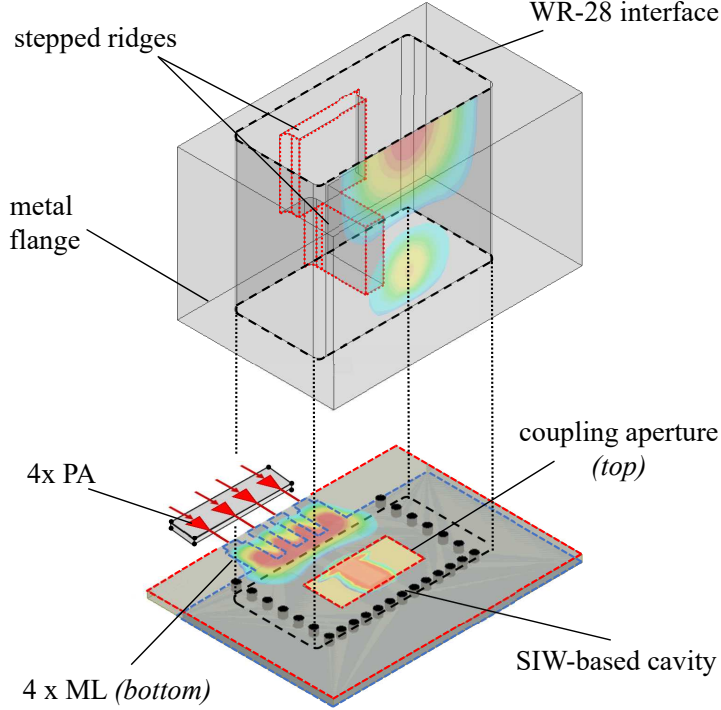


Figure 3.1: A detailed model of the proposed spatial power-combining module. The  $TE_{10}$  mode propagation inside the WG and direct coupling to the array of MLs is illustrated.

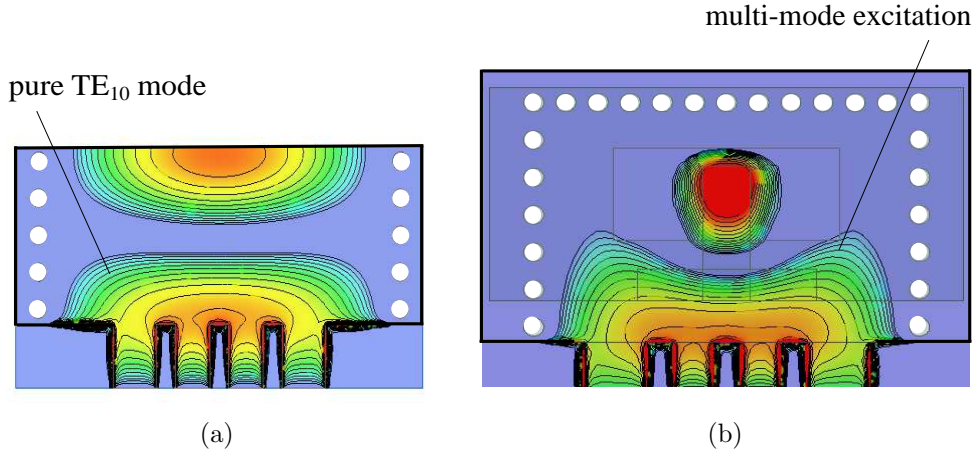


Figure 3.2: Magnitude of the real part of the E-field distribution at 30 GHz inside: (a) A single-mode SIW excited by an array of MLs [Paper A,B]; (b) Over-moded cavity with the open aperture excited by an array of ML.

region very sensitive to fabrication uncertainties. For efficient aperture coupling, the bottom ridge should be located inside the coupling aperture, however, in practice there is a gap corresponding to the thickness of the copper foil on the top PCB layer. It means that laminates with thin copper layers and low surface roughness have to be used. The top ridge is needed to match the ridge WG mode to the conventional WR-28 mode. The design parameters are presented in [Paper F].

## 3.2 Critical Effects of Coupled Power Amplifiers

In linear microwave circuits such as passive filters, antennas, etc., conjugate matching is used to maximize the power transfer between the source and load. However, a PA does not directly transfer power from its input to the load; it generates RF output power and delivers it to the load by converting the DC power. In order to maximize the power generated by the PA, its output needs to be terminated by the optimum load, which is different from the conjugated output impedance. The optimum load impedance of a typical PA could be found by performing the load-pull test, in which the output of the PA is terminated by a set of loads and for each of those the output power (usually at 1-dB compression point) is evaluated. Then, constant power contours plotted on the Smith chart allows us to find the optimal load impedance as well as to predict performance degradation in the case of non-optimal loads, as exemplified in Figure 3.3. In linear circuits, reduction of the accepted output power caused by mismatch is expressed as:

$$\text{Mismatch Power Loss}_{\text{dB}} = -10 \log_{10}(1 - |\Gamma|^2), \quad (3.1)$$

where  $\Gamma$  is the complex output reflection coefficient normalized by the optimal PA load. For example,  $|\Gamma|_{\text{dB}} = -10$  dB results in 0.46 dB power reduction. However, based on the load-pull data, non-linear PAs are intrinsically more sensitive to the load variations, and hence, deliver much less power to a non-optimum load [96]. As it will be exemplified later,  $|\Gamma|_{\text{dB}} = -10$  dB may result in  $\geq 1$  dB power reduction (See Figure 3.3). Moreover, the power efficiency of the PA is also highly dependent on its load impedance, and hence, should be considered in combination with the output power.

In the case of  $N$  PAs coupled through a non-isolated power combiner, the actual output load of an individual PA can be represented by the active reflection coefficient at the combiner input ports:

$$\Gamma_n = \frac{1}{G_n} \sum_{m=1}^N G_m S_{nm}, \quad (3.2)$$

where  $S_{nm}$  is the S-parameter from combiner port  $m$  to  $n$ , while  $G_m$  is the complex gain of the  $m$ -th PA. The active impedances at the combiner input ports are assumed

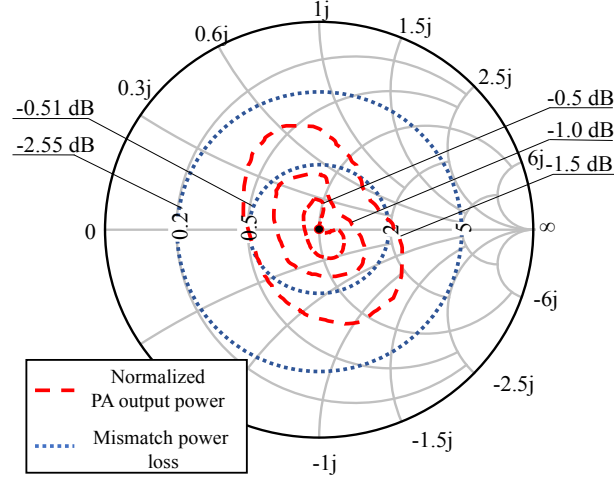


Figure 3.3: A realistic PA output power reduction based on the load-pull data (red) compared to the power reduction due to the impedance mismatch in linear networks (Equation (3.1)).

to be optimal in case of identical PAs (uniform excitation):  $G_n = G_m | n, m \in \{1 \dots N\}$ . However, in practice, the difference between individual PAs might be significant due to the different thermal regimes of each PA and/or due to fabrication uncertainties. Therefore, interfacing PAs with varying and non-equal gains ( $G_n \neq G_m | n, m \in \{1 \dots N\}$ ) to a non-isolating combiner ( $S_{nm} | n \neq m \neq 0$ ) affects the active impedances at the combiner input ports, and hence, degrades the individual PA performance.

To investigate the behavior of a realistic PA in conjunction with the proposed transition, an output stage based on a conventional single-ended common-base amplifier has been interfaced with the designed power-combining module. The PA design is implemented in  $0.25 \mu\text{m}$  SiGe:C BiCMOS technology [97], which is also the technology used for the quad-channel RFIC in our experimental verification (*cf.* Section 3.3). Figure 3.4 shows the PA schematic. SiGe HBTs in common-base configuration are widely used at high frequencies due to the higher maximum available power gain and relatively high output load compared to the common-emitter configuration [98, 99]. An output matching circuit based on transmission lines has been used in order to match the output stage to a  $50\text{-}\Omega$  load. The remaining design parameters are presented in [Paper F].

The load-pull simulations have been performed in Keysight’s ADS using a harmonic balance technique. Figure 3.5 shows the simulated output power in 1-dB compression point (P1dB) and efficiency contours at 28 GHz in the load reflection coefficient plane. The clusters of points show active  $\Gamma_{1,2}$  of the multi-port power combiner in the presence of normally distributed phase and amplitude errors represented non-identical PAs. As one can see, most of the active load realizations remain within the region of high efficiency and high output power, although for higher  $\sigma$  the cluster of points is more spread. This study has been used to determine the PA requirements in terms of the maximum allowable relative difference of the phase and amplitude.

### 3.2. CRITICAL EFFECTS OF COUPLED POWER AMPLIFIERS

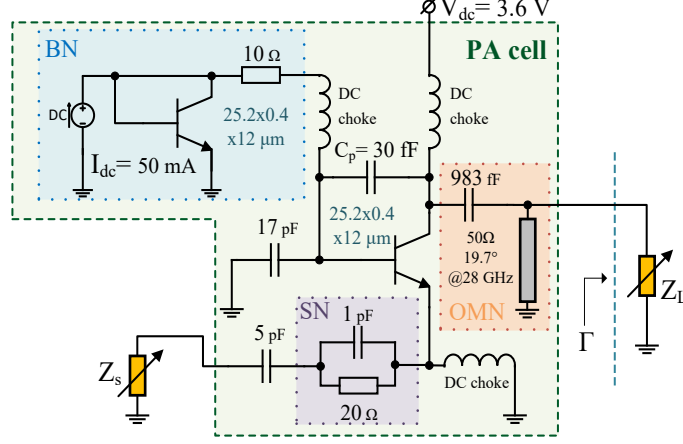


Figure 3.4: Simulated Class-A single-ended common-base output PA stage in SiGe HBT technology. OMN=output matching network, BN=bias network, SN=stability network. An active load sweep is performed.

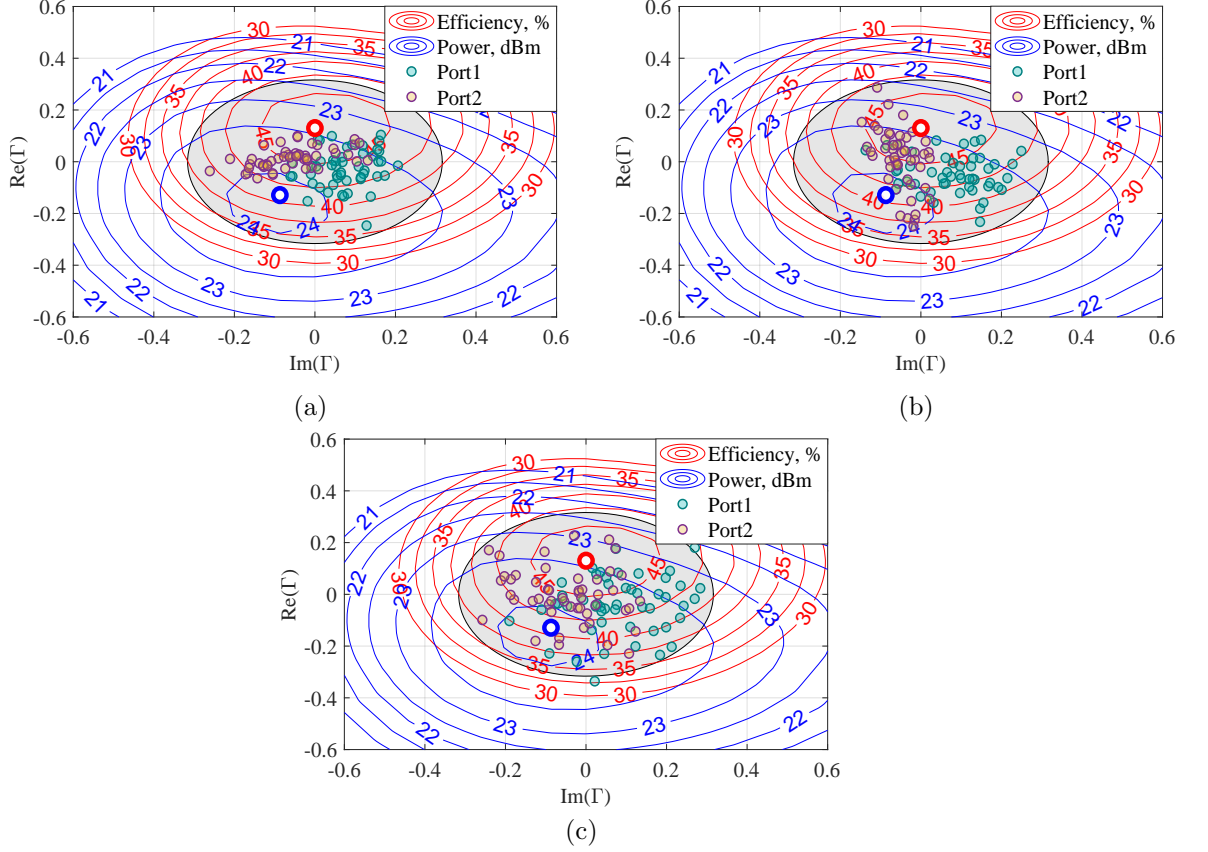


Figure 3.5: Simulated PA P1dB output power (blue) and efficiency (red) contours at 28 GHz in the load reflection coefficient plane. The cluster of points represent  $\Gamma_{1,2}$  of the power-combining module in the presence of normally distributed: (a) Phase errors with  $\mu = 0^\circ$ ,  $\sigma = 15^\circ$ ; (b) Amplitude errors  $\mu = 0$  dB,  $\sigma = 1$  dB; (c) Both amplitude and phase errors.

The results show that good performance (relative output power reduction  $\leq 1$  dB) can be expected as long as PA gain variations remain within  $\pm 15^\circ$  for the phase and  $\pm 1$  dB for the amplitude.

### 3.3 Experimental Validation

#### 3.3.1 Fabricated Prototype

The fabricated power-combining module prototype has four 50- $\Omega$  coaxial input ports for testing with a standard VNA and a single output WR-28 antenna interface, as shown in Figure 3.6. The divergent MLs were included in the DUT to be able to

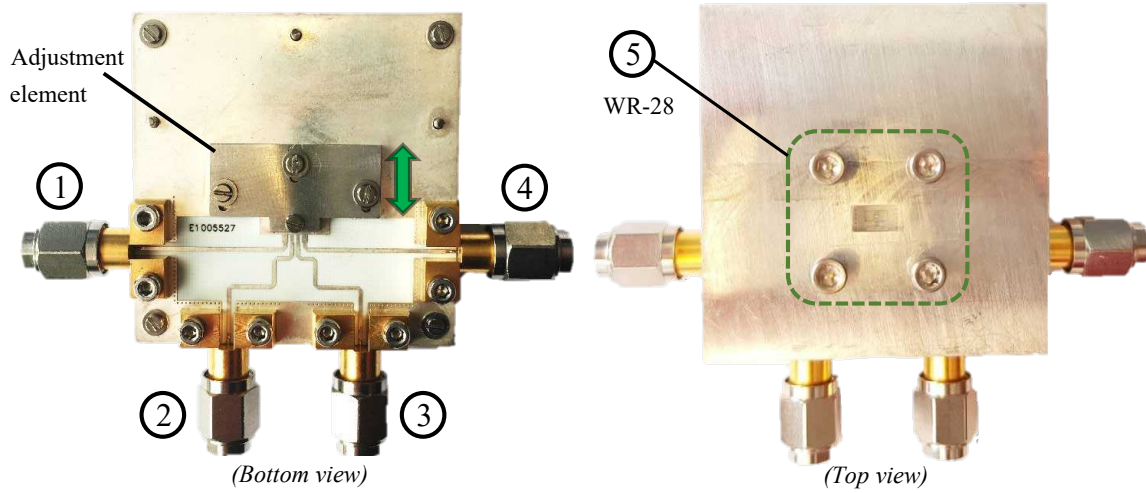


Figure 3.6: Fabricated spatial power-combining module prototype. The adjustment element constitutes a movable metal plate bolted to the flange in the aperture area to control pressure contact between the PCB and the aluminum flange.

mount RF connectors to the PCB and to decouple the extended routing of MLs. By exploiting symmetry, the designed two-port-only calibration kit (the same as for the B2B configuration) suffices to largely remove the effect of the four connectors from the measurement results. The structure is formed by stacking a standard double-sided PCB on the aluminium WG flange with embedded ridges. The bottom side of the flange has conically-shaped guide pins (dowels) for the stack alignment and threaded holes to mount the  $4 \times 2.4$  mm edge connectors. It allows to remove the bottom clamps of the connectors. This prevents undesired field leakage from occurring through the gap formed by the connector's body and the PCB edges. As discussed in the previous section, the region between the etched aperture and the bottom ridge is very sensitive to fabrication tolerances, therefore an extra adjustment element was developed as indicated on the left-hand-side photo. It consists of a movable metal plate bolted

to the flange in the aperture area. The metal plate has a threaded hole with a trimming screw, which can be used to control pressure contact between the PCB and the aluminium flange. The top side of the flange has a standard WR-28 interface, which can be also used like an open-ended WG radiating element. The stack has on overall size of approximately  $46 \times 46 \times 6$  mm.

### 3.3.2 Measurement Results

The measured active reflection coefficients of the symmetric 50- $\Omega$  input ports are shown in Figure 3.7 (a), (b). The obtained  $|\Gamma_1|$  and  $|\Gamma_2| < -13$  dB in the desired frequency range and  $< -10$  dB over whole range (24.5–37.8 GHz). The measured and simulated WR-28 port reflection coefficients are shown in Figure 3.7 (c) (coaxial ports are terminated as shown in Figure 3.6). It is seen that  $S_{55}^{\text{WR-28}} < -14$  dB over 24.5–37.8 GHz. This corresponds to the 50% bandwidth. All curves are close

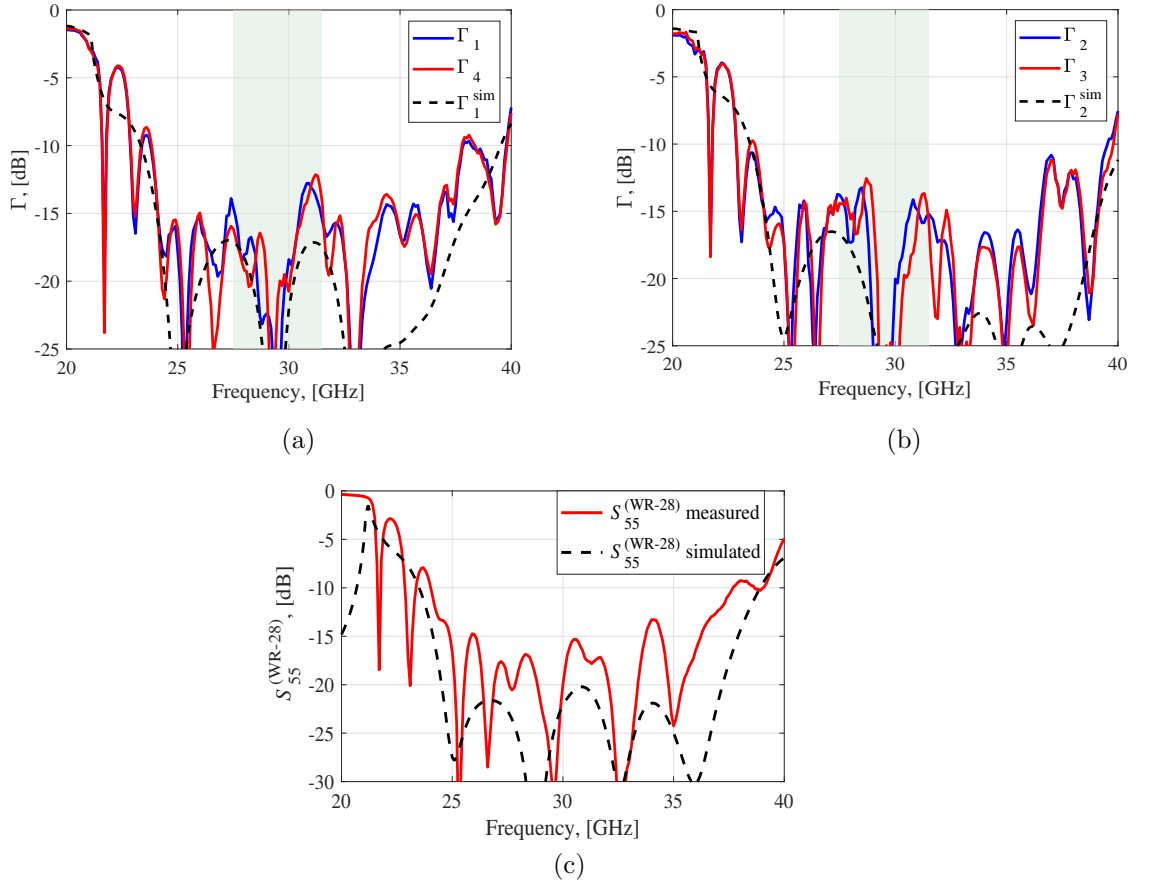


Figure 3.7: Measured (solid) and simulated (dashed): (a) Active reflection coefficients of the 50- $\Omega$  port 1 and port 4; (b) Active reflection coefficients of the 50- $\Omega$  ports 2 and port 3; (c) Reflection coefficient of the WR-28 port. The colored regions indicate the bandwidth of the employed commercial transmitter.

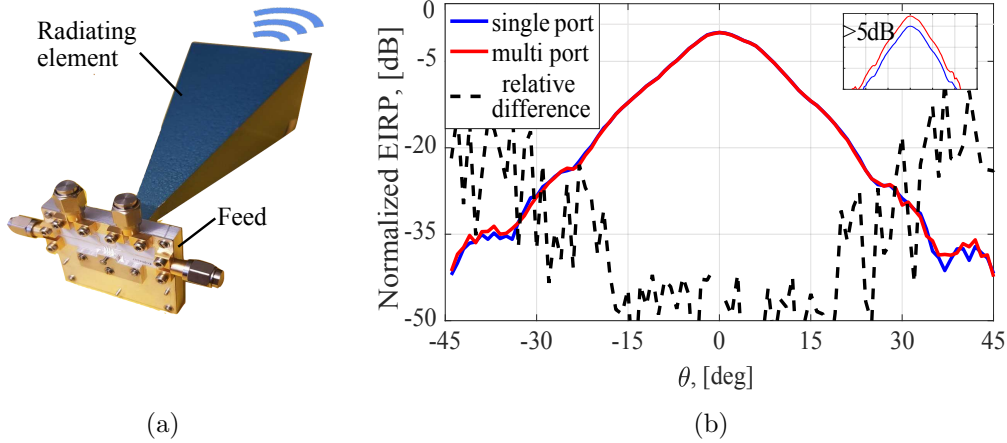


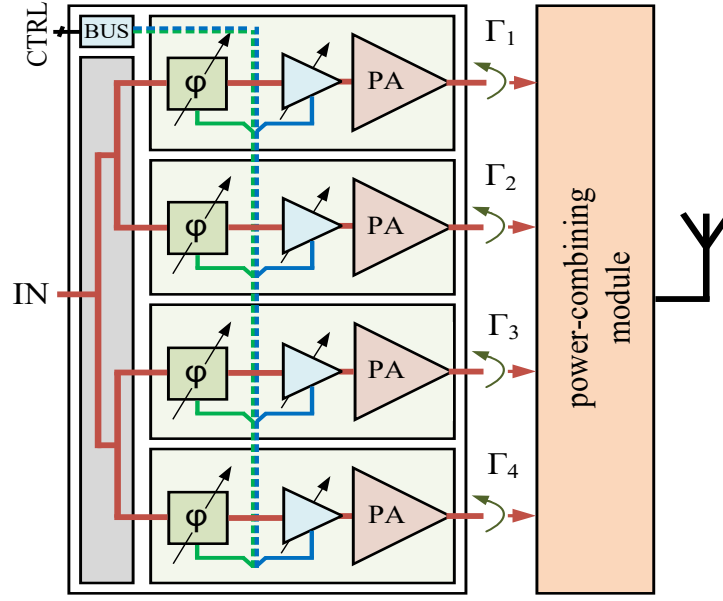
Figure 3.8: (a) The standard gain horn antenna fed by the developed multi-port power-combining module; (b) Measured H-plane normalized EIRP pattern of the standard gain horn antenna connected to the proposed spatial power-combining module (red) and conventional probe-type feed (blue) at 28 GHz. The relative difference is shown by the black dashed line.

to each other and in good agreement with the simulations shown by black dashed lines. Visible ripples are attributed to the connector interfaces and bent MLs which cannot be completely de-embedded by the designed two-port TRL calibration kit (See 2.18 (b)), since in practice the ports are slightly different.

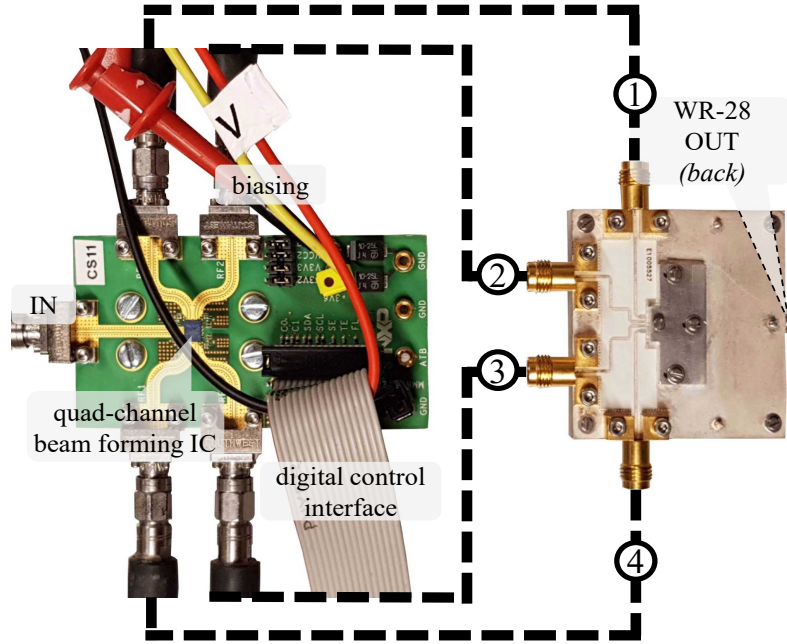
The performance of the proposed spatial power-combining module has been investigated in conjunction with a standard gain horn antenna at the desired frequency range. The standard probe-type coaxial-to-waveguide transition Anritsu Wiltron 35WR28 was used as a reference feed. Figure 3.8 shows the measured H-plane radiation pattern of the standard gain horn antenna in-pair with the proposed power-combining module at 28 GHz. The resulting radiation pattern was combined from four embedded element patterns each of those corresponding to the excitation of one port while terminating the other ports. As one can see, the relative difference between the measured patterns with the single port and multi-port feeding is negligible ( $< -35$  dB within the angular region of  $\pm 20^\circ$ ). This difference is comparable with a relative measurement uncertainty, which increases to  $-20$  dB at larger angles. This fact confirms a good rejection of higher-order propagating modes that, in general, can be excited through asymmetric feeding. The tested power-combining module allows to achieve  $\geq 5$  dB higher output power and hence increases the EIRP in comparison with the reference feed having a normalized EIRP pattern. The conclusions are the same for the E-plane patterns and these results have therefore been omitted.

In order to test the proposed concept in the presence of the critical effects of realistic PAs, the fabricated power-combining module has been interfaced with a quad-channel beamforming SiGe HBT RFIC transmitter [94], as shown in Figure 3.9 (a). The beamforming RFIC has one input and four output independent RF branches, each of which includes a Class-A PA operating in the 26.5–29.5 GHz frequency band.





(a)



(b)

Figure 3.9: (a) Architecture of the quad-channel beamforming SiGe HBT RFIC in connection with power-combining module; (b) Measurement setup for evaluating the power-combining module in conjunction with PAs (vector network analyzer and cables are not shown).



The beamforming RFIC on the evaluation board has been connected to the multi-port combiner by four short coaxial cables (See Figure 3.9 (b)). Such a connection allows for extra flexibility during the calibration and measurements. In practical applications, the RFIC can be directly mounted on the same PCB without any cables and routing lines. The gain and phase of each branch can be controlled via a digital interface. This ability has been used to compensate for various lengths of cables between the beamforming RFIC board and the power combiner. It allows driving the proposed structure with a calibrated equal amplitude and phase distribution as well as to examine the effect of amplitude and phase variations.

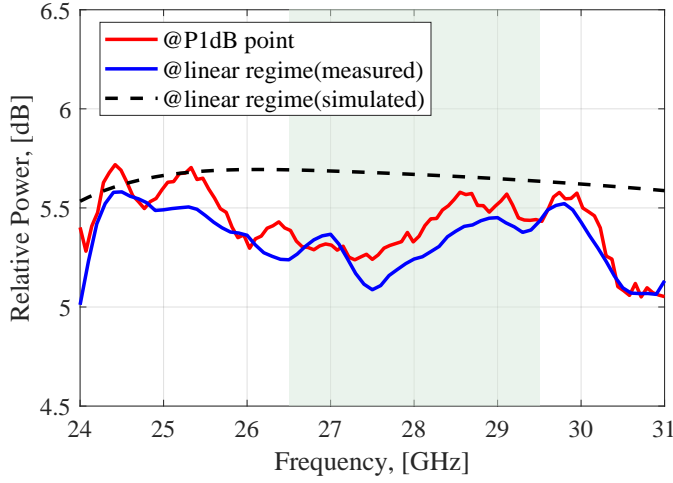


Figure 3.10: Simulated (dashed) and measured (solid) relative increase of the generated output power of the  $4\times$ PA combined by the proposed module, with respect to a single PA in non-linear (P1dB point) and linear regime. The colored region shows the operation band of PAs.

Figure 3.10 shows the relative increase of the generated output power of the  $4\times$ PA combined by the proposed module with respect to a single PA over the 24–31 GHz frequency range for different PA operational regimes. The measured results are compared to the EM simulated model, which accounts for dielectric losses. The measured result in the linear regime is close to the simulation, however, the average level is a bit lower due to the losses in the extended routing of the MLs. The dielectric and radiation losses have been estimated based on the simulated data. At 30 GHz, the total simulated losses of the DUT are 0.55 dB, where the contribution of dielectric and radiation losses are 0.19 and 0.36 dB, respectively. Radiation losses are dominant and attributed to the bent MLs, but these can be eliminated through direct MMIC interfacing. The overall insertion loss of the proposed spatial power-combining module without extended routing lines is estimated not to exceed 0.3 dB.

Figure 3.11 shows the measured combined power compared to the output power of each PA versus input power. The input and output powers were normalized to obtain 0 dB gain at the P1dB point. The non-linear behaviour of the joint PA and power-combining module is similar to that of a single PA. The performance reduction in

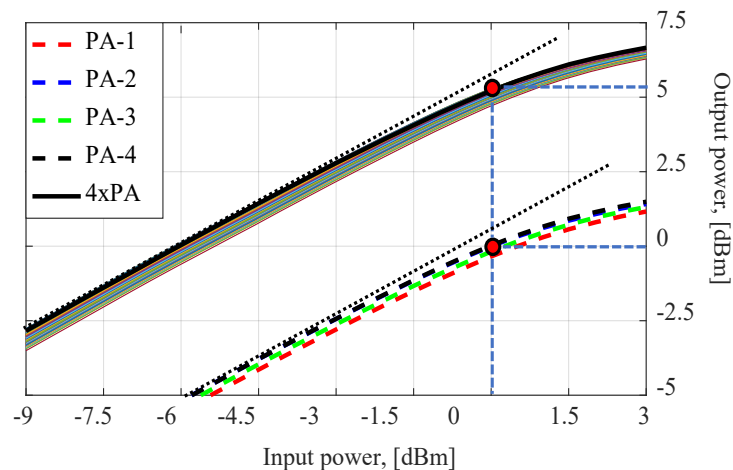


Figure 3.11: Normalized measured output power versus input power for single PAs (dashed) and after combination with the proposed power-combining module (solid) at 28 GHz. The set of curves shows measured performance reduction in the presence of  $\pm 15^\circ$  phase variation.

the presence of phase errors has been investigated by manually adjusting the phase shift for each beamformer branch. The measured set of curves (semitransparent) correspond to  $\pm 15^\circ$  phase variation. As one can see, in the worst scenario the output power decrease is less than 1 dB, which is in good agreement with simulations (See Figure 3.5).

### 3.4 Summary

The designed power-combining module facilitates efficient mm-Wave power generation and integration with antenna elements over a 42% bandwidth (24.5–37.8 GHz), where the total power loss due to this module is  $\leq 0.5$  dB in simulations and  $\leq 0.7$  dB in measurements. Moreover, the losses do not significantly increase with the number of added amplifiers, in contrast to conventional on-chip power combining techniques,

Table 3.1: Comparison between state-of-the-art solutions and the proposed designs

Reference	Number of channels	Frequency, [GHz]	Bandwidth, [%]	Losses, [dB]
CMOS on-chip [60]	2	22-26	16.7	1.4
CMOS on-chip [62]	2	16-27	51.2	1
CMOS on-chip [63]	2	30-40	29.2	1.7
CMOS on-chip [60]	4	22-26	16.7	2.4
[this work]	4	24.5-37.8	42	0.2
[this work]	8	25.1-36.4	37	0.3

as shown in Table 3.1. There is no considerable difference between the measured relative power increase in the linear and non-linear regimes. Hence, the spatial power-combining module does not affect the PA performance over the whole input power range. A typical difference between the gains of realistic PAs does not exceed the found acceptable limits for the power-combining module, *i.e.* within  $\pm 15^\circ$  and  $\pm 1$  dB for the phase and amplitude respectively. Furthermore, the antenna pattern measured with this module shows negligible deformation due to non-identical PAs.

The concept is expected to play an important role in high-power mm-Wave transmitters, where both low insertion losses and optimal active device load matching are important requirements.

## Watt-Level mm-Wave SiGe Power Amplifier

As shown in Chapter 1, active array transmitters with high-EIRP are required in order to compensate for the increased propagation and material losses at mm-Wave frequencies. The most straightforward way of achieving the desired EIRP levels is to generate high RF power (25 – 30 dBm) per antenna element [100]. However, achieving such a high power level at Ka-band is very challenging for the existing semiconductors, especially Si-based devices, due to their relatively low breakdown voltage. Despite this fact, Si-based technologies have become more attractive for emerging mm-Wave applications due to their low cost and high integration capabilities compared to III-V compound semiconductors. Moreover, the current maximum output power limit of existing mm-Wave Si-based PAs could be overcome by the proposed power combining transition owing to its intrinsically low insertion losses, which are virtually independent of the number of interfaced PAs.

This chapter describes the design and implementation of such as spatial power-combined Watt-level PA at Ka-band in SiGe BiCMOS technology, which is suitable for integration with mm-Wave array antennas. The design and performance of the combined PA and its individual building blocks are reported. The chapter starts by presenting an architecture of the combined PA and determining the performance requirements for its individual PA-cell. Based on the determined requirements, the PA-cell design and optimization aspects are described in detail with special attention to the compensation of active circuitry parasitics and passive components EM modeling. The obtained PA-cell design and performance are followed by the combined PA design and optimization description. In contrast to a stand-alone PA-cell, the design of the combined PA is more challenging since various critical multiphysics effects occurring in the joint structure have to be taken into account. Thus, a more holistic multiphysics design flow, including joint EM-circuit-thermal optimization, is presented (See Figure 4.18). It allows achieving the optimal system-level large-signal

performance of the combined PA while mitigating the thermal issues. Moreover, the chapter includes important practical considerations regarding the fabrication and assembly of the combined PA as well as its performance testing. The obtained performance of the combined Watt-level PA and its individual PA-cell are discussed in comparison with the existing PAs, where typically lossy on-chip power combining solutions are used.

## 4.1 Power Amplifier Architecture

This section presents a system-level architecture of the designed Watt-level mm-Wave PA and introduces its individual building blocks, which are described in detail in the following sections. Figure 4.1 shows the architecture of the Watt-level PA employing the proposed transition with power combining functionality. The design is based on a chip with an array of identical PA-cells, each of which is parallel-fed by using an on-chip power divider (the PA-cell design is detailed in Section 4.2). Although the presence of the lossy on-chip divider reduces the gain of the combined PA with respect to a single PA-cell, it does not significantly affect PAE due to the relatively high gain of individual PA-cells. The chip's multiple outputs are flip-chip interconnected to the power combiner placed on a laminate, which obviates the need for a potentially lossy on-chip power combiner. In order to simplify a validation of the combined PA and its comparison to conventional PA architectures with a single output port, a tapered ML transition is employed on the other side of the combiner. In practical applications, the design will include a single standard rectangular WG as an output interface (*cf.*

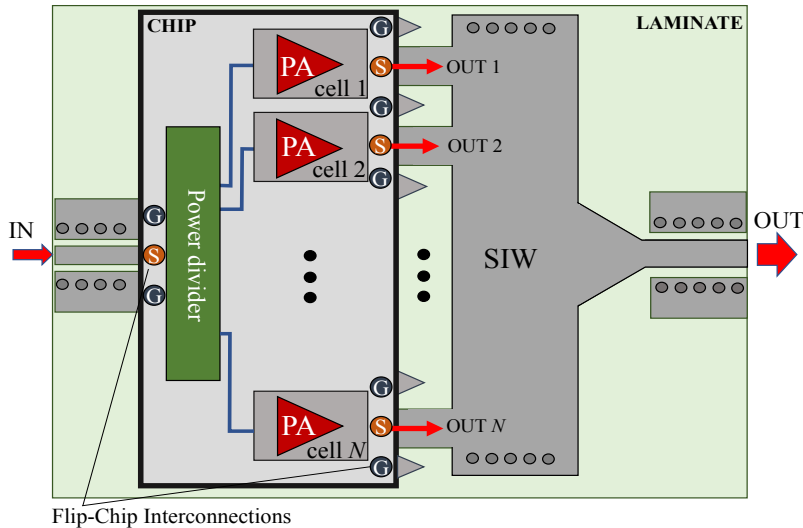


Figure 4.1: The architecture of the designed Watt-level mm-Wave PA employing the proposed transition with the power combining functionality. A chip with multiple PAs is flip-chip interconnected to the SIW combiner placed on a laminate.

Chapter 3) or directly an SIW-based antenna element [90, 91, 101]. Therefore, the tapered ML transition will not be needed.

Currently, there are no commercially available chips suitable for the proposed architecture. Moreover, reported single PA designs implemented in Si-based processes at these frequencies either have insufficient output power ( $\leq 15$  dBm) [102–104] or include lossy power combiners, which dramatically reduce efficiency and limit the operation bandwidth [105, 106]. As a result, the performance of the combined PA might be restricted by the moderate performance of its PA-cell. Therefore, the essential next step towards the realization of the efficient Watt-level spatial power-combined PA is to design a custom PA-cell, of which the stand-alone performance has to be on the edge of the current state-of-the-art in Si-based mm-Wave single-stage PAs [107–109].

The main performance targets are:

- High output power <sup>1</sup>( $\geq 23$  dBm);
- High PAE <sup>1</sup> ( $\geq 25\%$ );
- Wide bandwidth ( $\geq 30\%$ );
- Compact size ( $\leq 0.5 \times 0.5$  mm).

The last item allows one to fit more PA-cells on the same chip, and hence, increases the combined output power.

## 4.2 Power Amplifier Cell

### 4.2.1 Overall Design Description

The PA design is implemented in an advanced high-speed SiGe process from NXP Semiconductors, which is one of the main industrial partners of the Silika project [70]. This process is derived from the highly successful QUBiC4 0.25  $\mu\text{m}$  BiCMOS technology family [97]. A high degree of commonality with the parent technology ensures low cost of wafers, high manufacturability, and high quality proven in high volume. The technology offers crucial features for mm-Wave designs, such as high-voltage (HV) and low-voltage (LV) HBTs with a high cutoff frequency, high-density metal-insulator-metal (MIM) capacitors, six metal layers for back-end interconnections, and deep trench isolation (DTI). The HV-device has intrinsically higher collector-emitter breakdown voltage, however its peak transition frequency, where current gain goes to unity,  $f_t/f_{\text{max}} = 90/200$  GHz is lower compared to the LV-device with  $f_t/f_{\text{max}} = 180/200$  GHz.

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<sup>1</sup>Performance is at 1-dB compression point

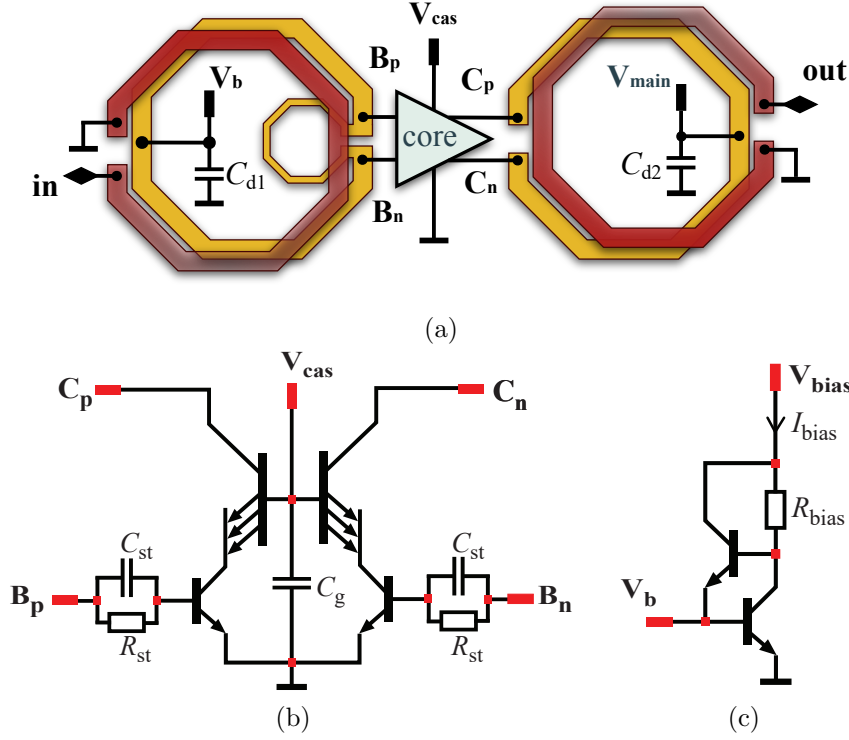


Figure 4.2: The PA-cell design: (a) Block diagram including input/output baluns configurations; (b) Differential cascode PA circuit diagram; (c) Biasing network circuit diagram.

Although an ideal common-emitter PA provides the highest power amplification (compared to other configurations) as it has both voltage and current gain, a common-emitter (CE) configuration is not the first choice for high-power mm-Wave PAs [110]. The latter is caused by the excessive base-collector parasitic capacitance,  $C_{bc}$ , of a large multi-fingers device required for the generation of high output current. Since the CE configuration is an inverting amplifier [47], the parasitic  $C_{bc}$  applies increasing negative feedback and hence, reducing the gain as the frequency increases. This phenomenon is called Miller effect [111] and could be represented by the increased equivalent input capacitance expressed as:

$$C_{in} = C_{be} + C_{bc} \cdot (K_u + 1), \quad (4.1)$$

where  $C_{be}$  is the physical base-emitter capacitance,  $K_u$  is the voltage gain of the PA. In contrast to the CE configuration, common-base (CB) PAs do not suffer from the Miller effect since they do not invert signal. However, their current gain is  $\leq 1$  [47].

In the present design, the PA-cell is based on a differential cascode configuration, which allows achieving both high gain and wide operation bandwidth by eliminating the Miller effect. The PA-cell consists of a differential CE input pair driving a differential CB output pair referenced to the emitter voltage of the CE pair [112], as shown in Figure 4.2. In this case, CE stages are loaded by the followed CB stages in such

a way that their voltage gain is unity. The latter results in a negligible increase of  $C_{in}$  due to the Miller effect (See Equation 4.1). The CE stage provides current gain, whereas the CB stage voltage gain. The cascode configuration also allows achieving a significant improvement in common-mode rejection compared to a conventional differential pair. Moreover, operation in differential mode doubles the output voltage, and hence, the output power, while it lowers the even-order harmonics compared to a single-ended structure [113]. However, since the chosen architecture requires PA-cells with single-ended  $50\text{-}\Omega$  input and output, balanced-to-unbalanced transformers (baluns) are required to convert a single-ended signal to differential and vice versa. In this design, stacked Marchand baluns based on coupled TLs are employed due to their wide frequency bandwidth and low insertion losses [114, 115]. A simple biasing network based on a buffered current mirror has been implemented to set the fixed cascode reference current corresponding to the class A/B operation point, as shown in Figure 4.2 (b). The designed PA-cell requires three DC biasing voltages:  $V_{main}$  – voltage applied to collectors of CB devices,  $V_{cas}$  – voltage applied to bases of CB devices, and  $V_{bias}$  – voltage required for the biasing circuit, which sets the operation point. The default biasing settings are:  $V_{main} = 5\text{ V}$ ,  $V_{bias} = 2.5\text{ V}$ ,  $V_{cas} = 1.5\text{ V}$ . To protect the PA from a possible electrostatic discharge (ESD) overstress during fabrication, assembling, and testing, the design is equipped with an ESD protection circuit.

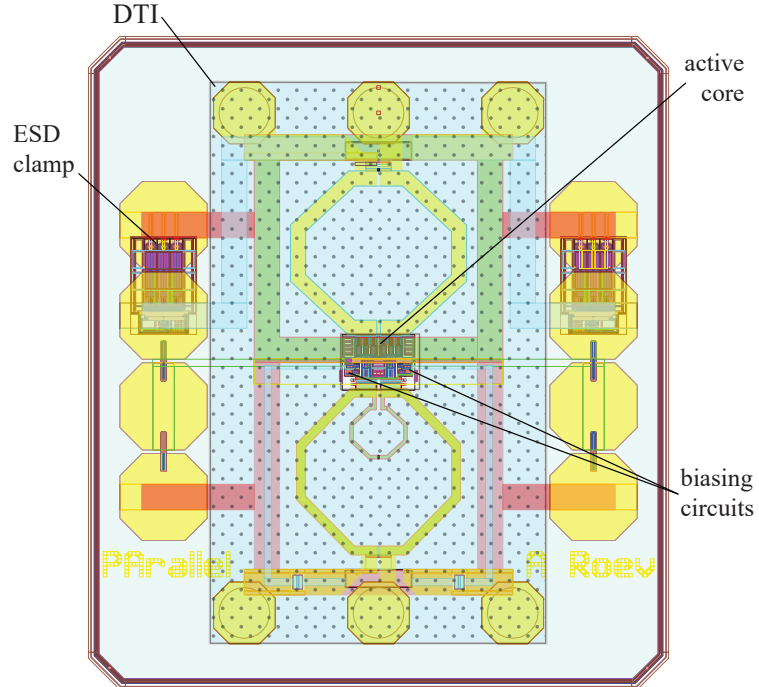


Figure 4.3: A top-level layout of the designed PA-cell including pads for on-wafer testing. The filling pattern indicates the position of the DTI layer.



In order to reduce the substrate parasitics and effectively increase the substrate resistivity, DTI is implemented below the baluns and RF pads. However, due to its high computational complexity, performing a full-wave simulation of a DTI layer is impossible. Therefore, to evaluate the impact of the DTI layer on the PA-cell performance, two types of PA-cells have been prepared for tape-out: with and without the DTI layer. Figure 4.3 shows a top-level layout of the PA-cell indicating the positions of its modules and pads for on-wafer probing. The filling pattern corresponds to the position of the DTI layer.

The design and optimization of the main PA-cell modules are described in detail in the following sub-sections.

### 4.2.2 Active Circuitry

Although the employed configuration does not suffer from the Miller effect, its input capacitance might still be significant due to layout parasitics of relatively large devices [116]. Figure 4.4 shows a simplified equivalent circuit model of the HBT, which includes layout parasitic effects [117]. Capacitors  $C_{bc}$ ,  $C_{be}$ ,  $C_{ce}$  represent inter-electrode capacitances between multiple base-emitter, base-collector, and collector-emitter fingers, respectively. The ohmic losses in routing lines and interconnections between different metal layers, required for parallel connection of the corresponding fingers, are represented by resistors  $R_c$ ,  $R_b$ ,  $R_e$ .

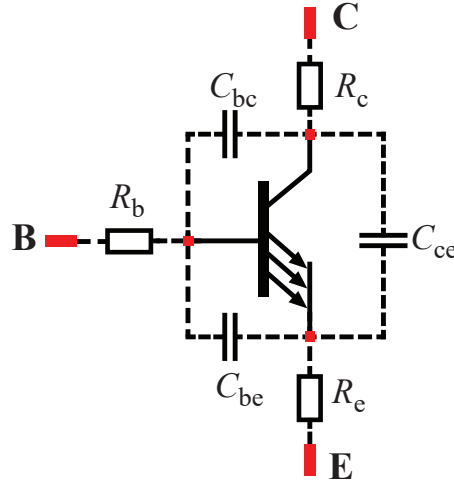


Figure 4.4: A simplified equivalent circuit model of the HV-HBT, which includes parasitic effects of the layout.

The total emitter area determines the maximum achievable output power of a device. Since the width of an emitter finger is typically set by the chosen technology, there are two degrees of freedom - emitter length and the number of fingers. Increasing the length of emitters leads to proportional power increase. However, it also

Table 4.1: The configuration of the designed HBTs

	HV-CB	LV-CE	LV-biasing (buffer)	LV-biasing (mirror)
Emitter width, $\mu\text{m}$	0.4	0.4	0.5	0.4
Emitter length, $\mu\text{m}$	25.2	25.2	4.5	1.0
Collector plug width, $\mu\text{m}$	1.3	1.3	1.3	0.5
Number of emitters	3	3	1	1
Number of cells	3	1	1	1

enlargements parasitic capacitances and, as a result, reduces the gain. Using devices with multiple relatively short fingers allows reducing inter-electrode capacitance, but this solution requires additional interconnecting lines, which increase parasitic resistances. Therefore, iterative optimization of the device topology has been used to maximize the emitter area and minimize layout parasitics.

The found optimal CB device is formed by a parallel connection of three HV-HBTs, each of which has three emitters with a length of  $25.2 \mu\text{m}$ , as shown in Table 4.1. The total HV-HBT emitter area is  $90.72 \mu\text{m}^2$ . The corresponding parasitic values are:  $C_{bc} = 15 \text{ fF}$ ,  $C_{be} = 17.2 \text{ fF}$ ,  $C_{ce} = 6.3 \text{ fF}$ ,  $R_c = 201 \text{ m}\Omega$ ,  $R_b = 399 \text{ m}\Omega$ ,  $R_e = 296 \text{ m}\Omega$ . In the used SiGe process, the optimal current density corresponding to the peak  $f_t$  is three times higher for LV devices as compared to HV devices [118]. Therefore, since in the employed cascode configurations, both types of devices share a common collector current, the emitter area of the LV-CE device should be three times smaller. As a result, the LV-CE device has the same emitter length as the CB device but only three fingers.

Even though the cascode configuration allows increasing isolation, the oscillation of the CB device, caused by parasitic inductance between the distributed base and ground, might still be an issue. Therefore, the shunt capacitor,  $C_g$ , has to provide the shortest possible connection between the CB device bases and ground. To do that,  $C_g$  is realized by a parallel connection of three banks, each of which consists of four poly-capacitors. The banks are placed in a symmetric way all around the CB devices; the total  $C_g = 1.5 \text{ pF}$ . Despite their moderate Q-factor compared to other capacitors [97], poly-capacitors do not require any extra interlayer interconnections suffering from high parasitic inductance. In order to enhance electrical stability at lower frequencies, additional high-pass shunt RC networks ( $R_{st} = 8 \Omega$ ,  $C_{st} = 1 \text{ pF}$ ) are connected to the bases of CE devices in a symmetric way. At the operation frequency band,  $C_{st}$  works as a bypass, and hence PA-cell gain is not degraded.

A simple active biasing network based on a buffered current mirror [119, 120] has been employed (See Figure 4.2 (b)). The emitter area of the input current-mirror device,  $S_1 = 0.4 \mu\text{m}^2$ , is chosen to be much smaller than the CE-device area in the cascode stage,  $S_2 = 30.24 \mu\text{m}^2$ . The ratio  $S_2/S_1$  results in the current gain of

75.6. The input current,  $I_{\text{bias}} = 265 \mu\text{A}$ , is defined by the resistor  $R_{\text{bias}} = 4 \text{ k}\Omega$ . The corresponding output current,  $I_c = 20 \text{ mA}$ , sets the class A/B operation point. Owing to its high current multiplication factor, the designed biasing circuit has negligible power consumptions ( $663 \mu\text{W}$ ) and hence does not affect the PA-cell PAE. A possible temperature gradient between the devices forming the current mirror causes a drift of the PA-cell operation point. To eliminate this effect, the biasing circuit is split into two parts, which are placed in close proximity to the CB devices, where the temperature hotspot is (See Figure 4.3).

### 4.2.3 Passive Circuitry

At mm-Wave frequencies, as the wavelength of on-chip signals becomes compared with circuit dimensions, conventional RC-extraction and EM modeling of stand-alone passive components are insufficient and lead to sub-optimal performance and, in the worst-case, failure of the design [121]. That results from ignoring the effects of interconnections, unwanted mutual coupling between closely spaced components, and distributed ground topology. The dominant impact of passive circuitry's realistic layout on the overall performance demands its inclusion at an early stage of design.

In the present case, the passive circuitry is mainly formed by input and output Marchand baluns based on coupled TLs and distributed ground topology placed around the interior layout, as shown in Figure 4.2 (b). The baluns are primarily needed to convert a single-ended signal to differential and vice versa [114, 115]. The output balun has an impedance transformation functionality in order to match the complex optimal load impedance of the core to  $50\text{-}\Omega$ . Based on the performed load-pull simulations (See Figure 4.5 (a)), the designed differential cascode stage has an optimal differential load represented by a parallel connection of  $C_L = -90 \text{ fF}$  and  $R_L = 70 \text{ }\Omega$ , as shown in Figure 4.6. This equivalent load allows for achieving both high output power ( $\geq 23.8 \text{ dBm}$ ) and efficiency ( $\geq 39\%$ ) over the wide frequency range ( $> 50\%$ ). However, since a passive balun circuitry cannot emulate the frequency behavior of negative capacitance, the obtained frequency bandwidth of the PA-cell is more narrow. For maximization of the PA-cell gain, the impedance of input balun needs to be conjugate matched to the core input impedance. The differential input impedance of the PA-cell core could be approximated as a series connection of relatively small resistance and positive capacitance. Therefore, to realize wideband conjugate matching, the input balun impedance should behave as a series connection of  $C_S = -279 \text{ fF}$  and  $R_S = 8.64 \text{ }\Omega$  (See Figure 4.6). The latter is obtained in the desired frequency range by using the balun with a high impedance transformation ratio and an additional compensation inductor. The DC biasing voltages,  $V_{\text{bias}}$  and  $V_{\text{main}}$ , are applied at the center tap of the corresponding baluns to eliminate the need for separate bias chokes, as shown in Figure 4.2 (a). Relatively large decoupling capacitors,  $C_{d1} = C_{d2} = 10 \text{ pF}$ , connecting the center taps of the baluns to the

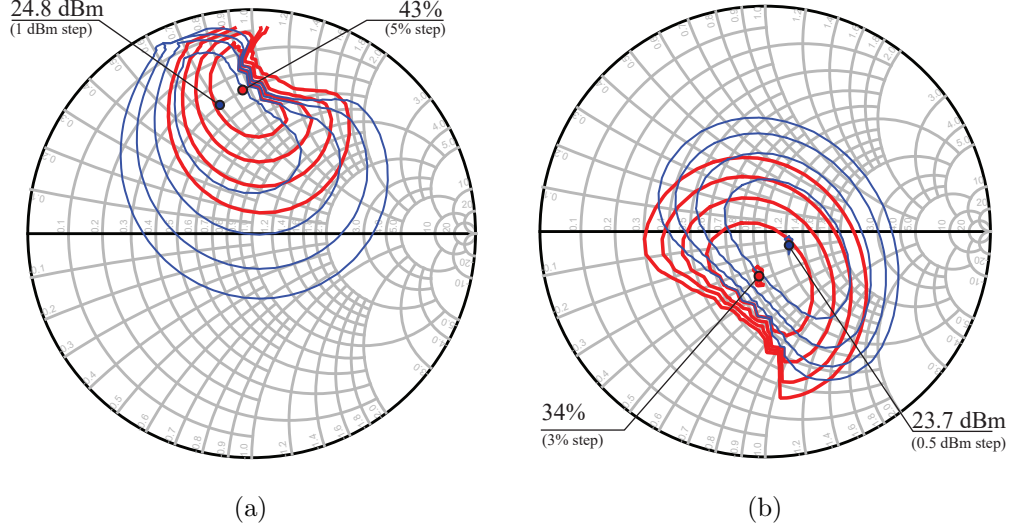


Figure 4.5: Simulated load-pull contours of PAE (red) and P1dB output power (blue) at 30 GHz: (a) PA-cell core with differential load; (b) Complete PA-cell with single-ended 50-Ω load.

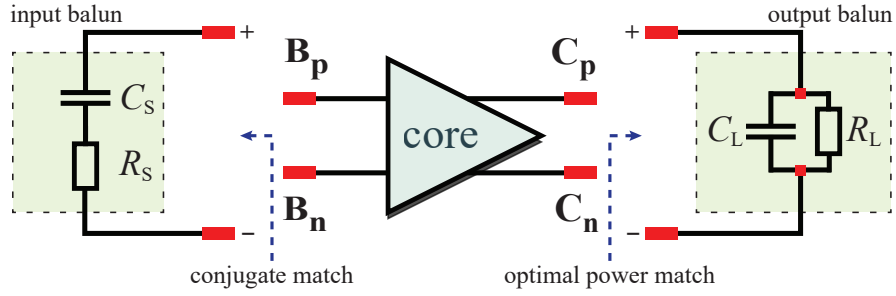


Figure 4.6: A simplified equivalent circuit model of the PA-cell core optimal input and output loads.

ground make a broadband low impedance path required for low-frequency stability and common-mode rejection. The baluns are placed on the top metal layer (M6/M5), which allows one to minimize the negative effect of substrate parasitics and reduce the resistive losses since these layers are thicker [97]. However, once the chip is flip-chip interconnected to the laminate, the performance of the baluns might be significantly affected by the presence of solder masks and laminate itself. Therefore it is essential to take these effects into account at the stage of PA-cell design.

Figure 4.7 (a) shows a circuit-level block diagram of the PA-cell simulation model used for passive circuitry optimization. It consists of RLC extracted circuit of the interconnected devices (core) and  $8 \times 8$  S-matrix representing the complete EM model of the structure, as shown in Figure 4.7 (b). The EM model has single-ended input and output ports placed on the laminate, four ports placed on-chip for connection of the PA-cell core, and two ports for applying biasing voltages and connecting decoupling capacitors. The baluns and ground topology geometry have been optimized using a finite element method EM-solver in Ansys HFSS, which perfectly works with com-

plex multiport models and allows setting arbitrary excitation during post-processing without resimulations. The key optimization goals are wideband impedance matching ( $\geq 40\%$ ) and high common-mode rejection ( $\geq 35$  dB). Moreover, the performed complete EM modeling allowed to identify the reason for possible PA-cell oscillations caused by the excessive inductive coupling between the top turns of input and output baluns leading to positive feedback. The latter issue is overcome by reorienting the

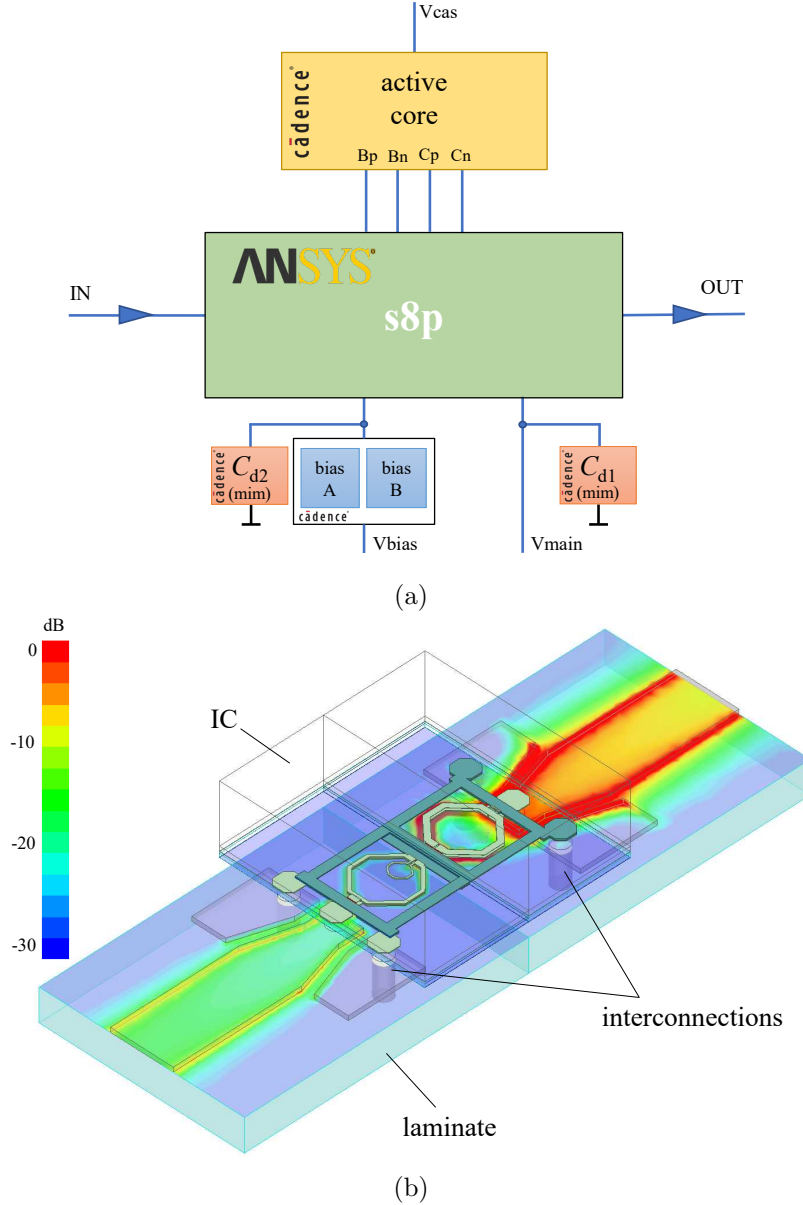


Figure 4.7: The simulation model of the PA-cell: (a) Circuit level block diagram; (b) EM model of the die flip-chip interconnected to the laminate. The color map represents the magnitude of the real part of the E-field distribution at 35 GHz.

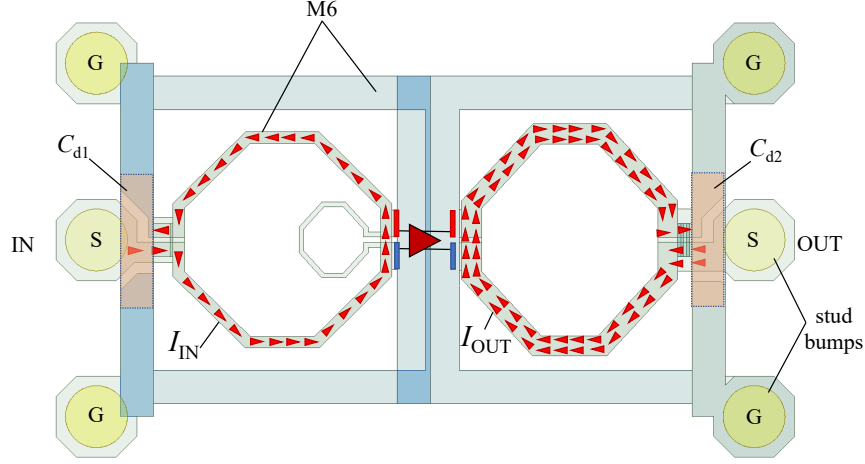


Figure 4.8: Simulated surface current density vector on the top turn of the input and output baluns at 35 GHz.

top turns of input and output baluns in such a way that the corresponding currents flow in different directions, as shown in Figure 4.8. The simulated  $K$ -factor confirms that this arrangement makes the PA-cell unconditionally stable. Figure 4.5 (b) shows the simulated load-pull contours of the complete PA-cell with single-ended 50- $\Omega$  load placed on the laminate. As one can see, the obtained peak values of the output power and PAE are reduced by 1.1 dB and 9%, respectively, compared to the PA-cell core with the optimal differential load. These values are found acceptable and mostly caused by losses in the output balun and interconnections to the laminate.

#### 4.2.4 ESD Protection Circuit

Shrinking the physical dimension of semiconductor devices allows one to advance their high-frequency performance and integrate more modules with different functionalities on the same chip. However, it makes chips more vulnerable to ESD overstress [122, 123]. The latter might lead to failures in junctions, isolation oxides, or metallization. In order to protect the designed PA from a possible ESD overstress during fabrication, assembling, and testing, the design is equipped with an ESD protection circuit, as shown in Figure 4.9. It consists of an ESD clamp circuit limiting voltage and multiple diodes connected in-between biasing pads and ground [124]. The diodes are inverse-biased under normal operating conditions. But when the voltage at DC pads rises above  $V_{\text{main}}$  or gets negative, some diodes become forward-biased forming a current discharge path, thereby protecting the PA [125]. To keep the design symmetry, the ESD protection circuit has been split into two parts, each of which is placed under the corresponding biasing pads located on the different sides of the PA-cell die, as shown in Figure 4.3.

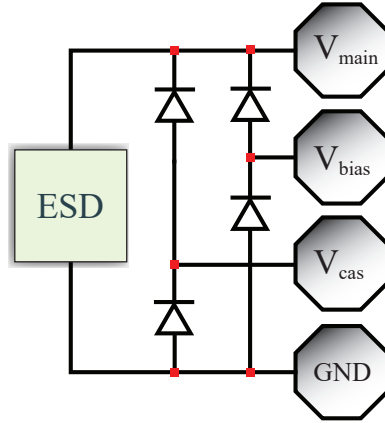


Figure 4.9: A simplified model of ESD protection circuit placed under the corresponding DC biasing pads.

### 4.2.5 Experimental Setup

To make an estimate of the combined PA performance and properly evaluate combining efficiency later, the designed stand-alone PA-cell needs to be priorly tested in both small and large signal regimes. For this reason, the stand-alone PA-cell design is equipped with pads for on-wafer measurements. The size of the fabricated PA-cell including pads for on-wafer measurements is  $0.8 \times 0.9$  mm.

Figure 4.10 shows a block diagram of the measurement test bench. The biasing voltages are applied from both sides of the chip by 125  $\mu\text{m}$  pitch Eye-Pass DC probes, each of which has a ground-power-power-ground (GPPG) configuration. That is needed to keep DC routing lines on the chip symmetric as well as to reduce the effect of their electrical resistance. RF probes have a standard GSG configuration with a 175  $\mu\text{m}$  pitch. A short-open-load-thru (SOLT) calibration substrate is used in order to de-embed effects of the probes from measurement results. Small-signal measurements have been directly performed using a 67 GHz Keysight PNA-X N5247A VNA, whereas large-signal measurements require an additional power calibration module and preamplifier driving the DUT with high power. In order to evaluate the efficiency of the designed PA-cell, its power consumption has been measured by a DC power supply with a remote interface, as shown in Figure 4.11. The expected measurement uncertainty does not exceed 0.2 dB and 1% for output power and efficiency, respectively.

Both types of reticles with and without the DTI layer are placed and measured on the same 150 mm wafer. Its relatively large surface area is in good thermal contact with a vacuum chuck, which has an ambient temperature of 25  $^{\circ}\text{C}$ . Therefore, additional cooling solutions are not required.

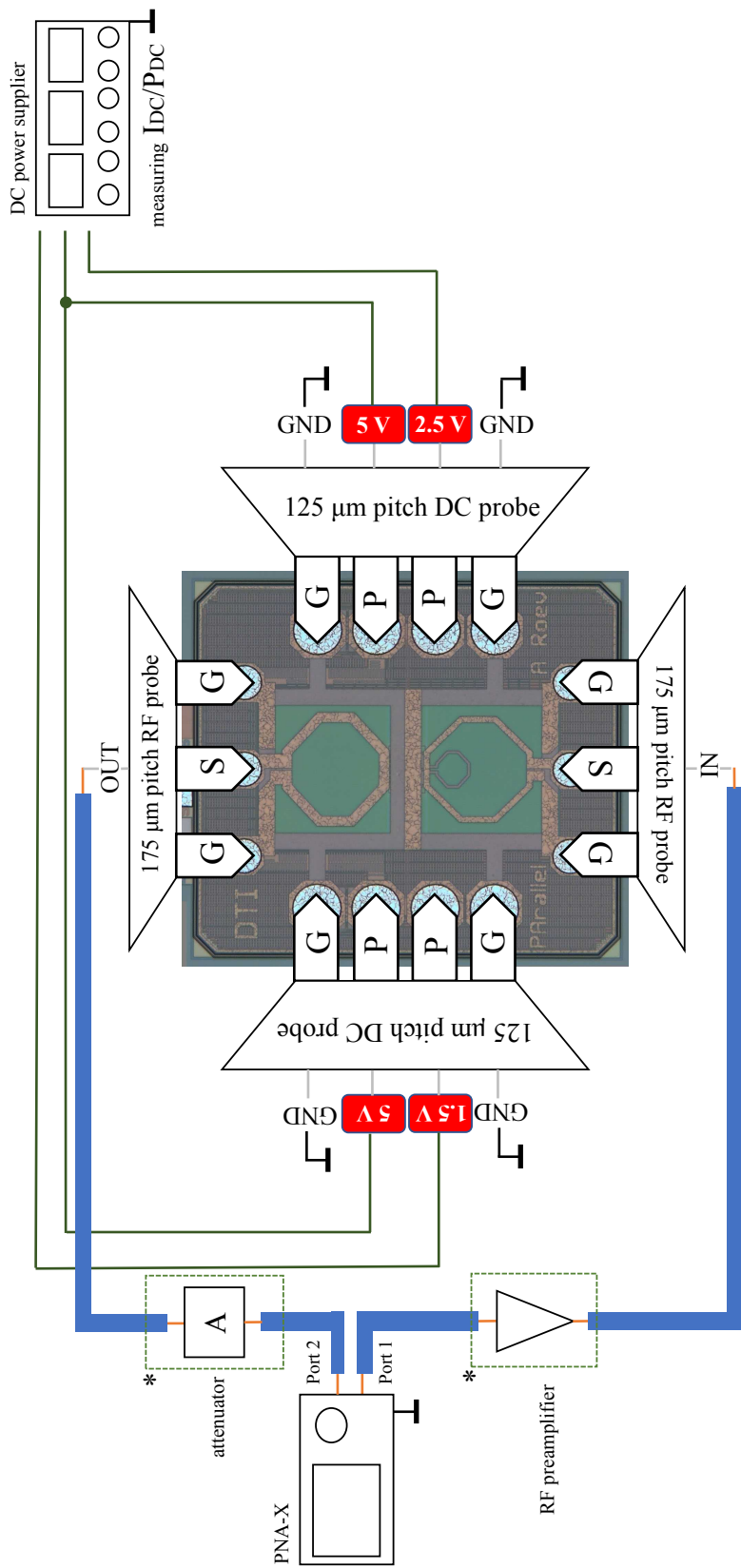


Figure 4.10: Block diagram of the measurement test bench. On-wafer measurements are performed using 175 μm GSG RF probes and 125 μm GPPG for the DC biasing. Large-signal measurements require an additional pre-amplifier driving the DUT with high power. In order to remain the measuring output signal within VNA dynamic range, a discrete attenuator is used.



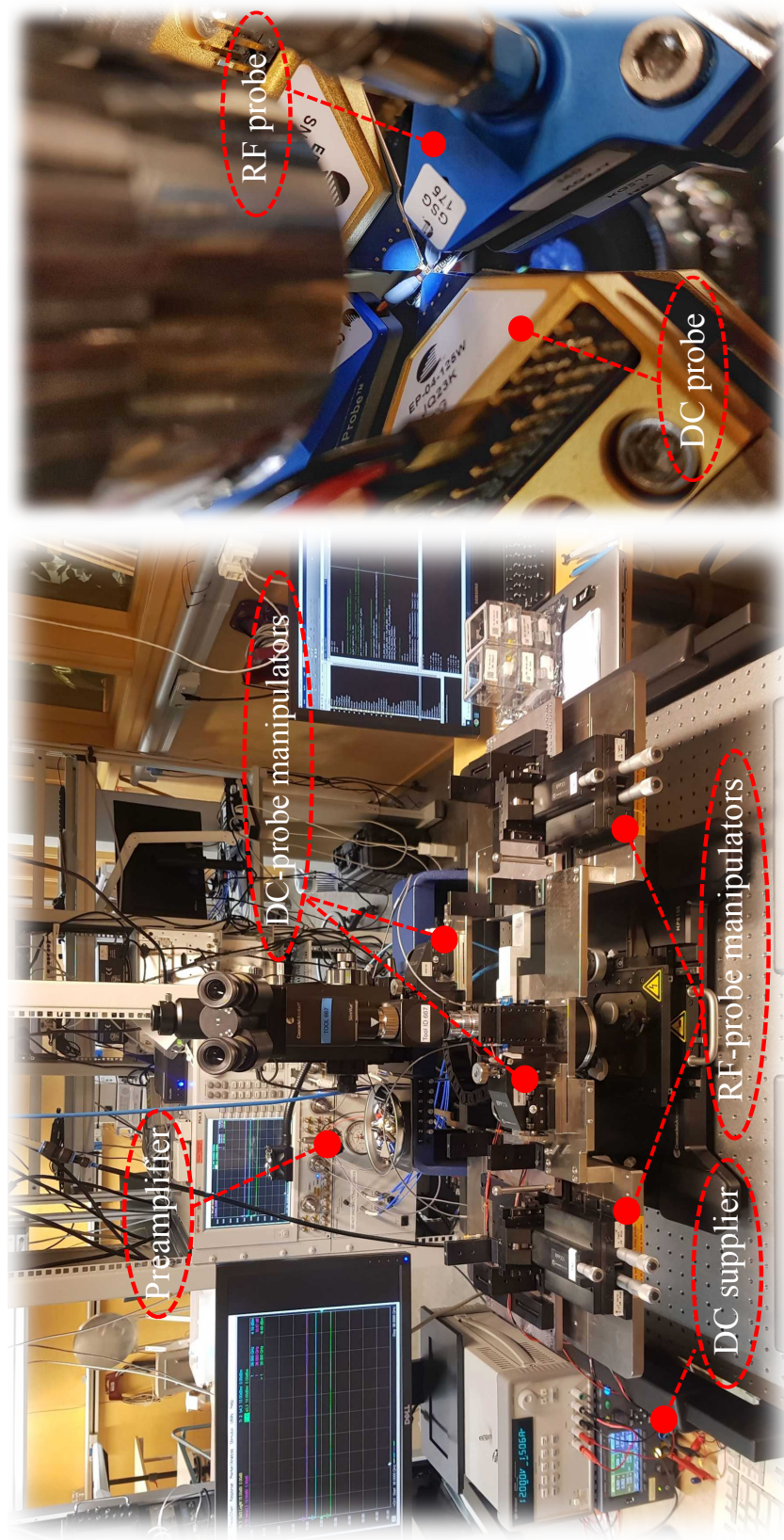


Figure 4.11: Photo of the measurement setup. On-wafer measurements are carried out using a Cascade Microtech mechanical probe station with four manipulators.

### 4.2.6 Measurement Results

The measured small-signal performance of both types of PA-cell<sup>2</sup> with and without the DTI layer is shown in Figure 4.12 (a) and (b), respectively. The presented results correspond to the samples with the highest measured low-signal forward gain,  $|S_{21}|$ . The corresponding simulated curves are shown by dashed lines as the reference. The measured low-signal curves over the 0.1 – 45 GHz frequency range for both designs exhibit similar behavior as the simulations. The input reflection coefficient,  $|S_{11}|$ , is below  $-10$  dB over the 25 – 45 GHz range resulting in  $\geq 57\%$  fractional bandwidth. The obtained wideband impedance matching results from the properly chosen equivalent circuit representation of the CE stage input impedance, which has

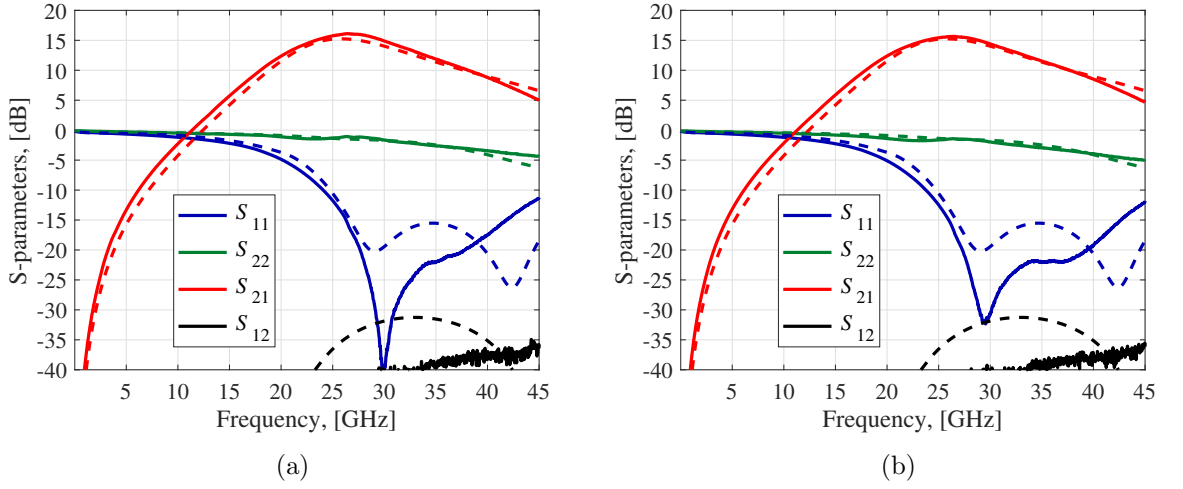


Figure 4.12: Simulated (dashed) and measured (solid) small-signal performance of the designed PA-cell<sup>2</sup>: (a) With DTI; (b) Without DTI.

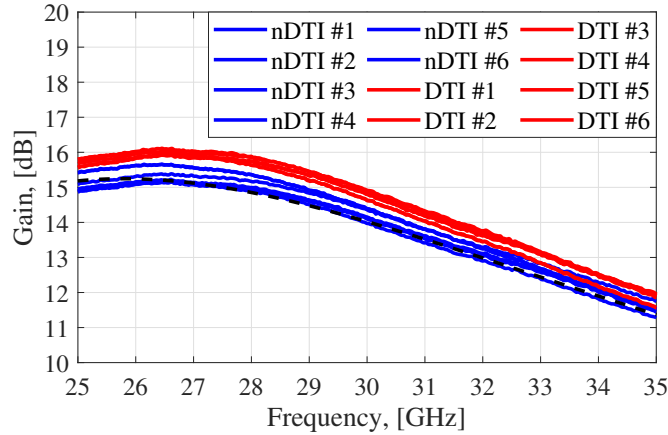


Figure 4.13: Measured forward power gain of the PA-cells with (red) and without (blue) DTI. The set of curves corresponds to different samples. The simulations are shown by the black dashed line.

<sup>2</sup>Samples with the highest measured gain

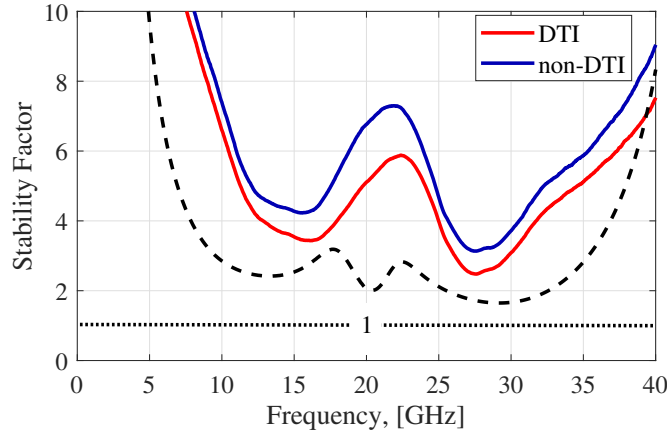


Figure 4.14: Simulated (dashed line) and measured (solid line) stability factor of the PA-cell<sup>3</sup> with (red) and without (blue) the DTI layer.

been used at the phase of the input balun optimization. However, the average level of  $|S_{11}|$  of the PA-cell without DTI is lower compared to the design with DTI. The latter might be explained by the increased losses in the output balun caused by the silicon substrate's low resistivity. The measured  $|S_{22}| \geq -5$  dB for both designs is a result of the performed optimal power matching, which is different from conjugate matching. However, for some applications that require the PA-cell output to act as the matched 50- $\Omega$  load, the existing PA-cell configuration might be supplemented by a negative feedback circuit. The measured reverse isolation,  $|S_{12}|$ , remains below  $-35$  dB levels over the entire frequency band, resulting from the carefully designed ground topology.

Figure 4.13 shows the measured forward power gain of the fabricated PA-cells. The sets of red and blue curves correspond to different tested samples with and without DTI, respectively. The maximum obtained PA-cell gain of 16.1 dB can be observed at 26.6 GHz and corresponds to the sample with DTI. The samples without DTI demonstrate the same frequency behavior, but their gain is 0.8 dB lower on average. The latter confirms a significant effect of substrate parasitics on the performance of input and output baluns. The simulated PA-cell gain demonstrates better agreement with the tested samples without the DTI layer. Therefore, the used equivalent substrate model does not accurately represent the isolation effect of DTI at Ka-band. Both designs demonstrate 3-dB bandwidth of 45%, which corresponds to 20.8 – 33 GHz frequency range. The calculated relative gain spread between the tested samples of the same type does not exceed 0.5 dB and is mainly attributed to die-to-die process variability. The effect of wafer-to-wafer process variation on the PA-cell performance has not been studied due to the limited number of available wafers. The stability  $K$ -factor calculated from the measured data confirms that the

<sup>3</sup>Samples with the highest measured gain

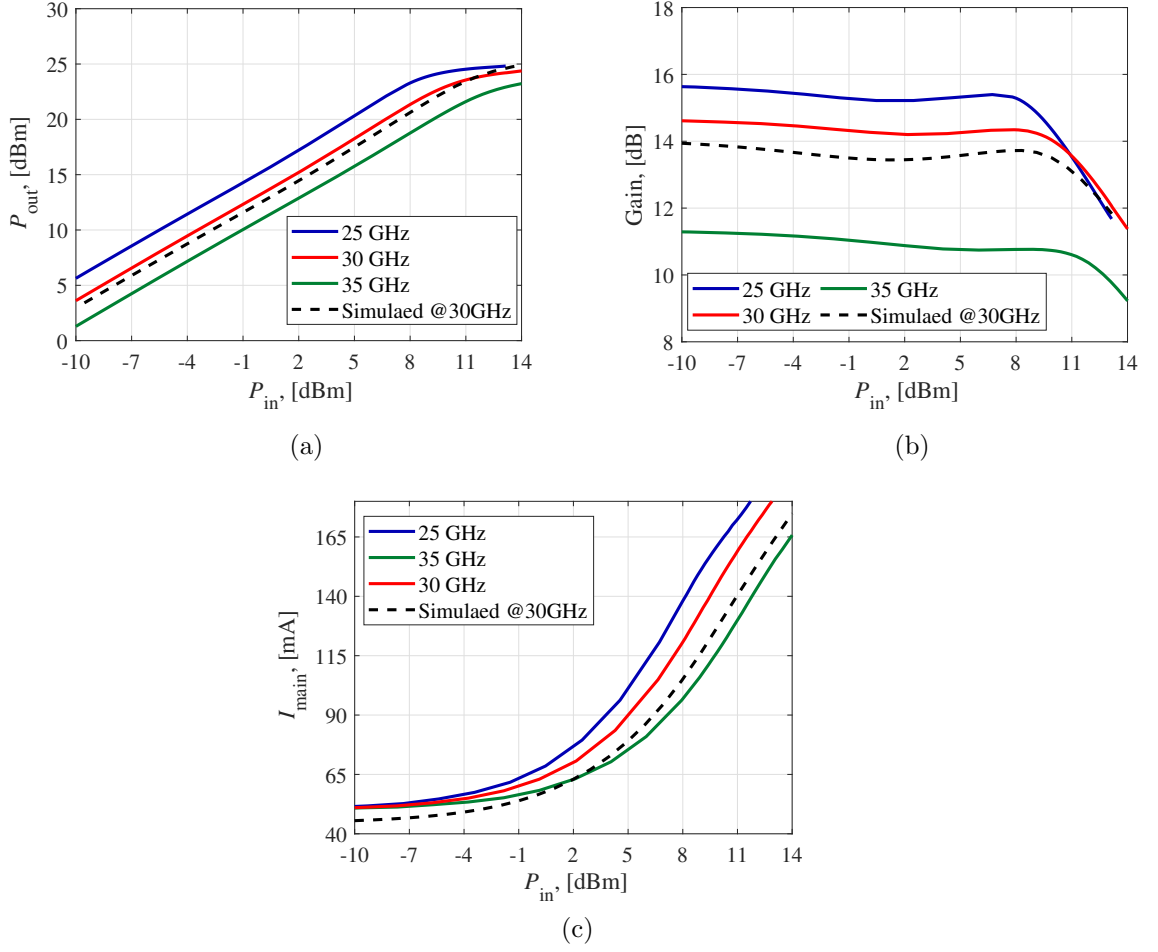


Figure 4.15: Measured (solid) and simulated (dashed): (a) output power, (b) power gain, (c) cascode collector current of the PA-cell<sup>4</sup> versus input power. The set of curves corresponds to different frequencies.

circuit is unconditionally stable (See Figure 4.14) [47]. The relatively higher  $K$ -factor values of the PA-cell without the DTI layer result from its intrinsically lower forward gain.

The output power,  $P_{out}$ , and power gain versus input power,  $P_{in}$ , are shown in Figure 4.15 (a) and (b), respectively. The results correspond to the sample with the DTI layer and the highest measured gain. As one can see, the gain variation before compression over different input power levels remains within  $\leq 0.5$  dB for all the tested frequencies. The latter is inherent for the chosen class A/B operation, which has low distortion. Although there is an offset ( $\leq 0.6$  dB) between the simulated (dashed) and measured curves, their behavior is in good agreement. Figure 4.15 (c) shows the cascode collector current,  $I_{main}$ , of the PA-cell with DTI as a function of  $P_{in}$ .

<sup>4</sup>Sample with the DTI layer and the highest measured gain

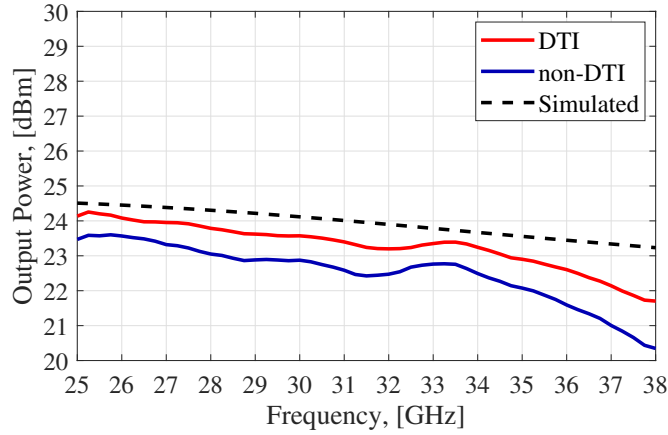


Figure 4.16: Comparison between the measured (solid line) and simulated (dashed line) output power levels of the PA-cell at 1-dB compression point ( $P_{1dB}$ ).

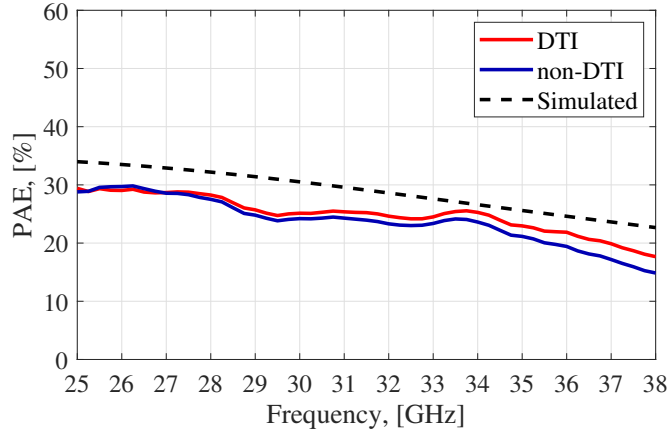


Figure 4.17: Measured (solid line) and simulated (dashed line) PAE of the PA-cell at 1-dB compression point.

The measured quiescent current has a value of 52.5 mA, which is 12% higher compared to the simulations shown by the dashed line. This relative difference remains constant over the different  $P_{in}$  levels and is attributed to the inaccurate device models. The cascode collector current exceeds a value of 140 mA in the output power compression region resulting in 0.7 W power consumption.

The PA-cell<sup>5</sup> output power and PAE over the operating frequency band (25 – 38 GHz) are shown in Figure 4.16 and 4.17, respectively. The results correspond to default biasing settings. The maximum obtained output power<sup>6</sup> of 24.2 dBm can be observed at 25.5 GHz and corresponds to the sample with the DTI layer. The measured output power of the PA-cell without the DTI layer demonstrates similar

<sup>5</sup>Samples with the highest measured gain

<sup>6</sup>Performance is at 1-dB compression point

behavior over the frequency, however, its level is 0.8 dB lower on average. The output power 1-dB bandwidth is about 12.2 GHz, ranging from 22.0 GHz to 34.2 GHz, and corresponds to a 43% fractional bandwidth.

The measured PAE of the PA-cell with DTI reaches the maximum value of 29.8% at 26.2 GHz and remains above 26% over the entire 1-dB  $P_{1dB}$  bandwidth. In contrast to output power, the measured PAE of the sample without DTI does not significantly degrade compared to the PA-cell with the DTI layer. The latter results from changing the load impedance of the PA-cell due to substrate parasitics in such a way that it leads to the maximization of its PAE. The differences between the measurements and simulations are believed to be due to the limited accuracy of the Si substrate EM model as well as complex distributed effects in the relatively large devices.

#### 4.2.7 Summary

Cross-comparison between two types of the fabricated PA-cells shows that the PA-cell with the DTI layer has overall better performance than the same design without DTI. The latter results from the reduced substrate parasitics and effectively increased substrate resistivity by inserting the DTI layer under the baluns and RF pads. Therefore, the further analysis includes the PA-cell with the DTI layer only.

Table 4.2 compares the developed PA-cell and the recently published silicon-based single-cell PAs operating in class A/B. The designed PA-cell has a wideband performance (43%) with both high efficiency ( $PAE \geq 26\%$ ) and high output power ( $P_{1dB} \geq 23.2$  dBm), which outperforms the state-of-the-art single-cell silicon-based PAs. The high output power and efficiency is the result of:

- the chosen differential cascode configuration, which eliminates the Miller effect;
- the minimized parasitic effects in multiple relatively large devices and interconnections between them;
- the carefully designed and optimized input and output baluns with wideband performance and low insertion losses.

The compact size of the PA-cell ( $\leq 0.8 \times 0.9$  mm) allows placing multiple cells on the same chip.

The next steps will be devoted to the implementation of a combined Watt-level PA employing the developed PA-cells in conjunction with the proposed spatial power-combining transition.

Table 4.2: Performance comparison of the state-of-the-art Ka-band single-stage Si-based PA-cells

Reference	Architecture	$P_{1dB}$ , [dBm]	Bandwidth (1-dB $P_{1dB}$ )	Gain (peak), [dB]	Bandwidth (3-dB gain)	PAE (peak), [%]	PAE over the band <sup>7</sup> , [%]	Area, [mm <sup>2</sup> ]	Technology
[102]	Triple-stacked FET differential stage	13.6	20–27.5 GHz 31%	10	19–43 GHz 77.5%	21.5	n/a	0.12 w/o pads	28nm bulk- CMOS
[103]	Single differential CE stage	16.7	26–39 GHz 40%	13	25.5–41 GHz 46%	11.2	$\geq 7$	1.83	0.13 $\mu$ m SiGe BiCMOS
[104]	Single cascode stage	15	25–30 GHz 18%	15.3	24.8–34 GHz 31%	15	$\geq 13.4$	0.24	0.25 $\mu$ m SiGe:C BiCMOS
[52]	Triple-stacked HBTs	20.9	26.5–40 GHz 40%	19	21.7–40 GHz 59%	23.5	$\geq 19.1$	1.63	0.13 $\mu$ m SiGe BiCMOS
This work	Single differential cascode stage	24.2	22–34.2 GHz 43% (measured from 25 GHz)	16.1	20.8–33 GHz 45%	29.8	$\geq 26$	0.72	0.25 $\mu$ m SiGe BiCMOS

<sup>7</sup> The PAE over the 1-dB  $P_{1dB}$  bandwidth



## 4.3 Combined Power Amplifier

### 4.3.1 Multiphysics Design Flow

Although the developed stand-alone PA-cell demonstrates the desired performance, which is overall in good agreement with simulations, the design of the combined Watt-level PA is not a straightforward combination of PA-cells and requires a dedicated optimization methodology. The latter is caused by the need to consider various critical multiphysics effects occurring in the joint structure. These effects are primarily related to:

- Mutual coupling between closely spaced PA-cells;
- DC routing lines and distributed ground topology;
- Crosstalk between parallel biasing circuits;
- Imperfect flip-chip interconnections;
- Presence of underfill and solder mask;
- Excessive heat generation from a relatively small die.

Ignoring the above effects in the design flow inhibits a proportional output power increase with the number of interfaced PA-cells and turns to an efficiency reduction. Moreover, strong mutual coupling between closely spaced PA-cells and parallel biasing circuits might cause positive feedback loops resulting in oscillations. Therefore, a holistic multiphysics design flow has been proposed to take these critical effects into account. Figure 4.18 presents a block diagram of the design flow, which consists of two design phases: *initial design phase*, where the PA-cell and power combiner are designed independently from one another, and *joint EM-circuit-thermal optimization*. In the initial design phase, the stand-alone PA-cell is optimized in such a way to realize the desired output power and efficiency over the wide frequency range; the power combiner is optimized to minimize insertion losses and active reflection coefficients of its input ports, assuming a uniform excitation scenario. The design and optimization of the PA-cell and spatial-power combiner are discussed in detail in Sections 4.2.2-4.2.3 and 2.3.2, respectively.

The PA-cell designed at the initial phase and the spatial power combiner are used as a starting point for the joint multiphysics optimization, as shown in Figure 4.18. It intends to achieve the stable operation and optimal system-level performance of the combined Watt-level PA in terms of PAE and output power over the wide frequency range while mitigating the thermal issues caused by a high power density in the relatively small chip. The joint optimization flow includes multiple steps performed in different software tools in the following order:



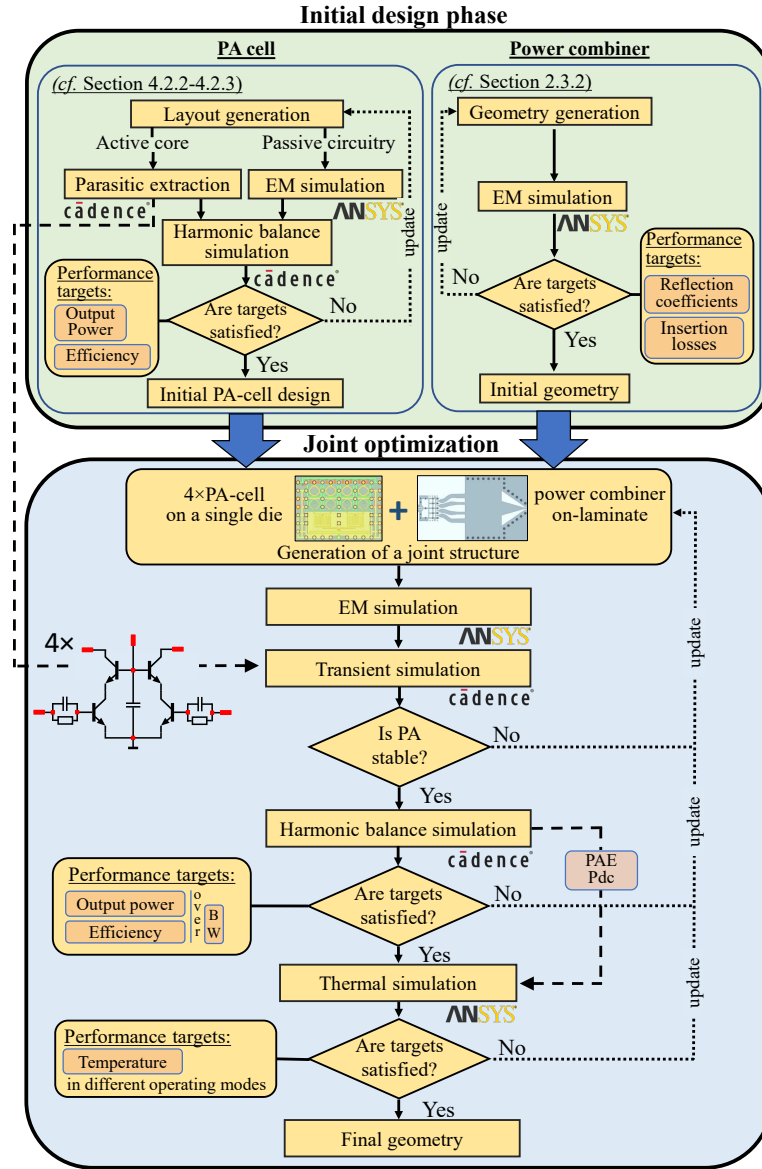


Figure 4.18: A multiphysics design flow for a mm-Wave SiGe spatial power-combined PA.

- Step 1.** Building a complete EM model of the combined PA passive circuitry and its simulation in Ansys HFSS;
- Step 2.** Evaluation of the achieved PA performance in conjunction with the extracted active circuitry in Cadence Virtuoso;
- Step 3.** Constructing the corresponding simplified thermal model of the joint structure and its simulation in Ansys Icepak and Ansys Fluid.

The consecutive design steps are discussed in detail in the following paragraphs.

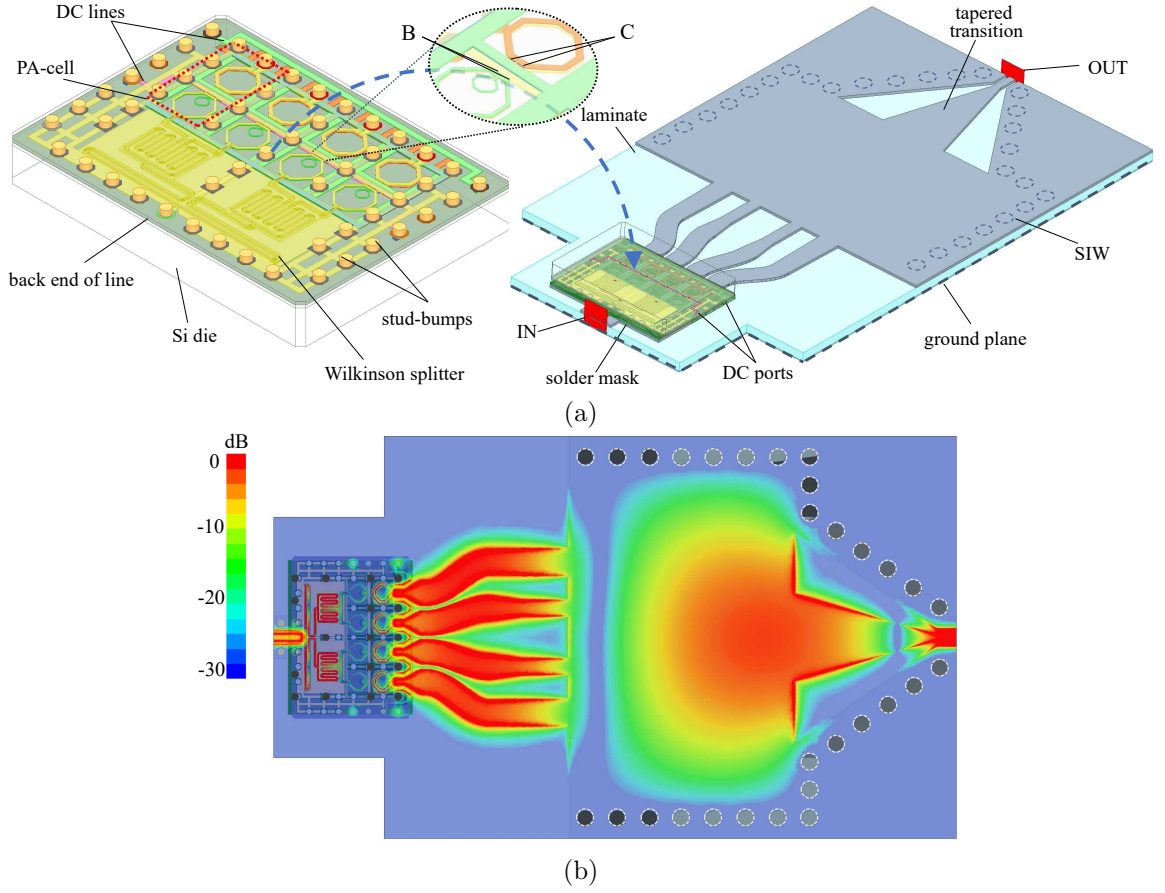


Figure 4.19: Simulation of the designed spatial power-combined PA containing  $4 \times$  PA-cells: (a) EM model of the die flip-chip interconnected to the combiner placed on the laminate; (b) Simulated magnitude of the real part of the E-field distribution at 35 GHz.

**Step 1.** The complete EM model of the combined PA is shown in Figure 4.19 (a). It consists of a silicon substrate with the actual back end of line (BEOL) topology interconnected to the laminate, where the ports for input and output interfaces are placed. The BEOL topology is formed by a 4-way TL-based Wilkinson power splitter with each output path followed by a PA-cell layout with five internal ports ( $B_p$ ,  $B_n$ ,  $C_p$ ,  $C_n$ ,  $V_{cas}$ ) for interconnecting the extracted differential active circuitry, as shown in Figure 4.2. To avoid potential asymmetries in the operation of parallel PA-cells caused by non-symmetric DC routing lines, each PA-cell is equipped with its own biasing circuit generating the required voltage locally. It allows to simplify the biasing network and mitigate potential asymmetries. The remaining feeding lines are included in the BEOL EM model. The ports for the external DC biasing ( $V_{main1,2}$ ,  $V_{cas1,2}$ ) are put on the laminate. The performance of the power splitter and PA-cells suited on the flip-chip die is affected by stud-bump interconnections as well as a lossy solder mask covering the laminate. Thus, the simulation model also includes the corresponding solder mask pattern and stud-bump interconnections. Figure 4.19 (b)

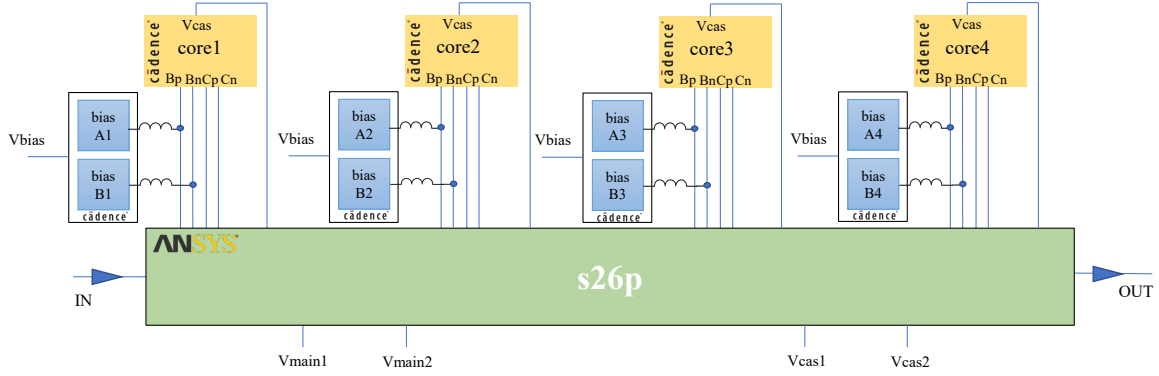


Figure 4.20: A circuit-level block diagram of the combined PA simulation test-bench.

shows the simulated magnitude of the E-field distribution of the combined PA at 35 GHz. It visualizes power splitting, parallel amplification, and spatial combing in SIW.

**Step 2.** A circuit-level block diagram of the simulation test-bench for the PA performance evaluation is shown in Figure 4.20. It consists of four identical RLC extracted circuits of the active core, derived in the initial designs phase, interconnecting with the complete EM model of the passive structure represented by a 26 ports S-matrix. The obtained at the previous step S-matrix characterizes the structure from DC up to the 6th-order harmonics. The above allows taking into account realistic losses in the DC biasing network by feeding supply voltages to parallel active circuitries through the simulated S-matrix. Such a multi-cell structure might suffer from oscillations caused by internal feedback loops. Therefore, time-domain simulations with a pulsed input signal have been used to examine circuit stability at internal nodes. The large-signal performance of the combined PA has been evaluated using a harmonic balance analysis. At this step, the PA geometry is numerically optimized to ensure circuit stability as well as to satisfy the main system-level performance goals.

**Step 3.** Despite the relatively high efficiency of the designed PA-cells (*cf.* Section 4.2.6), placing multiple parallel PA-cells in close proximity to each other on one die causes excessive heat generation resulting in a significant internal temperature increase. The latter might negatively affect device performance and reliability [126]. There are three main mechanisms of heat transfer: conduction, convection, and radiation. Due to its relatively small surface area, heat radiation is negligible for the present design. As a result, the following two paths contribute the most to heat dissipation:

- Convection from the surface of the chip to the air;
- Conduction through interconnecting stud-bumps to the laminate and then convection to the air.

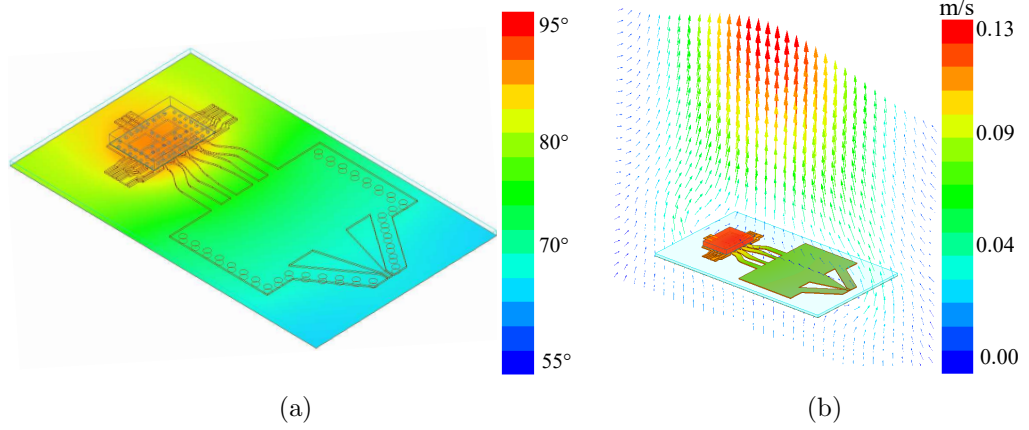


Figure 4.21: Thermal analysis in large-signal operation: (a) Surface temperature; (b) Air velocity corresponding to natural convection. The heat source power is 2.5 W; the ambient temperature is 25°C.

The performed thermal simulations show that the heat transfer path through stud-bumps is the most effective in the present design and accommodates more than 80% of total heat dissipation [127]. Consequently, it is essential to minimize thermal resistance between the die and laminate by placing a grid of stud bumps on the corresponding dummy ground pads all around the interior chip layout [128]. Furthermore, the laminate should be designed in such a way as to support efficient convection of heat from its top metal layer to the air. Figure 4.21 shows a simulation thermal model of the combined PA, where a point heat source is placed inside the silicon substrate. The power level of the heat source corresponds to the output power and efficiency values obtained in the previously performed harmonic balance analysis. The simulations have been performed in Ansys Icepak. The obtained steady-state surface temperature of the chip must be within the safe operation region under the condition of natural convection, as shown in Figure 4.21.

The above described iterative optimization flow of the chip topology and its corresponding footprint on the laminate continues until both the desired large signal performance and safe temperature regime are obtained. The found optimal pitch between adjacent PA-cells is 370  $\mu\text{m}$ , allowing one to put one row of grounded pads for stud-bumps between PA-cells and hence prevent undesired coupling effects while mitigating long DC routing lines. Moreover, a grid of ground stud-bumps has been placed all around the interior layout to realize proper galvanic and thermal connections between the chip and laminate. The pitch between adjacent stud-bumps is 180  $\mu\text{m}$ . The designed input power splitter is formed by CPW TLs with a signal path on the top metal (M6) and a patterned ground shield on the lower metal layer (M4). The use of thicker top metal layers reduces resistive losses and mitigates the effects of substrate parasitics. In spite of that, the performed EM simulations of the stand-alone splitter show high insertion losses reaching a  $-7.8$  dB level at 35 GHz. This

fact makes off-chip power combining solutions more preferable at these frequencies as they have intrinsically lower insertion losses (*cf.* Section 4.3.4).

### 4.3.2 Fabrication and Assembly Considerations

In contrast to conventional PA architectures with embedded power combiners, where the output reference plane is directly placed on-chip, implementing the proposed spatial power combined PA is more challenging since it requires multiple fabrication and assembly steps. Various imperfections occurring in fabrication and assembly processes might significantly degrade the PA performance as well as its reliability. Therefore, it is essential to choose proper fabrication technologies and materials, ensuring their minimal impact on the PA performance. This sub-section discusses several fabrication and assembly considerations mainly related to the test-board and flip-chip interconnections.

The developed test-board containing the SIW-based power combiner and its two back-to-back configurations is shown in Figure 4.22. The board contains four copies of each configuration, which are grouped in the corresponding reticles. Such an arrangement allows one to extend the surface area of each board and hence fix it properly on a vacuum chuck intended for relatively big wafers. Multiple reticles are required for checking the performance variation caused by fabrication and assembling uncertainties as well as for performing stress tests, where some active samples might be damaged. The designed configurations are intended to be tested directly on-laminate with the use of miniature contact probes. The latter simplifies a calibration procedure and makes the board more compact since bulky RF connectors, interconnecting lines, and transitions are not needed.

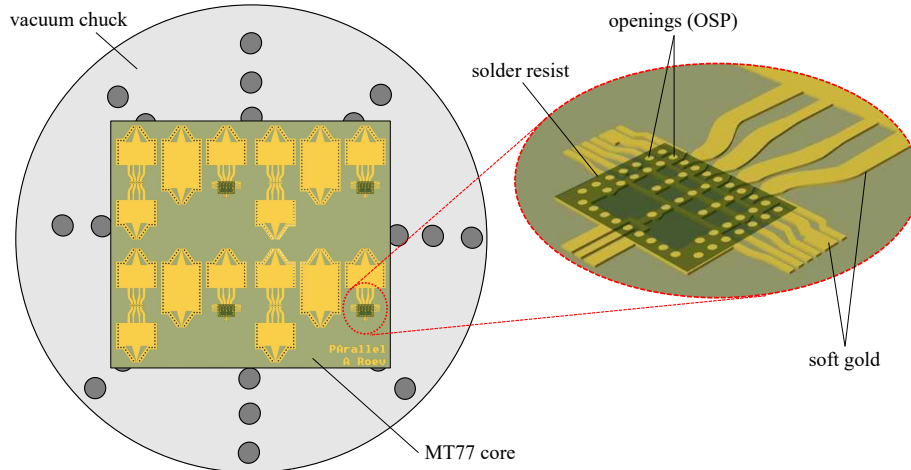


Figure 4.22: The designed test-board containing the SIW-based power combiner and its two back-to-back configurations arranged in four reticles.



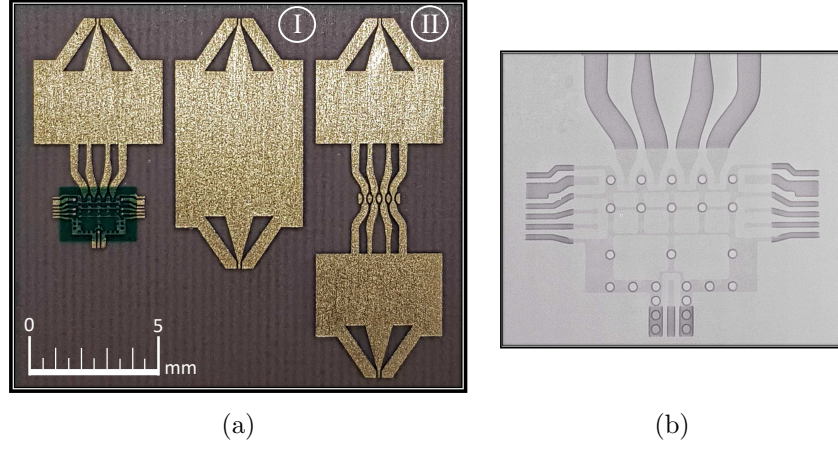


Figure 4.23: Fabricated board: (a) Layout of the designed power combiner including its two back-to-back configurations; (b) X-ray image of the board area corresponding to the chip footprint.

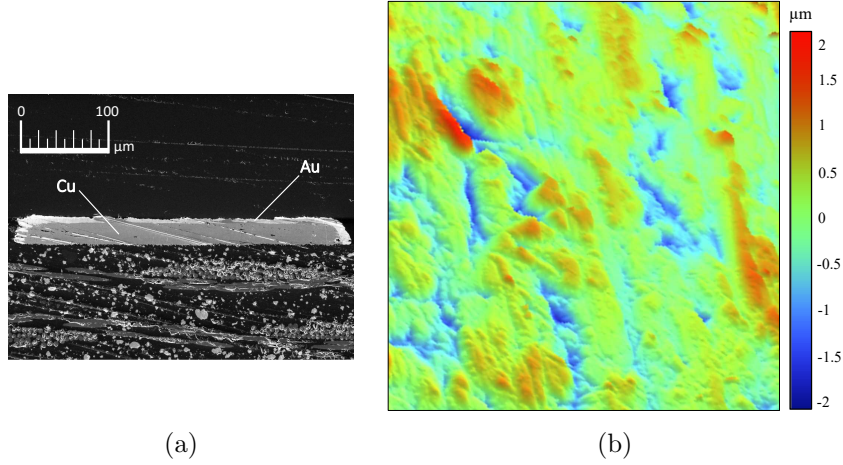


Figure 4.24: The results of scanning electron microscopy: (a) Cross-section of the fabricated board indicating the quality of the gold finishing on top of the copper trace; (b) Map of the surface roughness ( $100 \times 100 \mu\text{m}^2$  area).

The board has a hybrid multilayer stack-up, which consists of three copper-clad laminates. The top and bottom substrates are Astra MT77 laminates with a relatively low thickness of  $127 \mu\text{m}$ , whereas the middle core is FR4 with a thickness of  $300 \mu\text{m}$ , which intends to make the structure more rigid. Since the SIW-based power combiner is embedded into the top laminate, its performance strongly depends on the substrate material properties. Astra MT77 laminate is characterized up to  $100 \text{ GHz}$ , where it shows acceptable performance with  $\epsilon_r = 3.66$  and  $\tan\delta = 0.0015$  [129]. The laminate area corresponding to the die footprint is covered by a solder resist with a thickness of  $12 \mu\text{m}$ , as shown in Figure 4.22. It prevents forming of solder bridges between closely spaced pads as well as simplifies die-laminate alignment. The solder resist openings are  $100 \mu\text{m}$  in diameter and are covered by an organic solderability preservative

Table 4.3: Measured surface roughness statistic of the fabricated board

Parameter	Description	Value, [nm]
$R_a$	Average roughness	341
$R_q$	RMS roughness	435
$R_t$	Maximum peak-to-valley difference	2155
$R_p$	Maximum peak height	755
$R_v$	Maximum valley depth	1400

(OSP) surface finish, which protects the copper pads from oxidation [130]. In order to interconnect the top and bottom laminates to the middle core, FR4 prepreg with a thickness of 150  $\mu\text{m}$  is used.

Figure 4.23 (a) shows the photo of the fabricated reticle. The SIW-based power combiner and its two back-to-back configurations occupy an area of  $16 \times 16 \text{ mm}^2$ . Figure 4.23 (b) shows the x-ray image of the board area corresponding to the chip footprint. The image indicates a grid configuration of the distributed ground on the top metal layer covered by the solder resist and positions of blind metalized vias. The vias must realize efficient RF and thermal connections between the chip and laminate ground planes.

The chosen way of on-laminate probing demands specific mechanical properties of a surface finish, which is deposited on the corresponding contact pads. In order to achieve a reliable electrical contact between the laminate and probe's tips as well as to avoid their mechanical breaking due to the excessive surface hardness, the Cu pads are covered by a thick layer of pure soft Au. The latter also eliminates the need for a lossy intermediate Ni layer, which intends to prevent metal migration when the Au layer is too thin [131]. The fabricated board cross-section indicating the metal content of the top traces is shown in Figure 4.24 (a). The image is a result of the performed scanning electron microscopy [132]. It allows evaluating the thickness of Au and Cu layers, which are in order of 6  $\mu\text{m}$  and 23  $\mu\text{m}$ , respectively.

The deposition of such a thick Au layer is accompanied by many technological challenges resulting in higher average surface roughness, which significantly impacts losses at mm-Wave frequencies [Paper G]. The measured surface roughness map of the board top metal layer covered by Au is shown in Figure 4.24 (b). The measured statistic parameters of the surface roughness calculated over the area of  $100 \times 100 \mu\text{m}^2$  are summarized in Table 4.3. Despite the moderate root-mean-square (RMS) roughness of 435 nm, the maximum peak height and valley depth reaches a 1  $\mu\text{m}$  level, which exceeds skin depth at Ka-band. To take into account the realistic surface roughness in EM simulations, the measured parameters are used to make a more accurate equivalent surface model in Ansys HFSS [133].

The flip-chip interconnection between the die and laminate is realized using an Au stud bumping process [134,135]. It allows one to realize the desired 180  $\mu\text{m}$  pitch

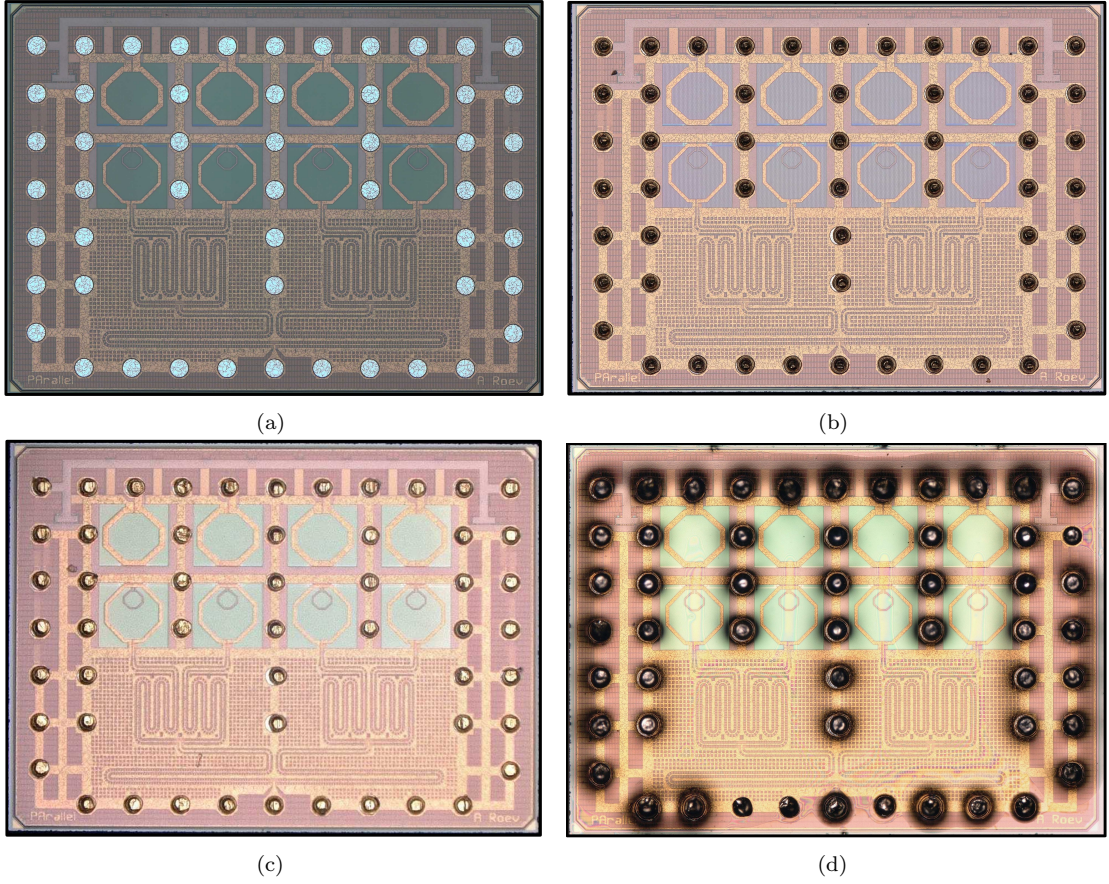


Figure 4.25: Photos illustrating preparation flow of the die for flip-chip interconnection: (a) Wafer dicing; (b) Bumps bonding; (c) Bumps planarizing; (d) Solder jetting.

between adjacent interconnections while offers low parasitic inductance [136]. In contrast to a solder bumps process, Au stud bumping does not require specific under bump metallization, which is needed to connect solder bumps to bond pads and avoid diffusion of metals into the die. Moreover, Au stud bumps allow the enforcement of heat transfer from the die into the laminate since their thermal resistance is  $5\times$  lower compared to SAC305 solder bumps.

Due to the relatively small amount of samples, stud bumping is performed on a single-chip level, as shown in Figure 4.25. The Au stud bumping process starts as a conventional wire bonding process from ball bonding. However, instead of forming a traditional wire-bond loop, the wire is cut just above the ball to keep a bump on the die pad, as shown in Figure 4.25 (b). The height of obtained bumps might vary a lot, which causes open circuits as well as non-balanced mechanical stress leading to the die fractures [137]. Therefore, at the next step, the bumps are planarized to make their height consistent (See Figure 4.25 (c)). The last step is solder jetting on top of the planarized stud bumps, as shown in Figure 4.25 (d). The height of stud bumps is  $32\text{ }\mu\text{m}$  while their diameter is  $65\text{ }\mu\text{m}$ . Once the die is completely bumped,



it is flipped and attached to the substrate by a reflow process. The die alignment to the corresponding solder mask openings on the laminate is performed using x-ray imaging. To ensure a good mechanical connection and minimize the stresses occurring due to differences in thermal expansion of the die and laminate, the gap between the flipped die and laminate is usually filled by underfilling compounds. However, this step is not essential for the present design due to the sufficient amount of closely-spaced stud bumps and therefore is omitted.

### 4.3.3 Experimental Setup

Although the combined PA has the same performance metrics as the previously tested PA-cell, the measurement setup required for its testing has significant differences. The latter results from the need to eliminate various thermal effects occurring in the closely spaced parallel PA-cells in the large-signal regime. Moreover, on-laminate measurements require the use of different probes and calibration substrates.

Small-signal measurements of the combined PA and the corresponding passive back-to-back configurations are directly performed using a 67 GHz Keysight PNA-X VNA in conjunction with 200  $\mu\text{m}$  pitch GSG RF probes suitable for landing on laminate. In order to de-embed effects of the probes from measurement results, a SOLT calibration substrate is used. The biasing voltages required for the combined PA are applied through two 125  $\mu\text{m}$  pitch Eye-Pass DC probes, each of which has four power tips. External biasing from both sides allows keeping on-chip DC routing lines symmetric as well as reducing the effect of their electrical resistance.

In contrast to a single PA-cell, whose large-signal measurements have been performed in continuous wave (CW) mode, large-signal performance evaluation of the combined PA requires a more sophisticated approach. Since the combined PA chip has four parallel PA-cells placed in close proximity to each other, their operation in CW mode at large power levels might lead to excessive heat generation, which causes a significant temperature increase. The latter renders measured data worthless because of the temperature-dependent behavior of semiconductor devices, which results in reducing their effective  $f_t/f_{\text{max}}$  and output power due to the decreased carrier velocity [138, 139]. To eliminate these undesired thermal effects, the large-signal performance of the combined PA is measured in a pulsed regime [140]. Figure 4.26 shows a block diagram of the pulsed mode test bench. Pulse modulation is performed using a programmable digital signal generator Keysight E8257D supporting custom envelope waveforms. In the present case, the sequence of rectangular pulses of the fixed width,  $\tau_p$ , and repetition frequency,  $F_p$ , is used as an envelope signal. By using an appropriate duty cycle,  $\tau_p \cdot F_p$ , the average power can be reduced significantly while maintaining high peak power [141]. Operation at lower average power levels allows one to reduce heat generation and hence minimize thermal effects. Assuming the ideal pulse-modulated signal, the PA peak output power can be expressed as:

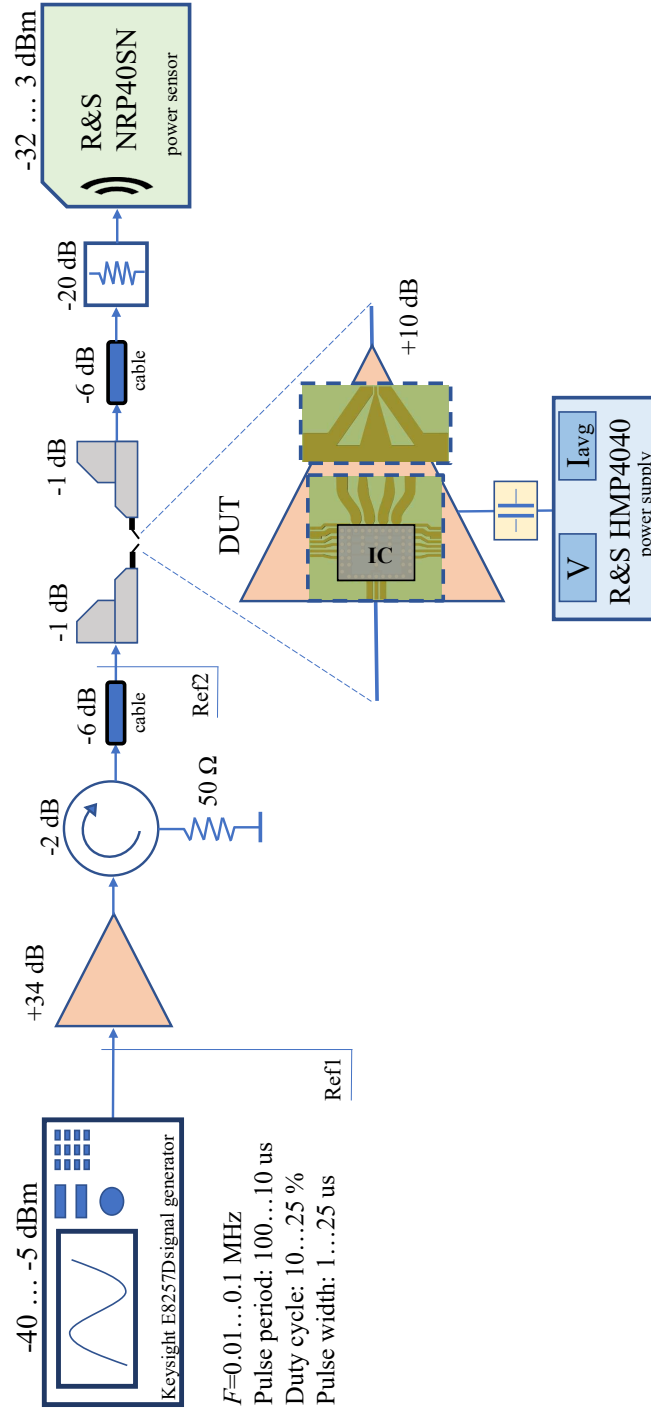


Figure 4.26: Block diagram of the pulsed mode test bench indicating the gain of each block. Pulse modulation is performed using a programmable digital signal generator supporting custom envelope waveforms. Average RF output power and DC power consumptions are measured.



Figure 4.27: Photo of the measurement setup. The measurements are carried out using a Cascade Microtech mechanical probe station with four manipulators.

$$P_{\text{peak}} = \frac{P_{\text{avg}}}{\tau_p \cdot F_p}, \quad (4.2)$$

where  $P_{\text{avg}}$  is the measured average output power. In order to evaluate the efficiency of the PA, its peak DC biasing current,  $I_{\text{peak}}$ , could be evaluated from the corresponding measured average current,  $I_{\text{avg}}$ :

$$I_{\text{peak}} = \frac{I_{\text{avg}} - I_0}{\tau_p \cdot F_p} + I_0, \quad (4.3)$$

where  $I_0$  is the measured quiescent biasing current. The chosen pulse duty cycle should be sufficiently low to avoid device self-heating effects. At the same time,  $\tau_p$  should be large enough to achieve steady-state operating conditions [142]. By balancing these guidelines, acceptable ranges of pulse duration and duty cycle are found to be 1–25  $\mu\text{S}$  and 10–25 %, respectively.

To drive the DUT with high power, a preamplifier followed by an isolator is employed, as shown in Figure 4.26. The isolator ensures that possible reflections from the DUT input port do not affect the preamplifier performance, which is taken into account during the initial calibration. Figure 4.26 shows the positions of two calibration reference planes, where actual input power levels are checked. The latter is needed for calculation of the PA large-signal gain. To evaluate the efficiency of the PA,  $I_{\text{avg}}$  is measured by a DC power supply with a remote interface. The PA output power is measured by a three-path diode power sensor R&S NRP40SN, which is placed on the same movable manipulator as the output RF probe (See Figure 4.27). The latter allows one to avoid measurement uncertainties caused by bending of interconnecting coaxial cables. The expected measurement uncertainty does not exceed 0.3 dB and 2% for output power and efficiency, respectively. The setup is equipped with a discrete attenuator to remain the measuring output signal within the power sensor dynamic range.

#### 4.3.4 Performance Evaluation

This sub-section presents the overall performance of the designed Watt-level spatial power-combined PA with a particular focus on the following metrics: small-signal forward gain, saturated output power, and PAE over the operating frequency band. The measured performance is compared with the corresponding simulations of the complete PA model described in Section 4.3.1. Moreover, to evaluate the relative output power increase and possible PAE degradation after combining four PA-cells, the measured individual PA-cell performance is indicated as a reference.

Prior to performing the combined PA tests, it is necessary to evaluate the performance of the on-laminate power combiner in its two back-to-back configurations: the complete back-to-back configuration (II) and the configuration excluding the arrangements of four MLs (I), as shown in Figure 4.23 (a). These initial tests allow one

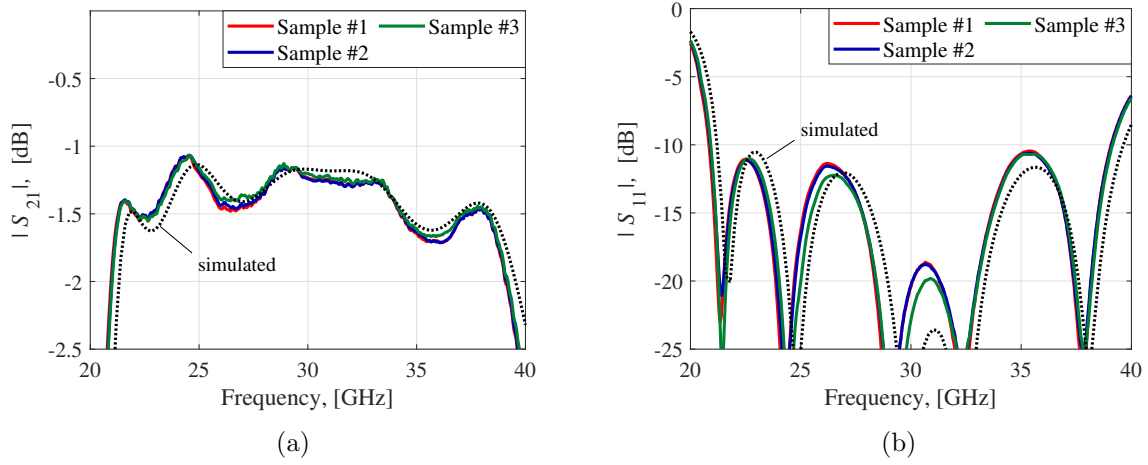


Figure 4.28: The measured and simulated (a)  $|S_{21}|$  and (b)  $|S_{11}|$  of the complete power combiner in a back-to-back configuration (II). The set of curves shows the spread between different samples.

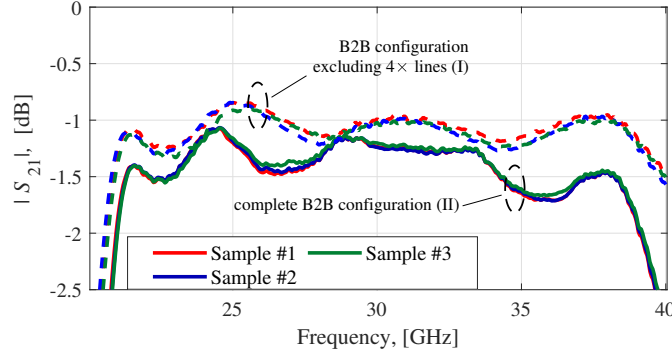


Figure 4.29: Comparison between the measured  $|S_{21}|$  of different back-to-back configurations, as shown in Fig. 4.23 (a). The set of curves shows the spread between the different samples.

to verify that the board manufacture has been done properly as well as to characterize losses in the power combiner and hence to predict the combined PA output power. The measured and simulated reflection coefficient,  $|S_{11}|$ , and transmission coefficient,  $|S_{12}|$ , of the power combiner in the complete back-to-back configuration (II) are shown in Figure 4.28 (a) and (b), respectively. The set of curves corresponds to different fabricated samples. The measured  $|S_{11}|$  does not exceed  $-10$  dB over the frequency range of  $22.5 - 38.5$  GHz. The obtained  $|S_{12}|$  reaches  $-1.2$  dB at  $28$  GHz and remains  $\geq -1.7$  dB over the  $22 - 38$  GHz frequency range. Therefore, the expected power reduction due to the combiner insertion losses is  $0.6$  dB in the middle of the operation band. All tested samples demonstrate a similar performance, which confirms the low sensitivity of the design to fabrication uncertainties. The measured results are in good agreement with simulations (shown by dashed lines), which verifies the correctness of the built EM model accounting for the impact of the realistic surface roughness on insertion losses. The latter is essential for the present

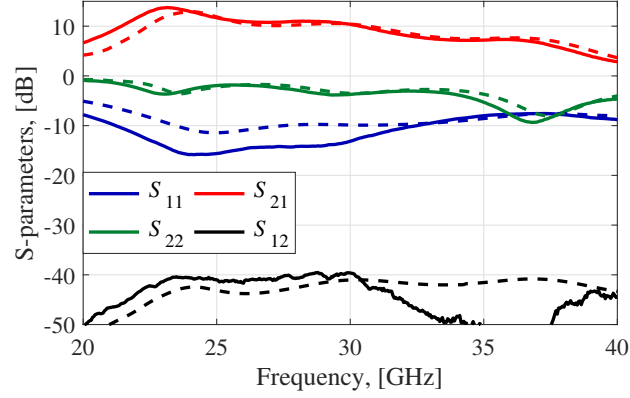


Figure 4.30: Simulated (dashed) and measured (solid) small-signal performance of the designed spatial power-combined PA. The results correspond to the sample with the highest measured gain.

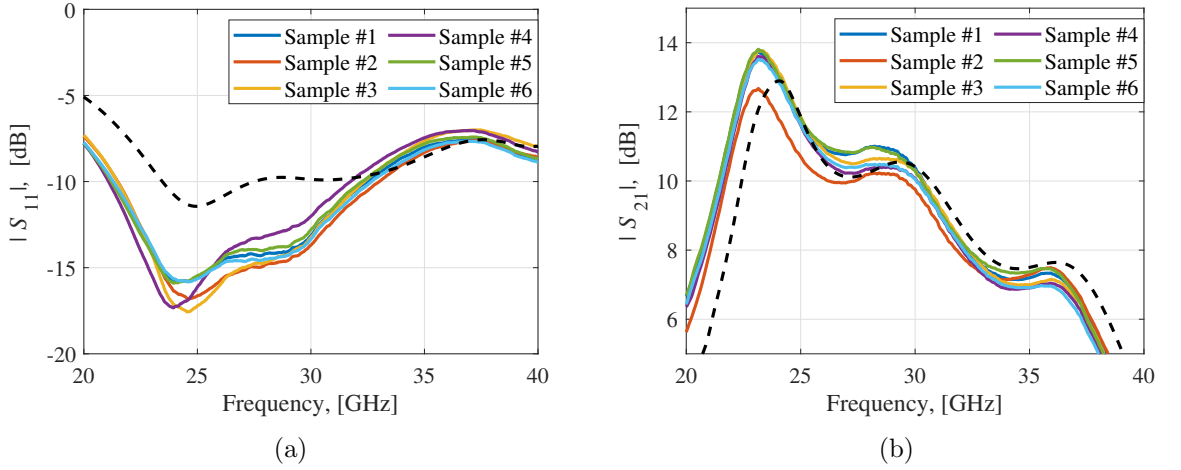


Figure 4.31: The measured (a) forward power gain,  $|S_{21}|$  and (b) input port reflection coefficient,  $|S_{11}|$ , of the spatial power-combined PA. The set of curves corresponds to different samples. The simulations are shown by the black dashed line.

design since, as shown in [Paper G], insertion losses are mainly caused by the realistic surface roughness, which becomes comparable with skin-depth at Ka-band. The measured  $|S_{12}|$  of the complete back-to-back configuration (II) and the configuration excluding the arrangements of four MLs (I) are shown in Figure 4.29 by dashed and solid lines, respectively. As one can see, the relative difference between the  $|S_{12}|$  of corresponding configurations does not exceed 0.5 dB. Thus, a single arrangement of four MLs has only 0.25 dB insertion losses. The remaining losses in the combiner are attributed to the SIW with tapered ML transition, which is required for test purposes only and in the future will be replaced by an antenna element. Figure 4.30 shows the small-signal performance of the combined PA<sup>7</sup> over the 20 – 40 GHz frequency

<sup>7</sup>Sample with the highest measured gain

range. The forward power gain,  $|S_{21}|$ , reaches 13.8 dB at 23.2 GHz and remains above 10.8 dB over the 21.7 – 29.5 GHz frequency range, resulting in 3-dB gain bandwidth of 30%. The input reflection coefficient,  $|S_{11}|$ , does not exceed  $-10$  dB over the 21.2 – 32.6 GHz range, resulting in 42% fractional bandwidth. The measured reverse isolation,  $|S_{12}|$ , does not exceed  $-38$  dB, which implies the circuit stability. Although the measured low-signal curves exhibit similar behavior to the corresponding simulations, the minimum of  $|S_{11}|$  and hence the maximum peak gain are shifted towards the lower frequencies. This is primary caused by inaccurate modeling of the solder mask effects on the input power splitter. Figure 4.31 (a) and (b) show the spread in low-signal performance of different tested samples in terms of their  $|S_{11}|$  and  $|S_{21}|$ , respectively. As one can see, for most of the samples, the curves are close to each other and demonstrate the relative spread comparable to one of the individual PA-cells (*cf.* Section 4.2). However, sample #2 exhibits a 1 dB lower gain over the range of 22 – 26 GHz compared to the rest of the tested samples, which is believed caused

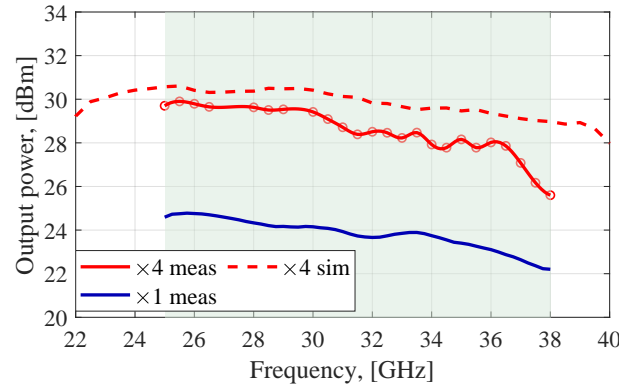


Figure 4.32: Comparison between the measured (solid red line) and simulated (dashed red line) saturated output power levels of the combined PA. The blue line shows the measured saturated output power of the PA-cell.

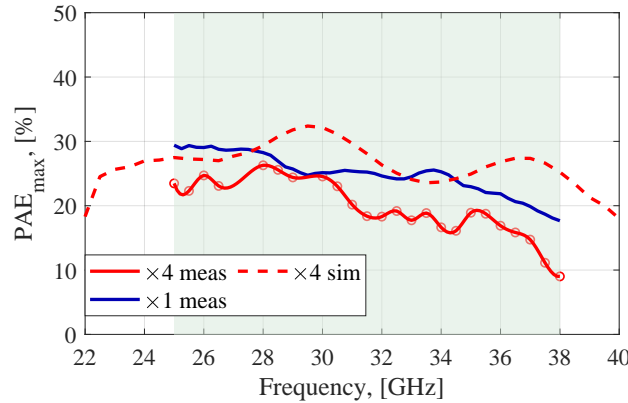


Figure 4.33: The measured (solid red line) and simulated (dashed red line) maximum peak PAE of the combined PA. The blue line shows the corresponding results of the PA-cell.

by assembly imperfections. In the present design, the effects of assembly imperfections are dominating over wafer-to-wafer process variation. Therefore, the further reported large-signal performance of the combined PA corresponds to the sample with the highest measured small-signal forward gain.

Figure 4.32 shows the measured (solid) and simulated (dashed) saturated output power of the combined PA under the default biasing voltages (*cf.* Section 4.2.2). The measured saturated output power of the PA-cell is shown by the blue line as the reference. The measured saturated output power reaches 30.0 dBm level at 25.5 GHz and remains above 29 dBm over the 23.0 GHz to 31.1 GHz frequency range, resulting in 29.9% 1-dB fractional bandwidth. As one can see, the obtained average relative power increase with respect to the PA-cell is around 4.5 dB, which is 1.5 dB lower compared to an ideal 4-way combining. This difference is caused by the losses in the combiner itself and in chip-laminate interconnections, which are 0.8 dB and 0.7 dB,

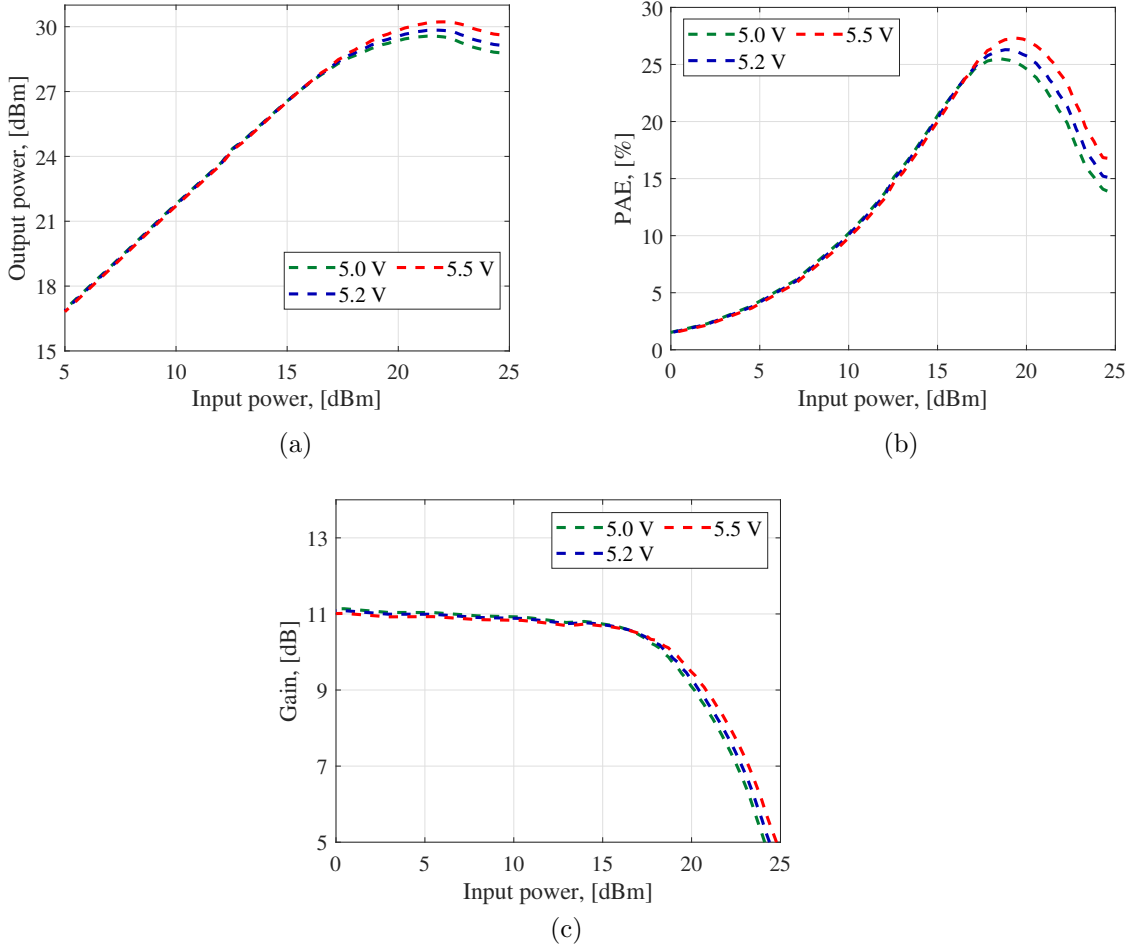


Figure 4.34: The measured (a) output power, (b) maximum peak PAE, (c) forward power gain of the combined PA versus input power at 28 GHz. The set of curves corresponds to different values of  $V_{\text{main}}$ .



respectively. The measured (solid) and simulated (dashed) PAE of the combined PA are shown in Figure 4.33. The measured peak PAE remains above 19% over the entire 1-dB power bandwidth and reaches the maximum value of 26.0% at 28.0 GHz. Compared to the individual PA-cell, the obtained PAE values are lower, which is caused by the above-mentioned losses in the combiner and interconnections leading to PAE reduction. The differences between the measurements and simulations are similar to the ones of the PA-cell and mainly attributed to the limited accuracy of the Si substrate EM model and complex distributed effects in the relatively large devices.

Although the PA-cell has been originally optimized assuming the fixed collector voltage,  $V_{\text{main}} = 5 \text{ V}$ , its active circuitry can still operate within the stable-operating-area (SOA) at higher values of  $V_{\text{main}}$ . The SOA of the individual devices is defined as an area in the voltage-current plane bounded by operation points at which electro-thermal instability occurs, leading to the device self-damage [143, 144].

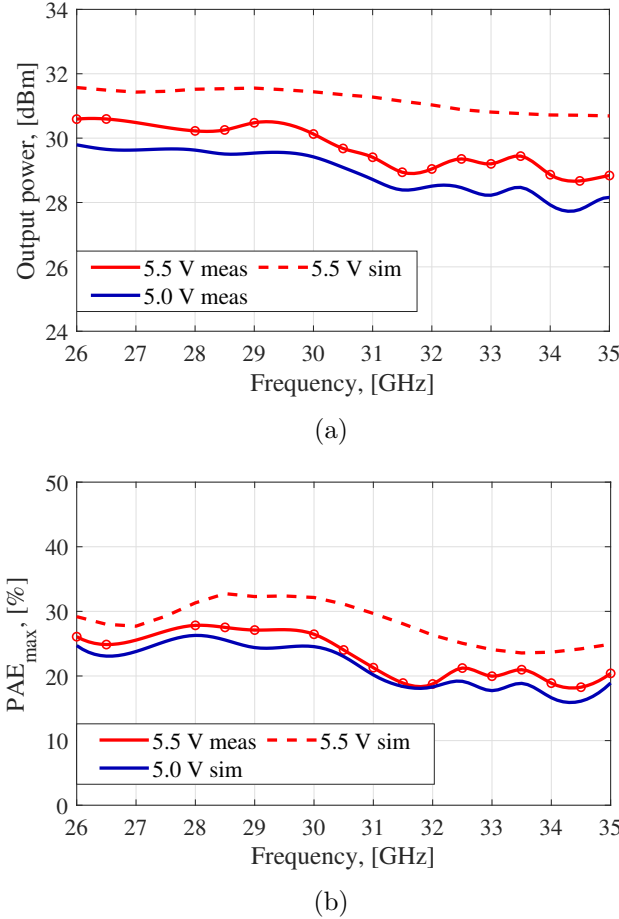


Figure 4.35: Comparison between the measured (a) saturated output power levels and (b) maximum peak PAE of the combined PA under different values of  $V_{\text{main}}$ . The corresponding simulation results are shown by the dashed line.

Based on the performed large-signal simulations, the operation point corresponding to  $V_{\text{main}} = 5.5$  V is still within the SOA. However, the further increase of  $V_{\text{main}}$  leads to electro-thermal breakdown of the CB device. Figure 4.34 exemplifies the effect of the increased collector voltage on the output power, PAE, and forward gain of the combined PA. These results are obtained from the performed input power sweeps at 28 GHz. As one can see, increasing  $V_{\text{main}}$  allows achieving higher output power, whereas the low-signal gain does not change. Thus, the higher input power is required to drive the PA into its compression, and as a consequence, the PAE maximum is shifted (See Figure 4.34 (b)). The measured gain of the combined PA has negligible variation over the different input power levels in the region before saturation, which confirms its inherent linearity.

The measured saturated output power and maximum peak PAE of the combined PA for the default (5.0 V) and the increased (5.5 V) values of  $V_{\text{main}}$  are shown in Figure 4.35 (a) and (b), respectively. As expected, for both cases the saturated output power and maximum peak PAE exhibit similar behavior over the frequency. However, the increase of  $V_{\text{main}}$  allows one to reach 0.8 dB higher power levels on average. The latter results from the corresponding increase of voltage swing across the CB devices. Since the increase of  $V_{\text{main}}$  also leads to higher DC power consumption, the obtained levels of peak PAE are similar for both cases.

## 4.4 Summary

The performance of the developed Watt-level PA and its individual PA-cell is summarized and compared with published state-of-the-art Si-based Ka/V-band PAs with a saturated output power of 23 dBm and larger [49, 61, 105, 145–149], as shown in Table 4.4. The key performance metrics are the saturated output power and its 1-dB bandwidth as well as maximum peak PAE and minimum peak PAE over the entire 1-dB power bandwidth.

As one can see, due to the relatively low breakdown voltage of silicon devices, the reported high-power PAs are based on combining signals from multiple smaller PA-cells. Although PAs working in switching modes, such as Class-E [148], have inherently high efficiency resulting from appropriate shaping of collector/drain voltage and current waveforms, most of the reported PA-cells operate in Class-AB. The latter results from better linearity of Class-AB PAs supporting complex modulation schemes without the need for major digital pre-distortion. However, Class-AB operation implies the fundamental limitation on the peak efficiency, which in practice is even more reduced due to various parasitic effects in large distributed devices as well as losses in output matching circuits and power combiners. In the present design, at the individual PA-cell level, these problems have been overcome by the carefully designed and optimized layout of the cascode configuration and low-loss baluns (See Section 4.2). As a result, the developed PA-cell has a wideband performance (38.6%)

Table 4.4: Performance comparison with state-of-the-art Ka/V-band Si-based PAs

Ref.	PA-cell architecture	Class	Combiner type	Output	P <sub>sat</sub>		P <sub>1dB</sub>		PAE	PAE@P <sub>1dB</sub>	Gain		Tech.	
					peak, dBm	1-dB BW	peak, dBm	1-dB BW			peak, %	over BW		peak, dB
Chappidi [146]	double-stacked with pre-driver	DPA	2-way non-isolated asymmetrical	50-Ω	23.7	30.0-50.0 GHz	-	-	28.0	>21	-	23.4	36.2-48.7 GHz	0.13um SiGe BiCMOS
Sarkar [145]	diff. cascode stage with pre-driver	AB	2-way on-chip T-combiner	50-Ω	23.8	-	23.2	27.0-31.0 GHz	32.7	-	>29	29.9	27.0-35.0 GHz	TowerJazz 0.18um SiGe BiCMOS
This work PA-cell	single diff. cascode stage	AB	NaN	50-Ω on chip SE	24.9	23.0-34.0 GHz	24.2	22.6-34.2 GHz	30.0	>24	>23	16.1	20.8-33.0 GHz	NXP 0.25um SiGe BiCMOS
Huang [147]	diff. cascode stage	A	2-way on-chip current combiner	50-Ω	26.0	22.0-30.0 GHz	23.2	21.0-28.9 GHz	34.0	>26	-	16.3	21.1-31.5 GHz	90nm CMOS
Wang [61]	diff. Doherty with pre-driver	AB + C	4-way on-chip DAT	50-Ω	28.3	23.0-31.0 GHz	26.8	-	30.4	>30	-	20.5	22.0-28.5 GHz	0.13um SiGe BiCMOS
Welp 5.0 V [49]	diff. cascode stage with pre-driver	AB	4-way on-chip Wilkinson	50-Ω	28.7	20.5-27.2 GHz	-	-	21.9	>15	-	16.1	-	Infineon 0.35um SiGe BiCMOS

Table 4.4: Performance comparison with state-of-the-art Ka/V-band Si-based PAs (*continued*)

Ref.	PA-cell architecture	Cla ss	Combiner type	Output	P <sub>sat</sub>		P1dB	PAE		PAE@P1dB	Gain		Tech.
				peak, dBm	1-dB BW	peak, dBm	1-dB BW	peak, %	over BW	peak, %	peak, dB	3-dB BW	
Datta [148]	double-stacked with pre-driver	E	8-way on-chip: current + slow wave combiner	50-Ω SE on chip	28.9	45.0-47.0 GHz 4.3%	-	25.0	>23	-	13.0	45.0-47.0 GHz 4.3%	0.13μm SiGe BiCMOS
Essing 5.5 V [105]	single cascode stage with pre-driver	AB	8-way on-chip current combiner	50-Ω SE on chip	29.1	25.5-30.0 GHz 16.2%	-	10.3	>8.5	-	20.2	26.5-30.3 GHz 13.3%	NXP 0.25μm SiGe BiCMOS
Nguyen 2.0 V [149]	diff. cascode stage with pre-driver	-	24-way DAT combiner	50-Ω diff. on chip	29.1	55.0-64.0 GHz 15.1%	-	18.4	>14	-	25.0	53.0-65.0 GHz 20.3%	45nm CMOS
Welp 5.8 V [49]	diff. cascode stage with pre-driver	AB	4-way on-chip lumped Wilkinson	50-Ω diff. on chip	30.8	19.5-27.0 GHz 32.2%	-	17.6	>13	-	16.1	-	Infineon 0.35μm SiGe BiCMOS
This work 5.0 V	single diff. cascode stage	AB	4-way spatial power combiner	50-Ω SE on laminate	30.0	23.0-31.1 GHz 29.9%	22.9-33.0 GHz 36.1%	26.0	>19	24.3	13.8	21.7-29.5 GHz 30.4%	NXP 0.25μm SiGe BiCMOS
This work 5.5 V	single diff. cascode stage	AB	4-way spatial power combiner	50-Ω SE on laminate	30.8	23.0-31.0 GHz 29.6%	23.0-33.0 GHz 35.7%	26.7	>20	25.1	13.9	21.6-29.5 GHz 30.9%	NXP 0.25μm SiGe BiCMOS

<sup>1</sup> Estimated from the reported table.

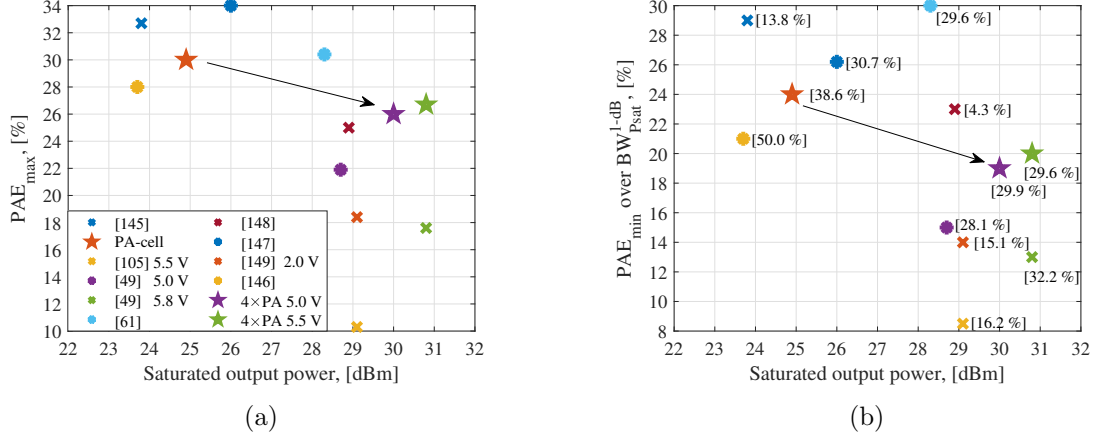


Figure 4.36: Performance comparison with state-of-the-art SiGe PAs at Ka/V-band: (a) Maximum peak PAE versus saturated power; (b) Minimum peak PAE over the entire 1-dB power bandwidth versus saturated power. The corresponding values of 1-dB power bandwidth are indicating in the squared brackets.

with both high PAE (30%) and high output power (24.9 dBm), which is the highest reported output power level obtained without the use of circuit-level power combining in Si-based technologies at Ka-band. Therefore, the developed PA-cell fulfills all the initial requirements to be a building block of the combined Watt-level PA (*cf.* Section 4.1).

In contrast to the previous designs where various on-chip power combining solutions are employed, in the present work, the array parallel PA-cells is interfaced to the low-loss spatial power combiner placed on the laminate. Thus, the presented performance metrics of the combined PA correspond to the output reference plane located on the laminate and hence include the effect of interconnection losses between the chip and laminate (0.5 – 0.8 dB). The latter is opposed to the previous works reporting the results of on-wafer measurements only, which ignore potential interconnection losses.

The combined PA, including four PA-cells, achieves the peak PAE of 26.7% in combination with 30.8 dBm maximum saturated output power, which is the highest achievable output power in practical applications, where the 50- $\Omega$  load is placed on a laminate. The high efficiency ( $\geq 20\%$ ) and output power ( $\geq 29.8$  dBm) over a wide frequency range (30%) exceed the state-of-the-art in Si-based PAs to the best of the author's knowledge. The achieved excellent performance of the combined PA is made possible by the proposed architecture with low-loss (0.6 dB) and wideband (54%) parallel spatial power combiner.

Figure 4.36 illustrates key performance metrics of the different Si-based PA realizations of Table 4.4. As one can see, combining four PA-cells results in a 5.1-dB maximum boost in output power with only 5% point degradation in PAE compared to a stand-alone PA-cell. Such an almost linear power scaling with low PAE re-

duction has been achieved using the proposed dedicated optimization flow, which considers various critical multiphysics effects occurring in the joint structure (See Sub-section 4.3.1). The joint EM-circuit-thermal optimization included in the design flow takes into account the effects of mutual coupling between closely spaced PA-cells, distributed DC feeding lines, and interconnections to laminate. Moreover, the used multi-physics approach allows mitigating the thermal issues caused by a high power density in a relatively small chip. Ignoring the above effects in the design flow leads to inaccurate modeling and suboptimal system-level performance. The demonstrated good agreement between simulations and measurements ( $\Delta P_{\text{sat}} = 0.8$  dBm,  $\Delta \text{PAE} = 5\%$ ) confirms the high simulation accuracy of the developed PA model.



## Conclusions

### 5.1 Summary and Achievements

In this work new power combining and integration solutions for efficient Watt-level mm-Wave transmitters in Si-based technologies have been developed and experimentally demonstrated. The main goal was to maximize output power and energy efficiency in combination with a wide operation bandwidth while maintaining a compact size for potential applications in dense antenna arrays with electrically small inter-element distances.

For this purpose, several novel contributions have been made that are summarized below according to the established specific objectives (*cf.* Section 1.2).

**Contribution area 1.** A novel power-combining architecture, where an array of parallel custom PA-cells suited on the same chip is interfaced with a single SIW placed on a laminate, has been developed. This allows one to directly excite SIW modes with high power through spatial power combining functionality, obviating the need for potentially lossy on-chip power combiners, which dramatically reduce efficiency and limit operation bandwidth. Moreover, it has simultaneously wide impedance bandwidth (50%) and low insertion losses (0.4 dB) while offering a compact planar form factor.

- The scalability of the proposed architecture in terms of the number of interfaced PA-cells has been investigated with the help of an approximate impedance matching model. The results obtained in Chapter 2 show that employing an appropriate substrate allows to interface up to 30 PA-cells with  $50\text{-}\Omega$  optimal load impedance into a single-mode SIW at Ka-band. Since the insertion losses in parallel power combining are virtually independent of the number of interfaced PA-cells, the proportional power increase is achieved. Therefore, the proposed architecture is a key enabler for high-power PAs at mm-Wave frequencies.



- An essential factor that has been addressed in the combined PA design procedure is mutual coupling effects between parallel PA-cells, which might be reduced by employing on-chip isolation load resistors. The performed study shows that using isolation resistors makes the proposed power-combining solution comparable with the classical Wilkinson power combiner in terms of sensitivity to non-uniform excitations.
- The proposed concept has been validated in the presence of critical effects of coupled PAs and in combination with a realistic antenna element. To do that, a 4:1 power combining module with a standard WR-28 output interface has been designed. The active performance of the module has been tested in combination with a commercial multichannel transmitter. The developed power-combining module facilitates efficient mm-Wave power generation over a 42% bandwidth (24.5 – 37.8 GHz) with the measured total power losses less than 0.7 dB. The PA-cell requirements in such a quad-channel transmitter configuration in terms of the difference between the PA-cell gains have been found within  $\pm 15^\circ$  and  $\pm 1$  dB for  $\leq 1$  dB power loss. The results of over-the-air tests presented in Chapter 3 confirm that the multi-port excitation has a negligible effect on the fed antenna pattern.

**Contribution area 2.** The developed PA architecture has been demonstrated through an example of the combined Watt-level PA containing four custom PA-cells implemented in 0.25  $\mu\text{m}$  SiGe:C BiCMOS technology. It achieves the peak PAE of 26.7% in combination with 30.8 dBm maximum saturated output power, which is the highest achievable output power in practical applications, where the 50- $\Omega$  load is placed on a laminate. The achieved excellent performance of the combined PA is made possible by the proposed architecture and more holistic multiphysics design flow.

- The custom PA-cell based on a differential cascode configuration operating in Class-AB has been developed. It allows achieving both high gain and wide operation bandwidth by eliminating the Miller effect. The PA-cell design and optimization aspects are described in detail in Chapter 4 with special attention to the compensation of active circuitry parasitics and EM modeling of passive components. The developed stand-alone PA-cell has a wideband performance (38.6%) with both high PAE (30%) and high saturated output power (24.9 dBm), which is the highest reported output power level obtained without the use of circuit-level power combining in Si-based technologies at Ka-band. The high output power and efficiency result from the differential configuration with minimized parasitic effects of multiple interconnected devices and the carefully designed output balun, which converts differential signals to single-ended and performs impedance matching while providing low insertion losses.

- Various critical multiphysics effects occurring in the joint structure have been taken into account using the proposed multiphysics design flow, including joint EM-circuit-thermal optimization. It allows achieving the optimal system-level large-signal performance of the combined PA while mitigating the thermal issues caused by a high power density in a relatively small chip. Moreover, Chapter 4 includes important practical considerations regarding the fabrication and assembly of the combined PA as well as its performance testing.
- The combined Watt-level PA containing four parallel PA-cell fed by an on-chip power divider has been developed and tested. To evaluate and minimize the negative effects of various imperfections occurring in fabrication and assembly processes on the PA performance, their impact has been investigated by testing multiple samples. The obtained high PA efficiency ( $\geq 20\%$ ) and output power ( $\geq 29.8$  dBm) over a wide frequency range (30%) exceed the state-of-the-art in Si-based PAs.

## 5.2 Future Perspectives

Since the present work has a relatively wide multidisciplinary scope covering both antenna and circuit designs, there are multiple perspective directions for future research and development.

### **Antenna design directions:**

The tapered ML transition used in the Watt-level PA on the other side of the combiner to make a conventional GSG output interface could be replaced by an SIW-fed antenna element. For example, it could be done in a similar fashion as in the power-combining module described in Section 3. Owing to its relatively small size in terms of wavelength, such an active antenna element with the desired spatial power combining functionality could be potentially used as a building block of beam steering high-EIRP array antennas [150–152]. Moreover, on an individual antenna element level, multiport feeding could be used to generate the higher-order modes, which provides extra degrees of freedom for obtaining additional functionalities, such as polarization diversity.

### **Circuit design directions:**

In the present work, the proposed PA architecture has been elaborated on an example of the PA containing four PA-cells. However, as shown in Chapter 2, there are no fundamental limitations on accommodating up to 30 PAs to a single-mode SIW at Ka-band. Therefore, further output power increase could be based on scaling up the original design. The multiphysics effects occurring in the joint structure could be addressed by the same EM-circuit-thermal optimization. Moreover, the efficiency of the combined PA could be increased by using PA-cells operating in

switching mode [153, 154]. The desired collector voltage and current waveforms could be achieved by introducing a tank resonant circuit in the SIW-based power combiner.

Although the proposed power-combining architecture has been originally developed to facilitate efficient high power generation, it could also be used in the context of parallel low-noise amplifiers (LNAs) [155]. In this case, the active impedance of ML ports should be optimized to realize optimal noise matching. The performed initial study (not included in this thesis) shows that using multiple parallel LNAs allows one to significantly improve the linearity of Rx chain without increasing noise figure. Therefore, the proposed architecture could be extended to a complete Tx/Rx front-end.

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## Part II

### Included Papers



# Wide-Band Spatially Distributed $TE_{10}$ Substrate Integrated Waveguide Transition for High-Power Generation at mm-Wave Frequencies

Artem Roev, Rob Maaskant, Marianna Ivashina, and Anders Höök

in *Proceedings of the 2017 International Symposium on Antennas and Propagation (ISAP), Phuket, 2017*, pp. 1-2.



# Wide-Band Spatially Distributed $TE_{10}$ Substrate Integrated Waveguide Transition for High-Power Generation at mm-Wave Frequencies

Artem Roev, Rob Maaskant, Marianna Ivashina, and Anders Höök

## Abstract

An array of microstrip lines is used for the direct excitation of the spatially distributed  $TE_{10}$  substrate integrated waveguide (SIW) mode. The proposed configuration can generate  $4\times$  more power with a  $4\times$  smaller form factor relative to a single microstrip-to-SIW transition, while offering a larger bandwidth. This is an important step toward the generation of high power in densely integrated mm-wave antenna systems.

## 1 Introduction

The generation and transmission of high power is a major challenge at mm-wave frequencies, since the atmospheric propagation and material losses are significant and increase as frequency increases. This is further exacerbated by the fact that semiconductors reduce in size and deliver less power when moving up into the mm-wave frequency region. Hence, more transistors are needed to overcome these limitations, but will collectively generate more heat. These problems must be overcome to, for instance, enable the high data throughputs that are envisioned for future 5G communication systems.

Substrate integrated waveguide (SIW) technology offers a low-cost low-profile mm-wave integration solution. However, a transition is needed to interface the principal SIW electromagnetic field mode to a single network node, or TEM-type transmission line (TL), so that a circuit component can be connected. A typically employed microstrip-to-SIW transition is shown in Figure 1 (a), where a tapered section is proposed to transform the distributed SIW to the spatially confined microstrip TL mode [1], [2]. We propose a transition that is more compact (no TL tapering needed) by interfacing an array of amplifiers to a single SIW port. This allows to directly feed the spatially distributed  $TE_{10}$  single SIW mode with high power. Note that this is different from the multi-mode concept in [3]. Our transition also exhibits larger impedance bandwidth characteristics. The proposed concept is illustrated in Figure 1 (b).



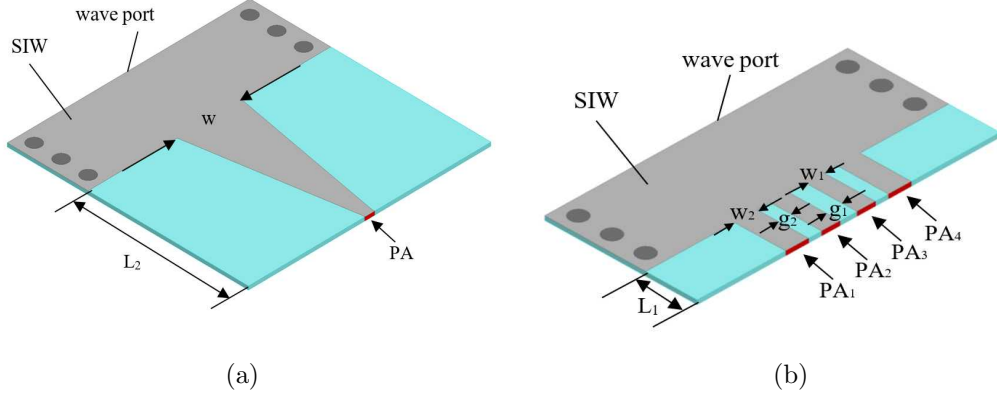


Figure 1: (a) Classical single microstrip-to-SIW transition; (b) Proposed multi-channel transition and optimization parameters.

## 2 Design Details

Our design aims at operating in the K/Ka-Band and is based on the proposed concept in Figure 1 (b) with indicated geometrical parameters. The structure is built on an RT5880 laminate with substrate thickness 0.127 mm and relative dielectric constant  $\epsilon_r = 2.2$ . The low dissipation factor ( $\tan\delta @ 10 \text{ GHz} = 0.0009$ ), thereby extending the applicability of RT5880 to Ka-band and above.

Our specific design employs four parallel microstrip lines, each of which is terminated by  $50\text{-}\Omega$  to represent the output resistance of a power amplifier. To expedient the simulations, the SIW vias were replaced by conductive side walls. Perfect electric conductors were used for the metals. Regarding Figure 1, the optimized designs for best impedance match are (in mm):  $w = 2.4$ ;  $L_2 = 6.5$ ;  $L_1 = 1.54$ ;  $w_1 = 0.54$ ;  $w_2 = 0.68$ ;  $g_1 = 0.5$ ;  $g_2 = 0.39$ . The SIWs are identical, width= 7.11.

## 3 Numerical Results

Figure 2 shows the field propagation inside the SIW and the coupled fields to the microstrip TLs when the SIW port is excited by the  $TE_{10}$  mode (i.e. receive mode). When transmitting, the active reflection coefficients of the microstrip TLs should be considered due to the strong electromagnetic coupling between them. The simulated active and passive wave port reflection coefficients of both the proposed transition and the conventional single-channel tapered microstrip TL are shown in Figure 3. The simulated multi-channel transition demonstrates a wide bandwidth performance relative to its single-channel counterpart. The simulated active  $|\Gamma_i|$  and passive  $|S_{ii}|$  reflection coefficient of the  $50\text{-}\Omega$  microstrip ports are shown in Figure 4. The active reflection coefficients are better than  $-30 \text{ dB}$  over the desired frequency range (27.5–31.5 GHz). The designed four-channel transition is almost four times more

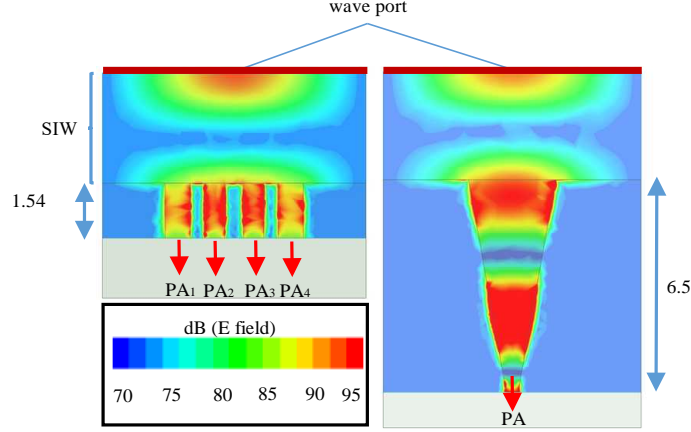


Figure 2: Magnitude of E-field distribution at 31.5 GHz (real part) and sizes (mm) of the proposed multi-channel transition and the conventional single-channel tapered microstrip transition.

compact (Figure 2) and allows to generate four times higher mm-wave output power as compared to a conventional tapered microstrip transition.

Figure 5 shows the microstrip port powers when the wave port is excited by 1 W (i.e. receive mode). The power distribution is near uniform (i.e.  $< 25\%$  variation, 250 mW is ideal), implying that the power amplifiers in the array are utilized effectively.

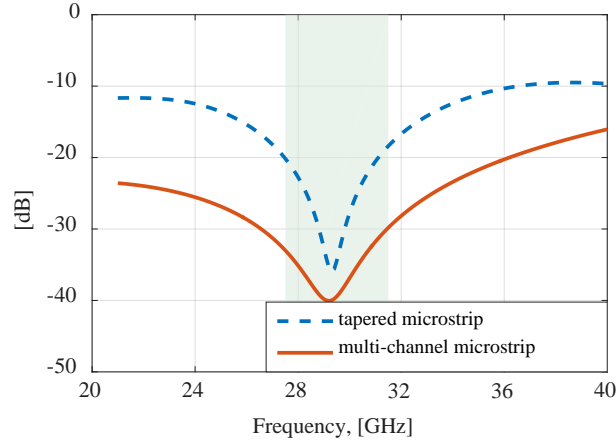


Figure 3: Simulated wave port reflection coefficient of the proposed multi-channel transition and conventional single-channel tapered microstrip transition.

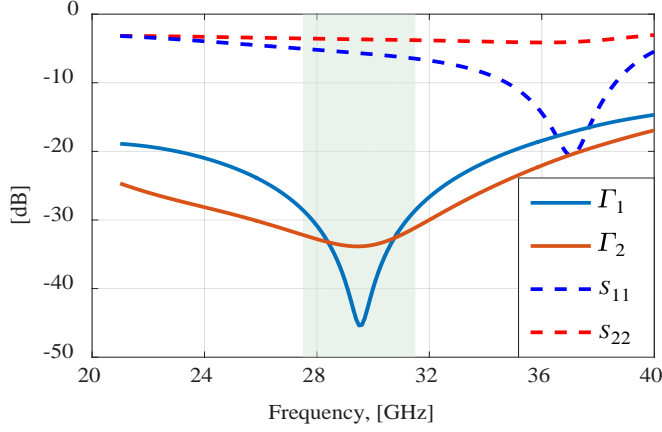


Figure 4: Simulated active and passive (dashed lines) reflection coefficient of the 50-Ω microstrip ports of the proposed transition.

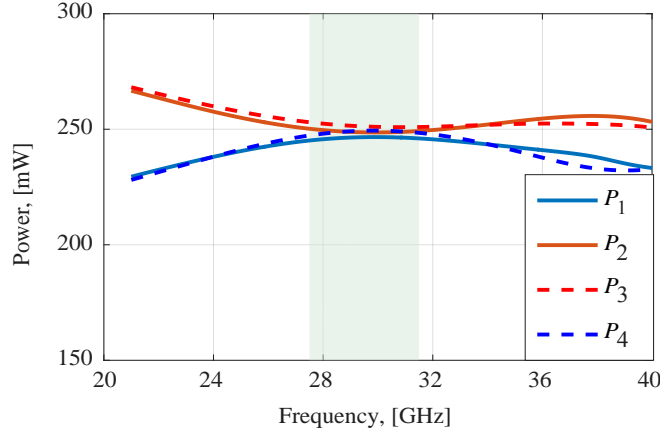


Figure 5: Simulated power accepted by the microstrip ports when the wave port is excited by 1 W.

## 4 Conclusions

A novel transition concept based on the direct excitation of the TE<sub>10</sub> substrate integrated waveguide mode by an array of strongly coupled microstrip lines has been proposed. The simulated active reflection coefficients of the four-channel transition at their microstrip ports and passive reflection coefficient at the wave port of a single transition are better than -30 dB over the desired frequency range (27.5–31.5 GHz). The quad-channel transition is four times more compact and allows to generate four times higher mm-wave output power compared to conventional tapered microstrip transitions. Its relatively short length allows to decrease transition losses and renders the structure suitable for much higher frequencies. The concept is expected to play a determining role in future mm-wave communication systems where both high-power generation and low-loss structures are required.

## 5 Acknowledgment

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## **Efficient Millimeter-Wave High Power Generation with Spatial Power-Combined Feeding Element**

Artem Roev, Rob Maaskant, Anders Höök, and Marianna Ivashina

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# Efficient Millimeter-Wave High Power Generation with Spatial Power-Combined Feeding Element

Artem Roev, Rob Maaskant, Anders Höök, and Marianna Ivashina

## Abstract

An efficient transition from a grid of amplifiers to a single substrate integrated waveguide (SIW) is presented. It is based on the excitation of the spatially distributed SIW mode with an array of parallel and strongly coupled microstrip lines (MLs), each of which is connected to an amplifier. The proposed configuration is optimized by minimizing the active reflection coefficients at the TL ports. This equalizes the amplifier optimal load impedances and excites the  $TE_{10}$  SIW mode most efficiently. Also, signals are transferred with nearly uniform power distribution at the amplifier outputs. Numerical results show that this configuration can generate  $16\times$  more power per unit volume relative to a single microstrip-to-SIW transition, while offering a larger bandwidth. A prototype has been developed to validate the proof-of-concept.

## 1 Introduction

The continued growth of data traffic in 5G wireless communication applications, short-range radars, and satellite communications, demands utilization of multi antenna systems at higher (mm-wave) frequencies [1], [2]. mm-Wave frequencies allow GHz bandwidths and hence significantly improve the data rate and systems throughput. However, efficient generation and transmission of high RF power is a major challenge at mm-wave frequencies, due to the increased propagation and material losses as well as output power limitations of semiconductor technologies. Monolithic microwave integrated circuits (MMICs) are traditionally based on Gallium Arsenide (GaAs) wafer processes. However, such circuits are expensive in mass production and complex to use for highly integrated structures, such as digital beamformers or radio modems for cellular handsets. Silicon technologies are more cost effective and more suitable for integration, but their maximum output power is limited due to low breakdown voltage [2]. This problem can be overcome by using many low-cost active devices per unit volume and combine them using series and parallel power combining techniques [3]. However, the latter solutions are potentially lossy since power is typically combined to a single point before leaving the MMIC. We propose a solution to this problem. Another challenge is the integration with radiating elements that are comparable in size at mm-wave frequencies.



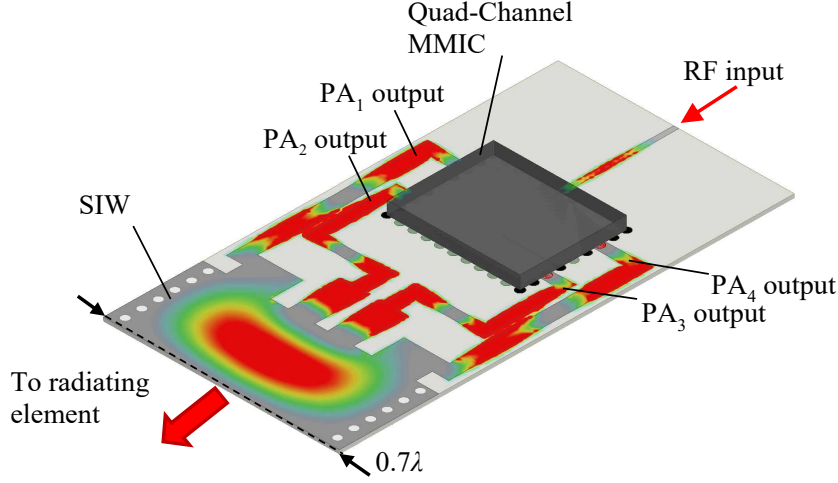


Figure 1: Illustration of the proposed concept of the transition interfacing four amplifiers situated inside an (NXP) MMIC chip to a single substrate integrated waveguide (SIW).

This paper presents a novel concept of the transition that can be employed between a single radiating element and an array of amplifiers to facilitate such integrated solutions. Figure 1 illustrates this transition, where an array of four amplifiers (situated inside a chip) is interfaced with a single substrate integrated waveguide (SIW) through four spatially distributed microstrip lines. Initial results for the spatially distributed SIW excitation have been presented in [4], where it was compared to a conventional single-channel tapered transition [5]. In addition to exciting printed circuit antennas, the SIW structure can be also be used to excite a metal waveguide in a direct contactless manner [6].

The goals of the current work are:

- (i) To describe the design methodology, including the optimization of the transition for a given field excitation (the focus is on compactness of the SIW structure for potential applications in antenna arrays, and efficient utilization of power amplifiers that should be driven by equal powers); and
- (ii) To design a proof-of-concept prototype, which demonstrates the predicted gain in performance, i.e.  $16\times$  higher power generation per unit volume in comparison to a single transition case. This also includes specific considerations for testing multi-channel transitions with a two-port only calibration.

## 2 Numerical Results

Figure 2 (a) shows the geometry of the proposed transition, and Figure 2 (b) illustrates the field propagation inside the SIW as well as the field coupled to the microstrip TLs when the SIW port is excited by the  $TE_{10}$  mode (i.e. receive mode).

Due to strong electromagnetic coupling between microstrip TLs [see Figure 2 (b)],

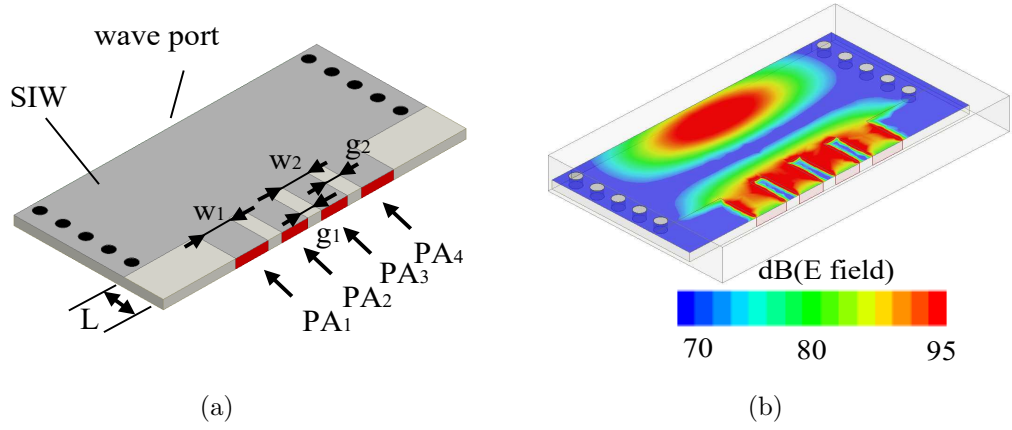


Figure 2: (a) The EM model of the proposed multi-channel transition and optimization parameters; (b) Simulated E-field amplitude distribution at 31.5 GHz (real part).

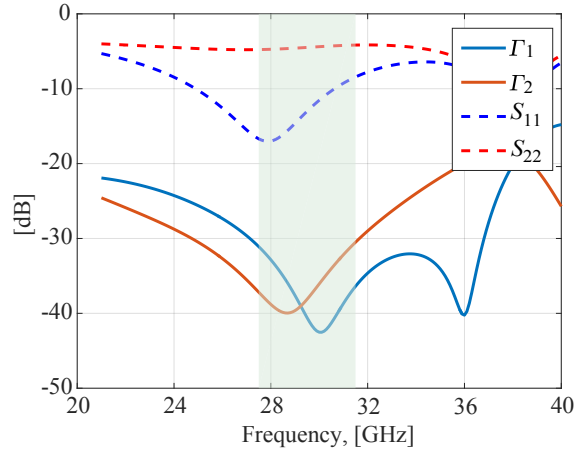


Figure 3: Simulated active and passive (dashed lines) reflection coefficients of the 50-Ω microstrip ports of the simulated transition, as shown in Figure 2. The colored region shows the operational bandwidth.

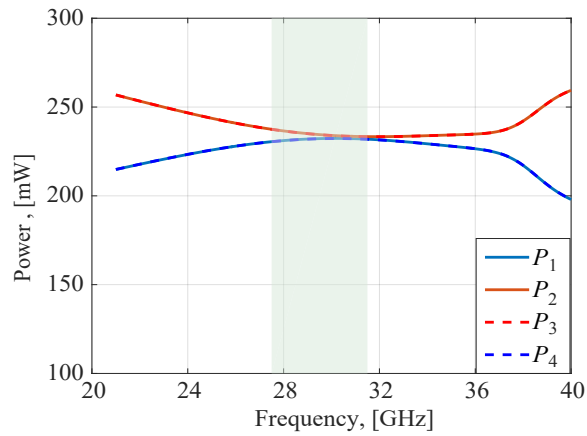


Figure 4: Simulated power accepted by the microstrip ports when the wave port is excited by 1 W.

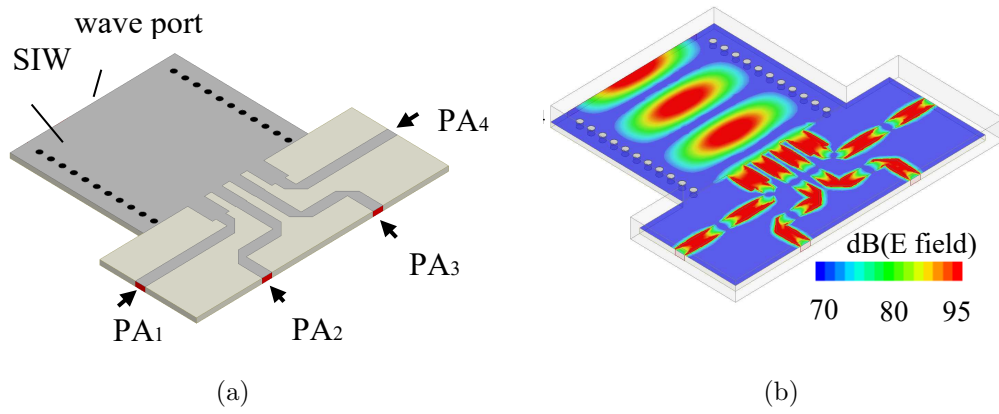


Figure 5: (a) Proposed transition including the array of short parallel transmission lines and the routing of the microstrip lines; (b) Magnitude of E-field distribution at 31.5 GHz (real part).

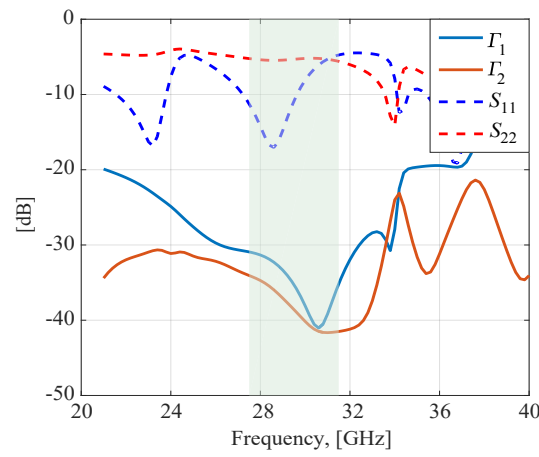


Figure 6: Simulated active (solid) and passive (dashed) reflection coefficients of the 50-Ω microstrip ports ( $\Gamma_n$ ) shown in Figure 5.

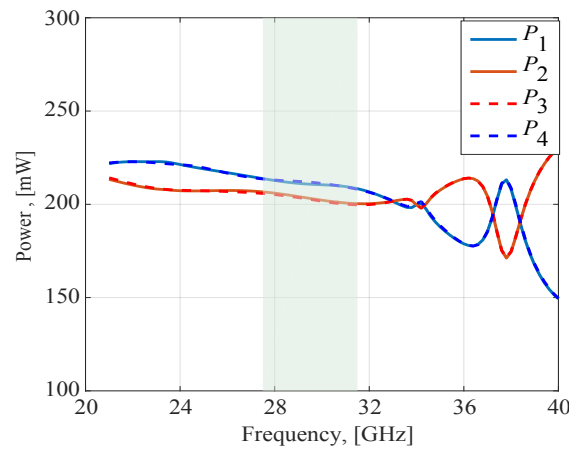


Figure 7: Power accepted by the microstrip ports when the wave port is excited by 1 W, as shown in Figure 5.

the active reflection coefficients of the microstrip TLs should be considered in the transmitting situation to optimize the design.

With the reference to Figure 2 (a), the structure is formed by RT4350 laminate with the thickness of 0.254 mm and relative dielectric constant of  $\varepsilon_r = 3.66$ . The width of the considered SIW is 7.11 mm, diameter and distance between vias are 0.3 mm and 0.63 mm respectively. The optimum design parameters for achieving the best active impedance matching are (in mm):  $L = 1.07$ ;  $w_1 = 0.71$ ;  $w_2 = 0.88$ ;  $g_1 = 0.37$ ;  $g_2 = 0.38$ . The 50- $\Omega$  simulated active and passive reflection coefficients ( $\Gamma_1$ ,  $\Gamma_2$ ,  $S_{11}$  and  $S_{22}$ ) in the desired frequency range (27.5–31.5 GHz) are shown in Figure 3. As one can see, the proposed multi-channel transition demonstrates wide bandwidth performance (50% relative bandwidth) with both  $|\Gamma_1|$ ,  $|\Gamma_2| \leq 20$  dB.

Figure 4 shows the microstrip port powers when the wave port is excited by 1 W (i.e. receive mode). The power distribution is nearly uniform (250 mW per channel is ideal) in the desired frequency range, implying that the power amplifiers in the array are utilized effectively. The performance degradation that is visible near 40 GHz is due to higher-order SIW modes. This was deemed acceptable and necessary to retain sufficient design freedom for optimizing the transition between 27.5 and 31.5 GHz.

Figure 5 and 6 show simulation results for the routing of 50- $\Omega$  microstrip lines to be able to mount RF connectors to the PCB and to decouple the microstrip lines. To achieve the same electrical length of the transmission lines, their physical length has been slightly tuned. After combination,  $|\Gamma_1|$  and  $|\Gamma_2|$  are well below  $-30$  dB within the desired frequency range (27.5–31.5 GHz). The power distribution remains nearly uniform across the transmission line ports (See Figure 7). However the average level of the accepted power becomes a bit lower (8% relatively to the previous case) due to losses in the bent microstrip TLs. It was verified that by adding the TLs to the connectors, the performance due to mutual coupling effects was not degraded and that the effects of these extra line lengths can be removed through a calibration procedure.

The E-field distribution inside the combined back-to-back structure, intended for experimental verification (to be presented in future), is shown in Figure 8. This simulation revealed an undesired field leakage between the dielectric-filled gap formed by the connector body. To remove this effect, both additional via holes and a slight tapering of the TL near the central pin of the connector (not visible in Figure 8) were introduced. After optimization, the reflection coefficient in the desired frequency range was shown to satisfy the requirements. The active reflection coefficients of the 50- $\Omega$  input ports that were obtained for the optimized connector interface are shown in Figure 9. Ripples up to  $-20$  dB are visible, which are produced by the connectors and bent microstrip TLs. These ripples can be removed by the designed 2-port TRL calibration kit, which consists of three standards:

- (i) Thru (T), where two error boxes are connected;
- (ii) Reflect (R), where the error box is grounded by a via;

(iii) Line (L), where the error boxes are connected through the quarter-wave length segment, corresponding to the central frequency (29.5 GHz).

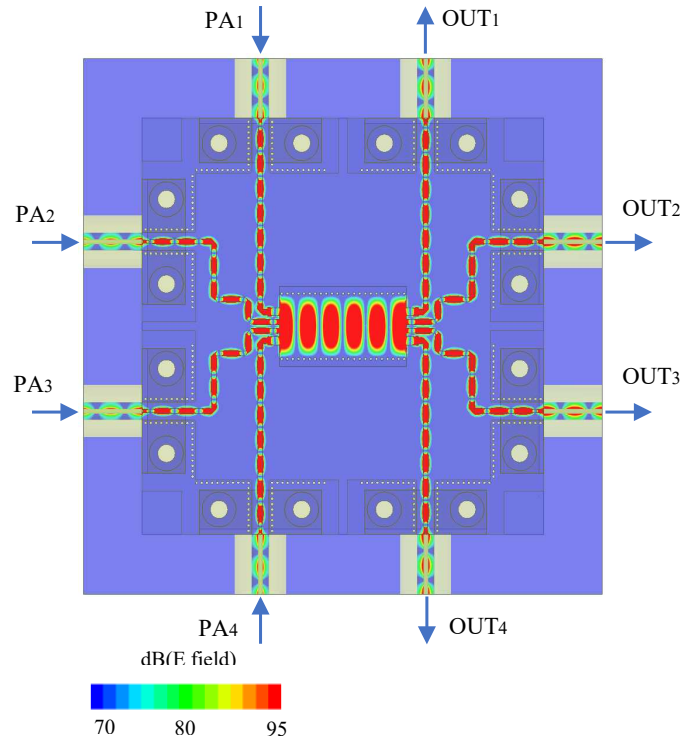


Figure 8: Simulated E-field amplitude distribution for the proof-of-concept prototype, when input ports are uniformly excited at 31.5 GHz (real part).

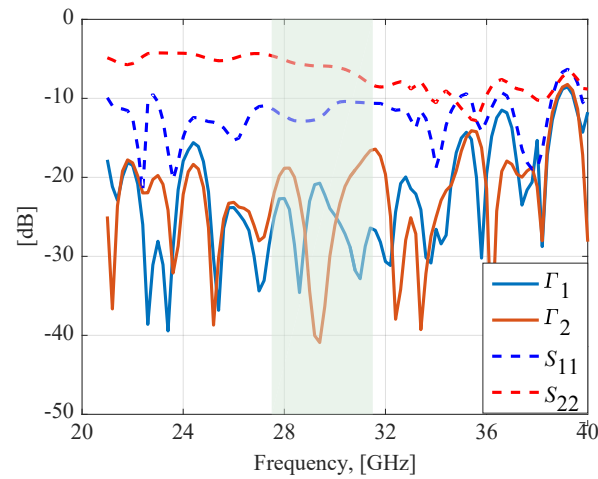


Figure 9: Simulated active (solid) and passive (dashed) reflection coefficient of the 50-Ω microstrip ports of the prototype, as shown in Figure 8.

### 3 Design of the Prototype

The designed prototype is a passive back-to-back structure, which has 4 input and 4 output 50- $\Omega$  coaxial ports for testing with a standard VNA (See Figure 10). The structure is built on a hybrid multilayer PCB with edge metallization, which is formed by stacking two dielectric material layers. The top RT4350 laminate has a substrate thickness of 0.254 mm and relative dielectric constant of  $\epsilon_r = 3.66$ . The bottom hardback substrate is FR4, which makes the structure more rigid.

The dissipation factor of RT4350 is low ( $\tan\delta @ 10 \text{ GHz} = 0.0037$ ), which extends the applicability of this laminate to Ka-band and above. Inner metal layers of the hybrid structure can be also used in the future for routing, bias, or control lines of an active device. The PCB has an overall size of approximately  $46 \times 46 \text{ mm}^2$  and is bolted by  $4 \times M1.6 \text{ mm}$  screws to an aluminum support. Figure 11 shows three parts of the model:

- the 1st part is the proposed transition between the SIW and multiple transmission lines (TL) (a),
- the 2nd part is the set of routing microstrip lines that are needed for testing (b),
- the 3rd part is the corresponding connector interface (c).

Due to strong electromagnetic coupling effects between the transmission lines in the SIW region, the device under test (DUT) includes divergent lines to make the routing lines to the connectors (light gray color) virtually independent. In this case, we can use a 2-port only calibration kit to remove the effect of the routing lines and connectors from the measurement results.

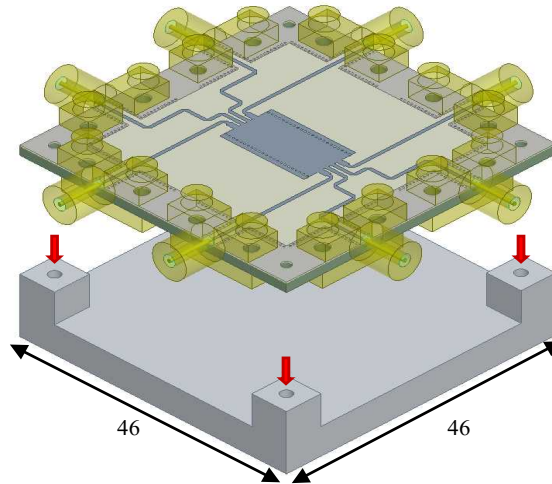


Figure 10: A mechanical model of the 8-port back-to-back prototype.

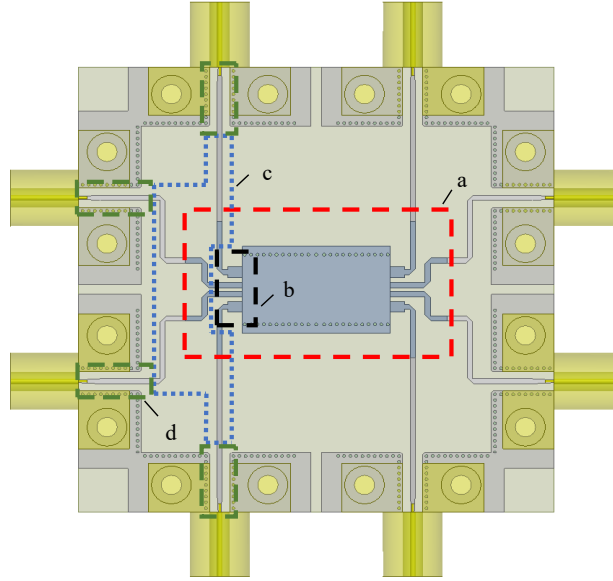


Figure 11: The detailed model of the proof-of-concept demonstrator: (a) the entire back-to-back structure including two connected transitions, (b) the proposed transition between SIW and four short and strongly-coupled transmission lines, (c) 50- $\Omega$  routing microstrip lines that decouple the transmission lines at the ports of the b2b for the purpose of testing, (d) connector interface regions.

## 4 Conclusion

A new transition for interfacing an array of four parallel amplifiers to a single substrate integrated waveguide has been optimized and examined. The predicted active reflection coefficients of all ports are better than  $-30$  dB over the desired frequency range (27.5–31.5 GHz), corresponding to a 50% relative bandwidth. Furthermore, a nearly uniform power distribution across the parallel ports confirms that the power amplifiers in the array can be utilized effectively. A proof-of-concept prototype with calibration kit is under construction; experimental results are to be presented later.

The concept is expected to play an important role in future mm-wave communication systems and MMIC designs, where both high-power generation and cost efficiency are important requirements.

## 5 Acknowledgment

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## Wideband mm-Wave Transition between a Coupled Microstrip Line Array and SIW for High Power Generation MMICs

Artem Roev, Rob Maaskant, Anders Höök, and Marianna Ivashina

in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 10, pp. 867-869, Oct. 2018.

*The layout of this paper has been revised in order to comply with the rest of the thesis.*



# Wideband mm-Wave Transition between a Coupled Microstrip Line Array and SIW for High Power Generation MMICs

Artem Roev, Rob Maaskant, Anders Höök, and Marianna Ivashina

## Abstract

A compact wideband transition between an array of microstrip lines (MLs) and a single substrate integrated waveguide (SIW) is presented. The spatially distributed fundamental SIW mode is excited by an array of parallel and strongly coupled microstrip lines (MLs). The proposed configuration is optimized by minimizing the active reflection coefficient at each ML port. Signals are transferred with nearly uniform power distribution across the ML ports, which facilitates an effective utilization of power amplifiers once interconnected. Measured results of the proof-of-concept demonstrator are in good agreement with simulations. The proposed configuration is capable of generating more power per footprint size relative to a single microstrip-to-SIW transition, while offering a 50% bandwidth. At the same time, the compactness of the ML-to-SIW transition makes it suitable for tight integration with MMICs and applications in wide-band array antennas.

## 1 Introduction

Efficient generation and transmission of high RF power is a major challenge at mm-wave frequencies, due to the increased propagation and material losses as well as output power limitations of semiconductor technologies [1]. Silicon-based technologies are often not the first choice due to their relatively low breakdown voltage, yet, significant research has been put into it as they enable cost-effective highly-integrated circuit solutions. The focus of the present work is on a compact wideband transition between a mm-wave integrated circuit and an antenna or waveguiding structure. The key design goals are: *(i) Wide frequency bandwidth* ( $\sim 50\%$ ); *(ii) Minimal power losses* when transmitting and combining signals from power amplifiers (PAs); *(iii) Quasi-optical power combining* using grid amplification techniques, i.e., employ multiple PAs to generate high mm-wave power in the range of 15–25 dBm per antenna element. This is challenging for Silicon integrated solutions particularly because the on-chip power combiner and the antenna interconnecting transition must be low

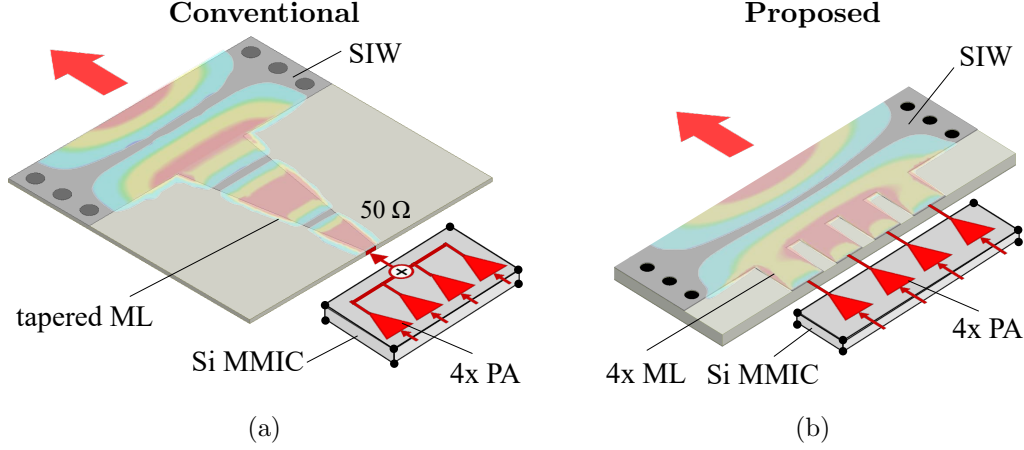


Figure 1: (a) Classical single channel transition interfacing an array of power amplifiers with an SIW; (b) The proposed novel transition.

loss [2]; (iv) *Minimal dimensions* to render the transition suitable for antenna integration, specifically for arrays (with inter-element-spacing  $< 0.8\lambda$ ), and allow for on-chip integration at a later stage.

Figure 1 (a) exemplifies a conventional microstrip line (ML) to substrate integrated waveguide (SIW) transition [3, 4], which was used as a starting point in our design. As illustrated, the chip with multiple PAs delivers high power to the input port of the transition which is then transferred to the SIW. The critical design parameter is the effective impedance of the SIW, which in practice is significantly lower than the typical  $50\text{-}\Omega$  interface impedance of the (PA) chip. Achieving optimal impedance match renders the transition long and therefore lossy, especially if a wide frequency bandwidth (BW) is required (See [3, 4], and Table I). This fundamental

Table 1: Comparison between state-of-the-art solutions and proposed design

Reference	Frequency, [GHz]	Bandwidth, [%]	Losses (b2b), [dB]	SIW width, [ $\lambda$ ]
single-, TE10 [3]	25-31	12	0.15	0.50-0.62
single-, TE10 [4]	17.5-30	50	1	0.44-0.76
multi-, TE20 [6]	20-40	50	2	0.57-1.14
multi-, TE10 [this work]	22-36	48	0.3	0.51-0.84

trade-off between BW and power losses for a single channel transition does not exist for the recently proposed multi-channel transition [5], which directly interfaces an array of PAs to an SIW via multiple spatially distributed MLs [See Fig. 1(b)]. Fig. 1 also visualizes the transfer from the ML mode(s) to the fundamental TE10 SIW mode. The MLs are closely spaced and, hence, strongly coupled, which causes mutual coupling effects to play a critical role in the proposed transition performance



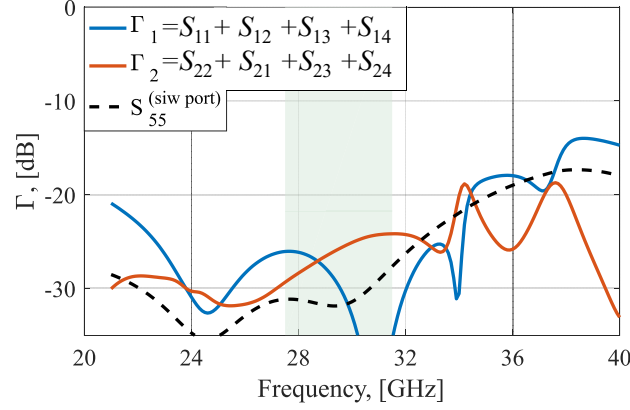


Figure 3: Simulated active reflection coefficients of the 50-Ω microstrip ports and wave port passive reflection (dashed) of the DUT, as shown in Figure 2. The colored region shows the band of interest.

It is worth mentioning that  $w_1$  and  $w_2$  are not equal due to the fact that active line impedances are different between the inner and outer two coupled all-excited MLs. The 50-Ω simulated active and passive reflection coefficients ( $\Gamma_1, \Gamma_2, S_{55}^{\text{siw}}$ ) in the desired frequency range (27.5–31.5 GHz) are shown in Figure 3. The multi-channel transition demonstrates wide BW (beyond 50% relative bandwidth) with both  $|\Gamma_1|$  and  $|\Gamma_2| < -15$  dB. A sensitivity study on  $\Gamma$  was performed and shows that  $|\Gamma|$  remains below  $-15$  dB in case of normal distributed phase errors of signals across the ML ports with a standard deviation  $< 15^\circ$ .

### 3 Prototype and Measurement Results

The designed prototype constitutes a passive back-to-back (B2B) structure employing 4 input and 4 output 50-Ω coaxial ports to allow for testing with a standard VNA (See Figure 4). The structure is built on a hybrid multilayer PCB, which is formed

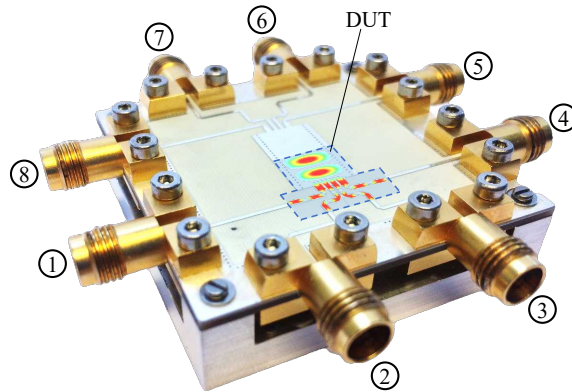


Figure 4: DUT in a back-to-back configuration.

### 3. PROTOTYPE AND MEASUREMENT RESULTS

by stacking two dielectric material layers. The top RT4350 laminate has a substrate thickness of 0.254 mm and  $\epsilon_r = 3.66$ . The bottom hardback substrate is FR4, which makes the structure more rigid. The interior metal layers of the hybrid structure can be used in the future for routing, bias, or control lines of an active device. The PCB has an overall size of approximately  $46 \times 46$  mm.

The measured  $\Gamma$  of the symmetric 50- $\Omega$  ports are shown in Figure 5. Curves are close to each other and in good agreement with the simulations shown by black dashed lines. Visible ripples are produced by the connector interfaces and bent microstrip TLs whose effects cannot be completely removed by the designed 2-port TRL calibration kit, since in practice ports are slightly different. However, the measured  $|\Gamma_1|$  and  $|\Gamma_2| < -13$  dB in the desired frequency range and  $< -10$  dB over the whole range (20–40 GHz). Insertion losses of the proposed DUT are shown in Fig. 6. The measured losses were de-embedded using the thru-standard of the designed calibration kit. Contributions of the dielectric and radiation losses have been estimated

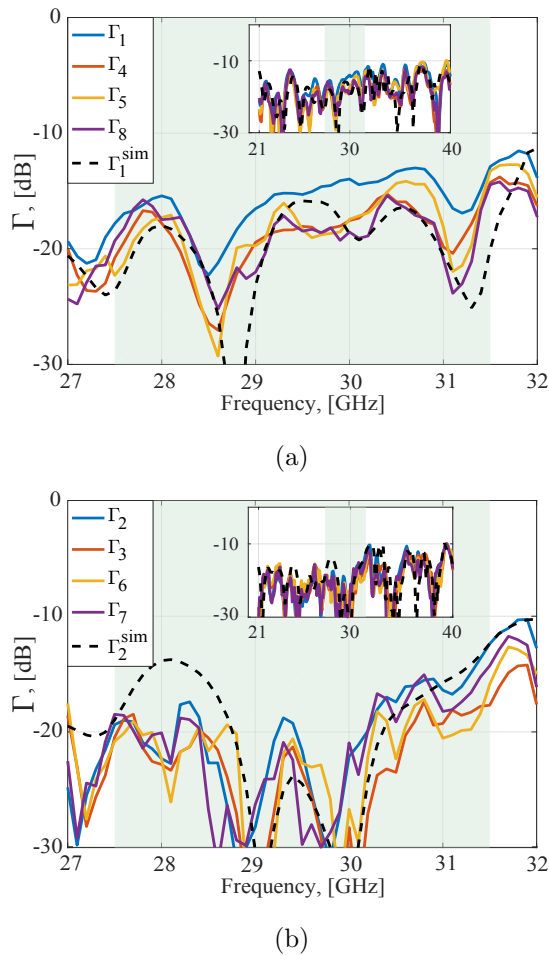


Figure 5: Measured (solid) and simulated (dashed) active reflection coefficient of the symmetric 50- $\Omega$  microstrip ports of the prototype (including effect of connectors), as shown in Figure 4.



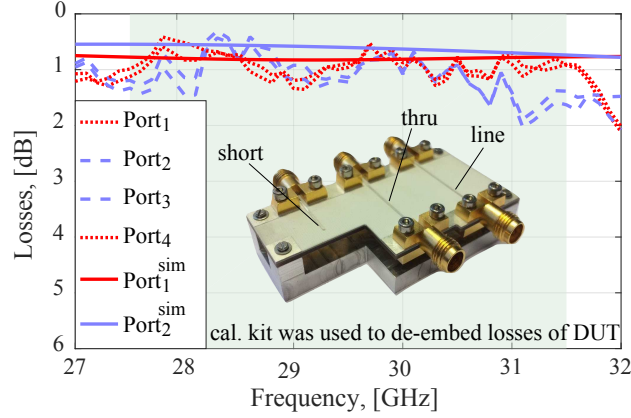


Figure 6: Measured (dashed) and simulated (solid) losses of proposed DUT.

using simulation data. At 30 GHz the total losses of the DUT are 0.73 dB, where the contribution of the dielectric and radiation losses are 0.28 dB and 0.45 dB, respectively. Radiation losses are dominant and attributed to the bent MLs in the DUT. The overall expected losses of the proposed transition without routing lines is estimated less than 0.3 dB.

## 4 Conclusions

A new transition for interfacing an array of parallel amplifiers to a single SIW has been optimized and examined in the context of its applications in wideband and high-efficiency array antenna transmitters. The proposed transition overcomes fundamental limitations of single-channel SIW transitions in simultaneously achieving a wide bandwidth and low power loss, and also outperforms the state-of-the-art multi-channel multi-mode transitions in terms of its compactness and power transfer/combining efficiency (See Table 1). The proof-of-concept experiments demonstrate a good agreement with simulated performance, where we have achieved an active impedance bandwidth defined at -10 dB of nearly 50%. The active reflection coefficients of all prototype ports are less than -14 dB over the desired frequency range (27.5–31.5 GHz), corresponding to a 50% relative bandwidth, and below -10 dB over whole range (20–40 GHz) with the estimated losses less than 0.3 dB. Furthermore, a nearly uniform power distribution across the parallel ports confirms that the power amplifiers in the array will be utilized efficiently. The concept is expected to facilitate high power generation and efficient power transmission in future mm-wave array antennas and MMIC designs.

## Acknowledgment

The work is a part of the Silicon-based Ka-band massive MIMO antenna systems for new telecommunication services (SILIKA) project, funded by the European Union's Horizon 2020 research and innovation program under the Marie Skłodowska Curie grant agreement #721732.

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## **N-Way Spatial Power Combining in SIW for High Power Generation MMICs – Scalability Bounds**

Artem Roev, Marianna Ivashina, Rob Maaskant, and Marion K. Matters-Kammerer

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# N-Way Spatial Power Combining in SIW for High Power Generation MMICs – Scalability Bounds

Artem Roev, Marianna Ivashina, Rob Maaskant, and Marion K. Matters-Kammerer

## Abstract

An N-way transition between an array of amplifiers and a single substrate integrated waveguide (SIW) is presented. Its operation principle is based on excitation of the spatially distributed  $TE_{10}$  mode with an array of parallel and strongly coupled microstrip lines (MLs). The paper discusses and evaluates the approximate scalability bounds of such a structure in terms of the number of input channels. The model shows that, by employing a thin substrate, more amplifiers are capable of interfacing a single SIW to increase the output power, which is an important conclusion in regards to a future on-chip implementation of the structure. The model has also been validated by numerical simulations.

## 1 Introduction

Increased propagation and material losses as well as output power limitations of semiconductor devices at mm-wave frequencies is a problem that is partly overcome by parallel and series power-combining of multiple active devices per single antenna element [1]. However, conventional circuit-level power combiner networks have inherent high insertion losses, which significantly increase with the number of channels [2]. A possible solution towards the efficient high power generation at mm-wave frequencies is the recently proposed multi-channel transition in [3], which directly interfaces an array of amplifiers to a single SIW via multiple closely separated microstrip lines (MLs), as illustrated in Figure 1. This allows one to directly excite the spatially distributed  $TE_{10}$  SIW mode with high power. Since the output power is proportional to the number of input channels, it is important to investigate the scalability of such a structure.

## 2 Scalability Study

The scalability of the structure will be examined with the help of an approximate impedance matching model. There are several definitions of the transmission line characteristic impedance, one of the most common are voltage-current and power-voltage [4]. For the quasi-TEM mode in a microstrip line (ML) all definitions converge

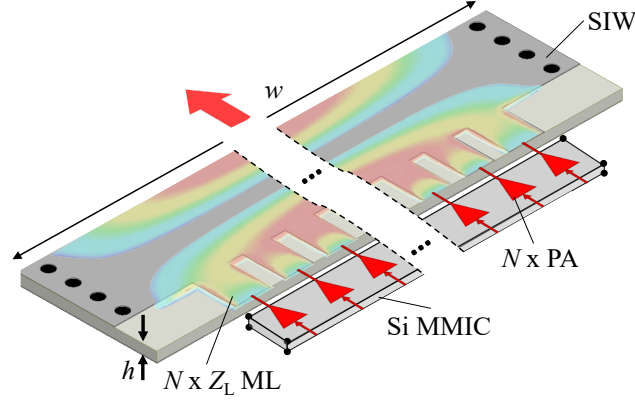


Figure 1: Compact transition interfacing  $N$  power amplifiers (possibly embedded in a single MMIC) to a single substrate integrated waveguide (SIW).

to the same characteristic impedance (if pure TEM), i.e., one that is solely a function of the ML geometry and is frequency independent [4,5]. Conversely, the characteristic impedance of the  $TE_{10}$  mode propagating in the SIW is not uniquely defined, however, the definitions differ by a scaling factor  $k$  only:

$$Z_{TE10} = k \frac{h}{w} \sqrt{\frac{\mu}{\epsilon}} \left( 1 - \frac{\lambda^2}{4w^2} \right)^{-1/2} \text{ where } \begin{cases} k = \frac{\pi}{2}, & \text{if V-I def.} \\ k = 2, & \text{if P-V def.} \end{cases} \quad (1)$$

An impedance matching model of the parallel power combiner could to first order constitute a parallel connection of  $N$  lines, each with an impedance  $Z_L$  connected to a common port. This implies that the equivalent impedance at this point is  $Z_L/N$ . The obtained equivalent impedance should be equal to the characteristic impedance  $Z_{TE10}$  of the SIW  $TE_{10}$  mode to realize a good impedance match. Thus, increasing the number of channels demands decreasing the characteristic impedance. This could be done by increasing the SIW width  $w$  or decreasing the height  $h$ . However, increasing  $w$  might lead to the excitation of higher-order modes. Figure 2 shows the estimated number of connected channels  $N$  as a function of the ML impedance for different substrate thicknesses  $h$ . The upper bound of the filled areas corresponds to the maximum number of channels, geometrically limited by the SIW width (the spacing between the lines is assumed to be equal to the line width). The lower bounds are set by the optimal impedance matching criteria. As one can see, employment of a thin substrate and high ML impedance channels allow for interfacing more amplifiers to a single SIW, and hence significantly increase the output power as compared to a single channel transition [See Figure 3]. Compactness of the proposed solution enables future on-chip realizations.

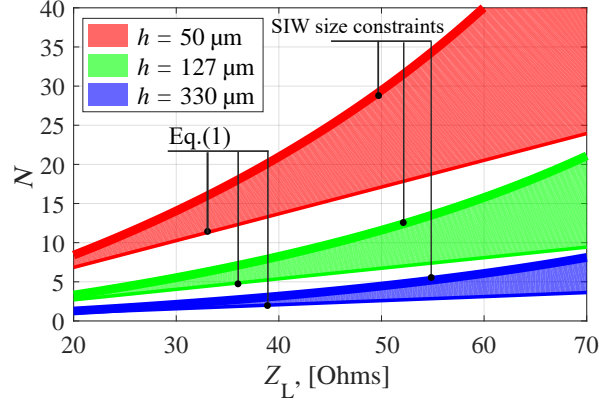


Figure 2: Estimated number of the connected microstrip ports as a function of the port impedance for different substrate height values  $h$ .

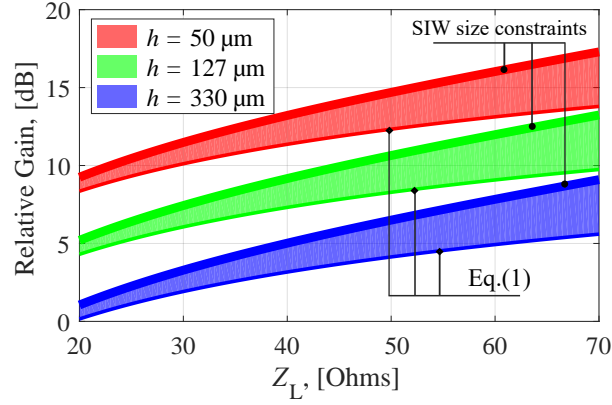


Figure 3: Estimated relative gain of the proposed structure w.r.t. a single-channel case as a function of the microstrip port impedance for different substrate height values  $h$ .

### 3 Numerical Results

To test the proposed scalability approach, a 10-way power combiner with  $50\ \Omega$  coplanar waveguide (CPW) ports has been designed, as shown in Figure 4. The port in Figure 4 (b) represents a ground-signal-ground chip interface. The employed SIW configuration is the same as the one used in [3], however the substrate thickness was reduced (from  $254\ \mu\text{m}$  to  $127\ \mu\text{m}$ ) to interface more channels. The 10-way configuration was optimized to realize active impedance matching: the simulated SIW-port passive reflection coefficient  $\Gamma_{\text{SIWport}}$  and active reflection coefficients  $\Gamma_A \dots \Gamma_E$  of the CPW ports are below  $-15\ \text{dB}$  and  $-10\ \text{dB}$ , respectively, over more than 30% bandwidth, as shown in Figure 5.



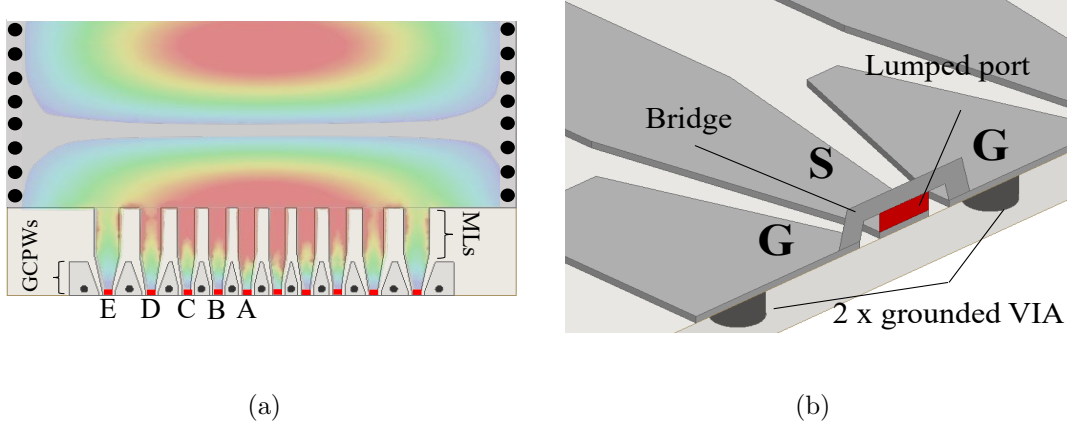


Figure 4: (a) Simulated E-field amplitude distribution in the 10-way power combiner with 50- $\Omega$  CPW input ports, when the input ports are uniformly excited at 31.5 GHz (real part); (b) The simulation model of the GSG port representing a chip interface.

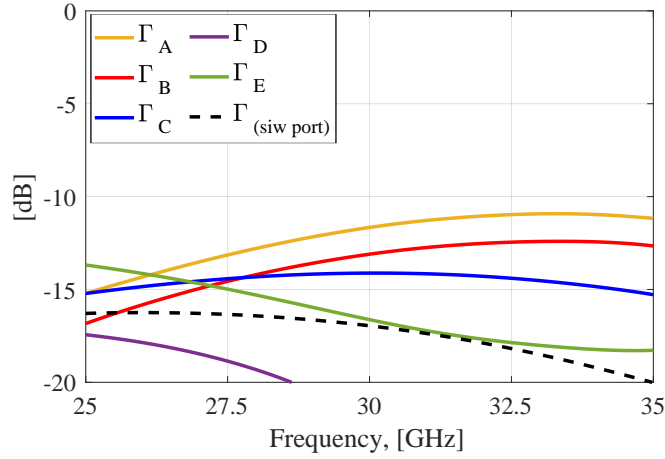


Figure 5: Simulated active reflection coefficients of the 50- $\Omega$  CPW ports and SIW-port passive reflection coefficient (dashed) of the 10-way combiner, as shown in Figure 4.

## Conclusions

The scalability of an array of  $N$  microstrip lines interfaced to a single substrate integrated waveguide (SIW) has been studied. It was shown that employment of a thin substrate along with a high ML impedance allows to maximize the number of channels that can be interfaced to a single SIW, and hence significantly increase the output power. Compactness of the proposed solution enables its future on-chip realization, which is an important conclusion. The special case of a 10-way power combiner with 50- $\Omega$  co-planar waveguide (CPW) input ports is presented. The proposed configuration is optimized by minimizing the active reflection coefficient at each input port. The simulated active reflection coefficients of the CPW-ports and passive reflection coefficient at the wave port of the structure are better than  $-10$  dB over more than 30% relative bandwidth (25–35 GHz). Numerical results validate the model and show

that this configuration allows for efficient power combining from multiple amplifiers, and hence can generate  $10\times$  more power relative to a conventional single transition, while offering a larger bandwidth for a very low profile design.

The work is a part of the Silicon-based Ka-band massive MIMO antenna systems for new telecommunication services (SILIKA) project, funded by the European Union's Horizon 2020 research and innovation program under the Marie Skłodowska Curie grant agreement #721732.

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## High Power mm-Wave Spatial Power Combiner Employing On-Chip Isolation Resistors

Artem Roey, Rob Maaskant, Marion K. Matters-Kammerer, and Marianna Ivashina

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# High Power mm-Wave Spatial Power Combiner Employing On-Chip Isolation Resistors

Artem Roev, Rob Maaskant, Marion K. Matters-Kammerer, and Marianna Ivashina

## Abstract

A spatial power combiner interfacing four power amplifiers (PAs) with isolation load resistors to a single substrate integrated waveguide (SIW) is presented. The isolation load resistors are envisioned on-chip and have been optimized to provide both the optimal active load impedance for the interconnected PAs as well as to mitigate undesired power combiner coupling effects due to non-equal excitations between PA channels. The proposed solution is compared to an ideal Wilkinson combiner in the presence of non-ideal PAs. The main performance targets are the combined output power, gain, and power efficiency at the 1-dB compression point. Simulation results demonstrate that introducing isolation load resistors allows to significantly reduce the impact of a non-uniform excitation on the combiner performance metrics.

## 1 Introduction

Increased propagation and material losses in combination with output power limitations of semiconductor devices represent a significant challenge for modern array antenna transmitters at mm-wave frequencies [1]. This challenge could be partly overcome by combining the power of multiple active devices on each antenna array element. However, conventional circuit-level power combining networks have inherently high insertion losses, which significantly increase with the number of active devices [2, 3], especially at higher frequencies. A possible solution toward more efficient high-power generation is the multi-channel transition in substrate integrated waveguide (SIW) technology employing spatial power combining [4]. This transition allows one to directly excite the  $TE_{10}$  SIW mode with high power. It avoids the use of a lossy on-chip circuit-level power combiner while enabling the direct integration of an antenna element with multiple power amplifiers (PAs) without additional interconnecting transitions. The advantages of the proposed solution become even more apparent for an increased number of input channels.

The challenge of the proposed solution is that mutual coupling effects between multiple channels have to be taken into account from the start of the design process. In [5] this transition has been optimized under the condition of a uniform excitation assuming identical PAs. However, realistic PAs are slightly different in their

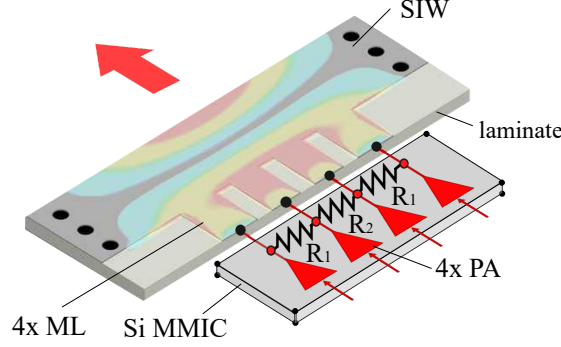


Figure 1: The proposed spatial power combiner interfacing four on-chip amplifiers with isolation load resistors to a single substrate integrated waveguide.

amplitude-phase characteristics due to different thermal regimes, semiconductor process variations and fabrication tolerances.

This paper presents a more robust spatial power combiner (SPC) design relative to the one in [4] with enhanced performance figures in the presence of a non-uniform excitation. Figure 1 illustrates this design solution, where three on-chip isolation load resistors are envisioned that are placed in-between the four PA outputs.

## 2 Concept and Operation Principle

In the original design [4] there are four input microstrip line (ML) ports with  $50\text{-}\Omega$  reference impedance and a single matched SIW port as an output. It has been optimized to realize active impedance matching for the uniformly excited case. The active reflection coefficients at the transition input ports are defined as  $\Gamma_n = \sum_{m=1}^4 A_m S_{nm}$ , where  $S_{nm}$  is the  $50\text{-}\Omega$  S-parameter from ML port  $m$  to  $n$ ,  $A_m$  is a random variable representing the complex excitation coefficient of port  $m$  simulating the effect of non-equal individual PAs. Generally, in order to reduce the effect of  $\{A_m\}_{m=1}^4$  on the active reflections  $\{\Gamma_n\}_{n=1}^4$ , the magnitudes of  $S_{nm}$  have to be minimized.

This minimization issue has been addressed by introducing isolation load resistors ( $R_1, R_2$ ) in-between the on-chip PA outputs (See Figure 1). In the case of an ideal uniform excitation the voltage difference between the ML input ports will be zero implying that no current will flow into the isolation resistors and hence there is no power dissipation. For a non-uniform excitation, the differential-mode power will be largely dissipated in the resistors. This enhanced isolation between the channels results in smaller variation of the input port active reflection coefficients  $\Gamma_n$ . It is pointed out that, despite the power dissipation in the isolation resistors, the expected combined output power may still be higher than the scenario without resistors. This is owing to the behaviour of the individual PAs, which deliver less power if the output load impedance is mismatched [6].

### 3 Numerical Validation Results

The optimal values of isolation load resistors have been found numerically by minimizing the coupling between the ML input ports while placing the resistors in-between those ports<sup>1</sup>. The full-wave EM-simulated  $5 \times 5$  scattering parameters of the SPC are shown in Figure 2a. Due to the symmetry of the SIW structure, the isolation load resistors between symmetric ports must be equal. An isolation resistor interconnecting the edge ports (1 and 4) cannot be implemented in practice since it requires long interconnecting lines. Thus there are only two optimization parameters, i.e.,  $R_1$  and  $R_2$ , which have been found to be  $108 \Omega$  and  $150 \Omega$ , respectively.

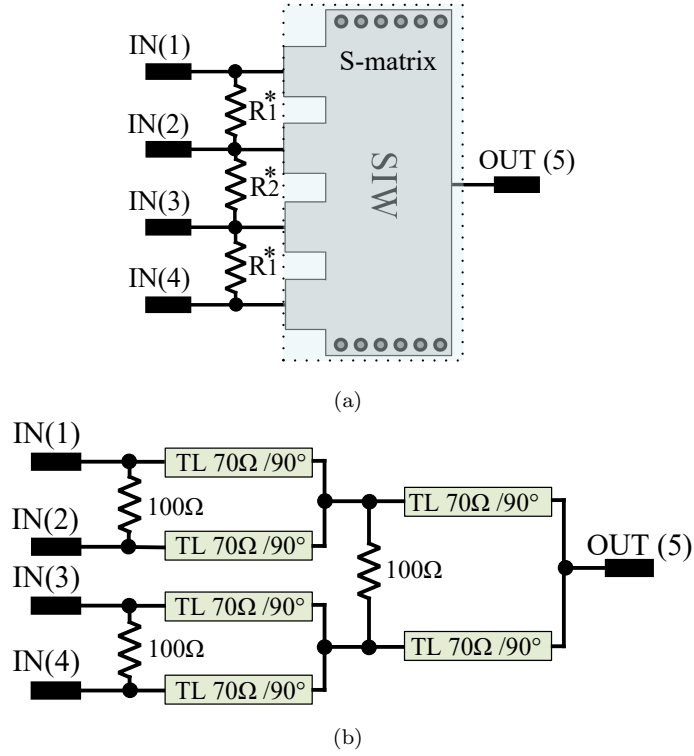


Figure 2: Simulation models of the 4-way power combiners: (a) spatial power combiner w/ and w/o isolation load resistors, (b) ideal Wilkinson power combiner.

For comparison, a  $50\text{-}\Omega$  Wilkinson power combiner built from ideal components was used as a reference [7]. It is formed by the connection of three 2:1 combiners each employing quarter-wave transmission lines (See Figure 2b). The central operation frequency is  $30 \text{ GHz}$ .

<sup>1</sup>The on-chip isolation load resistors are assumed ideal.



### 3.1 Scattering Parameters

The S-parameter simulations have been performed in Keysight's ADS software. Figure 3a shows the simulated results of the SPC with and without the isolation load resistors (dashed and solid line, respectively) along with the Wilkinson power combiner case (black line). Since in the ideal 4:1 Wilkinson power combiner all input ports are identical, the transmission coefficients from each input port to the output port are equal to -6 dB over a wide frequency range. This is different for the SPC,

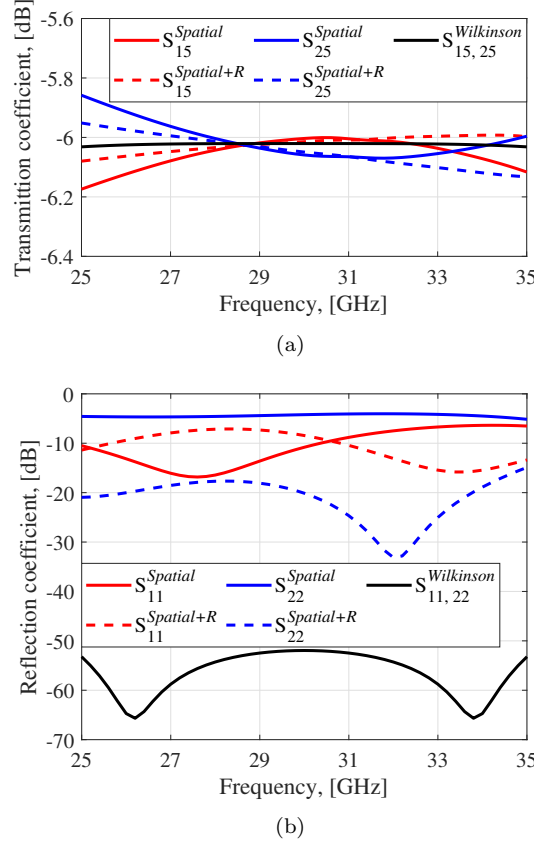


Figure 3: (a) Simulated transmission, and (b) Simulated input port reflection coefficients of the spatial power combiner w/ and w/o isolation load resistors (dashed and solid line, resp.) and an ideal Wilkinson power combiner (black line). The results for symmetric ports are omitted.

where the input ports are not identical due to the distributed  $TE_{10}$  mode structure. Therefore, using the isolation resistors allows to minimize the differences between the input channels and hence increase the efficiency of the PAs.

Figure 3b shows the corresponding passive reflection coefficients. As one can see, the design solution with isolation resistors allows reducing reflections from port 2. The  $S_{22}$  magnitude remains below -15 dB over the 25–35 GHz band, which is more than 13 dB lower in comparison to the case without resistors.

Figure 4 shows the mutual coupling coefficients, where we observe much lower

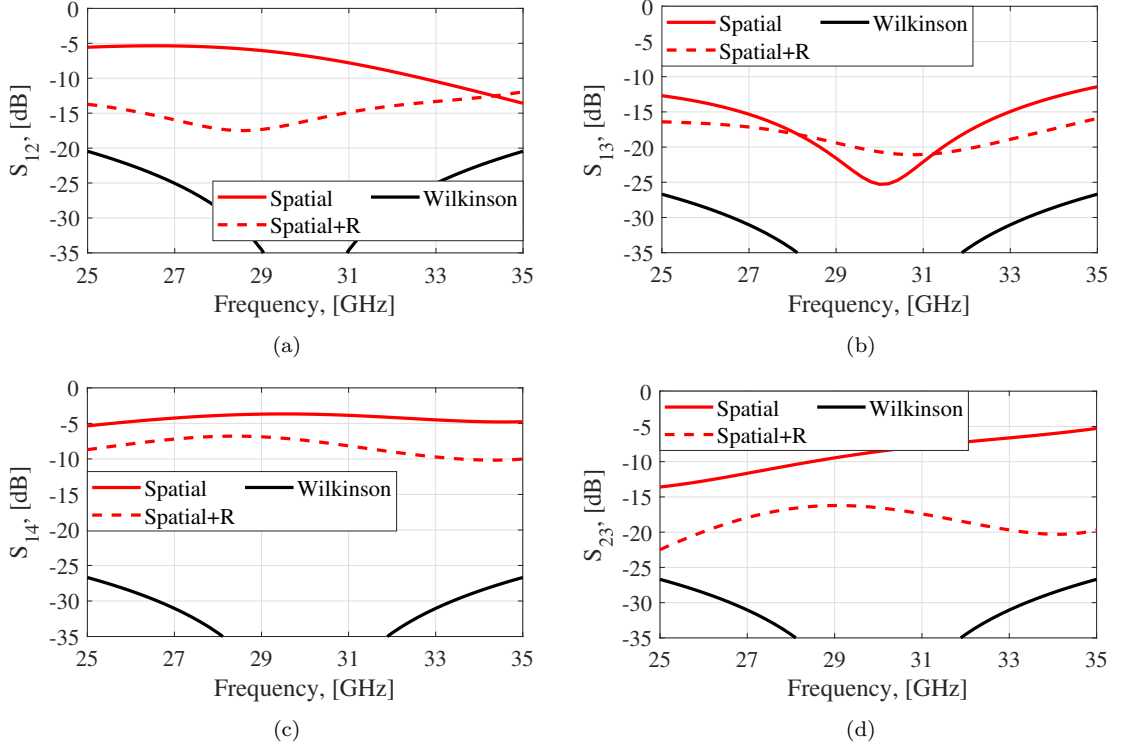


Figure 4: Simulated mutual coupling between the input ports of the spatial power combiner w/ and w/o isolation load resistors (dashed and solid lines, respectively) and an ideal Wilkinson power combiner (black line). The results for symmetric ports are omitted.

magnitude values in comparison to the original design with no isolation resistors. In particular, the  $|S_{23}|$  and  $|S_{13}|$  remain below -15 dB, and  $|S_{12}|$  and  $|S_{14}|$  remain below -12 dB and -7 dB, respectively, over the 25–35 GHz band. The relatively high level of  $|S_{14}|$  could be reduced by introducing another resistor between the edge ports. The ideal Wilkinson combiner intrinsically has a good input matching and exhibits excellent isolation properties.

### 3.2 Total Performance in Presence of PAs

In order to evaluate the performance of the power combiners in conjunction with non-identical PAs, a simulation test-bench has been proposed (See Figure 5). It has a single 50- $\Omega$  input port interfaced to an ideal 1:4 power splitter. The power splitter feeds an array of identical common-base PA-modules in SiGe HBT technology [8]. The power amplifiers are power-matched to the 50- $\Omega$  load impedance. In practice, phase variations of the PA gain dominate over amplitude drifts. This effect is emulated by four independent phase shifters with normally distributed phase values  $\{\phi_n\}_{n=1}^4$ . The normal distribution is defined by the mean value  $\mu = 0^\circ$  and standard deviation  $\sigma = 10^\circ$ . The outputs of the PAs are interfaced to the matched

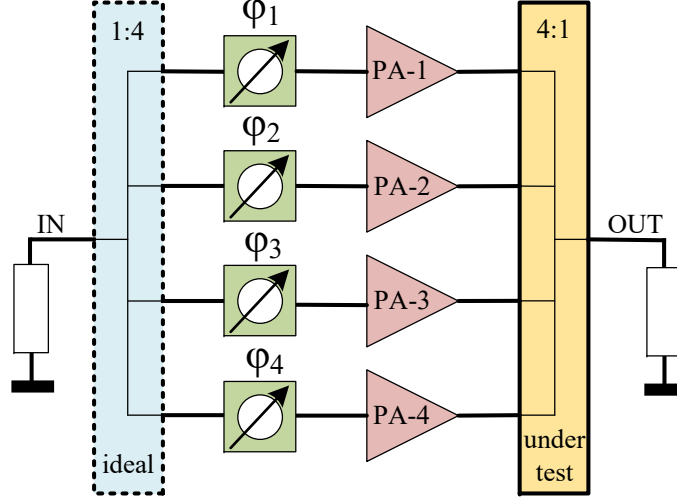


Figure 5: Simulation test-bench for combined PA performance evaluation in the presence of normally distributed phase errors, used for the ideal Wilkinson power combiner and the spatial power combiners w/ and w/o isolation load resistors.

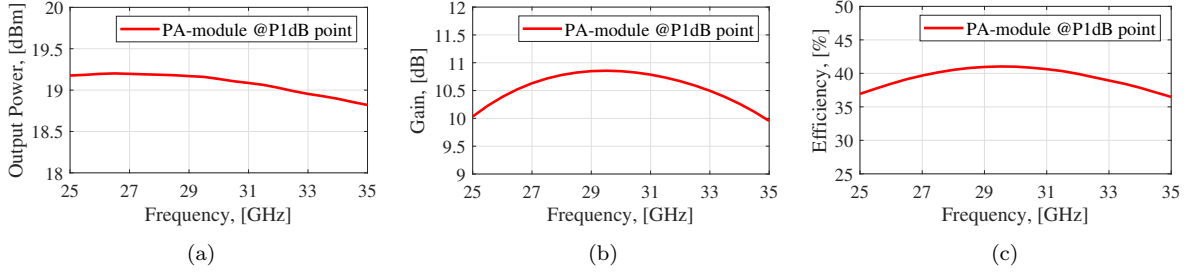


Figure 6: Simulated performance of a single PA-module @P1dB compression point: (a) output power; (b) gain, and; (c) efficiency.

4:1 power combiners as discussed above. The performance of such a joined active structure has been investigated in terms of PA metrics. Figure 6 shows the gain, output power, and efficiency of a single PA at the 1-dB compression point (P1dB) over the 25–35 GHz band. Ideally, the P1dB output power level after combining four PA channels should be 6 dB higher than that of a single PA, whereas the gain and efficiency values should remain the same. However, these performance targets are not feasible for realistic devices where phase variations are not negligible. Figure 7 shows the active reflection coefficients at the SPC input ports for the uniform excitation case. The level of reflections are below  $-25$  dB over the 25–35 GHz band for all combiners, as expected. Figure 8 shows the simulated yield of the combined PAs as obtained with the test-bench in Figure 5. The yield analysis is based on statistical variations of the introduced phase errors  $\{\phi_n\}_{n=1}^4$ . This is needed to determine how

### 3. NUMERICAL VALIDATION RESULTS

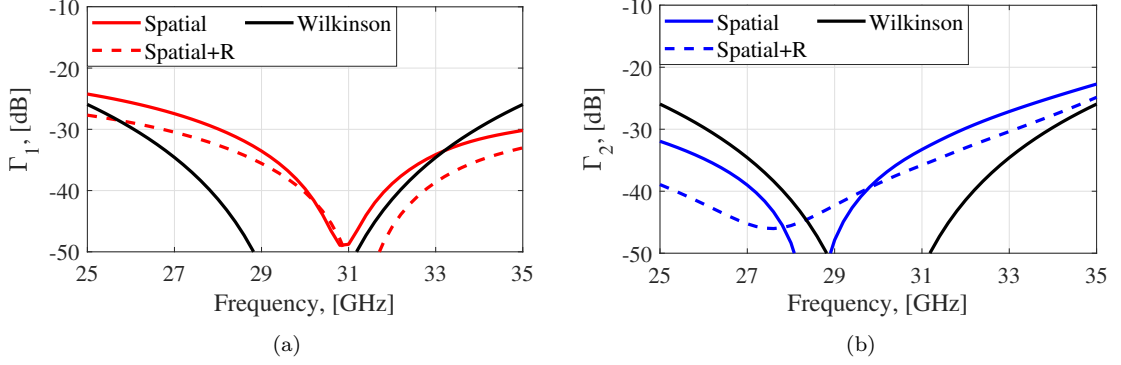


Figure 7: Simulated input port active reflection coefficients (uniform excitation) of the spatial power combiner w/ and w/o isolation load resistors (dashed and solid lines, respectively) and the ideal Wilkinson power combiner (black). The results for symmetric ports are omitted.

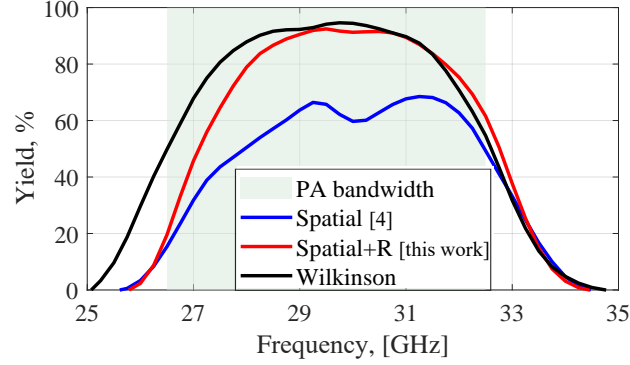


Figure 8: Performance yield of the PAs in conjunction with the spatial power combiner w/ and w/o isolation load resistors (red and blue lines, respectively) and an ideal Wilkinson power combiner (black line) in the presence of normally distributed phase errors with  $\sigma = 10^\circ$ . Positive performance yield if @P1dB, Gain  $\geq 10.5$  dB, Power  $\geq 24.5$  dB, Efficiency  $\geq 35\%$ .

many possible phase combinations satisfy the following performance specifications which be met simultaneously:

- Output power<sup>2</sup>  $\geq 24.5$  dBm;
- Gain<sup>1</sup>  $\geq 10.5$  dB;
- Power efficiency<sup>1</sup>  $\geq 35\%$ .

The colored region in Figure 8 shows the operating bandwidth of a single PA-module, where the desired specifications could be potentially satisfied. It is seen that more than 90 % and 80 % of the realizations satisfy the desired specifications over the 29–31 GHz and the 28–32 GHz bands, respectively. It confirms that the proposed spatial power combiner with isolation load resistors is a good alternative to the conventional Wilkinson power combiner in terms of a low sensitivity to a non-uniform excitation.

<sup>2</sup> Performance is at 1-dB compression point.

## 4 Conclusion

A low-loss spatial power combiner with enhanced port-isolation properties has been optimized and examined. It avoids the use of a lossy on-chip circuit-level power combiner while enabling the direct integration of an antenna element. The isolation load resistors allow reducing the coupling effects between PA channels, without increasing the losses in the case of a uniform excitation. The power combining performance in the presence of a non-uniform excitation caused by non-incidental PAs has been statistically analyzed. Simulations show that the proposed solution allows to significantly reduce the negative impact of a non-uniform excitation on the overall output power, gain, and power efficiency at the 1-dB compression point.

The concept is expected to play an important role in high-power MMICs, where both low insertion losses and optimal active device load matching are important requirements.

## Acknowledgment

The work is a part of the Silicon-based Ka-band massive MIMO antenna systems for new telecommunication services (SILIKA) project, funded by the EU's Horizon 2020 under the Marie Skłodowska Curie grant agreement #721732.

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## A Wideband and Low-Loss Spatial Power Combining Module for mm-Wave High-Power Amplifiers

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# A Wideband and Low-Loss Spatial Power Combining Module for mm-Wave High-Power Amplifiers

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and Marianna Ivashina

## Abstract

We present a low-loss power combiner, providing a highly integrated interface from an array of mm-wave power amplifiers (PAs) to a single standard rectangular waveguide (WG). The PAs are connected to an array of parallel and strongly coupled microstrip lines that excite a substrate integrated waveguide (SIW) based cavity. The spatially distributed modes then couple from the cavity to the rectangular WG mode through an etched aperture and two stepped ridges embedded in the WG flange. A new co-design procedure for the PA-integrated power combining module is presented that targets optimal system-level performance: output power, efficiency, linearity. A commercial SiGe quad-channel configurable transmitter and a standard gain horn antenna were interfaced to both ends of this module to experimentally demonstrate the proposed power combining concept. Since the combiner input ports are non-isolated, we have investigated the effects of mutual coupling on the transmitter performance by using a realistic PA model. This study has shown acceptable relative phase and amplitude differences between the PAs, *i.e.* within  $\pm 15^\circ$  and  $\pm 1$  dB. The increase of generated output power with respect to a single PA at the 1-dB compression point remains virtually constant (5.5 dB) over a 42% bandwidth. The performed statistical active load variation indicates that the interaction between the PAs through the combiner has negligible effect on the overall linearity. Furthermore, the antenna pattern measured with this combiner shows negligible deformation due to non-identical PAs. This represents experimental prove-of-concept of the proposed spatial power combining module, which can be suitable for applications in MIMO array transmitters with potentially coupled array channels.

## 1 Introduction

Highly integrated millimeter-wave transceivers with high output power and efficiency are of high demand for the next-generation wireless communication systems, imaging,

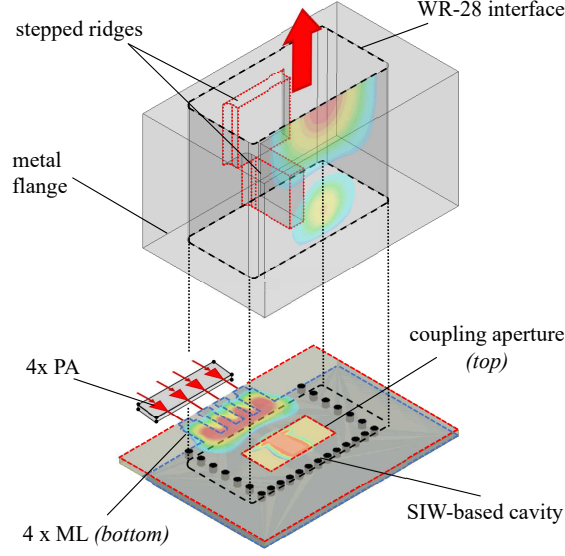


Figure 1: A detailed model of the proposed spatial power combining module. The PAs are interfaced to an SIW-based cavity with a coupling aperture through 4 spatially distributed microstrip lines (MLs) located on the bottom layer. The electric field of the resonant cavity mode is concentrated near the bottom orthogonal ridge and subsequently coupled through the etched rectangular aperture into the metal WR-28 flange with stepped ridges. The  $TE_{10}$  mode propagation inside the WG and direct coupling to the array of MLs are illustrated.

and radar applications. Although III-V compound semiconductors are traditionally used for implementing the mm-wave power amplifiers, silicon is becoming more favorable due to its low cost and high integration capability [1]. However, the typical RF power that needs to be delivered by power amplifiers (PAs) in emerging applications is beyond the current state-of-the-art of silicon devices due to their relatively low breakdown voltage [2]. This problem can be overcome by combining signals from multiple PAs into a single radiating antenna element. However, this approach is not well-suited for IC solutions, since an on-chip combiner as well as an antenna and its interconnecting transition should be low-loss [3–6]. Moreover, losses in conventional circuit power combiners exacerbate if the number of channels increases [7, 8]. This fact limits the feasible combined output power and reduces efficiency. Table 1, which presents state of the art mm-wave integrated power combiners, exemplifies this effect for two CMOS-based combiners with 2 and 4 channels [8–10]. Another challenge is the integration with antenna elements, which are comparable in size to ICs at these frequencies [11–13].

A possible solution towards the efficient wide band high power silicon-based transmitters at mm-wave frequencies is the recently proposed multi-channel transition with spatial power combining functionality [14], where an array of strongly-coupled microstrip lines (MLs) interface a single substrate integrated waveguide (SIW). The corresponding back-to-back configuration is a passive structure, hence, the effects of

Table 1: Comparison between state-of-the-art solutions and proposed design

Reference	Number of channels	Frequency, [GHz]	Bandwidth, [%]	Losses, [dB]
CMOS on-chip [8]	2	22-26	16.7	1.4
CMOS on-chip [9]	2	16-27	51.2	1
CMOS on-chip [10]	2	30-40	29.2	1.7
CMOS on-chip [8]	4	22-26	16.7	2.4
[this work]	4	24.5-37.8	42	0.2
[this work]	8	25.1-36.4	37	0.3

imperfect PAs on the radiation performance of an interconnected antenna element remain to be studied. This study is important to conduct because the MLs are not isolated ( $-8$  dB). The PAs will therefore couple via the common SIW structure. In turn, the input ML active impedances change with the ML excitation. These active input impedances are the load impedances presented to interconnected PAs. The PA output power, efficiency, and non-linear distortion are highly dependent on the load impedance [15]. Consequently, the combined output power is affected by unequal PA signals; any deviation from the optimum PA load impedance leads to an output power and efficiency reduction [16].

Given the above motivation, the novel contributions of the current work are: (i) *a new design procedure* of the spatial power combiner in the presence of the critical effects of power amplifiers in linear and non-linear regimes; (ii) *experimental proof-of-concept* using a commercially available multi-channel PA IC. The key performance metrics are the combined output power, power efficiency, linearity, impedance matching and radiation pattern stability due to unequal PA input signals. This analysis approach allows to determine the requirements for the multi-channel transmitter gain spread in conjunction with the power combining module.

## 2 Design of the Power Combining Module Including the Effects of PAs

Figure 1 shows a detailed model of the designed power combining module, which employs the spatially distributed excitation of the SIW-based cavity modes by an array of, in this case, four coupled MLs. A conventional waveguide interface was used as an output port to demonstrate the power combining performance and to measure the antenna pattern degradation of a standard gain horn in the presence of imperfect PAs and manufacturing tolerances. Furthermore, to integrate a WG interface, the design concept of the  $90^\circ$  bent interface between an SIW-based cavity with etched aperture and a stepped ridge WG has been employed [17]. However,

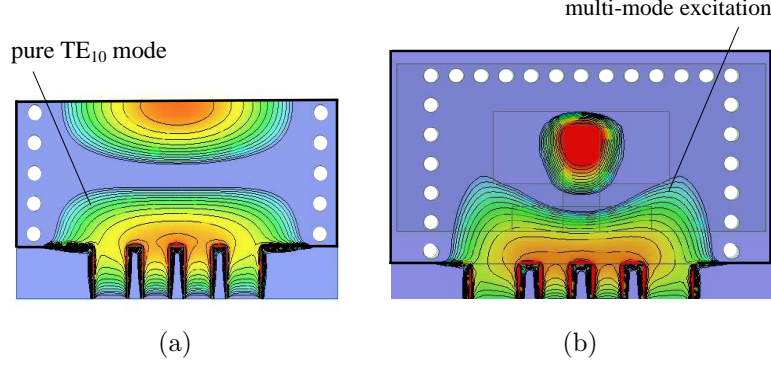


Figure 2: Magnitude of the E-field distribution at 30 GHz inside: (a) a single-mode SIW excited by an array of MLs [14]; (b) over-moded cavity with the open aperture excited by an array of ML.

instead of using the relatively bulky and long multi-section SIW in [17], the desired multi-mode field distribution in the relatively wide SIW cavity is in this case directly created by an array of coupled MLs [14]. The direct multi-mode excitation allows to reduce the size of the transition and hence the losses in comparison with [17]. The consequence is that our transition becomes inseparable and, therefore, must be designed and characterized as a single integrated multi-port unit. In contrast to the previous back-to-back design [14], where four quasi-TEM modes are matched to a single  $TE_{10}$  mode (See Fig. 2 (a)), the present structure has been optimized to directly match the over-moded cavity with an open aperture, as shown in Figure 2 (b). In this case, the electric field of the resonant cavity mode is concentrated near the bottom orthogonal ridge and is coupled through the etched rectangular aperture into the metal WR-28 flange with stepped ridges. Due to the low substrate height and different medium the aperture region becomes very sensitive and hence challenging for assembling. Figure 3 shows the geometry of the designed prototype. The divergent MLs were included in the device under test (DUT) to be able to mount RF connectors to the PCB and to decouple the extended routing of MLs<sup>1</sup>. By exploiting symmetry, a two-port-only calibration kit is sufficient to de-embed most of the effects of the four connectors from the measurement results. The structure employs the RO4350 laminate with thickness 0.254 mm and relative dielectric constant  $\epsilon_r = 3.66$ .

As mentioned above, the output power, efficiency, and non-linear distortion are highly dependent on the PA load impedances [15]. These loads can be represented by active reflection coefficients at the combiner input ports:

$$\Gamma_n = \frac{1}{G_n} \sum_{m=1}^N G_m S_{nm}, \quad (1)$$

<sup>1</sup> The extended microstrip lines and coaxial connectors can, in typical applications, be eliminated by mounting the MMIC directly onto the PCB. Although such a structure will be more compact it will not affect the conclusions of the present study.

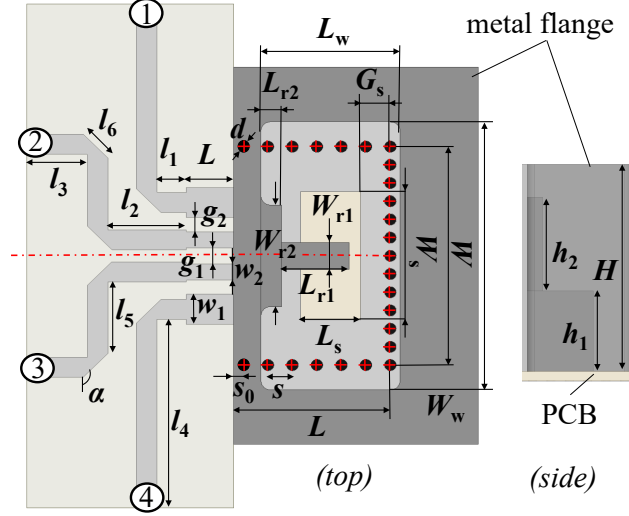


Figure 3: The geometry of proposed DUT including bent divergent routing lines to connectors.

where  $S_{nm}$  is the S-parameter from combiner port  $m$  to  $n$ , while  $G_m = A_m e^{-j\phi_m}$  is the complex gain of the  $m$ -th PA. The active impedances at the combiner input ports are assumed to be optimal for achieving high output power and efficiency in case of identical PAs (uniform excitation). However, in practice, individual PAs can differ due to the different thermal regimes of each PA and/or due to fabrication uncertainties. Therefore, interfacing PAs with varying and non-equal gains ( $G_n \neq G_m | n, m \in \{1 \dots N\}$ ) to a non-isolating combiner ( $S_{nm} | n \neq m \neq 0$ ) affects the active impedances at the combiner input ports, and hence, degrades the individual PA performance. Taking the above effects into account, a more holistic design procedure has been proposed (See Fig. 4). It consists of two design phases: initial passive design phase similar to work [14] and statistical co-optimization, which includes large-signal behavior of coupled realistic PAs. In the first phase, an initial module geometry is created based on the initial system specifications, such as the number of PAs, optimum load impedance, and operation frequency. This geometry is numerically optimized under the condition of uniform excitation to satisfy the initial performance goals: active reflection coefficients and insertion loss levels over a certain frequency bandwidth.

In the second design phase, the initially realized geometry is co-optimized in conjunction with a large-signal PA model. Individual PA gains are statically varied using Monte Carlo method in order to emulate a realistic PA gain spread. The performance of such a joint active structure is evaluated in terms of PA metrics: output power, efficiency, linearity. If the performance targets are satisfied for all possible realizations, the final geometry is obtained. Otherwise, the module geometry needs to be updated. The above procedure also allows one to determine the maximum allowable variation of the PA gains.

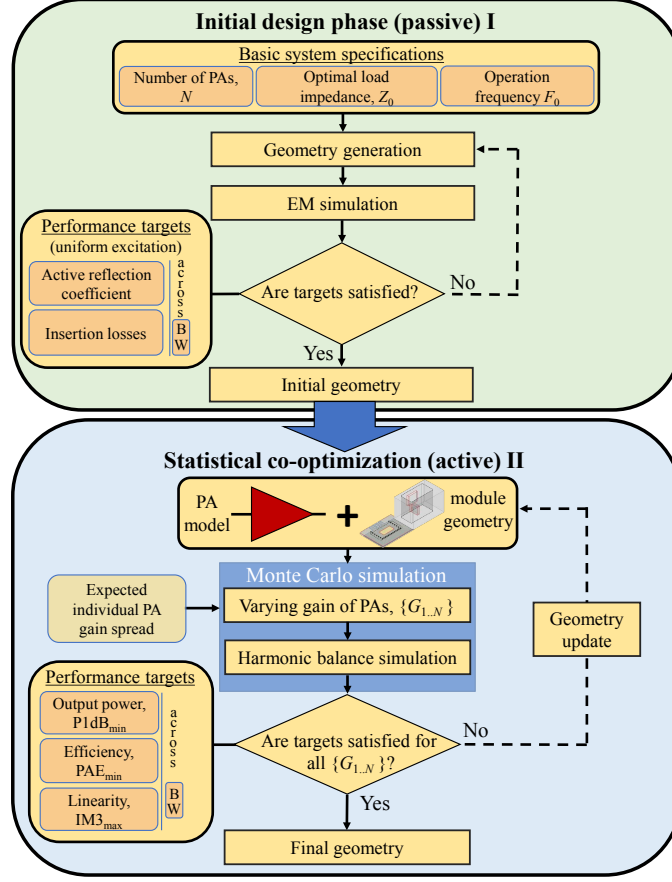


Figure 4: A co-design optimization flow for the spatial power combining module.

In the present design an output stage based on conventional single-ended common-base amplifier has been employed (See Fig. 5). The design is implemented in  $0.25\mu\text{m}$  SiGe:C BiCMOS technology [18], which is also the technology used for the quad channel IC in our experimental verification (*cf.* Section 3). SiGe heterojunction bipolar transistors (HBTs) operated in the common-base configuration are widely used at high frequencies due to the higher maximum available power gain and relatively higher output load compared to the common-emitter configuration [19, 20]. The scale of the HBT has been chosen in such a way to operate near peak current density while remaining in safe operation in terms of electro-thermal breakdown [21]. This resulted in a high-voltage HBT with a  $0.4 \times 25.2 \times 12 \mu\text{m}$  emitter area. A simple biasing network based on the current mirror has been employed,  $I_{dc} = 50 \text{ mA}$  corresponds to the class A/B operation point. In order to improve electrical stability at lower frequencies an additional high-pass shunt RC network ( $20 \Omega$ ,  $1 \text{ pF}$ ) has been used. An output matching circuit based on transmission lines has been used in order to match the output stage to  $50\text{-}\Omega$  load. The capacitor  $C_p = 30 \text{ fF}$  represents a typical parasitic layout capacitance. The load-pull simulations have been performed

## 2. DESIGN OF THE POWER COMBINING MODULE INCLUDING THE EFFECTS...

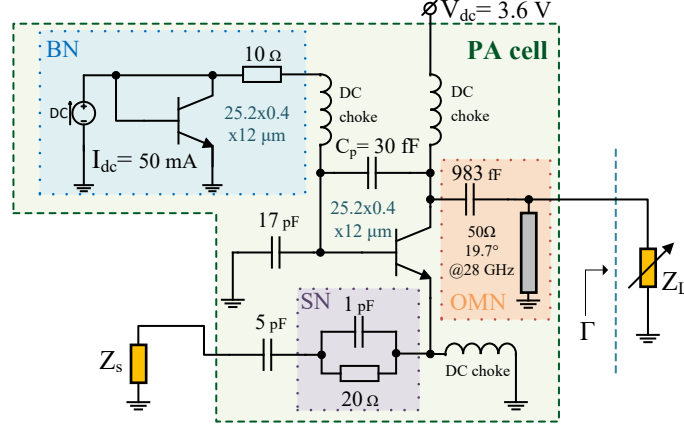


Figure 5: Simulated Class-A single-ended common-base output PA stage in SiGe HBT technology. OMN=output matching network, BN=bias network, SN=stability network. An active load sweep is performed.

in Keysight ADS using a harmonic balance technique. The simulated PA output power at 1-dB compression point (P1dB) reaches the maximum value of 23.5 dBm and remains above 23 dBm over the entire PA operation bandwidth (26.5–29.5 GHz). The corresponding power efficiency at P1dB point is above 35%. The maximum PA gain of 8.5 dB is observed at 28 GHz.

Figure 6 shows the simulated P1dB output power and efficiency contours at 28 GHz in the load reflection coefficient plane. The clusters of points represent  $\Gamma_{1,2}$  of the multi-port power combiner in the presence of normally distributed phase and amplitude deviations representing non-identical PAs with standard deviation,  $\sigma$ , of 1 dB and  $15^\circ$ , respectively. As one can see, most of the active load realizations remain within the region of high efficiency and high output power, although for higher  $\sigma$  the cluster of points is more spread.

Another important performance metric of a PA is its linearity. Nonlinear properties of the PA interconnected to the power combining module have been quantified by performing a two-tone test. The relative magnitude of the output third-order intermodulation (IM3) products has been used as a measure of nonlinearity. The IM3 products are the most critical ones for this design since they appear in the operating frequency range. In the performed test, two spectrally pure tones at frequencies  $f_1$  and  $f_2$  are applied to the PA input port. The tones are centered around the center frequency,  $f_0 = 28$  GHz, and separated by  $\Delta f = 0.1$  GHz, such that  $f_1 = f_0 - \Delta f$  and  $f_2 = f_0 + \Delta f$ . A large input signal drives the PA into its nonlinear operating range. As a result, IM3 products appear in the output signal at frequencies  $2f_1 - f_2$  and  $2f_2 - f_1$ . Figure 7 shows the magnitude of the output IM3 products relative to the corresponding fundamental tones as a function of the two-tone input power for a single PA (curve  $\times 1$ ) and the combined PA ( $\times 4$ ). As expected, operating at higher output power levels leads to a significant increase in the relative magnitude of



IM3 components. Asymmetry of the magnitude of the upper and lower IM3 products is similar for both considered cases and indicates the memory effects in the nonlinear transfer function of the PA. The IM3 curves for the combined PA are 5.5 dB shifted compared to the single PA case whereas their shapes are the same for both configurations. The latter confirms that the module itself has no effect on linearity. However, the output impedance mismatch caused by non-equal PA gains might affect the linearity of the combined PA. Figure 8 shows the relative output IM3 products in the load reflection coefficient plane for a single PA. The testing is carried out at  $f_0 = 28$  GHz with  $\Delta f = 0.1$  GHz,  $P_{\text{in}} = 10$  dBm. The cluster of points represents  $\Gamma_{1,2}$  of the power combining module in the presence of normally distributed phase

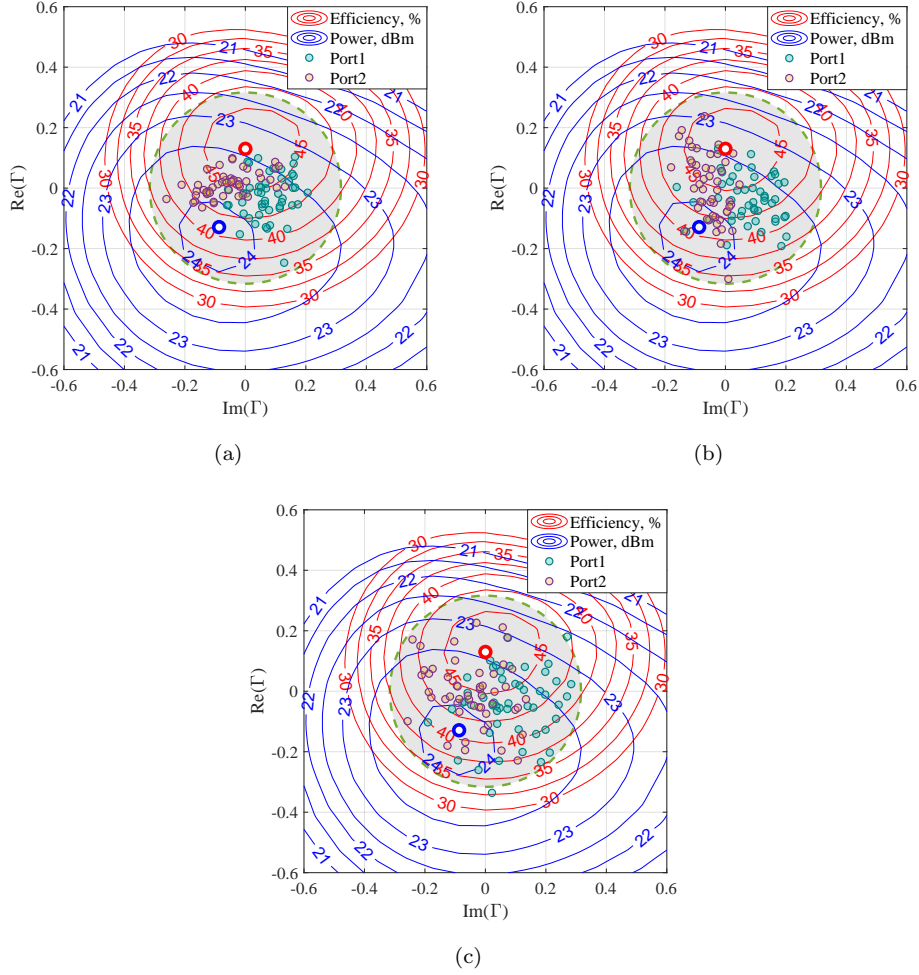


Figure 6: Simulated PA P1dB output power (blue) and efficiency (red) contours at 28 GHz in the load reflection coefficient plane. The cluster of points represent  $\Gamma_{1,2}$  of the power combining module in the presence of normally distributed: (a) Phase errors with  $\mu = 0^\circ$  and  $\sigma = 15^\circ$ ; (b) Amplitude errors with  $\mu = 0$  dB and  $\sigma = 1$  dB; (c) Both amplitude and phase errors. The colored regions indicate  $|\Gamma_{1,2}| \leq -10$  dB.

## 2. DESIGN OF THE POWER COMBINING MODULE INCLUDING THE EFFECTS...

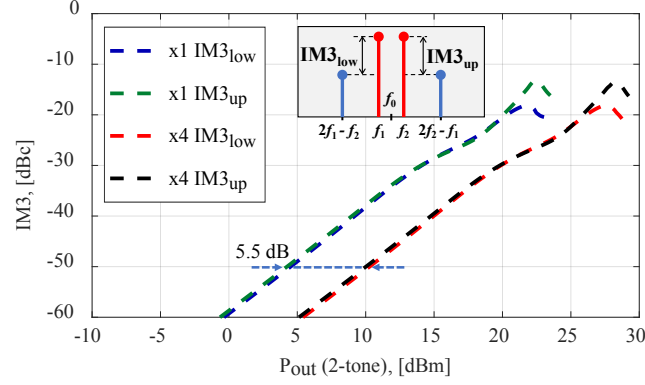


Figure 7: Simulated output third-order intermodulation products relative to the corresponding fundamental tones as a function of the two-tone output power in case of a single PA ( $\times 1$ ) and the combined PA ( $\times 4$ ). The testing was carried out at  $f_0 = 28$  GHz with two-tone spacing of  $\Delta f = 0.1$  GHz.

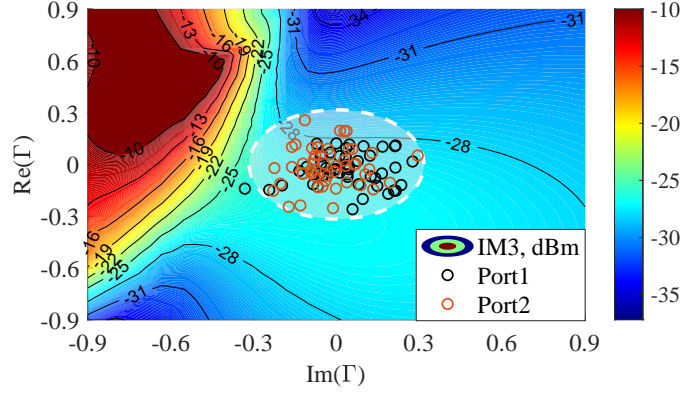


Figure 8: The output third-order intermodulation product relative to the fundamental tone in the load reflection coefficient plane. The testing was carried out at  $f_0 = 28$  GHz with two-tone spacing of  $\Delta f = 0.1$  GHz,  $P_{in} = 10$  dBm. The cluster of points represent  $\Gamma_{1,2}$  of the power combining module in presence of normally distributed phase and amplitude deviations with  $\sigma = 1$  dB and  $15^\circ$  respectively. The colored regions indicate  $|\Gamma_{1,2}| \leq -10$  dB.

and amplitude with standard deviation,  $\sigma$ , of 1 dB and  $15^\circ$ , respectively. As one can see, most of the active load realizations correspond to the same relative IM3 level ( $-28$  dBc), which indicates a negligible effect of the load mismatch on the combined PA linearity. The conclusions are the same for different input power levels,  $P_{in}$ , and these results have therefore been omitted. A combined PA could be considered as a single unit with a nonlinear transfer function. Therefore, conventional techniques such as feedback, feed forward, analog and digital pre-distortion are applicable for its linearization [22].

This study has been used to determine the PA requirements in terms of the maximum allowable relative difference of the phase and amplitude. The results show that good performance (relative output power reduction  $\leq 1$  dB) can be expected

Table 2: The optimum design parameters, as shown in Figure 3.

$L_w$	$W_w$	$G_s$	$L_s$	$W_s$	$W_{r1}$	$L_{r1}$	$W_{r2}$	$L_{r2}$	$H$
3.56	7.11	0.77	1.53	3.40	0.71	1.72	2.69	0.53	6.00
$w_1$	$w_2$	$g_1$	$g_2$	$s_0$	$s$	$d$	$W$	$h_1$	$L$
0.79	0.43	0.42	0.38	0.25	0.63	0.3	5.79	2.32	1.21
$l_1$	$l_2$	$l_3$	$l_4$	$l_5$	$l_6$	$\alpha$	$h_2$		
0.74	2.00	1.54	5.00	1.9	0.63	135°	2.71		

as long as PA gain variations remain within  $\pm 15^\circ$  for the phase and  $\pm 1$  dB for the amplitude. The corresponding optimum combiner design parameters (in mm) are shown in Table 2.

A non-uniform input port excitation also causes the higher-order modes in the SIW-based cavity to be excited with different amplitudes. Higher-order modes at the antenna side of the discontinuity radiate out directly if these are propagating modes and thus affect the radiation pattern shape when excited strongly. If higher-order modes are evanescent, they will store different amounts of reactive energy at the transition depending upon their excitation, which in turn affects the PA matching as well as the PA gain, efficiency and output power, also for the dominant propagating mode. The latter effect is already modeled by the existing dominant mode S-parameter matrix. Finally, the amplitude level of the higher-order evanescent modes could still be significant in the closely located output port. Interfacing a radiation element supporting the propagation of higher-order modes to such a port might degrade the radiation pattern shape. Thus it is important to investigate the aperture modal content and their excitation profile in the presence of a non-uniform excitation.

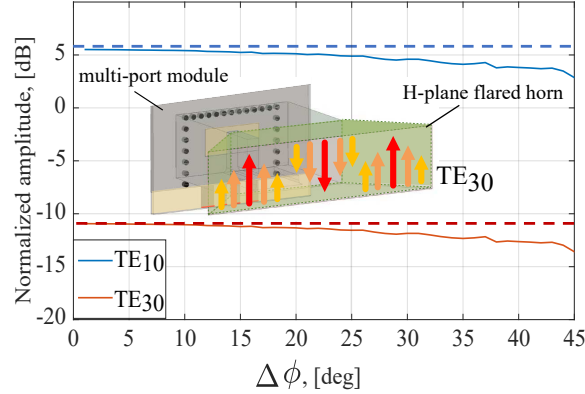


Figure 9: Simulated amplitudes of the propagating  $TE_{10}$  (blue) and  $TE_{30}$  (red) modes in the aperture of a H-plane flared horn with multi-port excitation in the presence of randomly distributed phase errors with maximum deviation  $\Delta\phi$ . The realizations corresponding the lowest  $TE_{10}$  amplitude are given for each  $\Delta\phi$ . Dashed lines show corresponding mode levels in case of a single-mode wave-port excitation at the horn base.

An H-plane flared horn supporting the propagation of  $TE_{10}$ - $TE_{30}$  modes has been simulated in conjunction with the proposed power combining module in the presence of randomly distributed phase errors with maximum deviation  $\Delta\phi$  at 30 GHz (See Fig. 9). The realizations corresponding to the lowest  $TE_{10}$  amplitude (worst-case scenario) are given for each  $\Delta\phi$ . Dashed lines show corresponding mode levels in the case of a single wave-port excitation. Due to the symmetry of the structure, the  $TE_{20}$  mode level is negligible and this result has therefore been omitted. As one can see, increasing  $\Delta\phi$  does not increase the  $TE_{30}$  mode level, in fact, the relative level to that of the main  $TE_{10}$  mode remains the same. Consequently, the total aperture field distribution is not a function of  $\Delta\phi$ , which confirms the pattern shape sustainability over a range of phase excitations.

### 3 Measurement Results

The designed passive prototype has four 50- $\Omega$  coaxial ports for testing with a standard VNA and a single WR-28 antenna interface (See the photos in Fig. 10). The prototype is formed by stacking a standard double-sided PCB on the aluminium WG flange, which contains embedded ridges. As discussed in the previous section, the region between the etched aperture and the bottom ridge is very sensitive to fabrication tolerances, and an extra adjustment element was, therefore, developed. It constitutes a movable metal plate with a trimming screw, which can be used to control pressure contact between the PCB and the aluminium flange. The top side of the flange has a standard WR-28 interface, which can also be used as an open-ended WG radiating element. The stack has an overall size of approximately  $46 \times 46 \times 6$  mm.

#### 3.1 Input Impedance Matching

The measured and simulated WR-28 port reflection coefficients are shown in Figure 11 with the 50- $\Omega$  terminated coaxial ports. It is seen that  $S_{55}^{WR-28} < -14$  dB from 24.5–

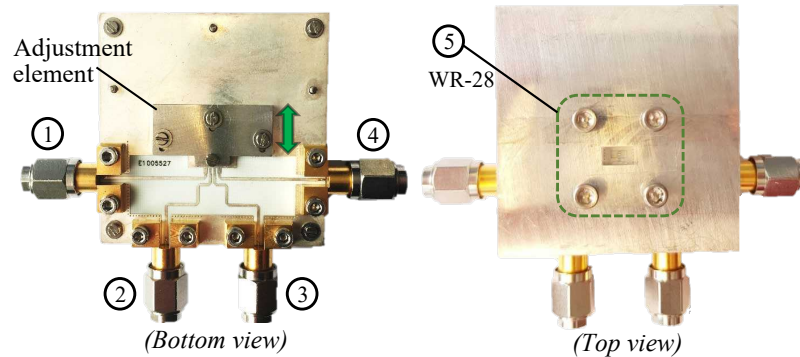


Figure 10: Fabricated spatial power combining module prototype.

37.8 GHz. The measured active reflection coefficients of the symmetric 50- $\Omega$  ports are shown in Figure 12. The active reflection coefficients are calculated from the measured  $5 \times 5$  S-matrix assuming the uniform excitation scenario. The obtained  $|\Gamma_1|$  and  $|\Gamma_2| < -13$  dB in the desired frequency range, and remain  $< -10$  dB for frequencies in the range 24.5–37.8 GHz. This corresponds to a 42% bandwidth. All curves are close to each other and in good agreement with the simulations shown by black dashed lines. Visible ripples are attributed to the connector interfaces and bent MLs, which cannot be completely de-embedded by the designed two-port TRL calibration kit, since the ports are slightly different in practice. The measured and simulated WR-28 port reflection coefficients do not exceed  $-15$  dB and  $-20$  dB, respectively. The observed difference between measurements and simulations is mainly attributed to the connector interfaces and bent MLs which cannot be completely de-embedded by the designed two-port ML TRL calibration kit, since in practice the ports are slightly different. Figure 12 (b) shows the coupling coefficients between the 50- $\Omega$  input ports. As one can see, the coupling between the edge ports ( $|S_{14}|$ ) reaches  $-7$  dB level, whereas the coupling between port 1 and port 3 ( $|S_{13}|$ ) is below  $-14$  dB over the entire PA operation frequency range. The relatively high  $|S_{14}|$  does not significantly affects the individual PA performance (*cf* Section 2) and mainly attributes to the coupling between the ports within SIW modes.

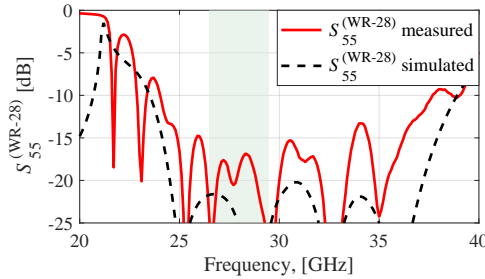


Figure 11: Measured (solid) and simulated (dashed) reflection coefficient of WR-28 port (coaxial ports are terminated), as shown in Fig. 10. The colored region shows the operation band of PAs.

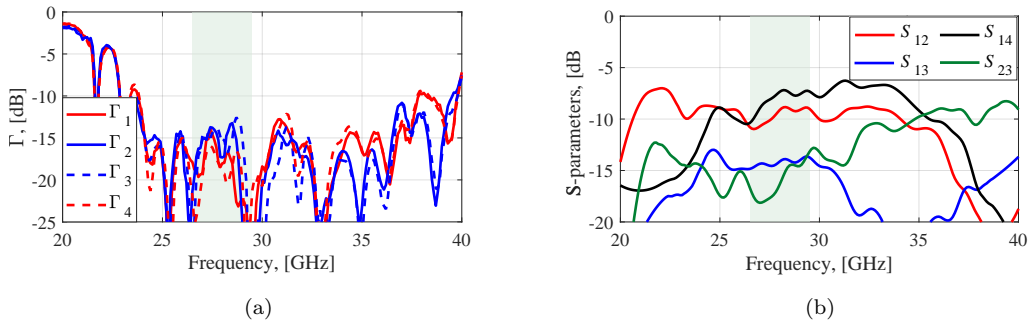


Figure 12: Measured: (a) Active reflection coefficients of the 50- $\Omega$  microstrip ports of the prototype (including effect of connectors), as shown in Fig. 10 (WR-28 port is terminated); (b) Mutual coupling coefficients between the input ports. The colored region shows the operation band of PAs.

### 3.2 Radiation Pattern

The radiation performance has been investigated in conjunction with a standard gain horn antenna at the desired frequency range.

Figure 13 shows the measured H-plane radiation pattern at 28 GHz that was obtained by combining four embedded element patterns, each of which corresponds to the excitation of one port while terminating the others. As one can see, the relative difference between the measured patterns with the single port and multi-port feeding is negligible ( $< -35$  dB within the angular region of  $\pm 20^\circ$ ). This difference is comparable with a relative measurement uncertainty, which increases to  $-20$  dB at larger angles. This fact confirms a good rejection of higher-order propagating modes that, in general, can be excited through asymmetric feeding. The conclusions are the same for the E-plane patterns and these results have therefore been omitted.

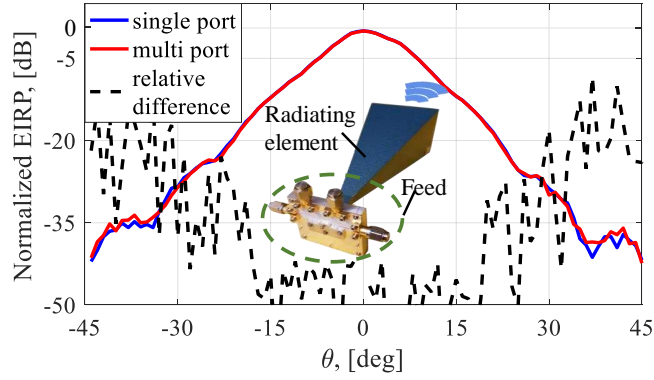


Figure 13: Measured H-plane normalized EIRP pattern of the standard gain horn antenna connected to the proposed spatial power combining module (red) and conventional probe-type feed (blue) at 28 GHz. The relative difference is shown by the black dashed line.

### 3.3 Power Combining

In order to demonstrate the proposed concept in the presence of the critical effects of realistic power amplifiers, the fabricated power combining module has been interfaced to Class-A/B PAs. The PAs are integrated as a part of a quad-channel beamforming SiGe HBT IC [23], as shown in Figure 14. The beamforming IC has one input and four output RF branches operating in the 26.5–29.5 GHz frequency band.

The beamforming IC input and output ports have a  $50\text{-}\Omega$  nominal impedance. The beamforming IC on the evaluation board has been connected to the multi-port combiner by four short coaxial cables. Such connection allows for an extra flexibility during the calibration and measurements. In practical applications the IC can be directly mounted on the same PCB without any cables and routing lines. The gain and phase of each branch can be controlled via a digital interface using a proprietary

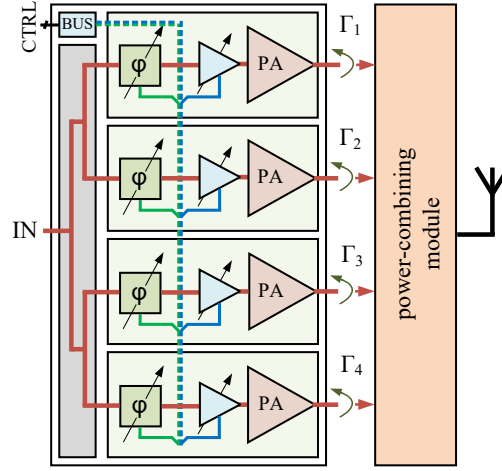


Figure 14: Architecture of the quad-channel beamforming SiGe HBT IC in connection with power combining module.

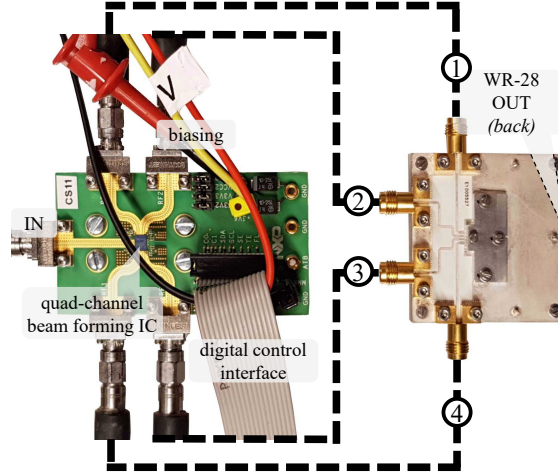


Figure 15: Measurement setup for evaluating the power combining module in conjunction with PAs (vector network analyzer and cables are not shown).

protocol. The phase and amplitude values have a 6-bit range, which results in  $\pm 5.6^\circ$  and 0.5 dB resolution for the phase and amplitude respectively. This ability has been used to compensate for various lengths of cables between the beamforming IC board and the power combiner. It allows driving the proposed structure with a calibrated equal amplitude and phase distribution, but also to examine the effect of amplitude and phase variations. The efficiency of PAs cannot be measured since the beamformer IC does not have separate biasing pins for the output stage. Figure 15 illustrates the measurement setup.

Figure 16 shows the relative increase of the generated output power of the  $4 \times \text{PA}$  combined by the proposed module with respect to a single PA over the 24–31 GHz



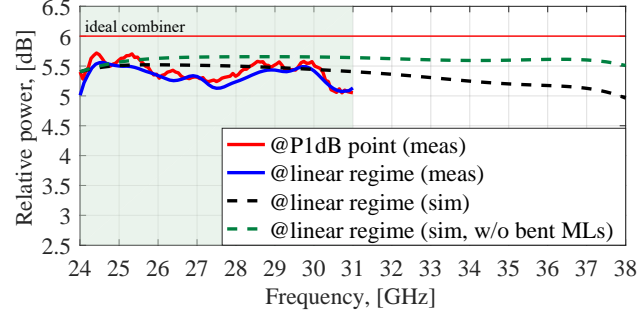


Figure 16: Simulated (dashed) and measured (solid) relative increase of the generated output power of the 4×PA combined by the proposed module, as shown Fig. 3, with respect to a single PA in nonlinear (P1dB point) and linear regime. The colored region shows the operation band of PAs.

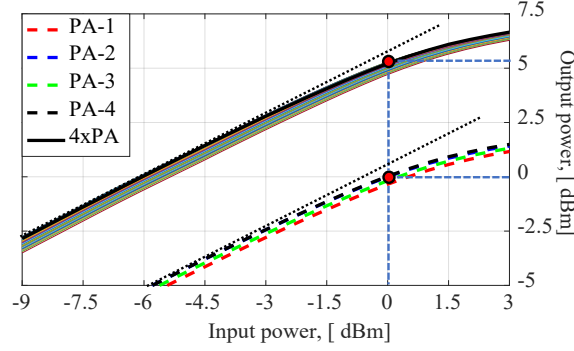


Figure 17: Normalized measured output power versus input power for single PAs (dashed) and after combination with proposed module (solid) at 28 GHz. The set of curves shows measured performance reduction in the presence of  $\pm 15^\circ$  phase variation.

frequency range for different PA operational regimes. The measured results are compared to the EM simulated model, which accounts for dielectric losses. The measured result in the linear regime is close to the simulation, however, the average level is a bit lower due to the losses in the extended routing of the MLs. The dielectric and radiation losses have been estimated based on the HFSS simulated data. At 30 GHz, the total simulated losses of the DUT are 0.55 dB, where the contribution of dielectric and radiation losses are 0.19 and 0.36 dB, respectively. Radiation losses are dominant and attributed to the bent MLs, but these can be eliminated through direct MMIC interfacing. The overall expected losses of the proposed spatial power combining module without extended routing lines do not exceed 0.3 dB. Since we are using a parallel power combiner, the losses do not significantly increase with the number of added amplifiers, in contrast to conventional on-chip power combining techniques (See Table 1). There is no considerable difference between the measured relative power increase in the linear and nonlinear regime.

Also, there is a slightly higher (0.3 dB) relative power increase in the nonlinear regime at some frequency points. This is due to the PA dissimilarities, which have



not been compensated for in the measurements. Hence, the spatial power combining module does not affect the PA performance over the whole input power range.

Figure 17 shows the measured combined power compared to the output power of each PA versus input power. The input and output powers were normalized to obtain 0 dB gain at the P1dB point. The nonlinear behaviour of the joint PA and power combining module is similar to a single PA. The performance reduction in the presence of phase deviations has been investigated by manually adjusting the phase shift for each beamformer IC branch. The measured set of curves (semitransparent) correspond to  $\pm 15^\circ$  phase variation. As one can see, in the worst scenario the output power decrease is less than 1 dB, which is in good agreement with simulations (See Fig. 6).

## 4 Conclusion

The joint optimization procedure of a spatial power combining module has been proposed and proven necessary to account for the critical effects of coupled PAs and to ultimately improve the large-signal performance of the combined PA. A class-A single-ended common-base output PA stage in SiGe HBT technology has been employed in the present design. The developed power combining module facilitates efficient mm-wave power generation over 42% bandwidth (24.5–37.8 GHz) where the total power loss due to this module is  $\leq 0.5$  dB in simulations and  $\leq 0.7$  dB in measurements. The performed statistical study shows that good performance (relative output power reduction  $\leq 1$  dB) can be expected as long as PA gain variations remain within  $\pm 15^\circ$  for the phase and  $\pm 1$  dB for the amplitude. The corresponding output impedance mismatch caused by non-equal PA gains has a negligible effect on linearity of the combined PA.

To the authors best knowledge, this is the first experimental demonstration of a compact parallel power combiner with optimal excitation of the SIW-based cavity modes through strongly-coupled microstrip lines. The increase of the total generated output power in the nonlinear regime of PAs @P1dB remains virtually constant (5.5 dB for  $4 \times \text{PA}$ ). The over-the-air tests confirm that the antenna pattern shape is stable with negligible degradation effects due to multi-port excitation. The low loss and wideband properties of the proposed solution is expected to play an important role in efficient high power wideband mm-wave transmitters.

## Acknowledgment

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# **A wideband mm-Wave Watt-level spatial power-combined power amplifier with 26% PAE in SiGe BiCMOS technology**

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# A wideband mm-Wave Watt-level spatial power-combined power amplifier with 26% PAE in SiGe BiCMOS technology

A. Roev, J. Qureshi, M. Geurts, R. Maaskant, M. Matters-Kammerer, and M. Ivashina

## Abstract

We present a wideband Watt-level power amplifier (PA) for Ka-band designed and implemented in 0.25  $\mu\text{m}$  SiGe:C BiCMOS technology. The core of the design is a chip with multiple custom PA unit cells, which are interfaced with a power combiner placed on a laminate. The power combiner is based on a principle of the recently proposed multichannel transition with spatial power combining functionality, where an array of strongly coupled microstrip lines interfaces a single substrate integrated waveguide. The custom-designed PA unit cell is a differential cascode amplifier, which has a wideband performance (23 – 34 GHz) with both high efficiency (30%) and high output power (24.9 dBm). The realized Watt-level PA combining four PA unit cells achieves a saturated output power of 30.8 dBm with 26.7% power-added efficiency. This combination of the high efficiency and high output power over a wide frequency band (30%) is an advantageous property of the proposed solution with respect to the previously published designs. The achieved high performance is the result of using the proposed architecture with low-loss (0.6 dB) and wideband (54%) parallel spatial power combiner. Moreover, the proposed joint EM-circuit-thermal optimization allows achieving optimal system-level performance by taking into account the effects of mutual coupling between closely spaced PA-cells, distributed DC feeding lines, and interconnections to laminate. In addition, a multiphysics approach used in the design flow allows mitigating the thermal issues caused by a high power density in a relatively small chip. This article describes the design and performance of the whole integrated structure and its individual components.

## 1 Introduction

The next-generation wireless communication systems, imaging, and radar applications demand integrated transmitters with high output power and efficiency at



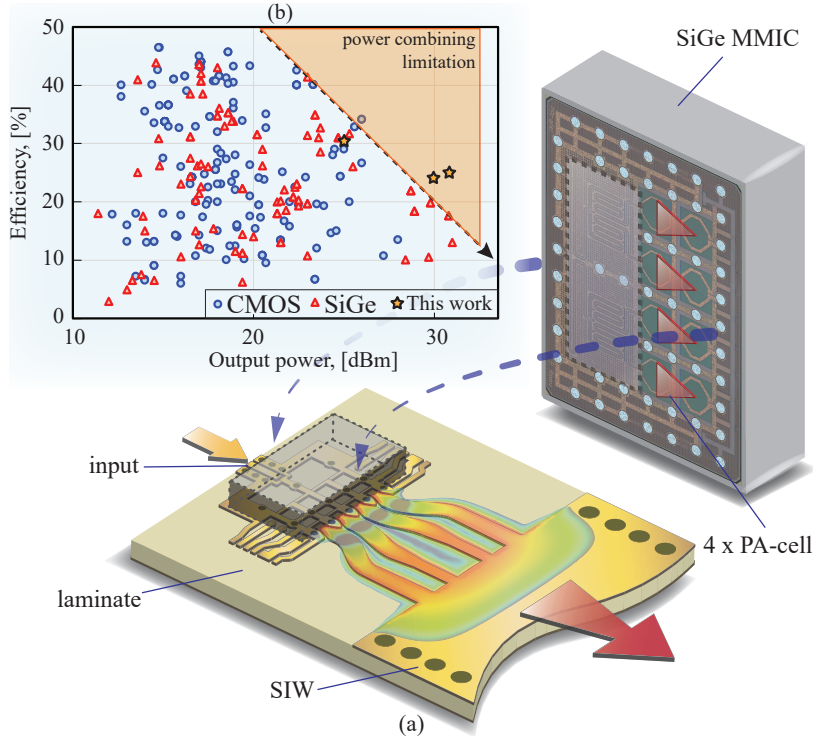


Figure 1: (a) An illustration of the designed spatial power-combined PA. The chip with  $4 \times$  PA-cells is flip-chip interconnected to a substrate integrated waveguide (SIW) placed on the laminate. The direct coupling of 4 distributed PAs to the  $TE_{10}$  mode and its propagation inside the SIW are illustrated. (b) The obtained performance is compared with reported mm-Wave Si-based PAs employing various on-chip combining solutions [3].

millimeter-wave (mm-Wave) frequencies. Despite the obvious advantage of a wide available spectrum, using mm-Wave bands is accompanied by many technological challenges. Mainly, this is due to the increased propagation and material loss, as well as limitations of the existing semiconductors, which deliver less power at these frequencies [1]. Although III-V compound semiconductors are traditionally used for implementing mm-Wave power amplifiers (PAs), silicon is becoming more favorable due to its low cost and high integration capabilities [2]. However, the relatively low breakdown voltage of silicon devices does not allow one to directly generate high RF power as required in the emerging future applications. The latter could be partly overcome by combining the power of multiple active devices. Unfortunately, conventional on-chip power combining networks have inherently high insertion losses at mm-Wave frequencies, which significantly increase with the number of interconnected devices. This fact limits the maximum potentially achievable combined output power and reduces efficiency of PAs [4–6], as shown in Fig. 1.

In this work, an efficient, parallel spatial power combining of an array of four custom SiGe PA unit cells integrated on the same chip is employed to realize a wideband Watt-level PA (See Fig. 1). The chip has a single input and multiple (4 in

the present example) outputs, which are interfaced with a power combiner placed on a laminate. The power combiner is based on the principle of the recently proposed multichannel transition with spatial power combining functionality [7], where an array of strongly-coupled microstrip lines (MLs) interfaces a single substrate integrated waveguide (SIW). This allows for the direct excitation of waveguide modes with high power, and hence, realizes a desired spatial power combining functionality, which obviates the need for potentially lossy on-chip power combiners. A tapered ML transition is used on the other side of the combiner to make the output interface suitable for conventional ground-signal-ground RF measurement probes. In practical applications, the design will include an SIW-based antenna element [8–10], and the tapered ML transition will be removed.

Currently, there are no commercially available chips suitable for the proposed architecture. Therefore, the chip containing the custom high-power PA unit cells is designed and implemented in 0.25  $\mu\text{m}$  SiGe:C BiCMOS technology. The PA unit cell is a differential cascode amplifier, which has a single-ended 50- $\Omega$  input and output.

This paper describes the design of the combined PA using a non-conventional EM-circuit-thermal optimization flow, which allows achieving optimal system-level performance. The performance of the combined PA and its individual components is presented with respect to the existing Si-based Ka-band PAs, where lossy on-chip power combining solutions are used. The main performance goal is high output power in combination with high efficiency over the wide frequency band.

## 2 Design Flow

In contrast to conventional stand-alone system-on-chip solutions, the proposed integrated structure has a relatively high design complexity caused by various multi-physics effects related to:

- Mutual coupling between closely spaced PA-cells;
- DC routing lines and distributed ground topology;
- Imperfect flip-chip interconnections;
- Presence of underfill and solder mask;
- Excessive heat generation from a relatively small die.

Ignoring these effects prevents the linear scaling of output power with the number of PA-cells and, as a result, leads to a reduction of efficiency.

In order to take the above effects into account, a more holistic multiphysics design flow has been proposed. It consists of two design phases: *initial design phase*, where the PA-cell and power combiner are designed separately from one another, and *joint*

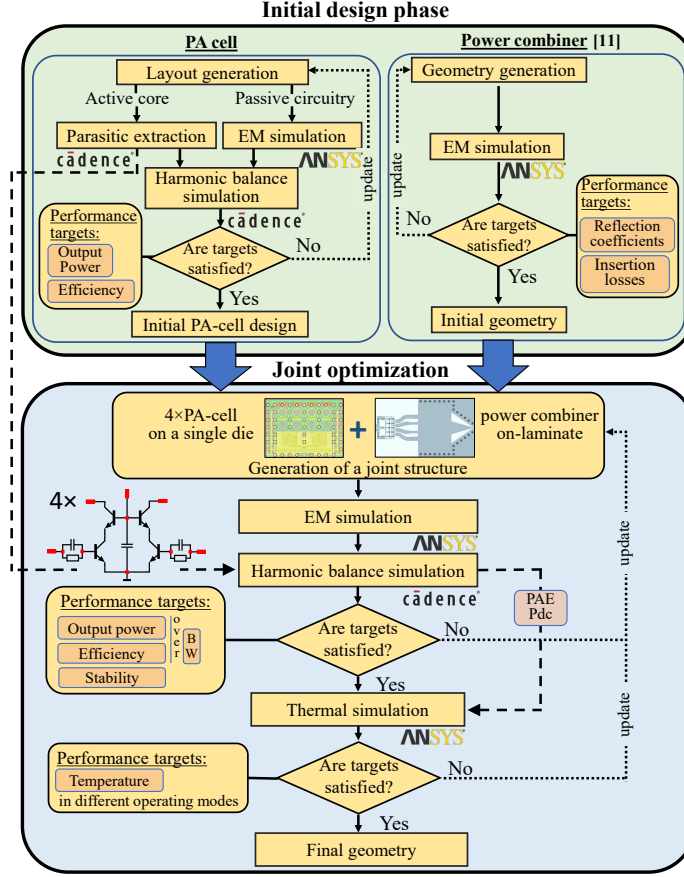


Figure 2: A multiphysics design flow for a mmWave SiGe spatial power-combined PA.

*EM-circuit-thermal optimization*, which allows achieving the optimal system-level performance of the combined PA in terms of power-added efficiency (PAE) and saturated output power ( $P_{\text{sat}}$ ) while mitigating the thermal issues caused by a high power density in the relatively small chip. In the initial design phase, the non-isolating combiner has been optimized to realize an optimal active impedance matching under the condition of uniform excitation (identical PA-cells). This optimization problem has been described in [11]. The key optimization targets are low active reflection coefficients of the input ports and low insertion losses. Therefore, the present work is focused on the joint optimization as well as the stand-alone PA-cell design. The corresponding design phases are discussed in detail in the following sections.

### 3 Power Amplifier Unit Cell

As mentioned before, commercial chips with the proposed architecture do not exist. Moreover, most reported single PA designs implemented in Si-based processes at these frequencies either have low output power ( $\leq 15$  dBm) [12–14] or include

lossy power combiners, which dramatically reduce efficiency and limit the operation bandwidth [15, 16]. Therefore, an essential next step towards the implementation of the proposed architecture is to design a wideband and high-power PA unit cell. The main performance targets are:

- High saturated output power ( $\geq 24$  dBm);
- High power-added efficiency ( $\geq 25\%$ );
- Wide gain bandwidth ( $\geq 35\%$ );
- Compact size ( $\leq 0.5 \times 0.5$  mm).

The latter allows one to fit more PA unit cells on the same chip, and hence, to increase the output power.

### 3.1 Circuit Design

The PA unit cell is a differential cascode amplifier [17], which has single-ended 50- $\Omega$  input and output, as shown in Figure 3. The common-base (CB) device is formed by a parallel connection of three high-voltage heterojunction bipolar transistors, each of which has three emitters. It allows to increase the output current, and thus output power. The total CB emitter area is  $9 \times 0.4 \times 25.2 \mu\text{m}^2$ . The common-emitter (CE) device is a low-voltage transistor, which optimal current density corresponding to the peak  $f_t$  is three times higher as compared to high-voltage devices of the used technology [18]. Therefore, since both types of devices share a common collector current in the employed cascode configuration, the emitter area of the low-voltage CE device is three times smaller.

A simple biasing network based on the current mirror has been employed (See Fig. 3 (b)), where the fixed reference current corresponds to the class A/B operation point. The default biasing settings:  $V_{\text{main}} = 5$  V,  $V_b = 2.5$  V,  $V_{\text{cas}} = 1.5$  V. In order to improve electrical stability at lower frequencies an additional high-pass shunt RC ( $R_s = 8 \Omega$ ,  $C_s = 1$  pF) network has been used.

Stacked Marshand baluns based on coupled TLs are used to convert a single-ended signal to differential, and vice versa [19, 20]. The output balun also performs an impedance transformation in order to match the relatively low PA unit cell optimal load impedance to 50- $\Omega$ . Based on the performed load-pull simulations (See Figure 4 (a)), the designed differential cascode stage has an optimal differential load represented by a parallel connection of  $C_L = -90$  fF and  $R_L = 70 \Omega$ . This equivalent load allows for achieving both high output power ( $\geq 23.8$  dBm) and efficiency ( $\geq 39\%$ ) over the wide frequency range ( $> 50\%$ ). Figure 4 (b) shows the simulated load-pull contours of the complete PA-cell with single-ended 50- $\Omega$  load. As one can see, the obtained peak values of the output power and PAE are reduced by 1.1 dB and 9%,

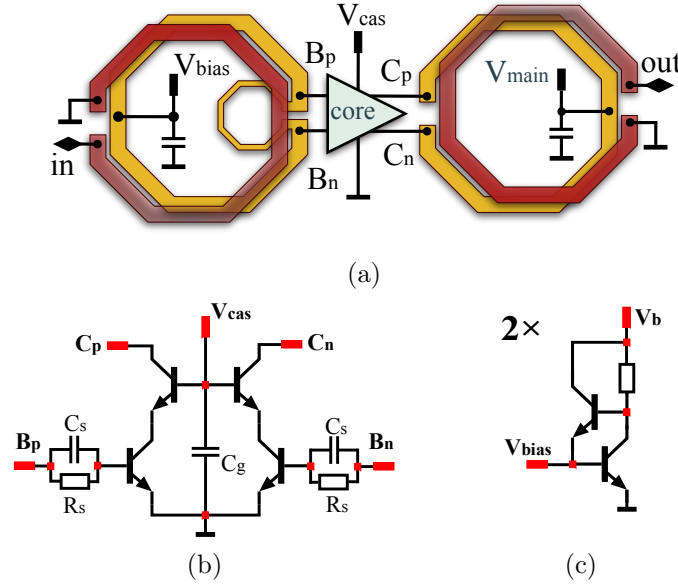


Figure 3: The PA unit cell design: (a) The block diagram of unit cell including input/output baluns configurations; (b) Differential cascode PA circuit diagram; (c) The biasing network circuit diagram.

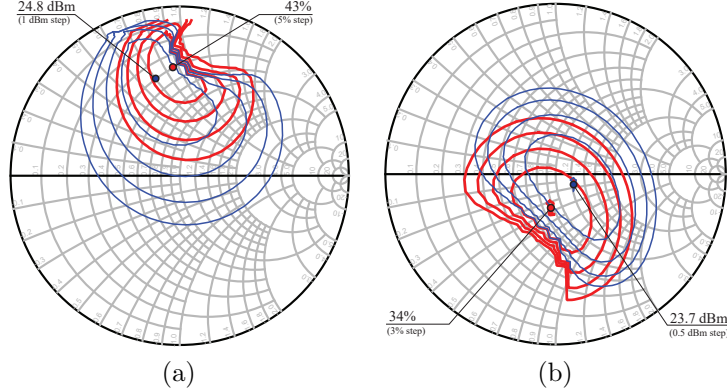


Figure 4: Simulated load-pull contours of PAE (red) and P1dB output power (blue) at 30 GHz: (a) PA-cell core with differential load; (b) complete PA-cell with single-ended 50-Ω load.

respectively, compared to the PA-cell core with the optimal differential load. These values are found acceptable and mostly caused by losses in the output balun and interconnections.

The input balun also includes an additional inductor in order to realize conjugate matching, and hence, to maximize the PA unit cell gain. DC biasing is applied at the center tap of the baluns to eliminate the need for separate bias chokes. The geometry of the baluns have been optimized using a finite element method EM-solver in Ansys HFSS. The key optimization goals are wideband impedance matching and high common-mode rejection. The simulation model of the PA unit cell consists of an  $8 \times 8$  S-matrix representing the baluns with the chip ground topology and RLC extracted

circuit of the interconnected devices. This is necessary to include layout parasitics of the distributed devices into account. Deep trench isolation is implemented below the baluns and RF pads in order to reduce substrate parasitic effects.

### 3.2 Measurement Results

The measured small-signal performance of the designed PA unit cell over the 0.1 – 45 GHz frequency range is shown in Figure 5. The maximum obtained PA gain ( $|S_{21}|$ ) of 16.1 dB can be observed at 26.6 GHz. The demonstrated 3-dB bandwidth is 45% and corresponds to 20.8 – 33 GHz frequency range. The input reflection coefficient ( $|S_{11}|$ ) is below –10 dB over the 25 – 45 GHz range (57%), while  $|S_{22}| \geq -5$  dB. The relatively high  $|S_{22}|$  level is caused by the realized optimal power matching, which is different from conjugate matching. The measured reverse isolation ( $|S_{12}|$ ) remains below –35 dB. The stability  $K$ -factor calculated from the measured data confirms that the circuit is unconditionally stable [21]. The measurement low-signal curves exhibit similar behavior as the simulations (shown by the dashed lines), however, the average levels are slightly different due to the modeling inaccuracies.

The PA unit cell saturated output power,  $P_{\text{sat}}$ , and maximum peak power-added efficiency (PAE) over the operation frequency band (25–38 GHz) are shown in Figure 6 and 7 respectively. The results correspond to the default biasing settings. The maximum obtained output power of 24.9 dBm can be observed at 25.7 GHz. The output power 1-dB bandwidth is about 10.5 GHz, ranging from 23.0 GHz to 34.0 GHz, and corresponds to a 38.6% fractional bandwidth. The maximum measured PAE reaches 30% at 26.2 GHz and remains above 24% over the entire 1-dB  $P_{\text{sat}}$  bandwidth. The differences between the measurements and simulations are believed due to the limited accuracy of the Si substrate EM model as well as inaccurate modeling of complex distributed effects in the relatively large devices.

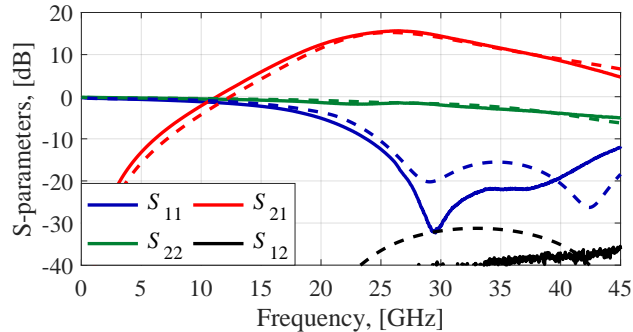


Figure 5: Measured (solid lines) and simulated (dashed lines) small-signal performance of the designed PA unit cell. The maximum obtained PA gain ( $|S_{21}|$ ) is 16.1 dB at 26.6 GHz.

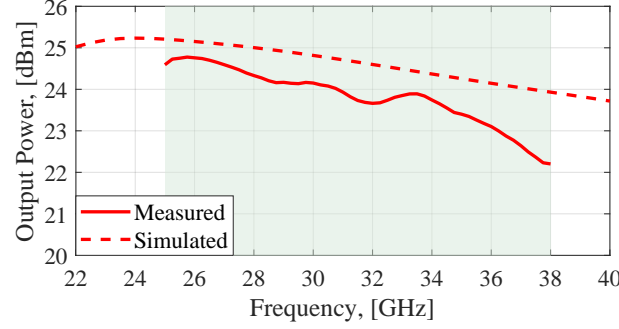


Figure 6: Comparison between the measured (solid line) and simulated (dashed line) saturated output power,  $P_{\text{sat}}$ , levels of the PA unit cell.

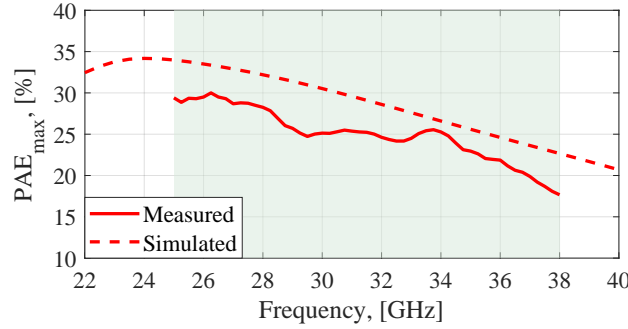


Figure 7: The measured (solid line) and simulated (dashed line) maximum peak PAE of the PA unit cell.

## 4 Combined Power Amplifier

### 4.1 Description of the Architecture

The above-described PA unit cell has been employed to realize the combined Watt-level PA as illustrated in Figure 1. The core of this design is the chip with an array of four identical PA unit cells, each of which is in-phase fed using a 4-way transmission-line based Wilkinson power splitter.

The splitter is based on coplanar-waveguide (CPW) transmission lines using the top metal layer (M6) for the signal and return paths and having a patterned ground shield on the lower metal layer (M4). Employing the top metal layers, which are thicker, allows one to reduce the resistive losses as well as to minimize the negative effect of substrate parasitics. However, based on the performed EM simulations, the insertion losses of the designed splitter still remain high and reach  $-7.8$  dB level at 35 GHz. Moreover, in practice, a flip-chip interconnected die lies on a board solder mask, which is intrinsically lossy and hence degrades a splitter/combiner performance. Therefore, off-chip power-combining solutions become more attractive due to their low insertion losses.

In order to potentially fit more parallel PA unit cells on a single die, and hence



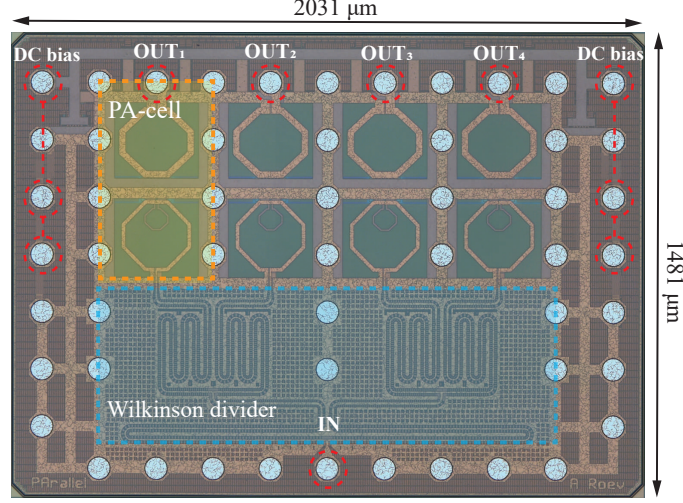


Figure 8: The die photo showing its interior architecture. The chip size including pads for stud bumping is  $2031 \times 1481 \mu\text{m}$  ( $2.9 \text{ mm}^2$ ).

increase the combined output power, the pitch between adjacent PA unit cells has been chosen to be  $370 \mu\text{m}$ . The latter allows putting one row of grounded pads between PA unit cells and hence prevent undesired coupling effects.

The chip is flip-chip interconnected using stud-bumps to the laminate, where the power combiner, input/output interfaces, and DC biasing lines are placed. In order to realize proper mechanical and galvanic connections between the chip and laminate, a grid of ground pads for stud-bumps has been placed all around the interior layout. The pitch between adjacent pads is  $180 \mu\text{m}$ . The final chip has an overall size of  $2031 \times 1481 \mu\text{m}$ , which corresponds to the area of  $2.9 \text{ mm}^2$ .

## 4.2 Joint EM-Circuit-Thermal Optimization

Although the initially designed stand-alone PA-cell and power combiner individually have the desired performance, the combined structure requires an additional joint optimization. Figure 9 (a) shows a complete EM simulation model of the combined PA. It includes the actual chip topology interconnected to the laminate, where input and output ports are placed. The chip model consists of a 4-way TL-based Wilkinson power splitter with each output path followed by a PA unit cell layout with five internal ports ( $B_p$ ,  $B_n$ ,  $C_p$ ,  $C_n$ ,  $V_{cas}$ ) for interconnecting a cascode active circuitry, as shown in Figure 3.

The networks required for distribution of the DC supply and bias signals to PA unit cells can introduce an asymmetry in the operation of those parallel cells as these networks are often implemented in an asymmetric way due to limitations within a chip topology. Moreover, these networks can increase the undesired electrical coupling between parallel PA unit cells. In order to avoid these undesired effects, the



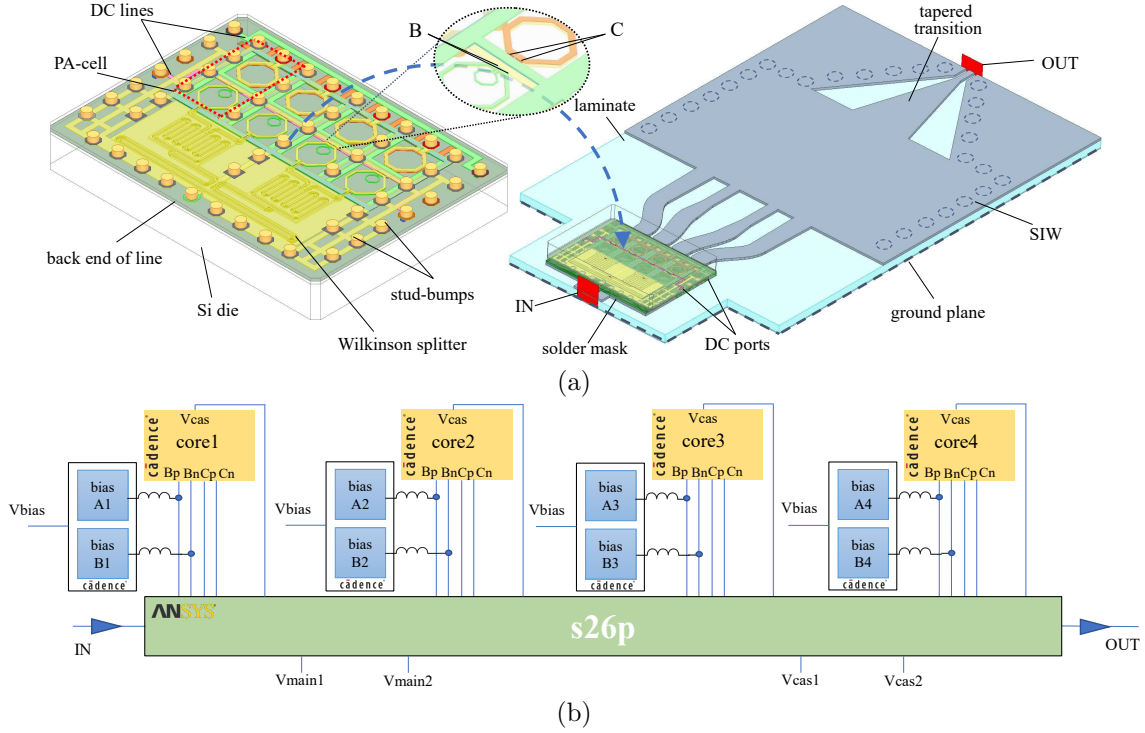


Figure 9: Simulation model of the designed spatial power-combined PA containing  $4 \times$  PA-cells: (a) EM model of the die flip-chip interconnected to the combiner placed on the laminate; (b) circuit-level block diagram.

required biasing voltage is locally generated at each active block (See Fig. 3 (c)), thereby simplifying DC routing lines and eliminating the potential asymmetry of the distribution network. The remaining routing lines are included in the chip EM model. The corresponding DC feeding ports ( $V_{\text{main}1,2}$ ,  $V_{\text{cas}1,2}$ ) are placed on the laminate. In order to prevent undesired coupling effects between parallel PA-cells, a row of grounded pads has been placed in-between adjacent PA-cells. In practice, a flip-chip interconnected die lies on a lossy solder mask covering the laminate. Therefore, a realistic solder mask pattern is also included in the simulation model.

Figure 9 (b) shows a circuit-level block diagram of the proposed simulation test-bench. It has four identical RLC extracted circuits of the active core, derived in the initial designs phase, which are interfaced with a 26 ports S-matrix, representing the complete EM model of the structure, as shown in Figure 9 (a). The HFSS-obtained S-matrix characterizes the structure from DC up to the 6th-order harmonics. The latter allows us to directly bias parallel active cores through the S-matrix, and as a result, take into account realistic losses in the DC biasing network. Since internal oscillation loops can exist within this multi-cell topology, the stability of the design is checked at distinctive internal nodes using time-domain simulations with a pulsed input signal. A harmonic balance analysis has been used to evaluate the large-signal performance of the PA. In this phase, the combined geometry is numerically optimized to ensure

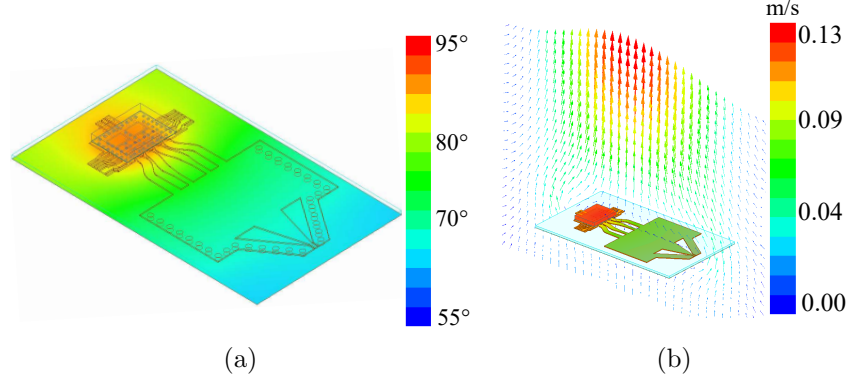


Figure 10: Thermal analysis in large-signal operation: (a) surface temperature; (b) air velocity. The ambient temperature is 25°C.

circuit stability as well as to satisfy the main system-level performance goals:  $P_{\text{sat}}$  and PAE over a certain frequency bandwidth.

Placing multiple parallel PA unit cells on one die causes higher power loss densities and, therefore, higher and faster temperature evolution inside the chip. Overheat might seriously reduce device performance and reliability [22]. Heat is transferred in three ways: conduction, convection, and radiation. Since heat radiation is effective only when source surface area is large enough, the following two paths are the main contribution to heat dissipation:

- Convection from the surface of the die to the air;
- Conduction through interconnecting stud-bumps to the laminate and then convection to the air.

Figure 10 (a) and (b) show the simulated steady-state surface temperature of the combined PA and air velocity in the surrounding region, respectively. The airflow corresponds to natural convection. The power level of a heat source, 2.5 W, corresponds to the output power and efficiency values obtained in the previously performed harmonic balance analysis. According to the thermal simulations, the heat dissipation path via stud-bumps is the most effective and accounts for 80% of total heat dissipation. Therefore, it is important to realize a proper thermal connection between the chip and laminate by placing a grid of ground pads for stud-bumps all around the interior layout. Moreover, the board should be designed in such a way as to realize the fastest possible heat transfer from the chip into the lower laminate metal layers. This iterative optimization process continues until both the desired large signal performance and safe temperature regime are obtained.

### 4.3 Spatial Power Combiner

The power combiner is based on a principle of the recently proposed multichannel transition with spatial power combining functionality, where an array of strongly coupled microstrip lines interfaces a single SIW [11].

Figure 11 shows the developed board containing the power combiner as well as its two back-to-back configurations, which are needed for test purposes. A tapered ML transition is used on the other side of the combiner to make the output interface suitable for conventional GSG RF measurement probes. In potential applications, the design will include an SIW-based antenna element, and the tapered ML transition will be removed. The non-isolating spatial power combiner has been designed through active impedance matching. The critical design parameters are the positions of MLs, the distances between MLs, their lengths and widths. The combiner has been optimized to realize an optimal active impedance matching under the condition of uniform excitation (identical PA unit cells). This optimization problem has been described in [23]. Figure 11 (b) shows the x-ray image of the board area corresponding to the chip footprint. It has a grid ground topology with blind metalized vias making a good RF connection between the chip distributed ground and the board bottom ground plane. Moreover, the metalized vias are involved in thermal heat transfer from the chip into the lower board metal layers. The footprint ground topology has been numerically optimized using Ansys HFSS.

The structure is built on a hybrid multilayer board, which is formed by stacking three core laminates. The top and bottom substrates are Astra MT77 laminates with the relatively low thickness of 127  $\mu\text{m}$ , whereas the middle core is FR4 with the thickness of 300  $\mu\text{m}$ , which makes the structure more rigid. Due to the relatively small size of the designed structure compared to a typical coaxial connector footprint, it has been decided to perform direct on-laminate measurements using miniature contact probes originally intended for on-wafer measurements. It allows one to eliminate the need for bulky RF connectors and relatively long interconnecting lines and transitions. The latter makes the structure more compact as well as simplifies a calibration procedure. However, the use of on-wafer probes on laminate imposes specific requirements on mechanical properties of the corresponding contact pads. In order to meet these requirements, a thick layer of pure gold has been deposited on top of the copper traces. Figure 12 (a) shows the image of the fabricated board cross-section, which is obtained by using scanning electron microscopy [24]. The measured thickness of the gold and copper layers are 6  $\mu\text{m}$  and 23  $\mu\text{m}$ , respectively. From the fabrication perspective, it is difficult to uniformly deposit such a thick gold layer over the whole board surface. As a result, higher surface roughness might be expected. Figure 12 (b) shows the measured surface roughness map of the area of  $100 \times 100 \mu\text{m}^2$ . The measured root-mean-squared roughness calculated over the entire measured surface is 435 nm, however, the maximum peak height and valley depth reach values of 755 nm and 1400 nm, respectively. These measurements have been used later for building a

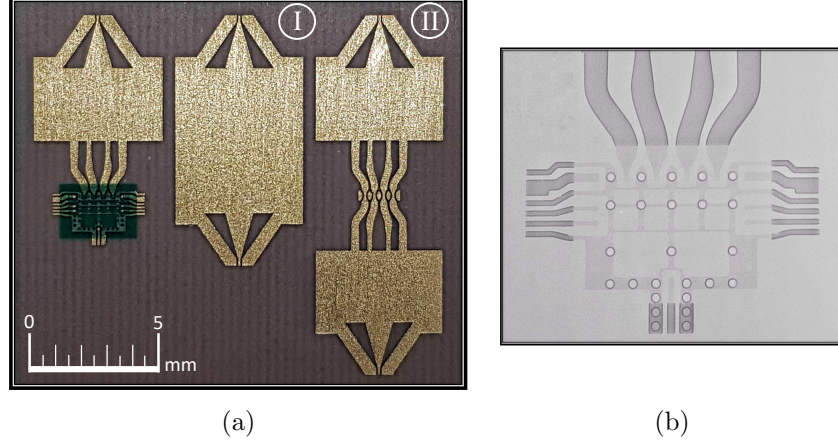


Figure 11: Fabricated board: (a) Layout of the designed power combiner including its two back-to-back configurations; (b) X-ray image of the board area corresponding to the chip footprint.

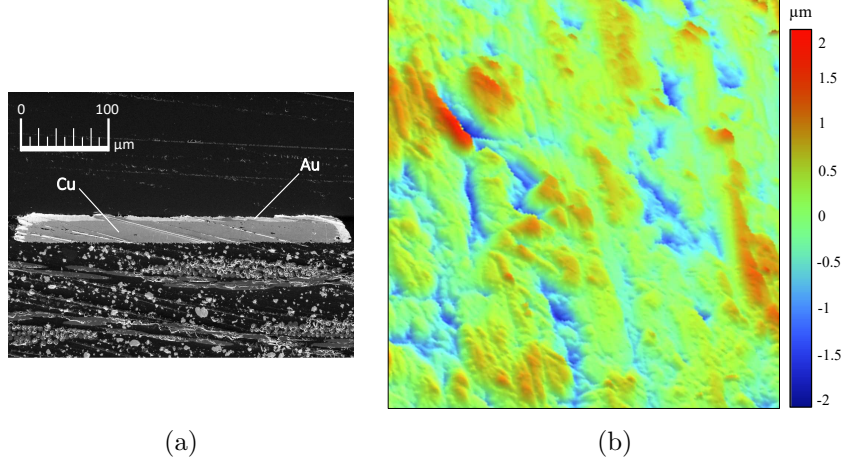


Figure 12: The results of scanning electron microscopy: (a) Cross-section of the fabricated board indicating the quality of the gold finishing on top of the copper trace; (b) Map of the surface roughness ( $100 \times 100 \mu\text{m}^2$  area).

more accurate equivalent surface model in Ansys HFSS.

The power combiner has been tested in two back-to-back configurations: the complete back-to-back configuration (II) and the configuration excluding the arrangements of four MLs (I), as shown in Figure 11. That has been done for three main reasons: verification that the board fabrication was completed satisfactorily, prediction of the measured combined output power reduction caused by the realistic combiner losses, and the characterization of the losses inside the SIW with a tapered ML transition.

Figure 13 shows the measured and simulated  $|S_{11}|$  and  $|S_{12}|$  of the power combiner in the back-to-back configuration (II). The simulations with and without taking into account the realistic surface roughness are shown by dotted and dashed lines, respectively. The set of curves indicates the spread between three measured sam-

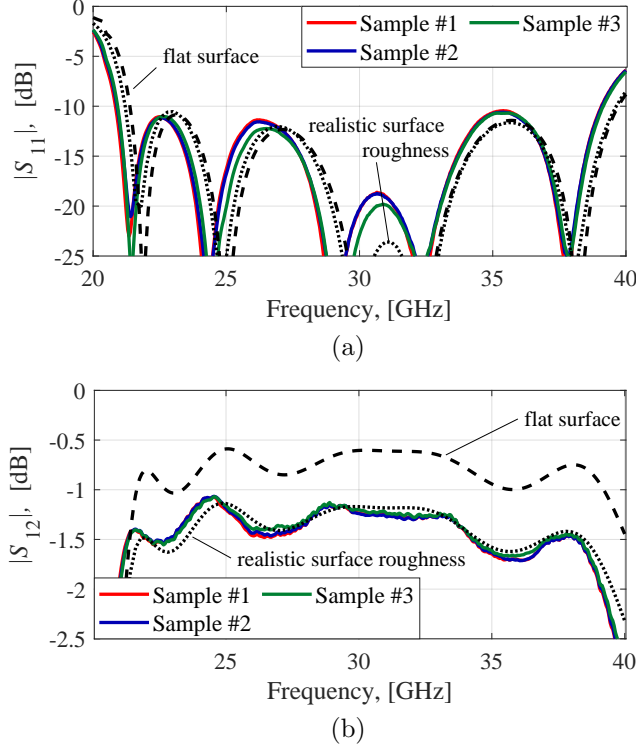


Figure 13: The measured and simulated (a)  $|S_{11}|$  and (b)  $|S_{12}|$  of the complete power combiner in a back-to-back configuration (II). The set of curves shows the spread between different samples.

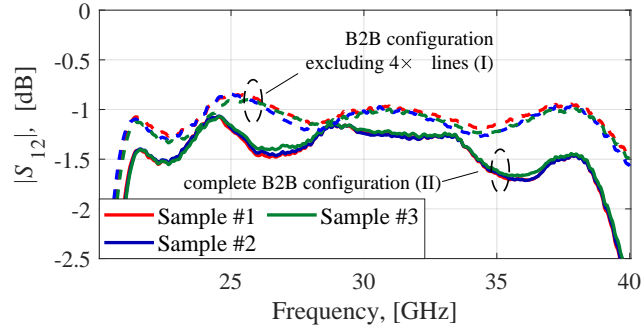


Figure 14: Comparison between the measured  $|S_{12}|$  of different back-to-back configurations, as shown in Fig. 11 (a). The set of curves shows the spread between the different samples.

ples. As one can see, the measured 50- $\Omega$  reflection coefficient,  $|S_{11}|$ , remains below  $< -10$  dB over the whole range (22.5 – 38.5 GHz). The different samples have a similar performance and are in good agreement with simulations. The measured transmission coefficient between the ports of the complete back-to-back configuration,  $|S_{12}|$ , remains  $\geq -1.7$  dB over the 22 – 38 GHz frequency range and reaches  $-1.2$  dB at 28 GHz, which results in approximately 0.6 dB insertion losses for a single combiner itself. Comparison between simulated and measured curves shows

that the used equivalent surface roughness model adequately describes the impact of the realistic surface roughness on insertion losses at Ka-band. Moreover, it has been shown that for the present design significant insertion losses are attributed to the realistic surface roughness. Therefore, using a thin layer of a final surface finishing with lower roughness allows one to reduce the insertion losses even more.

Figure 14 shows the measured  $|S_{12}|$  of the configuration (II) and the configuration excluding the arrangements of four MLs (I), as indicated in Figure 11 (a). The relative difference between the measured transmission coefficients does not exceed 0.5 dB, implying that a single arrangement of four MLs has only an insertion losses of 0.25 dB. The rest of the losses in the developed prototype are attributed to the SIW with tapered ML transition, which could be considered as a part of an antenna in the potential applications.

#### 4.4 Measurement Results of the Combined Power Amplifier

The measurement setup for the assembled active prototype is illustrated in Figure 15. The biasing voltages are applied from both sides of the chip by 125  $\mu\text{m}$  pitch Eye-Pass DC probes, each of which has four power tips. This is needed to keep DC routing lines on the chip symmetric as well as to reduce the effect of their electrical resistance. RF probes have a standard GSG configuration with a 200  $\mu\text{m}$  pitch. A short-open-load-thru calibration substrate is used in order to de-embed effects of the probes from measurement results. Small-signal measurements have been directly performed using a 67 GHz Keysight PNA-X N5247A VNA, whereas large-signal measurements require an additional power calibration module and preamplifier driving the PA under test with high power. Due to the limited operating frequency range of the employed preamplifier, the large-signal measurements have been performed over the 25–38 GHz bandwidth. To evaluate the PAE of the designed PA, its power consumption has

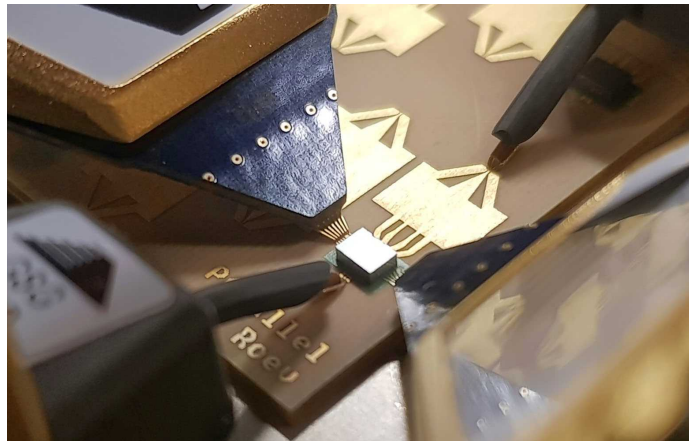


Figure 15: The measurement setup. The measurements are carried out using a Cascade Microtech mechanical probe station with four manipulators.



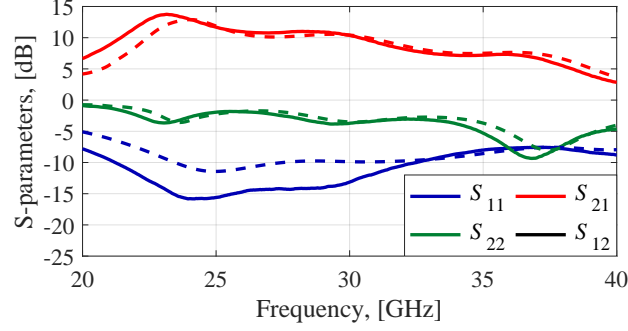


Figure 16: Measured small-signal performance of the combined PA. The maximum obtained PA gain ( $|S_{21}|$ ) is 13.8 dB at 23.2 GHz.

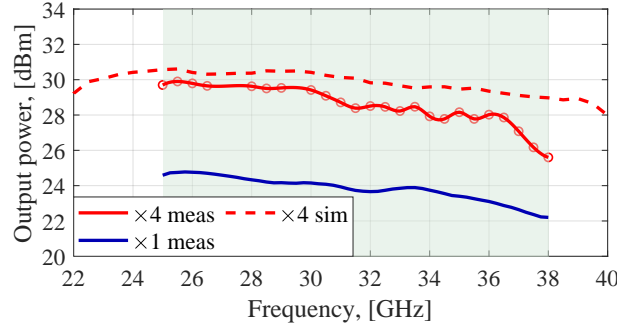


Figure 17: Comparison between the measured (solid red line) and simulated (dashed red line) saturated output power levels of the combined PA. The blue line shows the measured saturated output power of the PA unit cell.

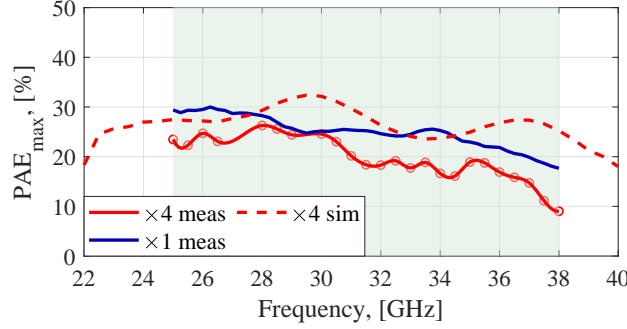


Figure 18: The measured (solid red line) and simulated (dashed red line) maximum peak PAE of the combined PA. The blue line shows the corresponding results of the PA unit cell.

been measured by a DC power supply with a remote interface. To eliminate various thermal effects in semiconductors, large-signal measurements have been repeated in a pulsed regime, where average power levels have been measured. However, there were no considerable differences between the results in continuous and pulsed operation modes.

The measured small-signal performance of the combined PA over the 20 – 40 GHz frequency range is shown in Figure 16. The maximum obtained  $|S_{21}|$  is 13.8 dB at

23.2 GHz. The 3-dB gain bandwidth is 30% and corresponds to 21.7 – 29.5 GHz frequency range. The  $|S_{11}|$  is below  $-10$  dB over the 21.2 – 32.6 GHz range (42%). The measured  $|S_{12}|$  remains below  $-35$  dB. The measured  $K$ -factor confirms that the circuit is unconditionally stable. The measured low-signal curves exhibit the same behavior as the simulations (shown by the dashed lines). However, the minimum of  $|S_{11}|$ , and hence the maximum peak gain, are shifted towards the lower frequencies. The latter is a result of the modeling inaccuracies of the input power splitter in the presence of the realistic solder mask.

The combined PA output power for the default biasing settings is shown in Figure 17. The blue line shows the measured output power of the PA unit cell as the reference. The maximum output power is 30.0 dBm at 25.5 GHz. The output power 1-dB bandwidth is 29.9%, ranging from 23.0 GHz to 31.1 GHz. Ideally, the output power level after combining four PA unit cells should be 6 dB higher than that of a single PA unit cell. However, the obtained average relative difference is around 4.5 dB, implying that the total power losses in the interconnections and combiner are 1.5 dB. Taking into account the measured losses of the complete back-to-back configuration (II), the losses caused by the flip-chip interconnections and the combiner itself are 0.8 dB and 0.7 dB, respectively. The measured maximum peak PAE reaches a value of 26.0% at 28.0 GHz and remains above 19% over the entire 1-dB power bandwidth (See Figure 18).

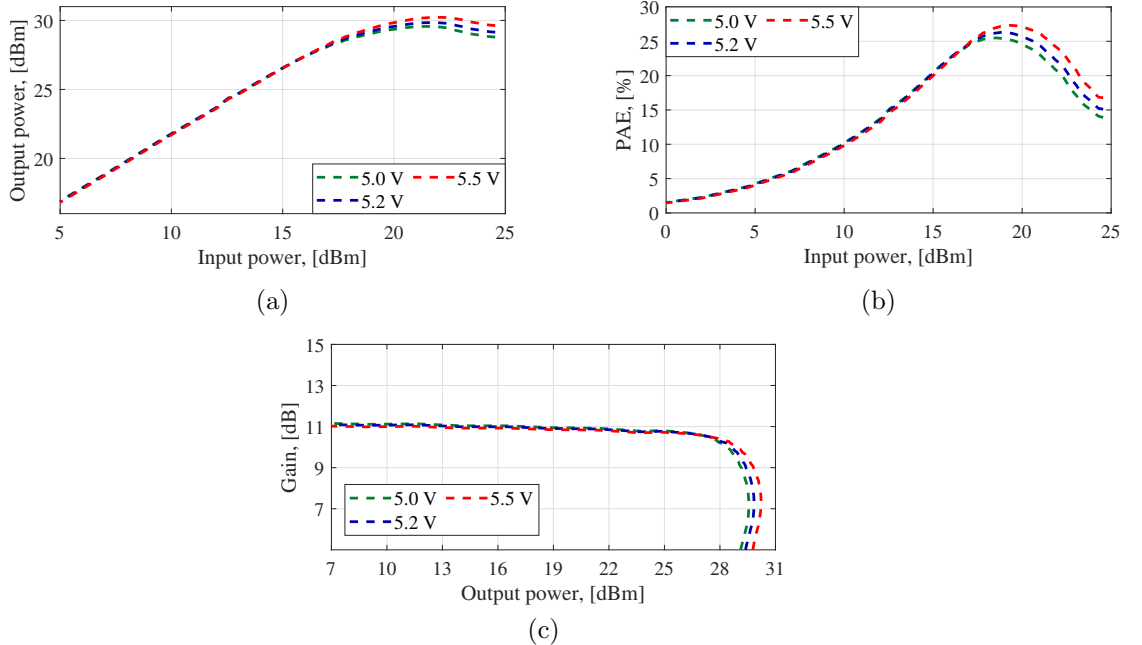


Figure 19: The measured (a) output power and (b) maximum peak PAE versus input power; (c) gain versus output power of the combined PA at 28 GHz. The set of curves corresponds to different values of  $V_{\text{main}}$ .



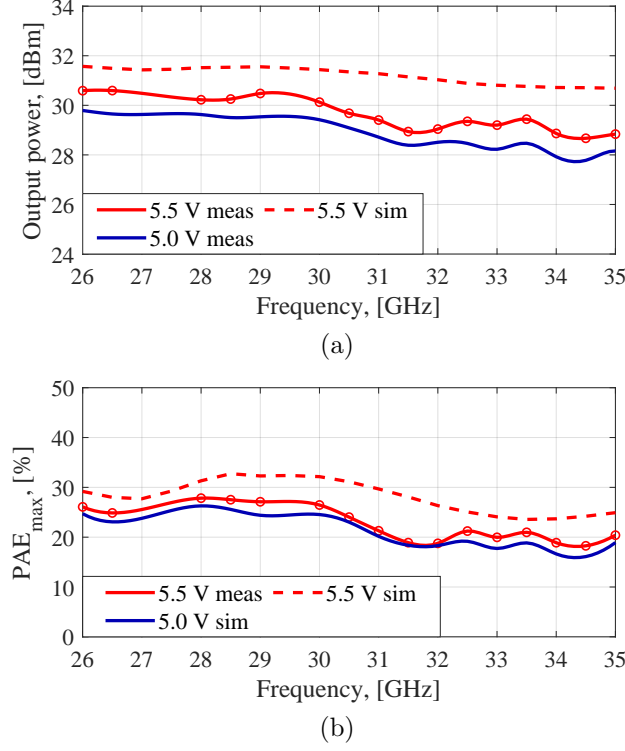


Figure 20: Comparison between the measured (a) saturated output power levels and (b) maximum peak PAE of the combined PA under different values of  $V_{\text{main}}$ . The corresponding simulation results are shown by the dashed line.

Figure 19 (a) shows the measured output power of the combined PA versus input power at 28 GHz. The set of curves corresponds to different collector voltage values,  $V_{\text{main}}$ . As one can see, by increasing  $V_{\text{main}}$ , the combined PA achieves higher output power, whereas the low-signal gain remains almost the same. The latter means that the higher input power is required to drive the PA into its compression, and as a result, the maximum of efficiency is shifted (See Figure 19 (b)). Figure 19 (c) shows the measured gain of the PA versus output power. The curves corresponding to different  $V_{\text{main}}$  exhibit similar behavior with negligible gain variation over the different power levels before compression, implying a good PA linearity inherent to class AB.

Figure 20 shows the comparison between the measured saturated output power levels and maximum peak PAE of the combined PA for the default (5.0 V) and the increased (5.5 V) values of collector voltage,  $V_{\text{main}}$ . The measured output power in the case of the increased  $V_{\text{main}}$  exhibits the same behavior over the frequency as in the default case (shown by the blue line); however, the average level is 0.8 dB higher, resulting in 30.8 dBm of peak power. Since the increase of  $V_{\text{main}}$  also leads to higher DC power consumption, the obtained PAE does not significantly change. The further increase of cascode voltage might lead to electro-thermal breakdown of common-base devices.

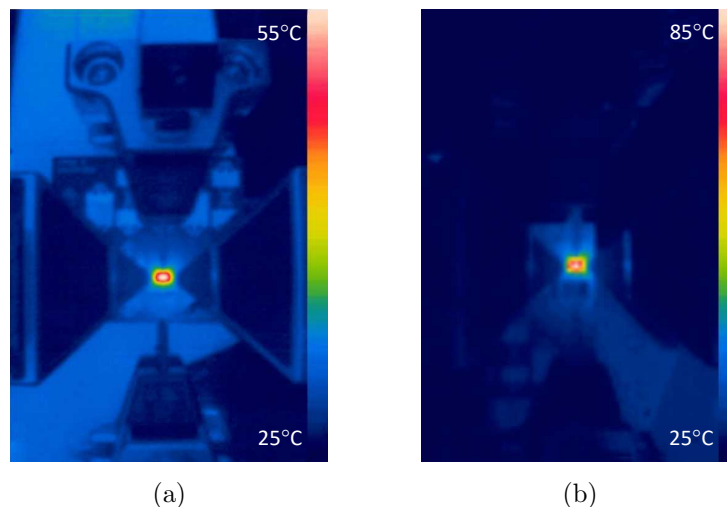


Figure 21: Thermography of the assembled PA board (top view): (a) pulsed mode with 25% duty cycle; (b) continuous mode.

Figure 21 shows thermal images of the PA prototype in a large-signal operation, which are taken by an infrared camera. As one can see, for both pulsed and continuous operation modes the chip surface temperature remains in the safe operating region by virtue of the carefully designed thermal paths. The further temperature reduction in the continuous operation mode might require additional active cooling solutions, for example, air forcing through a fan. The latter could also be included in the thermal simulation model.

## 5 Discussion

In Table I, the developed combined PA and the PA unit cell are compared with published state-of-the-art SiGe PAs at Ka-band with a saturated output power,  $P_{\text{sat}}$ , of 23 dBm and larger [25–30]. The main performance metrics are the saturated output power and its 1-dB bandwidth as well as maximum peak PAE and minimum peak PAE over the entire 1-dB power bandwidth. Due to the relatively low breakdown voltage of silicon devices, the generation of such an amount of power is very challenging and requires combining signals from multiple smaller PA unit cells. In contrast to the present work, where the low-loss spatial power combiner is placed on the laminate, the previous designs employ various on-chip power combining solutions. Note that the output power reference plane of the presented combined PA is located on the laminate. As a result, the reported performance values include the effect of interconnection losses between the chip and the laminate (0.5 – 0.8 dB), as opposed to the previous works where potential interconnection losses are excluded from the analysis since the results of on-wafer measurements only are reported. Therefore,

Table 1: Performance comparison with state-of-the-art Ka-band SiGe PAs

Ref.	PA-cell architecture	Combiner type	Output	Psat		P1dB		PAE		PAE@P1dB		Gain		Tech.
				peak, dBm	1-dB BW	peak, dBm	1-dB BW	peak, %	over BW	peak, %	over BW	peak, dB	3-dB BW	
Chapidi [25]	double-stacked with pre-driver	2-way non-isolated asymmetrical	50-Ω SE on chip	23.7	30.0-50.0 GHz 50.0%	-	-	28.0	>21	-	-	23.4	36.2-48.7 GHz 29.4%	0.13μm SiGe BiCMOS
Sarkar [26]	diff. cascode stage with pre-driver	2-way on-chip T-combiner	50-Ω SE on chip	23.8	-	23.2	27.0-31.0 GHz 13.8% <sup>1</sup>	32.7	-	32.7	>29	29.9	27.0-35.0 GHz 25.8%	TowerJazz 0.18μm SiGe BiCMOS
This work PA-cell	single diff. cascode stage	NaN	50-Ω on chip SE	24.9	23.0-34.0 GHz 38.6%	24.2	22.6-34.2 GHz 40.8%	30.0	>24	29.8	>23	16.1	20.8-33.0 GHz 45.0%	NXP 0.25μm SiGe BiCMOS
Huang [27]	diff. cascode stage	2-way on-chip current combiner	50-Ω SE on chip	26.0	22.0-30.0 GHz 30.7%	23.2	21.0-28.9 GHz 31.6%	34.0	>26	-	-	16.3	21.1-31.5 GHz 39.5%	90nm CMOS
Wang [3]	diff. Doherty with pre-driver	4-way on-chip DAT	50-Ω diff. on chip	28.3	23.0-31.0 GHz 29.6%	26.8	-	30.4	>30	30.2	-	20.5	22.0-28.5 GHz 25.7%	0.13μm SiGe BiCMOS
Welp 5.0 V [28]	diff. cascode stage with pre-driver	4-way on-chip Wilkinson	50-Ω diff. on chip	28.7	20.5-27.2 GHz 28.1%	-	-	21.9	>15	-	-	16.1	-	Infineon 0.35μm SiGe BiCMOS
Datta [29]	double-stacked with pre-driver	8-way on-chip current + slow wave	50-Ω SE on chip	28.9	45.0-47.0 GHz 4.3%	-	-	25.0	>23	-	-	13.0	45.0-47.0 GHz 4.3%	0.13μm SiGe BiCMOS
Essing 5.5 V [15]	single cascode stage with pre-driver	8-way on-chip current combiner	50-Ω SE on chip	29.1	25.5-30.0 GHz 16.2%	-	-	10.3	>8.5	-	-	20.2	26.5-30.3 GHz 13.3%	NXP 0.25μm SiGe BiCMOS
Nguyen 2.0 V [30]	diff. cascode stage with pre-driver	24-way DAT combiner	50-Ω diff. on chip	29.1	55.0-64.0 GHz 15.1%	-	-	18.4	>14	-	-	25.0	53.0-65.0 GHz 20.3%	45nm CMOS
Welp 5.8 V [28]	diff. cascode stage with pre-driver	4-way on-chip lumped Wilkinson	50-Ω diff. on chip	30.8	19.5-27.0 GHz 32.2%	-	-	17.6	>13	-	-	16.1	-	Infineon 0.35μm SiGe BiCMOS
This work 5.0 V	single diff. cascode stage	4-way spatial power combiner	50-Ω SE on laminate	30.0	23.0-31.1 GHz 29.9%	28.7	22.9-33.0 GHz 36.1%	26.0	>19	24.3	>16	13.8	21.7-29.5 GHz 30.4%	NXP 0.25μm SiGe BiCMOS
This work 5.5 V	single diff. cascode stage	4-way spatial power combiner	50-Ω SE on laminate	30.8	23.0-31.0 GHz 29.6%	29.7	23.0-33.0 GHz 35.7%	26.7	>20	25.1	>16	13.9	21.6-29.5 GHz 30.9%	NXP 0.25μm SiGe BiCMOS

<sup>1</sup> Estimated from the reported table.

the developed solution demonstrates the highest achievable saturated output power in practical applications, where the 50-Ω load is placed on a laminate. Furthermore, the SIW-based power combiner could be directly integrated as a part of an antenna, thereby eliminated extra transition losses and making the overall structure more compact. The combined PA has a wide band performance with both high efficiency and high output power, which outperforms the state-of-the-art silicon-based PAs. It results in a 5.1-dB maximum boost in output power with only 5% point degradation in PAE compared with a single PA unit cell. Moreover, the proposed architecture allows for interfacing more parallel PA unit cells while offering almost constant power combining losses.

## 6 Conclusion

A wideband Watt-level PA employing a new power-combining architecture has been designed and implemented in 0.25 μm SiGe:C BiCMOS technology. This design

includes a chip with multiple custom PA unit cells, which are interfaced using a spatial power combiner on a laminate. In this approach, the strongly coupled MLs from the array of PAs are interconnected to a single SIW. The custom-designed PA unit cell is a differential cascode amplifier, which has single-ended  $50\text{-}\Omega$  input and output. It has a wideband performance ( $23 - 34\text{ GHz}$ ) with both high efficiency (30%) and high output power (24.9 dBm).

The combined PA including four PA unit cells achieves a maximum saturated output power of 30.8 dBm in combination with 26.7% PAE, which exceeds the state of the art to the best of the authors' knowledge. The high efficiency ( $\geq 20\%$ ) and output power ( $\geq 29.8\text{ dBm}$ ) over a wide frequency range (30%) are the result of using the proposed architecture with low-loss (0.6 dB) and wideband (54%) parallel spatial power combiner. Moreover, the optimal system-level performance has been achieved by taking into account the effects of mutual coupling between closely spaced PA-cells, distributed DC feeding lines, and interconnections to laminate in the joint EM-circuit-thermal optimization. In addition, a multi-physics approach used in the design flow allows mitigating the thermal issues caused by a high power density in a relatively small chip. Despite the relatively high design complexity of the proposed PA, it is expected to play an important role in efficient high-power wideband mm-Wave transmitters.

## Acknowledgment

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# **Transition Arrangement between an SIW Structure and a Transmission Line Arrangement**

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*Swedish patent application: M1 P2SE00 AB/ab 2017-10-27.*



M1 P2SE00 AB/AB 2017-10-27

# Transition Arrangement between an SIW Structure and a Transmission Line Arrangement

Artem Roev, Rob Maaskant, and Marianna Ivashina

## Abstract

The present invention relates to a transition arrangement (100) comprising at least one transition between a substrate integrated waveguide, SIW, structure (1) and a transmission line arrangement (4). The transmission line arrangement comprises an array of two or more interfacing transmission lines, TLs, (4) the, or each, SIW of the SIW structure (1) is transforming/combining/splitting the transmission-line electromagnetic field modes, e.g. microstrip co-planar or coaxial modes, into the SIW-based structure's electromagnetic field mode or modes, such that for the, or each, transition between a said single mode or over-moded substrate integrated waveguide, SIW structure (1), the said array of two or more interfacing transmission lines, TLs, of the transmission line arrangement (4) are simultaneously transmitting and/or receiving to act as an SIW-TL impedance transforming, or matching, structure such that EM fields are coupled from the SIW (or TLs) structure to the TLs (or SIW) structure, thereby spatially combining or splitting the electromagnetic power.

## 1 Technical Field

The present invention relates to a transition arrangement comprising a transition between an SIW (Substrate Integrated waveguide) structure interface and a transmission line arrangement having the features of the first part of claim 1.

## 2 Background

The generation and transmission of high power is a major challenge at mm-wave frequencies, since the atmospheric propagation and material losses are significant and increase as frequency increases. This is further exacerbated by the fact that semiconductors reduce in size and deliver less power when moving up into the mm-wave frequency region. This problem can be overcome by using many low-cost active devices per unit volume and combine their signals using series and parallel power combining techniques. However, the latter solutions are potentially lossy since power is typically combined to a single point before leaving the MMIC. Substrate integrated

waveguide (SIW) technology offers a low-cost low-profile mm-wave integration solution, either on-PCB or on-chip while the SIW interface keeps the fields spatially distributed without having to combine the power to one point.

US 20120242421 A1 [1] shows a transition between an SIW and a microstrip line, which has a single channel. The microstrip line needs to be tapered for impedance matching purposes to interface the larger SIW structure. This tapering increases both the size of the structure and the Ohmic losses, and is expensive too due to the large chip area that it requires.

### 3 Summary

It is therefore an object of the present invention to provide a transition arrangement comprising a transition between an SIW or an SIW antenna interface and an array of two or more transmission lines, as initially referred to, through which one or more of the above-mentioned problems are overcome.

It is also a particular object to provide a transition arrangement which is easy and cheap to fabricate (PCB or MMIC technology).

It is a particular object to provide a transition arrangement which can be used for very low frequencies up to very high frequencies.

Further yet it is a particular object to provide a transition arrangement which is compact.

Another particular object is to provide a transition arrangement capable of working in transmission and/or receiving mode.

Still another particular object is to provide a transition arrangement which can be integrated on an MMIC, and which particularly provides a contactless contact connection possibility to off-chip circuitry.

Still further it is a particular object to provide a transition arrangement allowing creation of large power modes in the SIW structure.

A most particular object is to provide a transition arrangement which can be used for different circuit arrangements, passive as well as active, one or more MMICs of arbitrary size, i.e. also large MMICs, and even more generally, circuits of many different kinds including hybrid circuits, RF circuits, for both millimetre waves and sub-millimetre waves.

Another object is to provide a transition arrangement allowing high overall radiation efficiency.

A further object is to provide a transition arrangement which has a good impedance matching capability and low-loss field mode conversion properties over the entire SIW waveguide bandwidth.

It is also an object to provide a transition arrangement which is reliable and precise in operation.

One or more of these objects are achieved through a transition arrangement as initially referred to having the features of the characterizing part of claim 1.

Advantageous embodiments are given by the respective appended dependent claims. According to the present invention it has been realized that, since the SIW electromagnetic mode(s) is (are) spatially distributed, this allows the power in this (these) mode(s) to be created or fed by an array of relatively small transmission lines that are interconnecting to the SIW structure while exciting these transmission lines preferably simultaneously. Since the transmission lines in the array can be strongly coupled, each of them must be matched to its active impedance that it sees. The idea of spatial power combining (and/or splitting) as such is not new and has been realized in so-called grid amplifiers (e.g. US5736908 [2]). However, such structures are typically bulky and cannot be directly integrated on-chip.

Through an arrangement as proposed in the present invention, integration on-chip, e.g. an MMIC (Monolithic Integrated Circuit) is enabled and at the same time a contactless connection possibility to the off-chip circuitry is enabled (see e.g. WO 2017137224 A1 [3]). The present invention is an extension of WO 2017137224 A1 in that it offers a novel solution to create larger powers for the mode (or modes) in the SIW structure. In fact, according to the present invention it has been realized that a power combining technique through an array of transmission lines can be used for microstrip-line-based transitions directly interfacing (i.e. without intermediate tapering) an SIW electromagnetic structure, as opposed to known microstrip-line-based transitions facing an SIW electromagnetic structure [4, 5].

## 4 Brief Description of the Drawings

The invention will in the following be further described in a non-limiting manner, and with reference to the accompanying drawings.

## 5 Detailed Description

As referred to earlier in this application, it has been realized that, since the SIW electromagnetic mode is spatially distributed, this allows the power in this (these) mode(s) to be created or fed by an array of smaller transmission lines that are interconnecting to the SIW structure while exciting these transmission lines preferably simultaneously, see e.g. the fields in Figure 3 below.

Figure 1 schematically illustrates a transition arrangement 100 according to a first embodiment of the invention comprising an SIW (Substrate Integrated Waveguide) structure 1 interfaced to an array of microstrip transmission lines (TLs) 4. The transition arrangement 100 comprises an SIW 1, which is formed on a dielectric substrate 3 by metalized vias 2. The dielectric substrate is provided on a ground

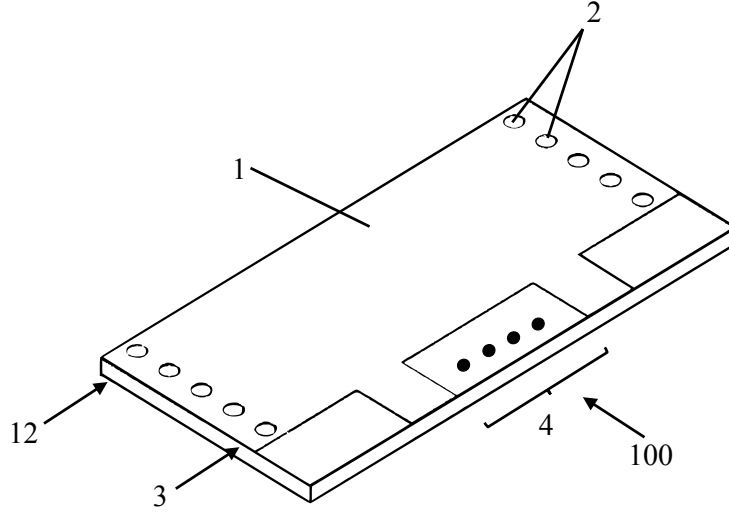


Figure 1: View in perspective an embodiment of the present invention in its most elementary form.

plane 12. The transmission line arrangement 4 comprises an array of  $N \geq 1$  parallel transmission lines connected to the top metal plate of the SIW structure 1. The transmission lines of the transmission line arrangement may have the same widths, or possibly different widths for (active) impedance-matching purposes. The dots in the Figure merely indicate that it is an array.

Figure 2 schematically illustrates a transition arrangement 101 according to a second embodiment of the invention involving an interface to a multimode SIW structure 1A, in this case an integrated horn antenna that is interfaced to, in this specific case, a transmission line arrangement 4A comprising an array of microstrip TLs. Optimally exciting the array of TLs 4A provides, besides increasing the input and thus the radiated power, also the possibility to control the amplitude excitation of the modal content in the over-moded SIW antenna structure 1A, thereby realizing an optimal aperture field distribution at the SIW antenna opening. The structure can also be used in the receiving situation. Similar elements bear the same reference numerals as in Figure 1 but they are indexed 'A', and they are therefore not further described here.

Figure 3 illustrates an embodiment comprising a transition arrangement 102, as a specific example, the field propagation inside the SIW structure 1B (magnitude of E-field) and the coupled fields to the transmission lines of here a transmission line arrangement 4B comprising four microstrip TLs when the SIW port is excited by the fundamental  $TE_{10}$  mode (i.e. receive mode). Similarly, in the transmit mode, the active reflection coefficients of the microstrip TLs 4B should be considered due to the strong direct electromagnetic coupling between them, and because of indirect coupling via the power-combining SIW structure 1B. Accounting for the coupling is very important for impedance-matching purposes of e.g. power amplifiers 7 that

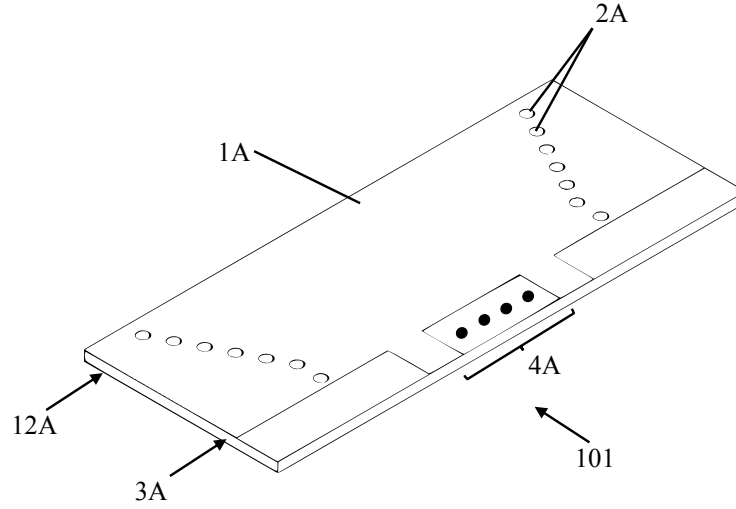


Figure 2: View in perspective of a transition arrangement comprising an antenna (or multimode SIW) according to another embodiment of the present invention.

must be matched to the active impedance it sees when all other transmission lines are also excited by power amplifiers.

The transition arrangement structure 102 of Figure 3 can also work as a receiving structure, thus as both a spatial power combiner and/or splitter (reciprocal network). Since the transmission lines 4B in the array can be strongly coupled, each of them must be matched to its active impedance that it sees.

The specific quad-channel transition e.g. based on the proposed transition arrangement 102 is four times more compact and allows to generate four times higher mm-wave output power compared relative to a conventional tapered microstrip-to-SIW transition. Similar elements bear the same reference numerals as in Figure 1 but they are indexed 'B', and they are therefore not further described here.

Figure 4 shows a specific implementation of the present invention comprising a transition arrangement 103 where an array of four amplifiers (situated inside an MMIC 9) is interfaced with a single SIW 1C through four spatially distributed microstrip lines of a transmission line arrangement 4C. Similar elements already discussed with reference to earlier Figures. bear the same reference numerals but they are indexed 'C', and they are therefore not further discussed here.

The inventive concept is applicable for in principle any circuit of an arbitrary size, active or passive, and it is not limited to any specific frequencies. The outline of the SIW vias further can have different shapes to e.g. form differently shaped horn antennas. Also, the invention is not limited to any specific circuit arrangements, but it is applicable to any circuit arrangement, e.g. RF circuits, MMICs, hybrid circuits, and is also intended to cover other (active or passive) circuits. It is also not limited to any particular number or type of SIW waveguides or antennas, nor to any particular ports, or to the arrangement and positions of ports, there may be two, three or more

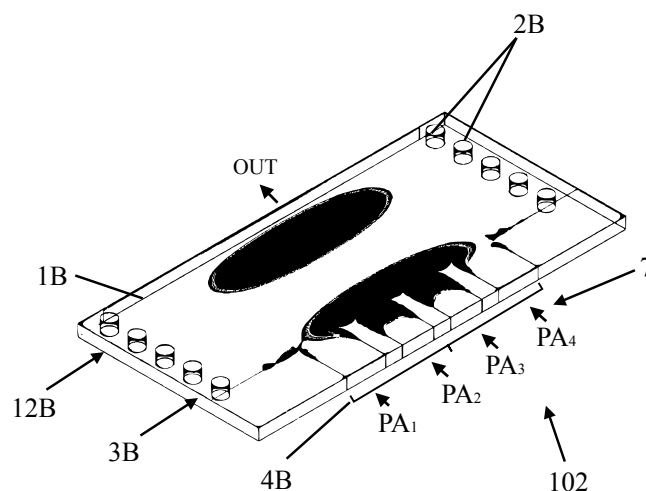


Figure 3: Illustration of the E-field amplitude distribution in a specific quad-channel structure based on the present invention.

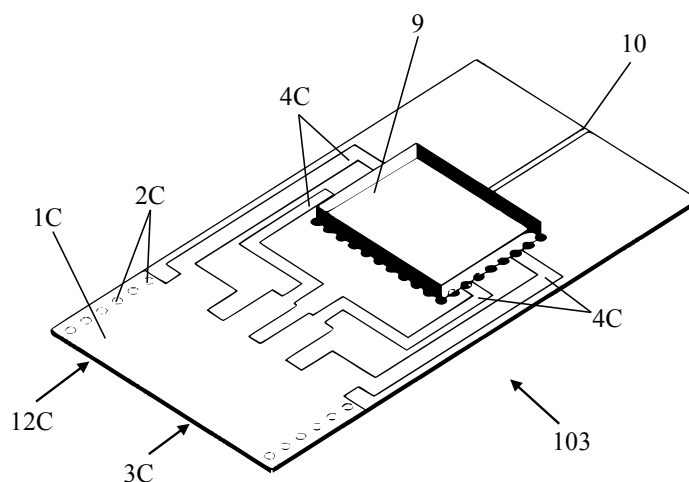


Figure 4: View in perspective of a transition arrangement according to the present invention involving active circuitry.

ports serving as input and/or output ports. Further, the invention covers different types of planar transitions, e.g. also comprising coplanar transmission lines, besides coaxial or microstrip lines.

It is among other things an advantage of the present invention that it provides a compact solution, thus potentially inexpensive, and less lossy due to shorter transmission lines with the additional feature that large (mm-wave) powers can be generated/handled. Typically, the SIW interfacing transmission lines are excited in-phase and equal amplitude, but if the SIW structure comprises an SIW antenna (e.g. 1A in Figure 2), the number of SIW modes is increased and the array of interfacing transmission lines can be excited differently to allow for the optimal SIW mode distribution inside the SIW antenna. This allows besides power generation to also

control the modal content in the SIW structure.

Furthermore, its relatively short length allows to decrease transition losses and renders the structure inexpensive and suitable for much higher frequencies. The concept is expected to play a determining role in future mm-wave communication systems where both high-power generation and low-loss low-cost structures are required. It should be clear that the invention is not limited to the specifically illustrated embodiments but that it can be varied in a number of ways within the scope of the appended claims.

## 6 Claims

1. A transition arrangement (100; 101; 102; 103) comprising at least one transition between a substrate integrated waveguide, SIW, structure (1; 1A; 1B; 1C) and a transmission line arrangement (4; 4A; 4B; 4C), characterized in that the transmission line arrangement comprises an array of two or more interfacing transmission lines, TLs, (4; 4A; 4B; 4C) the, or each, SIW of the SIW structure (1; 1A; 1B; 1C) is transforming/combining/splitting the transmission-line electromagnetic field modes, e.g. microstrip, co-planar or coaxial modes, into the SIW-based structure's electromagnetic field mode or modes, such that for the, or each, transition between a said single mode or over-moded substrate integrated waveguide, SIW structure (1; 1A; 1B; 1C), the said array of two or more interfacing transmission lines, TLs, of the transmission line arrangement (4; 4A; 4B; 4C) are simultaneously transmitting and/or receiving to act as an SIW-TL impedance transforming, or matching, structure such that EM fields are coupled from the SIW (or TLs) structure to the TLs (or SIW) structure, thereby spatially combining or splitting the electromagnetic power.

2. A transition arrangement (101; 101; 102; 103) according to claim 1, characterized in that the transmission lines of the transmission line arrangement are uncoupled.

3. A transition arrangement (101; 101; 102; 103) according to claim 1, characterized in that the transmission lines of the transmission line arrangement are coupled.

4. A transition arrangement (101; 101; 102; 103) according to any one of the preceding claims, characterized in that the transmission lines of the transmission line arrangement are equal.

5. A transition arrangement (100; 101; 102; 103) according to any one of claims 1–3, characterized in that the transmission lines of the transmission line arrangement are unequal.

6. A transition arrangement (101) according to any one of the preceding claims, characterized in that the SIW structure (1A) comprises an SIW antenna, e.g. a horn antenna, the outline of which, i.e. waveguide side walls, may have an arbitrary tapering profile.

7. A transition arrangement (102) according to any one of the preceding claims, characterized in that it at least comprises a transmitting arrangement.



8. A transition arrangement (100; 101) according to any one of the preceding claims, characterized in that it comprises a passive arrangement. 9. A transition arrangement (102; 103) according to any one of the preceding claims, characterized in that it comprises an active arrangement.

10. A transition arrangement (102) according to claim 9, characterized in that it comprises, or is associated with, a circuit arrangement (9) comprising one or more circuits (7), e.g. power amplifiers (PA<sub>1</sub>-PA<sub>4</sub>).

11. A transition arrangement (103) according to claim 9 or 10, characterized in that comprises or is associated with a circuit arrangement comprising an MMIC, an RF circuit or a hybrid circuit.

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# Curriculum Vitae

Artem Roev was born on 11-06-1992 in Izhevsk, Russian Federation. He received his B.Sc. and M.Sc. degrees with honor in Technical Physics from the Peter the Great St.Petersburg Polytechnic University (Saint Petersburg, Russia) in 2014 and 2016, respectively. From 2014 to 2016, he was with the Institute of Applied Astronomy of the Russian Academy of Sciences (IAA RAS) as an Electronics Engineer in the field of antenna systems for remote sensing applications. From 2016 he started a dual-degree Ph.D. project at Chalmers University of Technology (Gothenburg, Sweden) and Eindhoven University of Technology (Eindhoven, The Netherlands) under the European Innovative Training Network “SILIKA: 5G mm-Wave Array Antenna Systems”. This doctoral program involved two industrial internships at SAAB AB (Gothenburg, Sweden) and NXP Semiconductors (Nijmegen, The Netherlands). During more than 1.5 year internship in BL Smart Antenna Solutions group of NXP Semiconductors, he was able to contribute to the design of ongoing RFIC products as well as finalize his own research project of which the results are presented in this dissertation.

The performed by him research has led to one patent application, three journal and four conference papers. The main outcomes of this work have been presented at prestigious international conferences such as the 12<sup>th</sup> European Conference on Antennas and Propagation (London, UK) and the IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (Atlanta GA, USA). Moreover, since his work is of interest to leading industrial partners, he has been selected twice (2018 and 2019) to receive the Ericsson Research Foundation grant.

Currently, his research interests include the design of passive and active components for integrated high-power antenna array transmitters. In particular, his focus is on SiGe BiCMOS technologies for mm-Wave applications.