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Mehdi Jahed, Johan S. Gustavsson, and Anders Larsson, *Fellow, IEEE, Fellow, OSA*

Abstract— **Monolithic multi-wavelength VCSEL arrays, with wavelengths of individual VCSELs precisely set in a post-epitaxial growth process, would enable compact multi-color light sources and transmitters for various sensing and datacom applications. Here we report on a numerical study of the requirements of spectral matching and balancing of DBR reflectances, optical confinement factor, and optical gain for uniformity of threshold current and slope efficiency over wavelength with wavelength set by intra-cavity phase tuning. The requirements are verified by an experimental demonstration of intra-cavity phase tuned VCSELs in the spectral range 1043-1067 nm with a wavelength spacing of 8 ± 1 nm enabled by precise Ar ion-beam etching. Small variations of threshold current and slope efficiency are achieved by close to ideal spectral matching and balancing. The VCSELs are GaAs-based with a dielectric SiO_2/TiO_2 top-DBR. We conclude that high uniformity of threshold current and slope efficiency is demanding in terms of spectral matching and balancing and requires not only very precise etching for intra-cavity phase tuning and precise thickness of the layers in the dielectric top-DBR, but also precise thickness and composition of the layers in the epitaxial semiconductor part.**

***Index Terms*—Vertical-cavity surface-emitting lasers, wavelength setting, threshold current, slope efficiency.**

I. Introduction

In an all-semiconductor vertical-cavity surface-emitting laser (VCSEL), the resonance wavelength, and therefore the emission wavelength, is set during epitaxial growth. Being able to set the wavelength in the post-growth fabrication process would enable small footprint monolithic multi-wavelength VCSEL arrays, which would benefit various multi-color sensing and datacom applications.

For short-reach optical interconnects, the VCSEL is the preferred light source because of superior cost and power efficiency [1]. Higher speed VCSELs [2] together with higher order modulation formats [3] have pushed the lane rate beyond 100 Gb/s [4], enabling an aggregate capacity in excess of 400 Gb/s over multiple (parallel) fibers [1]. An even higher aggregate capacity can be achieved using multiple cores per fiber (space division multiplexing, SDM) [5] or multiple wavelengths per fiber (wavelength division multiplexing, WDM) [6]. This allows for scaling the capacity of VCSEL-based optical interconnects much beyond 1 Tb/s [7].

Four-channel course WDM (CWDM) with 30 nm channel spacing (850, 880, 910, 940 nm), known as SWDM4, has demonstrated up to 400 Gbit/s (4 × 100 Gb/s) single fiber capacity [6], [8]. In such transceivers, discrete VCSELs fabricated from different epitaxial wafers are assembled and multiplexed. With an increasing number of wavelengths, the footprint increases, which becomes increasingly problematic for applications requiring small footprint and high bandwidth density, such as transceivers for co-packaged optics [9].

Smaller footprint and higher bandwidth density would be enabled by monolithic multi-wavelength VCSEL arrays with densely spaced VCSELs. However, in such arrays, the channel spacing has to be reduced to accommodate a sufficient number of channels within the limited optical gain bandwidth of the active region in the VCSEL. On the other hand, a channel spacing sufficiently large to cope with wavelength drift with temperature is needed. For GaAs-based VCSELs at ~1000 nm, with a drift of ~0.1 nm/°C and accounting for the limited gain bandwidth, arrays of 4 to 8 channels with a corresponding spacing of 8 to 4 nm, depending on the temperature range, seems reasonable for uniform performance over the array.

Small footprint and high bandwidth density also require a compact integration platform for multiplexing and fiber coupling. With silicon nitride (SiN) being transparent at the wavelengths of GaAs-based VCSELs, this is offered by SiN photonic integrated circuits with low-loss waveguides, multiplexers, and tapered couplers [10]. Angled flip-chip integration of VCSEL arrays over grating couplers enables uni-directional coupling and eliminates optical feedback to the VCSEL [11], [12]. For efficient coupling of light from the VCSELs to the single-mode SiN waveguides, the VCSELs have to be single-mode and their linear polarization state has to be stable and properly aligned to the grating couplers. In addition, the wavelengths of the VCSELs in the array and their

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spacing have to be accurately controlled.

The resonance wavelength of a VCSEL is set by the phase of the reflections from the distributed Bragg reflectors (DBRs) and the optical length, or the propagation phase delay, of the cavity separating the DBRs. Any of these phase values can be used to control the emission wavelength. Among all the techniques demonstrated for post-growth wavelength setting [13]-[23], intra-cavity phase tuning is most effective and flexible for controlling the resonance wavelength among individual VCSELs on a wafer. It is based on precise thinning of the p-type current injection layer above the active region and the n-type bottom-DBR of a VCSEL with a dielectric top-DBR [23]. Thinning by precise dry etching is done before the dielectric DBR deposition, thus changing the optical length and propagation phase delay of the cavity.

Uniform performance of VCSELs in a monolithic multi-wavelength VCSEL array with wavelengths set by intra-cavity phase tuning requires careful considerations of the spectral dependence of optical gain, DBR reflectances, and optical confinement for minimum variation of cavity loss and threshold gain with wavelength. Critical balancing of these dependencies is needed for uniformity in terms of e.g., threshold current and slope efficiency.

Here we report on a numerical study of the requirements of spectral matching and balancing for uniformity of threshold current and slope efficiency over wavelength with wavelength set by intra-cavity phase tuning. The requirements are verified by an experimental demonstration of four single-mode VCSELs in the spectral range 1043-1067 nm with a wavelength spacing of 8 ± 1 nm enabled by precise Ar ion-beam etching [24]. Small variations of threshold current and slope efficiency are achieved by close to ideal spectral matching and balancing. The VCSELs are GaAs-based with a dielectric SiO_2/TiO_2 top-DBR.

The paper is structured as follows. Section II presents the VCSEL design and the numerical analysis. The VCSEL fabrication process and experimental data from measurements of spectra, threshold currents, and slope efficiencies, along with a comparison with data from the simulations, are reported in Section III. Finally, a summary with conclusions is presented in Section IV.

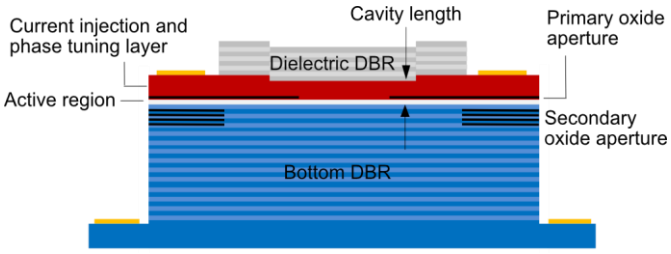

Fig. 1. Intra-cavity contacted oxide-confined VCSEL with a dielectric top-DBR. The cavity length is controlled by thinning the current injection layer before dielectric top-DBR deposition.

II. VCSEL Design and Numerical Analysis

The GaAs-based intra-cavity contacted VCSEL with a dielectric top-DBR is shown in Fig. 1. The semiconductor part, with a 30.5 pair n-type $GaAs/Al_{0.90}Ga_{0.10}As$ bottom-DBR, an active region with three strain compensated 6/10 nm $In_{0.27}Ga_{0.73}As/GaAs_{0.90}P_{0.10}$ quantum wells (QWs), and a p-type GaAs current injection layer was grown by metal-organic chemical vapor deposition (MOCVD). The bottom-DBR is modulation doped and has graded composition interfaces. The top-DBR is a 6-pair SiO_2/TiO_2 dielectric DBR. A 20 nm $Al_{0.98}Ga_{0.02}As$ layer is positioned just above the active region for the formation of a primary oxide aperture for transverse optical and current confinement. An additional four 20 nm $Al_{0.96}Ga_{0.04}As$ layers are inserted below the active region for the formation of larger oxide apertures to reduce capacitance. In the simulations that follow, a temperature of 25°C was assumed.

The full VCSEL structure with refractive index and optical field intensity along the optical axis is shown in Fig. 2. Thinning of the current injection layer reduces the optical length of the cavity and shifts the resonance to shorter wavelengths. The variation of resonance wavelength with etch depth, calculated using a 1D effective index method [25], is shown in Fig. 3. The thickness of the cavity (active region + current injection layer) sets the resonance wavelength at 1086 nm before thinning of the current injection layer. It is further found that the resonance wavelength blue-shifts by 0.95 nm per 1 nm of etching. Therefore, a ±1 nm precision in wavelength requires a ±1 nm precision in etch depth. In a

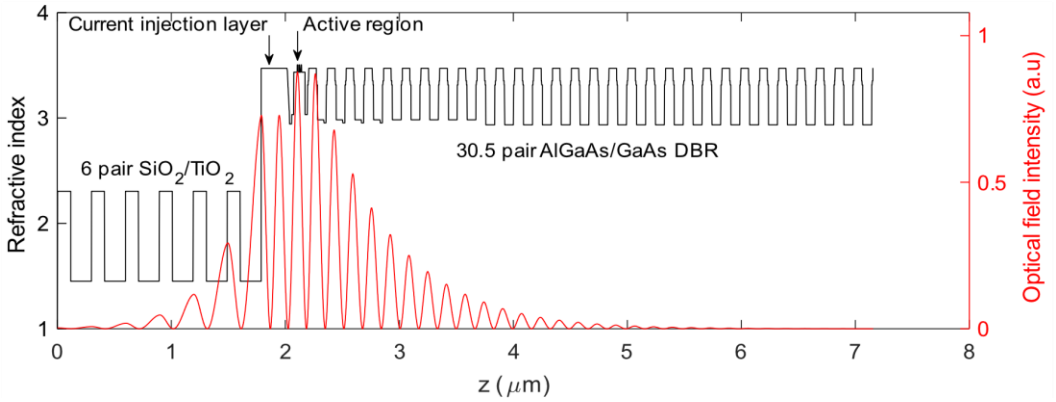

Fig. 2. Refractive index and optical field intensity along the optical axis of the full VCSEL.

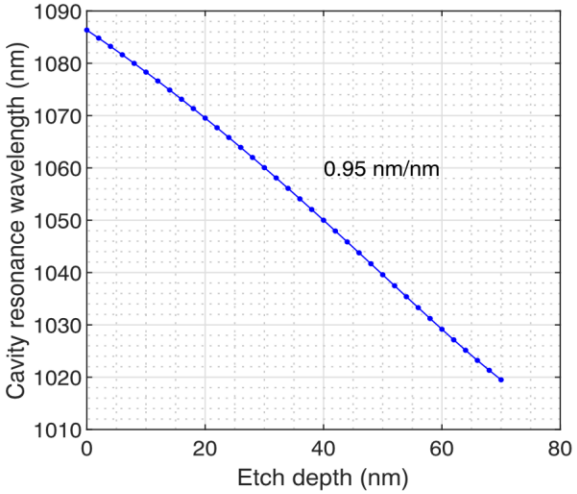

Fig. 3. Resonance wavelength vs. etch depth into the current injection layer.

single-mode oxide-confined VCSEL, the size of the oxide aperture also has an effect on the resonance wavelength since the effective mode index varies with the mode size. We therefore also calculated the variation of resonance wavelength with etch depth for an aperture size from 4 to 10 μm, using a 2D effective index method [26], and found that a variation of the aperture/mode size shifted the wavelengths by less than 0.5 nm from the wavelengths predicted by the 1D effective index method.

For uniform performance in terms of threshold current and slope efficiency over a certain wavelength range, the spectral dependence of a number of parameters has to be considered. This includes the DBR reflectances, the optical confinement factor (since the optical standing wave moves with wavelength and therefore the overlap with the QWs depends on wavelength), and the optical gain in the QWs. With proper spectral alignment, the wavelength dependence of threshold gain can balance the spectral dependence of optical gain, resulting in small variations of threshold current over wavelength. Likewise, small variations of slope efficiency can be achieved by spectral matching of the DBR reflectances.

Fig. 4 shows the spectral reflectance of the 30.5 pair GaAs/AlGaAs bottom-DBR and the 6 pair dielectric SiO_2/TiO_2 top-DBR (with light incident from the cavity), calculated using the transfer matrix method [27]. The refractive indices of the semiconductor layers were calculated using the Afromowitz model [28] while the refractive indices of the dielectric layers (deposited by sputtering) were extracted from measurements using ellipsometry (1.4476 for SiO_2 and 2.3074 for TiO_2 at 1050 nm). Fig. 4 further shows that the bottom-DBR is spectrally aligned to the highest reflectance region of the top-DBR. It also shows the much

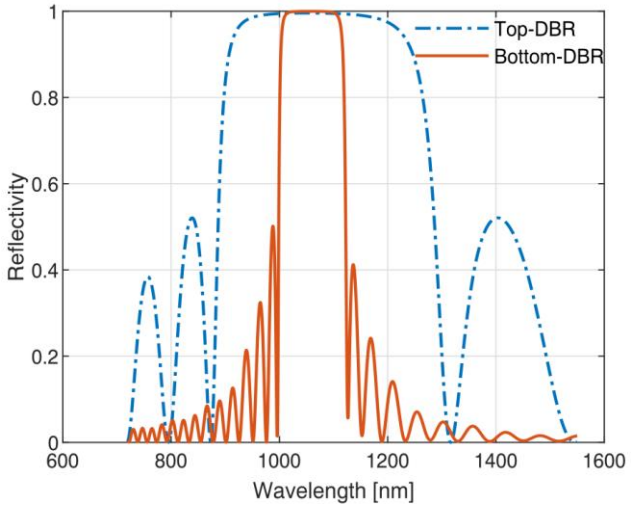

Fig. 4. Spectral reflectance of the semiconductor bottom-DBR and the dielectric top-DBR.

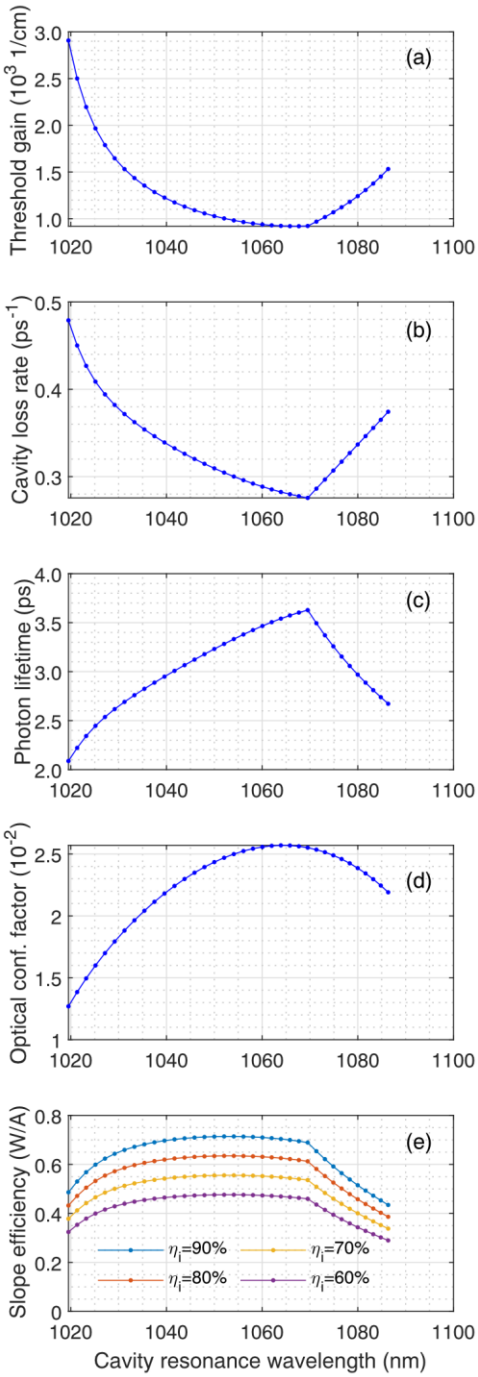

Fig. 5. Calculated dependence of (a) threshold gain, (b) cavity loss rate, (c) photon lifetime, (d) optical confinement factor, and (e) slope efficiency on wavelength. The slope efficiency is calculated at different internal quantum efficiencies (η_i).

wider stopband of the dielectric DBR due to the larger index contrast. Therefore, the width of the stopband of the bottom-DBR (63 nm for reflectivity higher than 99.9%), together with the spectral dependence of optical gain, sets a limit on the achievable wavelengths with uniform performance.

The calculated variation of important resonator parameters (threshold gain, cavity loss rate, photon lifetime, optical confinement factor, and slope efficiency) with wavelength (etch depth, Fig. 3) is shown in Fig. 5. The slope efficiency is calculated for different internal quantum efficiencies. The large increase of threshold gain and cavity loss and decrease of photon lifetime and slope efficiency at wavelengths >1070 nm is caused by a highly doped 20 nm thick region at the top of the p-type current injection layer used for the formation of a low resistance p-contact. The high concentration of holes in this layer (higher than in other parts of the current injection layer) results in high optical loss due to free-carrier absorption. Therefore, etching through this layer is required, which limits wavelengths to less than 1070 nm. The accelerating increase of cavity loss at short wavelengths, and the associated increase of threshold gain and decrease of photon lifetime and slope efficiency is caused by a reduction of the bottom-DBR reflectance as the wavelength approaches the edge of the stopband.

The resulting dependence of threshold gain on wavelength at wavelengths <1070 nm shows an increase of threshold gain with decreasing wavelength (Fig. 5(a)). This is to balance the spectral dependence of threshold gain against the spectral dependence of optical gain for uniformity of threshold current over wavelength. The optical gain and spontaneous emission characteristics of the active region were calculated using SimuLase [29], which is based on microscopic many-body models. First, spontaneous emission spectra were calculated for QW thicknesses from 5.5 to 6.0 nm at a carrier density of 2×10^{17} cm^{-3} (Fig. 6), which is the estimated carrier density generated when performing photoluminescence (PL) measurements on active region calibration samples. The measured PL peaks at 1044 nm, which suggests that the actual thickness of the QWs is 5.7 nm. This is therefore the QW thickness used for the gain calculations. Fig. 7 shows the spectral gain characteristics at carrier densities from 1.8×10^{18} cm^{-3} to 3.5×10^{18} cm^{-3}, where we have also inserted the spectral dependence of threshold gain from Fig. 5(a). From this, the spectral dependence of threshold carrier density can be calculated. This is shown in Fig. 8. Clearly, the higher gain on the short wavelength side of the gain peak at a given carrier density balances the higher threshold gain at short wavelengths, resulting in a weak and symmetric dependence of threshold carrier density on wavelength around ~1050 nm. This should be reflected in the wavelength dependence of the threshold current.

In the following section, we investigate the uniformity of threshold current and slope efficiency for VCSELs over the spectral range of interest, with wavelengths set by intra-cavity phase tuning. This is in order to verify the critical requirements of spectral matching and balancing for uniformity suggested by the numerical simulations.

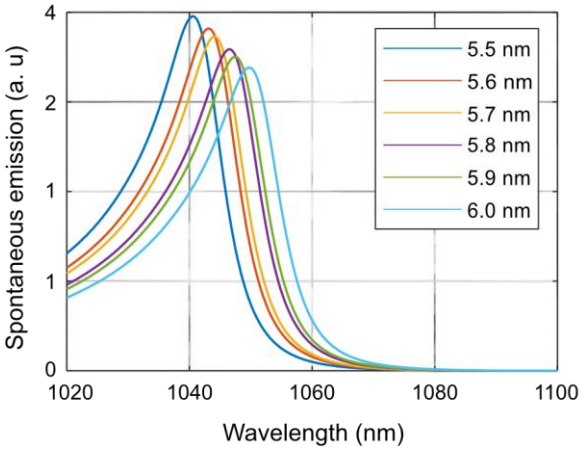

Fig. 6. Spontaneous emission spectra of the active region for different QW thicknesses (5.7-6.0 nm) at a carrier density of 2×10^{17} cm^{-3}.

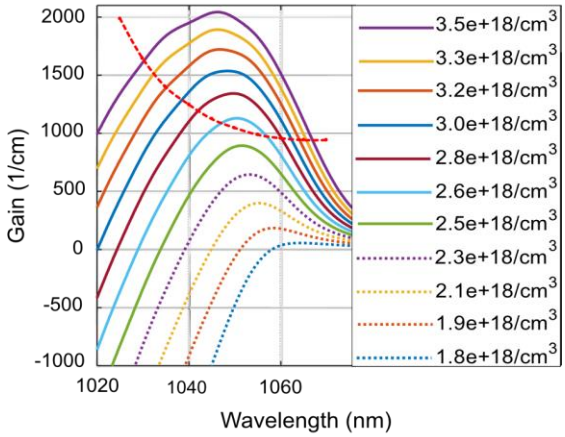

Fig. 7. Gain spectra for 5.7 nm thick QWs at different carrier densities. The carrier densities are listed in the inset. The dashed line shows the threshold gain from Fig. 5(a).

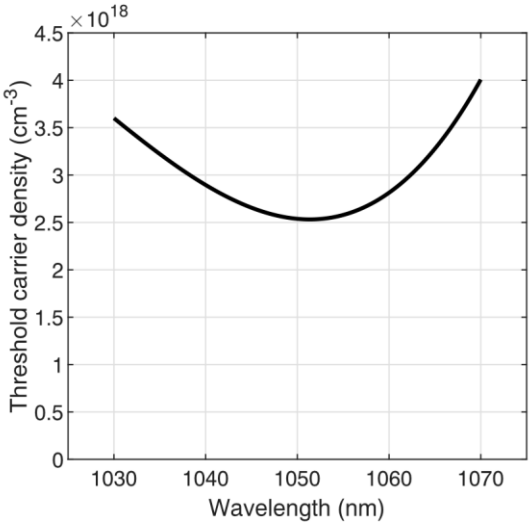

Fig. 8. Calculated threshold carrier density vs. wavelength from Fig. 7.

III. Experimental Verification

Among the steps involved in the fabrication of intra-cavity phase tuned VCSELs, thinning of the current injection layer by etching and dielectric DBR deposition are most critical.

VCSELs were fabricated on ~1 cm^2 wafer pieces, with each piece divided into four quadrants. In each quadrant, the current injection layer was thinned by dry etching. The difference in etch depth between quadrants is ~8 nm to reach the target 8 nm wavelength spacing.

To have a stable, precise, and reproducible etch rate for thinning the current injection layer, Ar ion-beam etching with neutral ions (pure physical etching) was used [24]. The etching was done in an Oxford Ionfab 300 Plus system equipped with an emitter for neutralizing the ion beam. The ion-beam current (controlling the ion density) and voltage (controlling the ion kinetic energy) were set at low values of 3 mA and 300 V, respectively, to have a low etch rate of ~0.5 Å/s [24]. The Ar flow rates for both the beam and the neutralizer were set at 4 sccm and the sample was rotated at 3 rpm during etching to have a uniform etch depth. Four etch steps were used. In the first step, the entire wafer was thinned below the thickness of the highly doped top part of the current injection layer. The subsequent etch steps, following masking of different quadrants by photoresist (AZ1512), were used to reach four levels of etching and therefore four wavelengths. The ±1 nm precision in etch depth achieved with the slow and physical etch process [24] will set the wavelengths, and therefore the spacing between wavelengths, with an accuracy of ±1 nm (Fig. 3). Following each etch step, the surface roughness was also examined using atomic force microscopy (AFM, SPM-Bruker Dimension 1300). It was found that the roughness of the etched surface was the same as that of an unetched surface [24]. This is essential since the surface is at the interface to the dielectric DBR where the optical field intensity is high (Fig. 2). Excessive roughness would scatter light and deteriorate VCSEL performance.

The dielectric DBR, composed of 6 pairs of SiO_2 and TiO_2 with quarter-wavelength thickness at 1050 nm (181.3 nm for SiO_2 and 113.8 nm for TiO_2), was deposited by sputtering. The thickness and refractive index of each layer were measured by ellipsometry. This was done by simultaneous deposition on an adjacent silicon wafer at each layer deposition. This minimizes the errors in thickness and refractive index, which is essential since errors, in the first pair in particular, also have an effect on the resonance wavelengths [24].

Upon close inspection of the epitaxial material, it was found that the thickness of the p-type current injection layer was thinner than specified, resulting in a resonance wavelength of 1064 nm before thinning, compared to the target 1086 nm (Fig. 3). This was compensated for by the deposition of an extra 58.8 nm thick TiO_2 layer before dielectric top-DBR deposition. The required thickness of this layer was determined using the 1D effective index method.

Following fabrication, we measured output power as a function of current (Fig. 9) and spectra (Fig. 10) for VCSELs at the four different wavelengths at 25 and 60°C. At a given

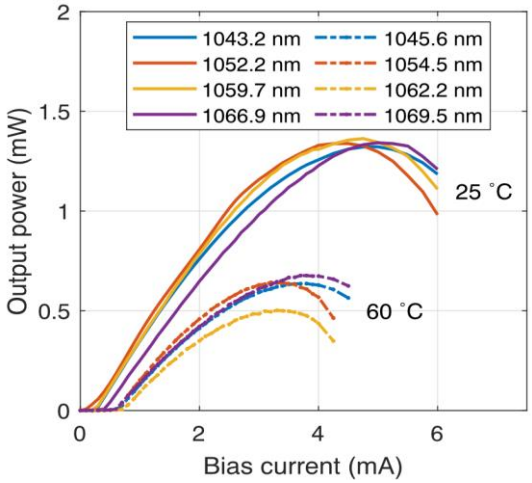

Fig. 9. Output power vs. current at 25 and 60°C for VCSELs at the four wavelengths shown in the inset. The wavelengths were measured at a current of 1 mA (Fig. 10).

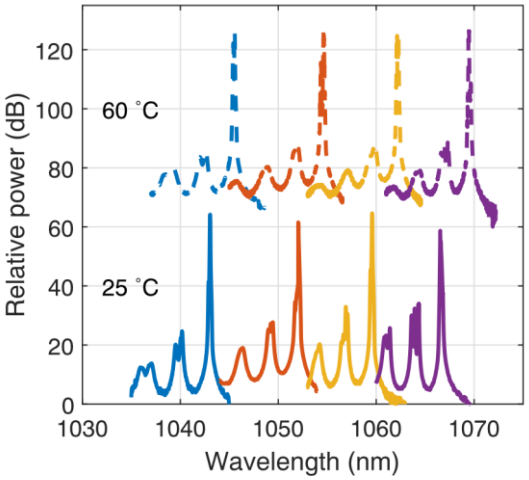

Fig. 10. Spectra at 1 mA for VCSELs at the four wavelengths at 25 and 60°C.

etch depth (wavelength) and target aperture diameter, there is a small variation in performance among VCSELs. This is due to small variations of the oxide aperture diameter. However, for the same aperture size, performance is uniform and reproducible. The VCSEL performance shown is typical for VCSELs with the same aperture size.

All VCSELs, with an oxide aperture diameter of 4 µm, are single-mode as required for efficient coupling through a grating coupler on a SiN platform for multiplexing. The suppression of higher order transverse modes exceeds 25 dB at a current of 1 mA (Fig. 10). The wavelengths are positioned in the spectral range 1043-1067 nm at 25°C and the spacing between wavelengths is 8 ± 1 nm as expected from the precision in etching and the dependence of wavelength on etch depth (Fig. 3).

Using the power vs. current characteristics in Fig. 9, we extract threshold currents and slope efficiencies and examine their uniformity over wavelength. At 25°C, the slope efficiency is close to constant at 0.47 W/A at the shorter wavelengths and drops to 0.41 W/A at the longest wavelength. This is in agreement with the simulations (Fig. 5(e)). For an

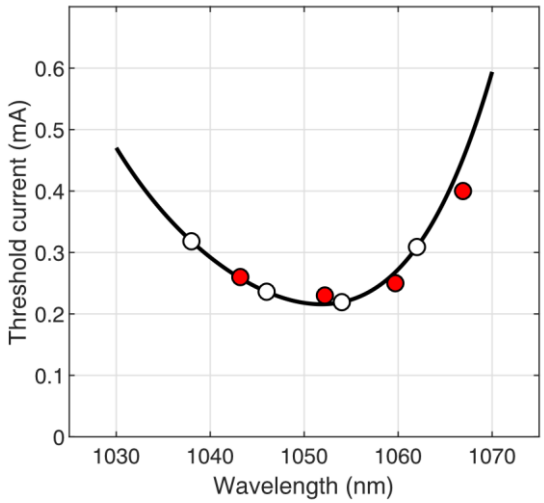

Fig. 11. Calculated threshold current (multiplied by a factor of 2.75) vs. wavelength at 25°C for 4 µm aperture VCSELs. The filled symbols show the measured threshold currents. The open symbols show that best uniformity with an 8 nm wavelength spacing would be achieved with the wavelength grid centered around 1050 nm.

estimation of internal quantum efficiency, we use the slope efficiency measured for larger aperture multimode VCSELs since larger aperture VCSELs do not suffer from as much optical scattering at the aperture as small aperture VCSELs [30]. VCSELs with a 10 µm aperture have a slope efficiency of 0.6 W/A at 25°C, which suggests an internal quantum efficiency of ~75%.

The maximum output power of these small 4 µm aperture VCSELs is limited to about 1.4 mW at 25°C. Higher single-mode power can be achieved by e.g., larger aperture/lower resistance VCSELs with an integrated mode filter for higher order mode suppression [31].

The differential resistance at 3 mA is ~300 Ω for the 4 µm aperture VCSELs. There is a small variation among VCSELs at different wavelengths, which is not correlated with the etch depth. Therefore, thinning of the current injection layers seems to have a minor impact on resistance.

The measured threshold currents are shown in Fig. 11. To compare with the expected variation of threshold current (I_{th}) with wavelength, we use the wavelength dependence of the threshold carrier density (n_{th}) from Fig. 8 and estimate the threshold currents from a balance between current injection and spontaneous recombination at threshold:

$$\frac{\eta_i I_{th}}{qV_a} = R_{sp}(n_{th}) \tag{1}$$

where η_i is the internal quantum efficiency, q is the electron charge, V_a is the active region volume, and R_{sp} is the spontaneous recombination rate. We further assume that spontaneous recombination is dominated by spontaneous emission and Auger recombination:

$$R_{sp}(n_{th}) = Bn_{th}^2 + Cn_{th}^3 \tag{2}$$

where B is the bimolecular recombination coefficient and C is the Auger recombination coefficient. With an internal quantum efficiency of 75% and using values of 1×10^{-10} cm^3/s and 8×10^{-30} cm^6/s for the bimolecular and Auger recombination coefficients [32], respectively, we find the dependence of threshold current on wavelength shown by the curve in Fig. 11. To fit to the measured threshold currents, we have multiplied the calculated threshold currents from equation (1) by a factor 2.75. This accounts for e.g., current spreading under the oxide aperture, optical scattering in the small aperture, and uncertainties in the recombination parameters. However, this is only to show the stronger dependence of threshold current than threshold carrier density on wavelength because of the square and cubic dependence of spontaneous recombination on carrier density in equation (2).

The estimated dependence of threshold current on wavelength (Fig. 11) agrees well with the calculated. Fig. 11 also shows that a blue-shift of the wavelength grid by ~5 nm (centering the grid around ~1050 nm) would result in even more uniform threshold currents over the four wavelengths.

IV. Conclusion

We have performed a numerical analysis of the requirements of spectral matching and balancing for uniformity of threshold current and slope efficiency over wavelength for VCSELs with wavelength set by intra-cavity phase tuning in a post-growth fabrication process. The spectral dependencies of DBR reflectances, optical confinement, and optical gain are accounted for. We have also verified the requirements by fabrication and testing of GaAs-based intra-cavity phase tuned single-mode VCSELs in the spectral range 1043-1067 nm with 8 nm wavelength spacing. Small variations of threshold current and slope efficiency are achieved by close to ideal spectral matching and balancing. The precise Ar ion-beam etching technique used allows for setting wavelengths and channel spacing with a precision of ±1 nm.

We conclude that optimum uniformity of threshold current and slope efficiency over the wavelength range considered (24 nm, to accommodate e.g., 4 wavelengths with 8 nm spacing) is demanding in terms of spectral matching and balancing. Only a few nm shift of wavelengths, DBR stopbands, or gain spectrum will have a strong effect on uniformity. Therefore, not only very precise etching for intra-cavity phase tuning and precise thickness of the layers in the dielectric top-DBR are needed, but also precise thickness and composition of the layers in the epitaxial semiconductor part containing the bottom n-DBR, the active region, and the p-current injection layer. Even with state-of-the-art equipment for epitaxial growth, etching, and deposition, this is challenging for the fabrication of monolithic multi-wavelength VCSEL arrays with uniform performance on full 4” or 6” wafers.

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