Thesis for the Degree of Licentiate of Engineering

Theory and Design of Efficient Active Load Modulation Power Amplifiers

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Abstract

The increasing demand for mobile data traffic has put new challenges and requirements for the development of the wireless communication infrastructure. The performance of the RF power amplifier (PA) is, in particular, of great importance, since it is the key building block for microwave transmitters in base stations and radio link equipment. The energy and bandwidth efficiency of the PA is vital for maximized channel capacity, reduced operational cost, and further integration. Among the efficiency enhancement techniques, active load modulation is one of the most widely used techniques. The overall objective of this thesis is to improve the average efficiency and bandwidth performance in active load modulation PAs for future wireless systems.

In the first part of the thesis, an analytically based combiner synthesis approach for the three-stage Doherty PA (DPA) is proposed and presented. A compact output combiner network, together with the input phase delays, is derived directly from transistor load-pull data and the PA design requirements. The technique opens up new design space for three-stage DPAs with reconfigurable high-efficiency power back-off levels. The utility of the proposed technique is demonstrated by the implementation of a 30-W gallium nitride (GaN) three-stage DPA prototype at a center frequency of 2.14 GHz. Measurement results show that the prototype circuit can linearly reproduce 20-MHz long-term evolution signals with 8.5- and 11.5-dB peak-to-average power-ratio (PAPR), providing average efficiencies of 56.6% and 46.8% at an average output power level of 36.8 and 33.8 dBm, respectively.

In the second part of the thesis, a novel PA architecture, the circulator load modulated amplifier (CLMA) is proposed and demonstrated. The CLMA is able to maintain high efficiency over large output power dynamic ranges. Moreover, the availability of wideband and low-loss circulators makes this architecture promising for wideband applications. Consequently, it has the potential to overcome many of the drawbacks of other architectures. The fundamental operational principle and theoretical performance of the CLMA are studied and presented. As a proof of concept, a demonstrator circuit based on GaN transistors is designed and characterized at 2.09 GHz. Measurement results show that the peak output power is 43.1 dBm and the drain efficiency is 73% at 6-dB output power back-off level.

In summary, the thesis presents two promising PA architectures for efficiency enhancement. The results of this thesis will therefore contribute to the development of energy efficient PAs for future mobile communication systems.

Keywords: Combiner synthesis, Doherty power amplifier, energy efficiency, deep power back-off, GaN, circulator, non-reciprocity, CLMA

List of Publications

Appended Publications

This thesis is based on work contained in the following papers:

[A] **H. Zhou**, J.-R. Perez-Cisneros, B. Langborn, T. Buisman and C. Fager, "A Generic Theory for Design of Efficient Three-stage Doherty Power Amplifiers," accepted for publication in *IEEE Trans. Microw. Theory Techn.*, Sep. 2021.

[B] **H. Zhou**, J.-R. Perez-Cisneros and C. Fager, "Circulator Load Modulated Amplifier: A Non-Reciprocal Wideband and Efficient PA Architecture," *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 603-605.

Other Publications

The content of the following publications partially overlaps with the appended papers or is out of the scope of this thesis.

[a] P. Saad, **H. Zhou**, J.-R. Perez-Cisneros, R. Hou, C. Fager and B. Berglund, "Doherty Load Modulation Based on Non-Reciprocity," accepted for a presentation at *European Microwave Conference,* 2021.

[b] J.-R. Perez-Cisneros, **H. Zhou**, C. Fager and K. Buisman, "Emulation of Non-Reciprocity applied in Load-Modulated Power Amplifier Architectures using Single Amplifier Load-Pull Measurements," accepted for a presentation at *European Microwave Conference,* 2021.

Notations and Abbreviations

Notations

α	Current ratio
β	Normalized input voltage level
β_B	Normalized input voltage at the back-off level
γ_B	Output power back-off levels
η	Drain efficiency
φ	Input current phase delay
θ	Output current phase delay
I_m	Current following through the main amplifier
I_a	Current following through the auxiliary amplifier
V_m	Output voltage of the main amplifier
V_a	Output voltage of the auxiliary amplifier
V_{ds}	Drain-source bias voltage
P_{DC}	DC power
P_L	Power delivered to the load termination
R_L	Load resistance
$\Re$	Function that gives the real part of a complex number

Abbreviations

ACLR	Adjacent Channel Leakage Ratio
ALM	Active Load Modulation
Aux	Auxiliary amplifier
CLMA	Circulator Load Modulated Amplifier
CW	Continuous Wave
DEPA	Distributed Efficient Power Amplifier
DLM	Dynamic Load Modulation
DPA	Doherty Power Amplifier
DSM	Dynamic Supply Modulation
DPD	Digital Predistortion
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
GaN	Gallium Nitride

LMBA	Load Modulated Balanced Amplifier
LTE	Long Term Evolution
Main	Main amplifier
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
RF	Radio Frequency
Si	Silicon

Contents

Chapter 1

Introduction

1.1 Motivation

The development of wireless communication technology has changed people's daily life significantly. The pandemic that started last year has also greatly impacted everyone's life and shaken the world's economy. Many social activities are taking place online during the pandemic, for instance, attending meetings and conferences, taking and teaching courses, and even socializing with friends. Faster and more reliable communication is, therefore, a desire from more and more users and societies.

In 2021, the global mobile data traffic has shown a 3-fold growth compared to the year 2018. The total number of Internet users throughout the world is projected to grow from 3.9 billion in 2018 to 5.3 billion by 2023 at a global yearly Internet user growth of 6 percent. In terms of population, this represents 51 percent of the global population in 2018 and 66 percent of global population penetration by the year 2023 [1]. Moreover, a 4-fold growth in data traffic from the year 2021 to 2026 is predicted [2], as shown in Fig. 1.1. The total number of mobile subscriptions is expected to be around 8.8 billion, among which there will be 3.5 billion 5G subscriptions globally, accounting for around 40 percent of all mobile subscriptions, by the end of 2026 [2]. To a large extent, this trend is driven by the ubiquitous connectivity realized through smartphones, tablets, the internet of things, smart homes and cities, autonomous vehicles and wearable technology, etc.

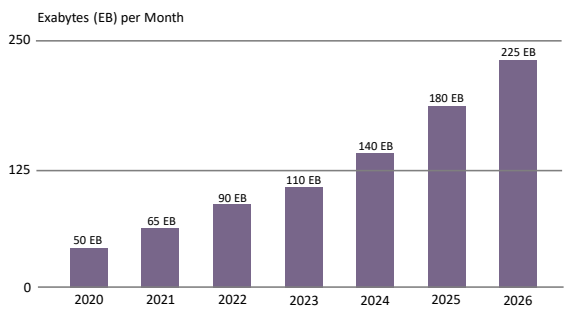


Figure 1.1: Projection of global mobile data traffic [2]

To cope with the increasing demand for mobile data traffic, there are many challenges in the development of the wireless communication infrastructure [3–5]. In particular, the performance of microwave transmitters is of great importance, and they are the key building blocks for any base station and radio link equipment. There are two main performance aspects of the microwave transmitter to enable high capacity, low cost and high speed of the wireless connections [6]: energy efficiency and bandwidth. The energy efficiency is perhaps the most important property of the transmitter, because its power consumption corresponds to a large part of the overall mobile network operational cost [7]. Moreover, the power consumption of transmitters increases the system complexity considerably since cooling equipment is often required to deal with heat dissipation. The cooling equipment draws a significant amount of power, which further multiplies the energy consumption because of low efficiency. The bandwidth performance is another important attribute. The scarcity of the frequency spectrum and the need for frequency planning has resulted in a widespread of carrier frequencies, therefore it is preferable if the PA can cover more frequency bands to reduce the system complexity and cost.

The essential building block of all mobile microwave transmitters is the power amplifier (PA). Its role is to amplify the signal power for achieving required system performance to ensure desired signal coverage. The two important performance aspects of microwave transmitters mentioned above result in profound impacts on the PA design requirements.

1.2 Efficiency enhancement techniques

The increasing demand on the spectrum efficiency in modern wireless communication systems requires more complex modulation schemes, thereby leading to communication signals with high peak-to-average-power ratio (PAPR). Consequently, PAs should be able to provide high efficiency over a large range of output power levels to ensure a high average energy efficiency when amplifying these high-PAPR communication signals [8]. Moreover, it is important that PAs can operate over larger bandwidth to support diverse signal bandwidth and frequency bands due to the increasing high data rate and scarcity of the available frequency spectrum. Over the decades, many efforts have been put into the research on enhancing the PA efficiency at its power back-off levels. Essentially, two types of efficiency-enhancement architectures can be found in literature: supply modulation and load modulation.

The supply modulation architecture often utilizes one additional control path, together with the PA path, to dynamically modulate the supply voltage of the PA path based on the signal envelope. An envelope elimination and restoration (EER) technique was firstly introduced in 1952, by L. Kahn [9], it was thereafter further improved and evolved to the envelope tracking (ET) technique in 1983 by A. Saleh and D. Cox [10], which is the most common supply modulation technique nowadays.

The load modulation technique can be divided into two types of architectures. One is referred to as dynamic load modulation (DLM) [11, 12], where tunable elements, such as switches or varactors, are used to modulate the load impedance of the PA as the signal envelope varies. The other is referred to as active load

modulation (ALM). Unlike the DLM, the ALM utilizes active current injection to modulate the load impedance. The ALM architectures employ multiple PAs that interact with each other through an output combiner network to enhance the PA back-off efficiency. Two of the most common ALM architectures are the outphashing and Doherty PA (DPA). The outphasing PA, originally introduced by H. Chireix in 1935 [13], uses two nonlinear outphased amplifiers with constant envelope to achieve load modulation. Whilst the DPA, which was firstly proposed by W. Doherty in 1936 [14], relies on the active current injection from the main and auxiliary amplifiers, together with a static phase delay between them, to realize the load modulation.

The DPA can be constructed with an analog input power splitter, proper phase delays and gate bias of the amplifier cells, and an output load modulation network. This makes the DPA a widely adopted architecture that does not require dual/multiple input or external control circuitry. The combination of efficiency enhancement and relatively simple circuit implementation has made the DPA by far the most attractive architecture in cellular base stations [15,16]. The drawback of the DPA is the limited RF bandwidth due to the transistor parasitics and the load modulation network [17], which is ideally realized by a quarter-wavelength transformer. Plenty of research has focused on techniques to improve the bandwidth of the DPA by the parasitic absorption into the load modulation network [18–20] and/or direct modifications of the load modulation network [21–26]. The bandwidth of the DPA is, however, still inherently limited by the output combiner network. To resolve this problem, several novel PA architectures with high efficiency and potential for wideband operations have been proposed recently, including the distributed efficient power amplifier (DEPA), originally proposed in [27], the load modulated balanced amplifier (LMBA), initially introduced in [28], and the circulator load modulated amplifier (CLMA) firstly proposed in [Paper B].

1.3 Thesis scope and outline

In the first part of this thesis, the research goal is to investigate the operational principle and theoretical performance of the most widely used PA architecture in microwave transmitters for mobile communications, i.e., the DPA. The theory of the traditional two-way DPA is reviewed. To cope with modern communication signals with even higher PAPR, the operation of the three-stage DPA is also introduced and reviewed. A generic theory for the design of three-stage DPA, based on [Paper A], is thereafter presented. The second part of the thesis first reviews the recently published load modulated PAs with high efficiency and wide bandwidth. It thereafter proposes a new PA architecture, referred to as CLMA, based on [Paper B]. The CLMA architecture can operate efficiently over large output power dynamic ranges. Moreover, compared to the DPA, the CLMA has great potential for wideband operation.

The thesis is organized as follows: Chapter 2 reviews the operation principles of the two-way DPA architectures and the analytical load-pull based combiner synthesis approach for two-way DPA. In Chapter 3, the theory of conventional and modified three-stage DPAs is reviewed. Based on [Paper A], a generic theory for the design of efficient three-stage DPA based on the analytical

combiner synthesis approach is then introduced. Chapter 4 reports a novel active load-modulation PA architecture with a non-reciprocal output combiner, based on [Paper B]. Finally, the thesis is concluded in Chapter 5 and future work is discussed.

Chapter 2

The two-way Doherty power amplifier

In the previous chapter, it was mentioned that many PA architectures have been proposed to enhance the PA back-off efficiency, and thereby improve the average efficiency of microwave transmitters with modern communication signals. Among those architectures, the DPA is established as the most popular architecture deployed in cellular base stations due to its simple circuit structure.

The purpose of this chapter is, to provide a complete analysis and comparison of different two-way DPA configurations. Then follows a review and explanation of an analytical load-pull based combiner synthesis approach for the practical design and implementation of the two-way DPA. This will form the basis for the analysis of the three-stage DPA in the following chapter.

2.1 Theory and operational principle

Figure 2.1 shows the basic configuration of the two-way DPA, which comprises a main (Main) and an auxiliary (Aux) amplifier cell, combined via a passive output combiner, and an input phase shifter to provide proper phase delay between the two branches. The working principle of the two-way DPA is that the impedance seen by the class-B biased Main cell is modulated through active current injection using the class-C biased Aux cell. This allows high efficiency to be maintained over a large range of output power.

The analysis of an ideal two-way DPA adopted here assumes that the transistors for the Main and Aux are modeled as ideal piece-wise voltage-controlled linear current sources with zero knee voltage. Under this assumption, higher harmonic components are short-circuited, and only the fundamental component is considered. The same drain bias and upper drain voltage limit are used for both the Main and Aux cells. Note that the above assumptions are adopted in the subsequent theoretical analysis throughout the entire thesis.

The analysis also assumes a representation where the load is initially merged with the two-way DPA output combiner into a reciprocal and lossy two-port combiner network. The realization of the actual combiner network involves a conversion from the lossy two-port network into a lossless three-port network

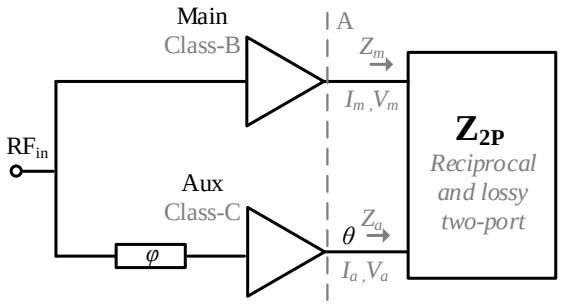


Figure 2.1: Block scheme of the generalized two-way DPA. The lossy and reciprocal two-port output combiner network is denoted as $\mathbf{Z_{2P}}$. Plane A represents the output plane of the amplifier cells. The input and output current phase delays are denoted as φ and θ, respectively.

terminated with a purely resistive load, which will be discussed in the next section. The impedance parameters of the reciprocal and lossy two-port combiner, $\mathbf{Z_{2P}}$, are derived using ideal current source models. The voltages and currents at the output of the Main and Aux cells are related through $\mathbf{Z_{2P}}$ as

$$\begin{bmatrix} V_m \\ V_a \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{12} & Z_{22} \end{bmatrix} \begin{bmatrix} I_m \\ I_a \end{bmatrix}, \tag{2.1}$$

where $Z_{12} = Z_{21}$ since the network is assumed to be reciprocal. The Main and Aux cells are represented by current sources having fundamental output currents I_m and I_a, respectively, that depends on the input voltage drive level $(0 \leq \beta \leq 1)$ as

$$I_m = \beta i_{m,M}, \tag{2.2}$$

$$I_a = \begin{cases} 0, & 0 \leq \beta \leq \beta_B \\ \left(\dfrac{\beta - \beta_B}{1 - \beta_B}\right) i_{a,M} \cdot e^{-j\theta}, & \beta_B \leq \beta \leq 1 \end{cases}, \tag{2.3}$$

where $i_{m,M}$ and $i_{a,M}$ are the maximum fundamental current magnitude from the Main cell and the Aux cell, respectively.

The amplitude of the output voltage from the Main cell should be kept constant and equal to its drain-source bias voltage V_{ds} all over the higher power region (when $\beta_B < \beta \leq 1$) to guarantee full utilization of its voltage swing capability, thereby ensuring high-efficiency operation. To fully determine the operation of the DPA, the current ratio between the maximum current of the Aux and Main cell should be decided as well. When this current ratio (α) is related by

$$\alpha = \frac{i_{a,M}}{i_{m,M}} = \frac{1}{\beta_B} - 1, \tag{2.4}$$

the resulting two-way DPA, as shown in Figure 2.2, has the commonly adopted configuration, where the Main and the Aux cells are combined via a $\lambda/4$-transmission line with a characteristic impedance $Z_T = R_{opt}$ at the output of the Main cell, and connected to a load $R_L = \beta_B R_{opt}$. Note that R_{opt} is the optimum class-B load resistance. Meanwhile, the input consists of a power

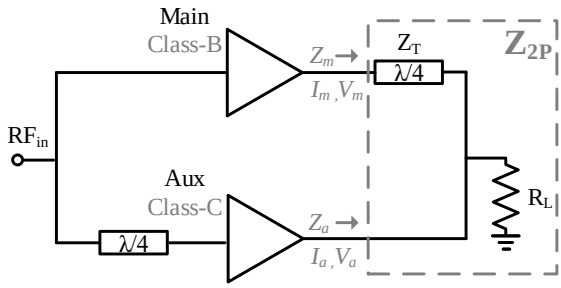


Figure 2.2: The conventional two-way DPA.

splitter and another $\lambda/4$-transmission line at the Aux input to provide the equal phase delay through the two amplifier paths. Figure 2.3 presents the current and voltage drive profiles of the Main and Aux cells from the two-way DPA with different back-off levels (β_B). The current profiles are normalized to the maximum saturated current and the voltage profiles are normalized to the drain-source bias voltage V_{ds}. To calculate the efficiency of the amplifier, the power delivered to the output load and DC-power consumption are first identified [29]:

$$P_L = R_L(I_m + I_a)^2 = \beta R_{opt}(I_m + I_a)^2, \tag{2.5}$$

$$P_{DC} = \frac{2V_{ds}(|I_m| + |I_a|)}{\pi}. \tag{2.6}$$

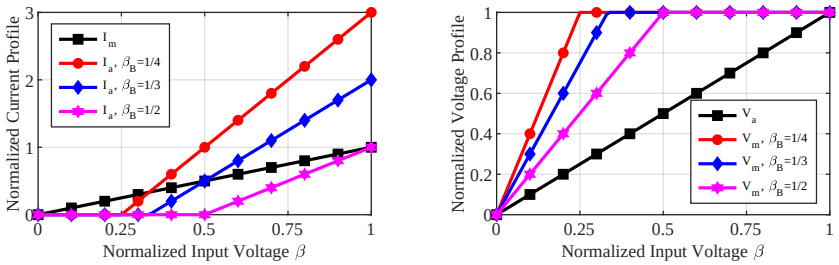
The drain efficiency (η) is therefore given by

$$\eta = \frac{P_L}{P_{DC}} = \frac{\pi\beta R_{opt}(I_m + I_a)^2}{2V_{ds}(|I_m| + |I_a|)}. \tag{2.7}$$

It should be stressed that the above calculation for the ideal PA efficiency is adopted in the subsequent theoretical analysis throughout the entire thesis.

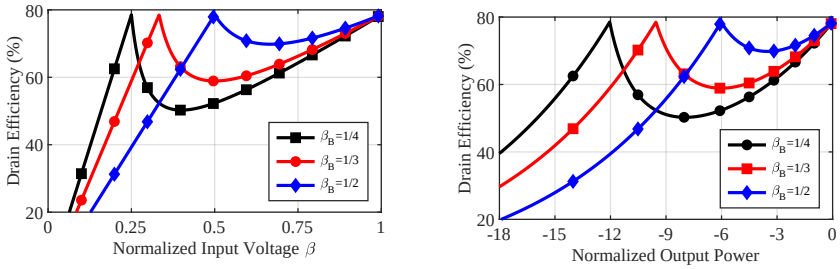
It can be observed from Figures 2.3 and 2.4 that, in order to increase the high-efficiency back-off power level of the two-way DPA, the current ratio (α) needs to be increased as well. The standard two-way DPA [14] enhances its efficiency at 6-dB output power back-off. It also requires the same fundamental current from the Main and Aux cells at the maximum drive level. The asymmetrical two-way DPA [30, 31], on the other hand, typically requires unequally sized Main and Aux cells to provide asymmetrical current ratios for extended high-efficiency output power back-off ranges. Note that the fundamental operation principle of the N-way DPA [32] is basically the same as the asymmetrical two-way DPA. The only difference is that the N-way DPA uses multiple Aux cells to achieve the asymmetrical current ratios, thereby increasing the high-efficiency output power back-off range.

It should be noticed that, as presented in Figure 2.4, the asymmetrical two-way DPA exhibits a significant drop in efficiency in the regions between the efficiency peaking points, especially for large output power back-off levels.



(a) (b)

Figure 2.3: (a) Normalized amplitude of the output currents and (b) output voltage profiles of the two-way DPA versus normalized input drive voltage, for $\beta_B = 1/4$, $1/3$, and $1/2$.



(a) (b)

Figure 2.4: Drain efficiency of the two-way DPA versus (a) normalized input drive voltage, and (b) normalized output power, for $\beta_B = 1/4$, $1/3$, and $1/2$.

2.2 The black-box combiner synthesis approach

The theoretical analysis in the previous section assumes that the transistors are represented by ideal current sources. However, in reality, the parasitic and non-linear effects of real transistors are significant, especially at microwave frequencies. The operation of real transistors, therefore, deviates greatly from that of ideal current sources. Figure 2.5 shows a typical realization of a two-way DPA, where additional offset lines and matching networks at the output of the Main and Aux cells are often adopted to accommodate the non-ideal behavior of real transistors at microwave frequencies.

By simply comparing Figure 2.2 with Figure 2.5, it is clear that the DPA implementation plays an important role in its performance. To fully utilize the transistor capabilities, instead of using fixed combiner topology as the conventional DPA, it is beneficial to use the transistor load-pull data and synthesize the entire combiner network directly to satisfy the high efficiency operating conditions. The load-pull based combiner synthesis approach, also referred to as the black-box combiner synthesis approach, was therefore proposed and demonstrated on a two-way DPA [33]. It was shown that the technique allows for an extended back-off efficiency range with identically sized Main and Aux transistors. It was then also extended to design an outphasing PA [34]. Moreover, the black-box approach was further explored for improving

linearity [35] and increasing PA-antenna integration [36, 37] in a microwave transmitter.

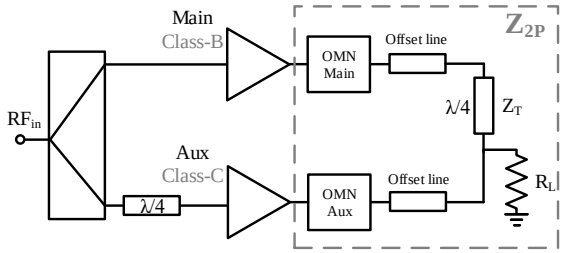


Figure 2.5: Typical realization of a two-way DPA.

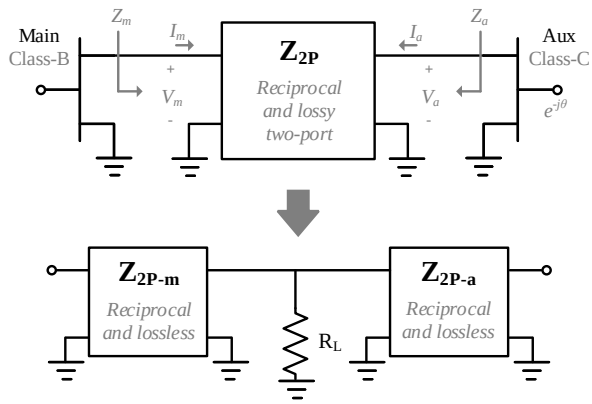


Figure 2.6: Block diagram of the conversion from the reciprocal lossy two-port combiner network to the reciprocal lossless three-port network terminated with a resistive load.

As presented in Figure 2.6, the black-box approach begins with the analytical synthesis of the reciprocal and lossy two-port DPA combiner with the load embedded [38]. Its impedance matrix is denoted $\mathbf{Z_{2P}}$. Note that the synthesis is based on the large-signal load-pull simulations or experiments, including the optimal output impedance at peak power and power back-off, as well as the off-state output impedance from the Aux transistor. To allow the lossy combiner network to be represented as a combination of two lossless networks ($\mathbf{Z_{2P-m}}$ and $\mathbf{Z_{2P-a}}$), together with a purely resistive load, e.g., a 50 Ω load, the following boundary condition should be satisfied [33]

$$\Re\{Z_{12}\}^2 = \Re\{Z_{11}\}\Re\{Z_{22}\}. \tag{2.8}$$

Together with the boundary condition above, the current phase delay between Main and Aux transistor branches, is determined as well.

After implementation with real circuit components, the combiner derived by the black-box approach often ends up with lower insertion loss and more compact size than other designs as it integrates matching and load-modulation functionality all together in its synthesis. Therefore, the black-box approach is also quite suitable for millimeter-wave integrated circuit designs [39–41], where

low-loss and compact-size combiner network are vital for circuit performance and manufacturing cost.

2.3 Chapter summary

This chapter has presented an idealized theory describing the basic operational principle of the standard and asymmetrical two-way DPAs. The black-box combiner approach, which is able to analytically synthesize the DPA combiner networks from the load-pull data, has been reviewed and demonstrated as well.

It has been shown that the standard two-way DPA was initially proposed to enhance the efficiency ideally up to 6-dB output power back-off. In order to further extend the high-efficiency output power back-off range to cope with the modern communication signals with larger PAPR, the asymmetrical two-way DPA (as well as the N-way DPA) has been reviewed. However, as presented in Figure 2.4, the efficiency of the asymmetrical two-way DPA drops considerably between its high-efficiency back-off and peak power levels when back-off ranges exceed 6 dB, and thus degrades average efficiency for modern communication signals. In the next chapter, the three-stage DPA will be demonstrated and analyzed to resolve this problem.

Chapter 3

The three-stage Doherty power amplifier

In the previous chapter, it was shown that the efficiency of the asymmetrical two-way DPA and N-way DPA drops considerably when trying to enhance the efficiency at deep backed off power levels. Consequently, the concept of the three-stage DPA was initially proposed by F. Raab in 1987 [42] to enhance the efficiency at two different output power back-off levels, denoted by γ_{B1} and γ_{B2} henceforth. Figure 3.1 shows a comparison between the efficiency versus output power performance of standard two-way, asymmetrical two-way, N-way, and three-stage DPAs. Essentially, two different types of three-stage DPA architectures can be found in the literature. One is referred to as the conventional three-stage DPA [43–48]. The other is referred to as the modified three-stage DPA [49–52].

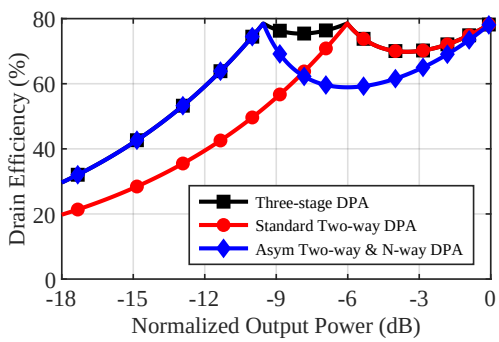


Figure 3.1: Drain efficiency versus normalized output power profiles of different DPA architectures: Standard two-way, asymmetrical two-way, N-way and three-stage.

In this chapter, the operational principle of the conventional and modified three-stage DPA will be firstly reviewed. Using a black-box combiner synthesis approach similar to the two-way DPA in the previous chapter, their operation and analysis are then generalized using the reciprocal and lossy three-port output combiner from the three-stage DPA with the load embedded. An analytical load-pull based three-port combiner synthesis method is thereafter

presented and used to design an ultra-compact and low-loss combiner network for the three-stage DPA. Finally, the design and characterization of a three-stage DPA following the proposed design methodology is demonstrated.

3.1 The conventional three-stage DPA

The operational principle of the conventional three-stage DPA can be described as: Its main amplifier (Main) cell is initially load-modulated by the first auxiliary amplifier (Aux1) cell in the low power region (when $\beta_{B1} < \beta \leq \beta_{B2}$). After that, the second auxiliary (Aux2) cell is turned on to modulate the common load of the two-way DPA, now consisting of the Main and Aux1 cells. Note that the current of the class-B biased Main cell first increases linearly, then it is saturated after the second back-off level, while the class-C biased Aux1 and Aux2 cells turn on sequentially at the first and second back-off levels, respectively.

The Main, Aux1, and Aux2 amplifier cells are represented by the current sources having fundamental output currents I_m, I_{a1} and I_{a2}, respectively, that depend on the input voltage as shown below:

$$I_m = \begin{cases} \left(\dfrac{\beta}{\beta_{B2}}\right) i_{m,M}, & 0 \leq \beta \leq \beta_{B2} \\ i_{m,M}, & \beta_{B2} \leq \beta \leq 1 \end{cases} \tag{3.1}$$

$$I_{a1} = \begin{cases} 0, & 0 \leq \beta \leq \beta_{B1} \\ \left(\dfrac{\beta - \beta_{B1}}{1 - \beta_{B1}}\right) i_{a1,M} \cdot e^{-j\theta_1}, & \beta_{B1} \leq \beta \leq 1 \end{cases} \tag{3.2}$$

$$I_{a2} = \begin{cases} 0, & 0 \leq \beta \leq \beta_{B2} \\ \left(\dfrac{\beta - \beta_{B2}}{1 - \beta_{B2}}\right) i_{a2,M} \cdot e^{-j\theta_2}, & \beta_{B2} \leq \beta \leq 1 \end{cases} \tag{3.3}$$

where $i_{m,M}$, $i_{a1,M}$ and $i_{a2,M}$ are the maximum fundamental current magnitude from the Main, Aux1, and Aux2 cells, respectively.

The amplitude of the output voltage from the Main cell should be kept constant at the drain-source bias voltage V_{ds} throughout the high power region (when $\beta_{B1} < \beta \leq 1$) to guarantee its full voltage swing capability, and thus high-efficiency operation. To fully determine the operation of the conventional three-stage DPA, the current ratio between its maximum current of the Aux1 and Main cell should be related by

$$\alpha_{1,M} = \frac{i_{a1,M}}{i_{m,M}} = \frac{1}{\beta_{B1}} - 1 \tag{3.4}$$

Similarly, the current ratio between its maximum current of the Aux2 and Main cell is given by

$$\alpha_{2,M} = \frac{i_{a2,M}}{i_{m,M}} = \frac{1}{\beta_{B1}} \left(\frac{1}{\beta_{B2}} - 1\right) \tag{3.5}$$

When fulfilling the above current ratios, the resulting conventional three-stage DPA, as shown in Figure 3.2, has the commonly adopted configuration.

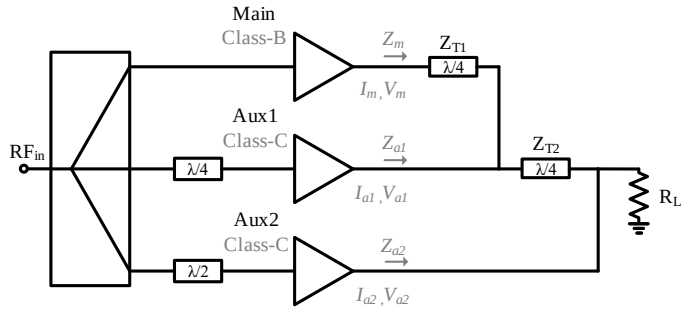


Figure 3.2: The conventional three-stage DPA.

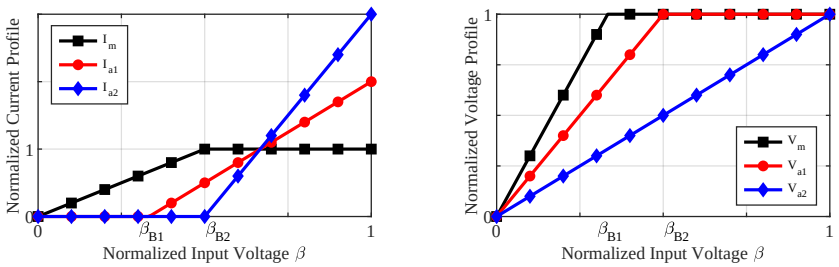


Figure 3.3: (a) Normalized amplitude of the output currents and (b) output voltage profiles of the conventional three-stage DPA versus normalized input drive voltage.

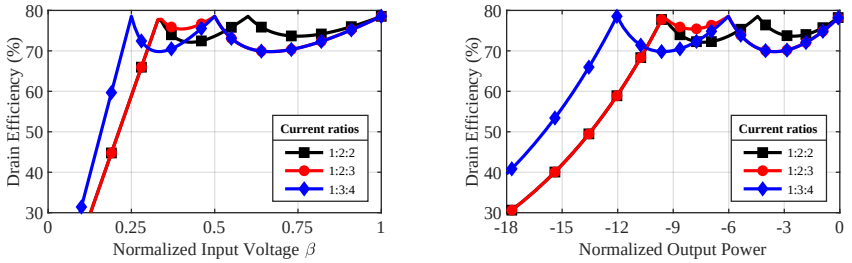
The Main and Aux1 amplifier cells are combined via a $\lambda/4$-transmission line impedance inverter with a characteristic impedance Z_{T1} at the output of the Main cell. The output of the Aux2 cell is connected to the joint output node of the Main and Aux1 cells, via another $\lambda/4$-transmission line with a characteristic impedance Z_{T2}. Z_{T1} and Z_{T2} are given by

$$Z_{T1} = \frac{R_L}{\beta_{B1}\beta_{B2}} \tag{3.6}$$

$$Z_{T2} = \frac{R_L}{\beta_{B2}} \tag{3.7}$$

Note that the load resistance $R_L = (1 - \beta_{B1})R_{opt,a2}$ is determined by the optimum loading condition of the Aux2 cell ($R_{opt,a2}$). The input consists of a power splitter, a $\lambda/4$-transmission line, and a $\lambda/2$-transmission line to provide the same phase delay through the three amplifier cell paths.

The drive profiles and theoretical efficiency performance of the conventional three-stage DPA are presented in Figures 3.3 and 3.4, respectively. As shown in the figure, the conventional three-stage DPA requires sub amplifier cells with different fundamental current components, i.e., unequal device peripheries, to provide the back-off efficiency reconfigurability. Besides, the Main cell is saturated after the Aux2 cell is turned on. The main drawbacks of this PA architecture are, thereby, the deep saturation of the Main cell, and the added complexity due to the different device peripheries of the three amplifier cells.



(a) **(b)**

Figure 3.4: Drain efficiency of the conventional three-stage DPA versus (a) normalized input drive voltage, and (b) normalized output power, for varying current ratios.

3.2 The Modified three-stage DPA

In the previous section, the convention three-stage DPA has been analyzed and investigated. The modified three-stage DPA was proposed in [49], where a modified output combiner with identical amplifier cells is utilized to enhance the efficiency at two fixed output power back-off levels, i.e., at 6-dB and 9.54-dB. Later it will be demonstrated that its output power back-off efficiency can also be reconfigured by using different device peripheries of the sub amplifier cells.

To analyze the operational principle of the modified three-stage DPA, similar to the previous cases, the Main, Aux1 and Aux2 amplifier cells are represented by current sources having fundamental output currents I_m, I_{a1} and I_{a2} that depend on the input voltage as follows:

$$I_m = \beta i_{m,M} \tag{3.8}$$

$$I_{a1} = \begin{cases} 0, & 0 \le \beta \le \beta_{B1} \\ \left(\dfrac{\beta - \beta_{B1}}{1 - \beta_{B1}}\right) i_{a1,M} \cdot e^{-j\theta_1}, & \beta_{B1} \le \beta \le 1 \end{cases} \tag{3.9}$$

$$I_{a2} = \begin{cases} 0, & 0 \le \beta \le \beta_{B2} \\ \left(\dfrac{\beta - \beta_{B2}}{1 - \beta_{B2}}\right) i_{a2,M} \cdot e^{-j\theta_2}, & \beta_{B2} \le \beta \le 1 \end{cases} \tag{3.10}$$

where $i_{m,M}$, $i_{a1,M}$ and $i_{a2,M}$ are the maximum current from the Main, Aux1 and Aux2 cells, respectively.

The amplitude of the output voltage of the Main cell from the modified three-stage DPA should be kept constant and equal to the drain-source bias voltage V_{ds} all over the higher power region to maximize its efficiency. Besides, to fully establish its operation, the current ratio between the maximum current of the Aux1 and Main cell should be given by

$$\alpha_{1,M} = \frac{i_{a1,M}}{i_{m,M}} = \beta_{B2}\left(\frac{1}{\beta_{B1}} - 1\right). \tag{3.11}$$

The current ratio between its maximum current of the Aux2 and Main cell is expressed as

$$\alpha_{2,M} = \frac{i_{a2,M}}{i_{m,M}} = (1 - \beta_{B2})\left(\frac{1}{\beta_{B1}} - 1\right). \tag{3.12}$$

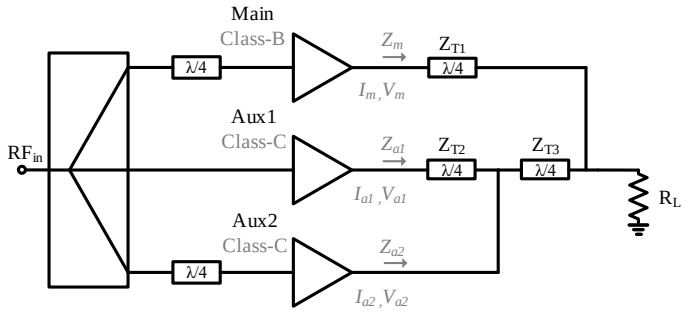
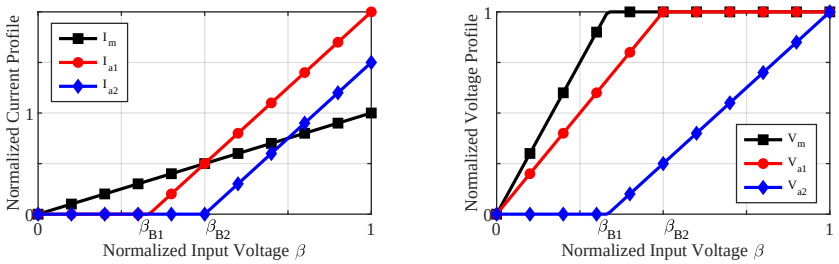


Figure 3.5: The modified three-stage DPA.



(a) **(b)**

Figure 3.6: (a) Normalized amplitude of the output currents and (b) output voltage profiles of the modified three-stage DPA versus normalized input drive voltage.

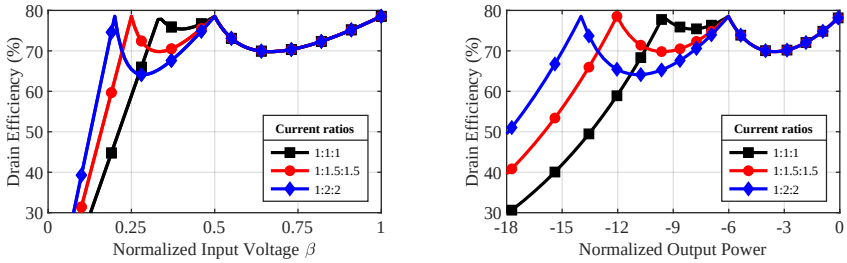
When fulfilling the above current ratios, the resulting modified three-stage DPA is shown in Figure 3.5. The Aux1 and Aux2 amplifier cells are combined via a $\lambda/4$-transmission line impedance inverter with a characteristic impedance Z_{T2} at the output of the Aux1 cell. The output of the Main cell is connected to the joint output node of the Aux1 and Aux2 cells, via another two $\lambda/4$-transmission line with characteristic impedances of Z_{T1} and Z_{T3}, respectively. Z_{T1}, Z_{T2} and Z_{T3} are given by

$$Z_{T1} = \sqrt{\frac{R_L R_{opt}}{\beta_{B1}}} \tag{3.13}$$

$$Z_{T2} = \frac{\beta_{B1}\left(\beta_{B2}-1\right) R_{opt}}{\beta_{B2}^2\left(\beta_{B1}-1\right)} \tag{3.14}$$

$$Z_{T3} = \frac{\beta_{B1}\left(\beta_{B2}-1\right)^2}{\left(\beta_{B1}-1\right)\left(3\beta_{B2}^2-3\beta_{B2}+1\right)}\sqrt{\frac{R_L R_{opt}}{\beta_{B1}}} \tag{3.15}$$

The drive profiles of the modified three-stage DPA is presented in Figure 3.6. The theoretical simulated results are shown in Figure 3.7, where the drain efficiency is plotted versus normalized input voltage and normalized output power, respectively.



(a) **(b)**

Figure 3.7: Drain efficiency of the modified three-stage DPA versus (a) normalized input drive voltage, and (b) normalized output power, for varying current ratios.

As can be seen, the modified three-stage DPA architecture exhibits two main advantages over the conventional one. One is that its main amplifier operates linearly throughout the complete power range. The other is that it is theoretically possible to enhance the back-off efficiency using the same fundamental current components from the three amplifier cells at the peak output power.

3.3 Generic three-port combiner synthesis for the three-stage DPA

In the previous section, the theoretical performance analysis of the three-stage DPA was presented with the transistors represented by ideal current sources. However, nonlinear and parasitic effects are significant in real transistors at microwave frequencies, which makes the ideal current source model inappropriate for the analysis. Moreover, for equally sized transistors, the Aux cells that operate in class-C mode, have a smaller fundamental current component compared to the class-B biased Main cells. This requires larger input power to drive the Aux amplifier cells. For the three-stage DPA, the degradation of the gain and PAE is more significant than for two-way DPAs since its Aux amplifiers are biased at even deeper class-C mode to ensure high efficiency at larger power back-off levels. Hence, even for the modified three-stage DPA, its PAE performance is severely affected by the two auxiliary cells. Therefore, to fully utilize each transistor's full capability, an analytical combiner synthesis approach based on the load-pull data is proposed in [Paper A], [53] and reviewed in this section.

As illustrated in Figure 3.8, the analysis of the three-stage DPA is generalized, consisting of two input phase shifters, main amplifier cell biased in class-B, auxiliary amplifiers biased in class-C, and a reciprocal and lossy three-port output combiner with the load embedded. Later, the conversion from the lossy three-port combiner to the lossless four-port combiner terminated with resistive load, will be presented when boundary conditions are met.

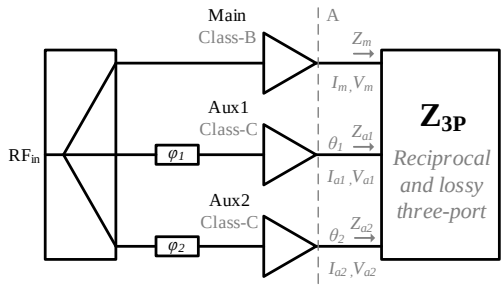


Figure 3.8: Generalized reciprocal and lossy three-port combiner used for the analysis of the three-stage Doherty PA. The load is terminated inside. Z_m, Z_{a1} and Z_{a2} denote, the impedances seen by the Main, Aux1 and Aux2 cells, respectively. Plane A represents the output plane of the amplifier cells. The input and output current phase delays are denoted as $\varphi_{1,2}$ and $\theta_{1,2}$, respectively [Paper A].

The voltages and currents shown in Figure 3.8 are related through $\mathbf{Z_{3P}}$,

$$\begin{bmatrix} V_m \\ V_{a1} \\ V_{a2} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{12} & Z_{22} & Z_{23} \\ Z_{13} & Z_{23} & Z_{33} \end{bmatrix} \begin{bmatrix} I_m \\ I_{a1} \\ I_{a2} \end{bmatrix} \tag{3.16}$$

3.3.1 The symmetrical three-stage DPA

The symmetrical three-stage DPA can be regarded as the modified three-stage DPA with current ratios less than unity, which better represents the fundamental current from the realistic Class-C biased Aux transistors with the same size as the Main transistors.

From (3.11), it is possible to obtain the impedance parameters of the reciprocal and lossy three-port combiner, based on the current ratios and optimal impedances of Main, Aux1, and Aux2 transistors. More specifically, the derived impedance parameters depend on $|\alpha_{1,M}|$, $|\alpha_{1,B2}|$ and $|\alpha_{2,M}|$, as well as the two output current phase delays θ_1 and θ_2. Furthermore, it should be verified that the derived lossy three-port combiner can be converted into a lossless four-port combiner having one of the ports terminated with a resistive load. To make this conversion possible, the following conditions are necessary and sufficient [54]:

$$\Re\{Z_{12}\}^2 = \Re\{Z_{11}\}\Re\{Z_{22}\} \tag{3.17}$$

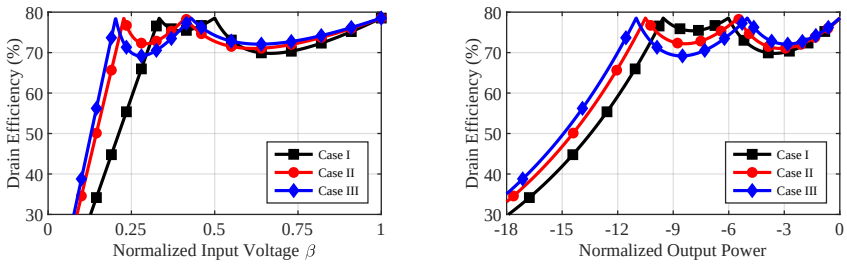
$$\Re\{Z_{13}\}^2 = \Re\{Z_{11}\}\Re\{Z_{33}\} \tag{3.18}$$

$$\Re\{Z_{23}\}^2 = \Re\{Z_{22}\}\Re\{Z_{33}\} \tag{3.19}$$

There are five unknown parameters, which combined with the three boundary conditions above, make the system under-determined. Two of the unknown parameters can thereby be selected freely. In order to better illustrate the output power back-off efficiency reconfigurability of the symmetrical three-stage DPA, three different cases are studied and illustrated. Table 3.1 presents the obtained parameters of three different cases, with the corresponding efficiency profiles shown in Figure 3.9. These results further prove that, based on the proposed method, it is possible to utilize the current ratios ($|\alpha_{1,M}|$ and $|\alpha_{2,M}|$),

Table 3.1: Different three-stage Doherty PA design cases

	Case I Modified	Case II Symmetrical	Case III
γ_{B1} (dB)	9.54	10.5	11
γ_{B2} (dB)	6	5.5	5
$\lvert\alpha_{1,M}\rvert$	1	0.85	0.85
$\lvert\alpha_{2,M}\rvert$	1	0.7	0.7
$\lvert\alpha_{1,B2}\rvert$	0.25	0.31	0.38
θ_1 (deg)	-90	-76.56	-67.61
θ_2 (deg)	0	25.86	31.42



(a) (b)

Figure 3.9: Drain efficiency of the symmetrical three-stage DPA versus (a) normalized input drive voltage, and (b) normalized output power, for Cases I, II and III in Table 3.1

together with the output current phase delays (θ_1 and θ_2) to design three-stage DPAs with high efficiency at two reconfigurable output power back-off levels (γ_{B1} and γ_{B2}).

3.3.2 Three-port black-box combiner synthesis

The ideal analysis of generic and symmetrical three-stage DPAs is covered in the previous section. However, as mentioned previously, the model of a realistic microwave transistor is much more complicated compared to the transistor model using ideal current sources. In the next step, it is therefore vital to generate an analytical load-bull based combiner synthesis method for the three-stage DPA, which is able to enable the highest possible efficiency and output power performance with real transistors. The method is here referred to as the three-port black-box combiner synthesis approach. Similar to the two-port black-box combiner approach, the Main and Aux transistors' optimal output impedance and power obtained from load-pull simulation or experiments at the peak, first, and second power back-off levels are first specified, together with the off-state output impedance from the two Aux transistors. A reciprocal and lossy three-port combiner, with impedance matrix $\mathbf{Z_{3P}}$, as presented in Figure 3.10a, is then determined analytically from the load-pull data to satisfy the optimal loading conditions. The lossy three-port combiner is, thereafter, converted to a lossless four-port combiner terminated with an external resistor when the three boundary conditions (3.17)-(3.19) are satisfied. Using these conditions, the phase delays between Main and two Aux amplifiers are determined. Finally,

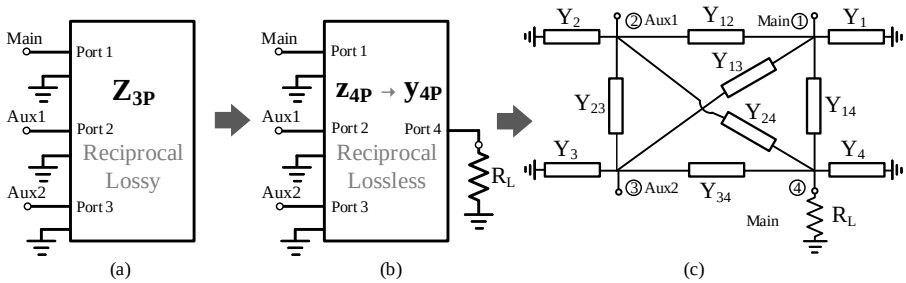


Figure 3.10: Step-by-step conversion of the generalized output combiner into a realizable network. First, the lossy and reciprocal three-port output combiner in (a) is converted to a lossless and reciprocal four-port output combiner terminated with a purely resistive load R_L in (b). Thereafter, the obtained four-port impedance parameters are transferred to the four-port admittance parameters, which can be converted into an equivalent network topology in (c) [Paper A].

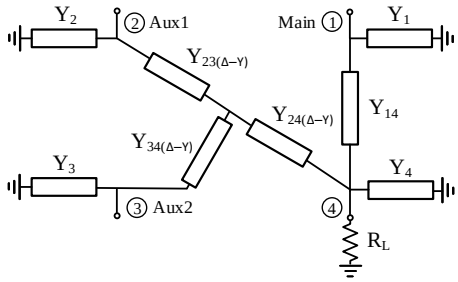


Figure 3.11: Simplified combiner network after tuning of z_{44} and $\Delta - Y$ circuit transformation [Paper A].

it is possible to realize the actual lumped-element combiner network from the four-port admittance parameters ($\mathbf{y_{4P}}$), as illustrated in Figure 3.10. The value of each element in the combiner network can thus be expressed as

$$Y_k = y_{kk} + \sum_{j=1, j\neq k}^{n} y_{kj} \tag{3.20}$$

$$Y_{kj} = -y_{kj}. \tag{3.21}$$

Note that there are two extra degrees of freedom when converting from the lossy three-port to lossless four-port combiner, i.e, z_{44} and R_L. These two parameters can thereby be tuned to further simplify the actual combiner, for instance, to avoid the cross elements Y_{12} and Y_{13} and to let the combiner directly interface the 50 Ω load termination. Furthermore, the layout of the combiner network can be even more compact and easier to fabricate, if $\Delta - Y$ circuit transformation is applied [55], as shown in Figure 3.11.

3.3.3 Circuit realization and results

To verify the proposed theory and design approach, [Paper A] has presented the design and measurement results of a three-stage DPA demonstrator circuit,

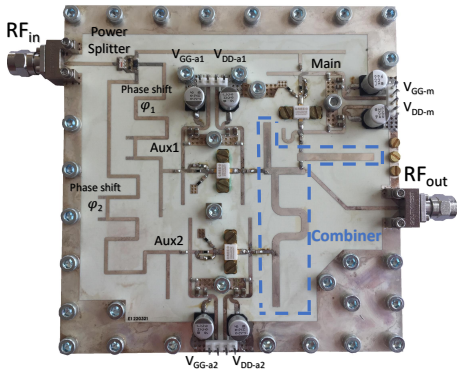


Figure 3.12: Photo of the fabricated three-stage DPA prototype presented in [Paper A].

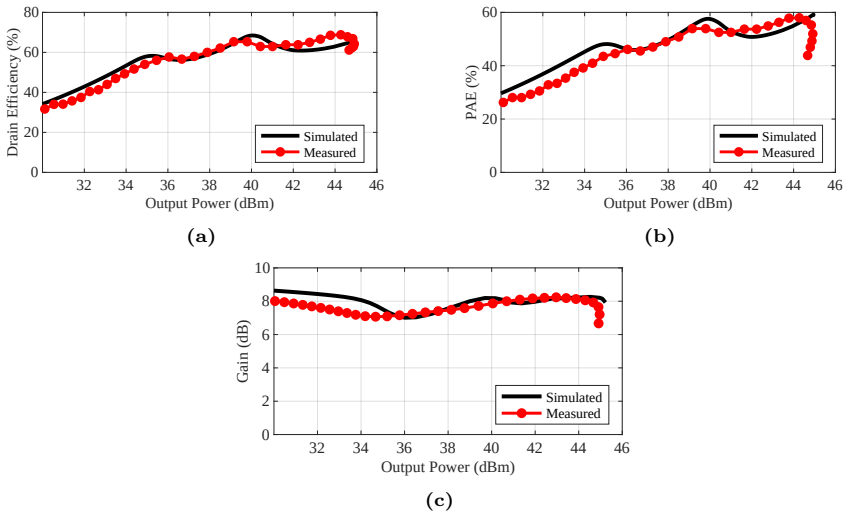
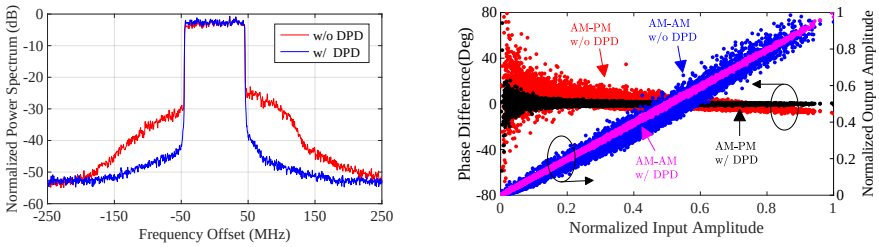


Figure 3.13: CW measurement results of the prototype at 2.14 GHz. (a) Drain efficiency versus output power, (b) PAE versus output power, and (c) gain versus output power.

depicted in Figure 3.12. The design goal is to obtain the highest possible efficiency performance at two different output power back-off levels at a 2.14 GHz center frequency. The circuit is implemented with three identically sized amplifier cells, and its input transmission lines are designed to provide proper phase delays to the two Aux branches. The compact output combiner network is implemented using the combiner synthesis technique described in the previous sections. The simulated and measured results indicate that the combiner network allows for high-efficiency performance at 2.14 GHz. The measured results when applying continuous-wave (CW) and digitally modulated signals are shown below.

The measured and simulated drain efficiency, PAE, and power gain at 2.14 GHz are plotted versus output power in Figure 3.13. The measured drain efficiency at 6-dB and 10-dB output power back-offs are 68% and 56%, respectively. The measured PAE at the same back-off levels is 56% and 45%, respectively. The agreement between measured and simulated results is in



(a) (b)

Figure 3.14: Modulated-signal measurement results of the three-stage DPA prototype at 2.14 GHz. (a) Measured spectrum with and without DPD, (b) measured AM-AM and AM-PM characteristics with and without DPD, when using the a 100-MHz 8.5-dB PAPR communication signal.

general very good, although the measured PAE and power gain show a small degradation compared to simulations in the lower output power region.

The demonstrator circuit is characterized at 2.14 GHz using Long Term Evolution (LTE)-like signals with varying PAPR and bandwidth to further examine its performance. Besides, digital predistortion linearization (DPD) with a generalized memory polynomial model has been used to evaluate the performance and the linearizability of the PA. The measured output spectrum with and without applying DPD is presented in Figure 3.14a. Without any linearization, the demonstrator circuit provides an average drain efficiency of 54.5% and an adjacent channel leakage ratio (ACLR) of below −26.3 dBc at an average output power of 36.2 dBm. After applying DPD, the ACLR of the prototype is improved to −45.7 dBc at an average output power of 36.2 dBm. The corresponding AM/AM and AM/PM characteristics are presented in Figure 3.14b.

3.4 Chapter summary

In this chapter, the fundamental operating principles of the conventional and modified three-stage DPA have been reviewed. Each operation type requires a fixed relation between its full current ratios and back-off levels. It is then demonstrated that the black-box method can broaden the design space by unlocking these constraints. This is particularly useful in the design of realistic three-stage DPAs where the class-C biased Aux amplifiers have a smaller fundamental current component compared to the class-B biased Main amplifiers.

An analytical load-pull based combiner synthesis approach for three-stage DPAs, together with the realization and simplification of the actual combiner circuit network, has been proposed and described. The resulting combiner network has, in many cases, much lower insertion loss and very compact size. A demonstrator circuit has been presented to verify the proposed technique. The measurement results show that the circuit provides excellent performance in terms of efficiency at deep output power back-off levels.

Chapter 4

The circulator load modulated amplifier

In the previous chapter, the principle of operation, as well as the practical implementations of the two-way and three-stage DPA have been illustrated and discussed. Compared to other highly efficient PA architectures, the DPA is by far the most widely adopted architecture in cellular base stations, thanks to its low circuit complexity and moderate linearity performance. However, the increasing demand for larger capacity in recent and future wireless communication systems calls for new PA architectures with both back-off efficiency enhancement and improved bandwidth performance.

This chapter first reviews recently published wideband PA architectures with back-off efficiency enhancement. A newly proposed efficient and wideband PA architecture with a non-reciprocal output combiner is then introduced in [Paper B]. The operational principle and theoretical performance of the proposed PA are thereafter demonstrated. Finally, as a proof of concept, design and characterization of the proposed PA is presented.

4.1 Literature review

Several PA architectures with large bandwidth and efficiency enhancement have been proposed recently. A distributed efficient power amplifier (DEPA) was introduced in [56,57]. This architecture is suitable for ultra-wideband PAs with high efficiency over large power back-off levels. However, the DEPA requires several auxiliary amplifiers, thus greatly increasing its circuit complexity, parallel loss, and size. Another architecture with high efficiency and wide bandwidth, named load modulated balanced amplifier (LMBA), was initially proposed in [58]. The LMBA comprises a balanced amplifier, which has an input quadrature coupler, an output quadrature coupler, and two amplifiers as the Main amplifier. It also comprises means to inject a control signal to the isolated port of the output quadrature coupler in order to modulate the impedance seen by the two Main amplifiers. More recently, the LMBA concept has been extended and the LMBA architectures with single RF input were further developed in [59]. The RF-input LMBA consists of an input power splitter, two class-B

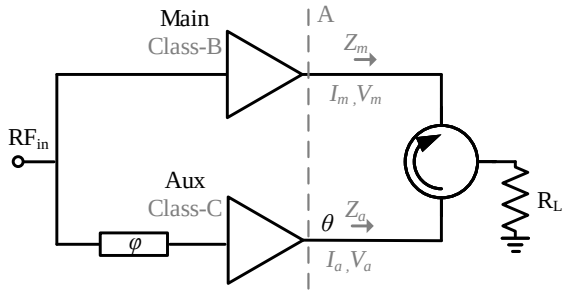


Figure 4.1: Block diagram of the circulator load modulated amplifier. Plane A represents the output reference plane of the amplifier cells. The input and output current phase delays are denoted as φ and θ, respectively.

biased main amplifiers that comprise a balanced amplifier configuration, and a class-C biased Aux amplifier that injects power into the isolated port of the output quadrature coupler. Furthermore, an inverted RF-input LMBA (ILMBA) architecture was proposed in [60–62]. It has the same circuit topology as the regular LMBA, except for the inverted location of the Main and Aux amplifiers. Note that the ILMBA exhibits extended high-efficiency output power back-off range with even wider bandwidth performance compared to the LMBA. Compared to the DPA, the LMBA type architectures have larger bandwidth since the bandwidth of the quadrature coupler is inherently wider than the one provided by the standard DPA. However, the circuit complexity of the LMBA is higher. The input and output quadrature couplers increase the loss in the circuit, as well as the circuit size. Moreover, the use of one extra transistor also adds cost.

A novel active load modulation PA architecture, referred to as the circulator load modulated amplifier (CLMA), was recently proposed in [Paper B], [63]. The topology employs two active devices and a non-reciprocal combiner, i.e. a circulator [64–67]. And it allows high efficiency to be maintained over a large output power dynamic range. Moreover, the availability of wideband and low-loss circulators makes this architecture promising for wideband applications. In summary, the CLMA has the potential to overcome many of the drawbacks of previously presented architectures.

4.2 Principle of operation

The CLMA architecture comprises a class-B biased Main amplifier, an Aux amplifier biased in class-C mode, and a circulator-based output combiner network as presented in Figure 4.1. The fundamental concept of the CLMA architecture can be described as follows: An Aux amplifier injects power into the output of the Main amplifier through the circulator to modulate its load impedance and thereby to maintain high efficiency at both peak power and power back-off. Due to the inherent non-reciprocal property of the circulator, the powers injected by the Main and Aux amplifiers are both fully delivered to the load. Moreover, the impedance seen by the Aux amplifier is maintained constant due to the high isolation from the Main to Aux port in the circulator.

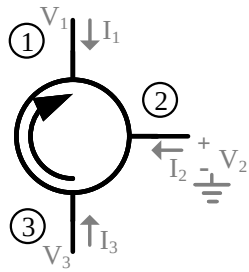


Figure 4.2: Block diagram of an ideal circulator used for basic analysis of the CLMA architecture.

To further analyze the operation principle of the CLMA, it is important to further study the circulator. As is well known, the scattering parameters of an ideal circulator, as depicted in Figure 4.2, can be expressed as

$$S_{circ} = \begin{pmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix}. \tag{4.1}$$

It is then straightforward to convert the three-port scattering parameters (S_{circ}) to admittance parameters. The operational mechanism of the CLMA can thereafter be analyzed using the three-port admittance parameter matrix of the ideal circulator. It should be stressed that this formulation assumes that the port currents, I_n, flow into the corresponding port of the circulator, and the voltages V_n are referenced to the common ground connection. The port currents and voltages are therefore related by

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = Y_0 \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{4.2}$$

where $Y_0 = 1/Z_0$ is the characteristic admittance of the circulator.

The Main (connected at port 1) and Aux (connected at port 3) amplifiers can be represented as current sources in the analysis, having magnitudes I_m and I_a, respectively. Thus, $I_1 = I_m$, $I_3 = I_a e^{j\theta}$, where θ is the output current phase delay between the Main and Aux amplifier branches. In addition, the output port (port 2) is terminated with a resistive load matched to the characteristic impedance of the circulator Z_0, so $V_2 = -Z_0 I_2$.

Substituting the above equations into the three-port admittance matrix from (4.2), the resulting three equations can be solved to obtain the expression for the impedance seen by the output of the Main amplifier, denoted as Z_m, as follows

$$Z_m = Z_0 \left(1 + 2\frac{I_a e^{j\theta}}{I_m}\right). \tag{4.3}$$

The above equation reveals that the impedance seen by the Main amplifier at the output can be dynamically modulated by the magnitude and output phase delay of the Aux current. Moreover, the relationship between the currents are given by

$$I_2 = I_m + I_a e^{j\theta}. \tag{4.4}$$

The power delivered to the output load is therefore given by

$$P_L = \frac{1}{2} Z_0 \Re\{I_m + I_a e^{j\theta}\}^2 \tag{4.5}$$

The power generated by the Main and Aux amplifiers can be expressed as

$$P_m = \frac{1}{2} I_m^2 Z_0 \Re\{1 + 2\frac{I_a e^{j\theta}}{I_m}\} \tag{4.6}$$

$$P_a = \frac{1}{2} Z_0 \Re\{I_a^2 \cos(\theta)^2\} \tag{4.7}$$

It can be noticed that $P_L = P_m + P_a$, which indicates that the power generated by the Main and Aux amplifiers is fully transferred to the output load.

4.3 Theoretical performance

In the previous section, it was shown that the impedance seen by the Main amplifier of the CLMA is load-modulated by the active current injection from the Aux amplifier. Furthermore, the power generated by both Main and Aux amplifiers can be fully recovered at the CLMA output port, and thus delivered to the load. To further investigate its theoretical performance, the Main and Aux amplifier cells are represented by current sources having fundamental output currents I_m and I_a that depend on the input voltage as

$$I_m = \beta i_{m,M} \tag{4.8}$$

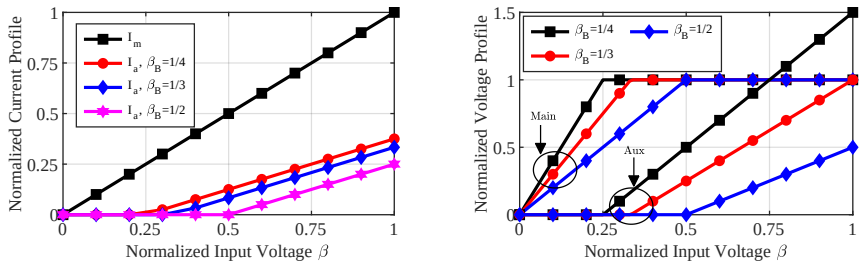
$$I_a = \begin{cases} 0, & 0 \leq \beta \leq \beta_B \\ \left(\dfrac{\beta - \beta_B}{1 - \beta_B}\right) i_{a,M} \cdot e^{-j\theta}, & \beta_B \leq \beta \leq 1 \end{cases} \tag{4.9}$$

where $i_{m,M}$ and $i_{a,M}$ are the maximum current from the Main and Aux amplifier cells, respectively.

The amplitude of the output voltage from the Main amplifier should be kept constant and equal to the drain-source bias voltage V_{ds} throughout the high power region (when $\beta_B < \beta \leq 1$) to guarantee its full voltage swing capability, and thereby high-efficiency operation. To fully determine the operation of the CLMA, the current ratio (α) between the maximum current of the Aux and Main amplifiers should be related by

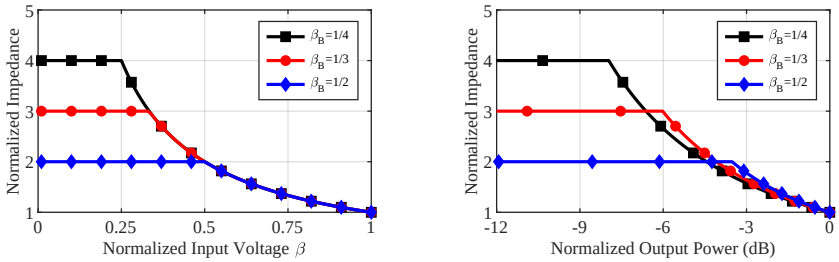
$$\alpha = \frac{i_{a,M}}{i_{m,M}} = \frac{1 - \beta_B}{2}. \tag{4.10}$$

In Figure 4.3, the current and voltage profiles of the CLMA are plotted versus the normalized input voltage (β). It can be observed from the figure that the fundamental peak current required from the Aux amplifier is much less than the one from the Main amplifier. Also, similar to the conventional two-way DPA, the current ratio (α) needs to be increased to increase the high-efficiency back-off power level of the CLMA. In addition, the maximum voltage swing required for the Aux amplifier varies with different back-off levels.



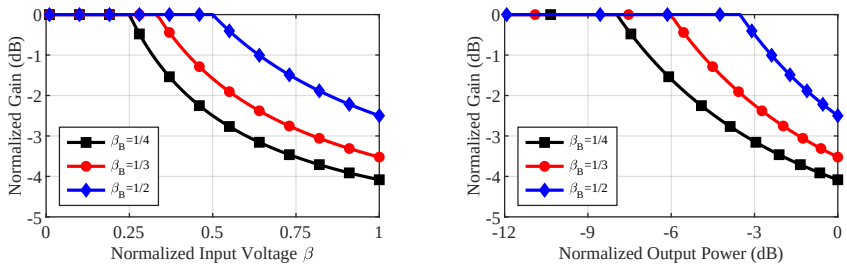
(a) (b)

Figure 4.3: (a) Normalized amplitude of the output currents and (b) output voltage profiles of the CLMA versus normalized input drive voltage, for $\beta_B = 1/4$, $1/3$, and $1/2$.



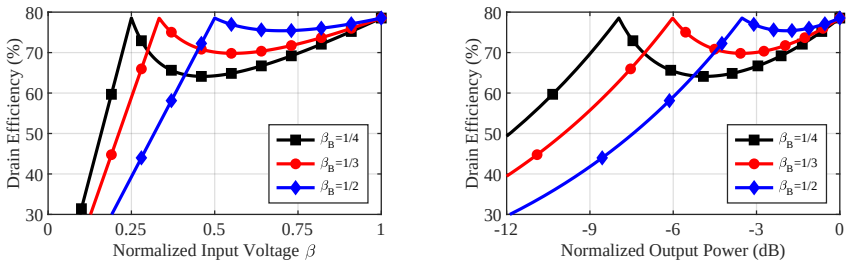
(a) (b)

Figure 4.4: Normalized optimal load impedance of the CLMA versus (a) normalized input drive voltage, and (b) normalized output power, for $\beta_B = 1/4$, $1/3$, and $1/2$.



(a) (b)

Figure 4.5: Normalized gain of the CLMA versus (a) normalized input drive voltage, and (b) normalized output power, for $\beta_B = 1/4$, $1/3$, and $1/2$.



(a) (b)

Figure 4.6: Drain efficiency of the CLMA versus (a) normalized input drive voltage, and (b) normalized output power, for $\beta_B = 1/4$, $1/3$, and $1/2$.

The ideal simulation results are shown in Figures 4.4-4.6, where the normalized load modulation, normalized gain and drain efficiency are plotted versus normalized input voltage and normalized output power, respectively. The theoretical analysis and performance presented in this section illustrate how a simple combination of the Main and Aux amplifiers, together with correct driving conditions and the non-reciprocal circulator combiner, results in enhanced efficiency performance at large back-off output power levels.

4.4 Demonstrator circuit

The proposed CLMA architecture is experimentally verified with a prototype circuit in [Paper B]. The circuit, shown in Figure 4.7, is implemented at a center frequency of 2.14 GHz, using two PA test boards with commercial 10-W GaN devices (CGH40010F from Wolfspeed) for its Main and Aux amplifiers. The output matching network of the Main amplifier presented in the figure is designed to maximize its back-off efficiency at the center frequency. The non-reciprocal combiner is realized by a circulator (SM2040C09 from Quest Microwave), which is selected for its low insertion loss, sufficient isolation, and wide bandwidth. Note that the CLMA concept is validated through a narrowband prototype in this work due to the limited bandwidth of the PA cells used. A wideband CLMA circuit is possible if wideband Main and Aux amplifier cells are designed together with a wideband circulator combiner.

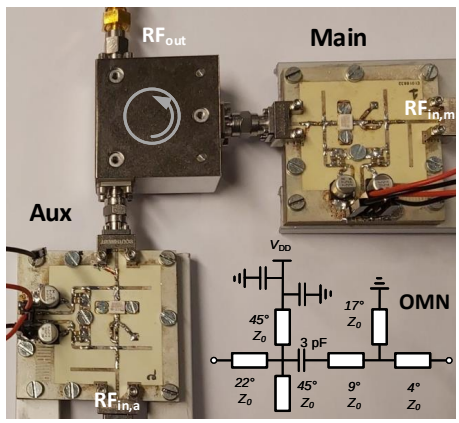


Figure 4.7: Photo of the circulator load modulated amplifier prototype circuit in [Paper B].

The CLMA circuit prototype has been characterized with static CW measurements. The drain bias of the Main and Aux amplifiers are set to 28 V and 34 V, respectively. The gate bias of the Main amplifier is in class-B mode with -3 V and quiescent current of 25 mA, while the Aux amplifier is biased in class-C mode with -6 V. An input power splitting ratio of approximately 50% has been employed. Optimum phase delay has been selected at each frequency.

Figure 4.8 shows the measured drain efficiency versus output power for frequencies between 1.99 and 2.14 GHz. As can be seen from the figure, there is a well pronounced back-off efficiency enhancement across those frequencies. The drain efficiency at 6 dB output power back-off level is maintained higher

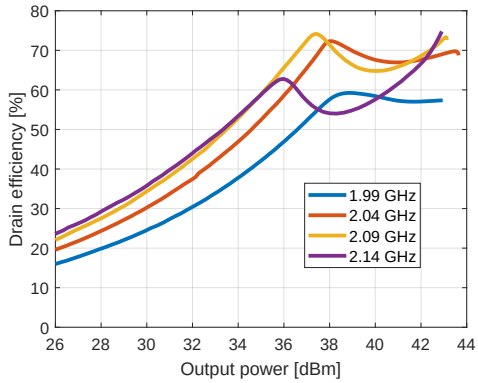


Figure 4.8: Measured drain efficiency of the circulator load modulated amplifier prototype circuit versus the output power, for several frequencies.

than 58% and the peak output power is larger than 42.9 dBm across 1.99-2.14 GHz frequency range. Furthermore, at 2.09 GHz, drain efficiencies of 73% and 48% are measured at 6 and 10 dB output power back-off, respectively.

4.5 Chapter summary

This chapter has proposed and illustrated the CLMA architecture with efficiency enhancement over a large output power range. The principle of operation and theoretical performance of the CLMA architecture are presented and discussed. It should be stressed that the CLMA has a great potential for wideband operation, thanks to the low-loss and wideband circulator combiner.

A CLMA demonstrator circuit has been developed to verify the theoretical findings. Large-signal characterization results show that the prototype circuit provides excellent performance in terms of efficiency enhancement at output power back-off. The results prove the utility of the CLMA and show that it is a potential candidate for future wireless transmitters.

Chapter 5

Conclusions and future work

5.1 Conclusions

With the increasing demand for data traffic, wireless communication systems require more spectrally efficient modulation schemes and frequency agility. As discussed in the introduction chapter, this has imposed challenges and requirements on the energy efficiency of the PA. Since several decades, the ALM technique has been widely used for improving the PA average efficiency. Among these, the DPA has become the most popular architecture in cellular base stations, thanks to its favorable tradeoff between low circuit complexity, moderate bandwidth, linearity, and high efficiency.

This thesis has first reviewed the theoretical performance and practical implementations of the two-way DPA. To further improve the efficiency at larger output power back-off levels, three-stage DPA architectures have been studied. An analytical load-pull based three-port combiner synthesis approach for the three-stage DPA is thereafter proposed and experimentally demonstrated. The methodology opens up a new design space, which enables a high power utilization factor of the transistors and thus enhanced efficiency and lower cost in three-stage DPAs. In particular, it allows highly efficient three-stage DPAs with identical transistors and compact output combiners to be designed and realized. The proposed theory and design methodology have been adopted and implemented by a prototype circuit using commercially available transistors. The measurement results not only show excellent efficiency, but the fact that the simulated predictions of gain, output power, and efficiency are in good agreement with measurements further proves the validity of the proposed design method.

Due to the inherently narrowband output combiner in traditional DPAs, it is often difficult for them to meet the increasing demands of frequency agility. The CLMA architecture is proposed to overcome this issue. The CLMA employs two transistors and a circulator as its output combiner, and maintains high efficiency over large output power back-off level when correct driving conditions are applied, the availability of wideband and low-loss circulators make this

architecture promising for wideband applications. A demonstrator circuit with GaN transistors and a commercially available circulator has been designed to verify the theory. The reported results show excellent efficiency performance at 2 GHz.

In summary, this thesis has presented a promising technique for improving the efficiency at the deep output power back-off level in the DPA. Moreover, it has proposed a new ALM PA architecture with high efficiency and potential for wideband operation. The results of this thesis will therefore contribute to the development of future energy-efficient, frequency-agile, and highly integrated wireless transmitters.

5.2 Future work

Based on the requirements and demand of future wireless transmitters, the author believes the following topics to be highly interesting directions for future research

- **Investigate and explore the potential of PA circuits for mm-wave applications.** The DPA circuit with the black-box approach, demonstrated in Chapters 2 and 3, is an interesting candidate for mm-wave integrated circuit applications due to the compact and low-loss output combiner, as well as the load-pull based practical implementation methods. It will be interesting to investigate the mm-wave DPA in advanced Si or GaN technologies.
- **Explore and expand the bandwidth capability of high-efficiency PAs.** Investigate the wideband matching techniques for highly efficient MMIC and hybrid GaN PAs with large output power.
- **Explore the bandwidth capability of the CLMA.** The CLMA demonstrator circuit presented in the thesis is a narrowband prototype. This is an initial verification of the concept. It has, however, great potential for wideband operation, we will continue to explore the CLMA architecture for efficient and wideband applications.

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