Low-loss K-band Photoconductive Switches in SIW Technology

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***Abstract* — A design approach for mmWave switches in substrate integrated waveguide (SIW) technology is demonstrated. The switch is based on a photoconductive element (PE) which represents a piece of an intrinsic silicon wafer with light modulated conductivity. Using both dielectric (high-resistivity) and conductive states of the PE, we can design a low-loss mmWave switching element. Owing to the light actuation, the control circuitry of the photoconductive switch (PS) is electrically separated from the high-frequency elements of the device. This solves the bottleneck of conventional mmWave switches based on PIN diodes, MOSFETs, MEMS, *etc.*, which are bulky and lossy due to decoupling filters and matching elements of control and biasing circuits. The proposed approach is generic and can be applied to many mmWave applications within 10 — 100 GHz such as 5G, WiGig, automotive radars, and others.**

***Keywords* — photoconductive switch, mmWave, substrate integrated waveguide.**

I. Introduction

In recent years, substrate integrated waveguides (SIWs) have attracted a lot of attention as the technology suitable for commercial mmWave systems [1] — [2]. Having a low-profile form-factor, owing to the standard printed circuit board (PCB) manufacturing process, SIW has several advantages over the microstrip lines [2]: relatively low dissipative losses; reliable shielding; high power handling [3]; low sensitivity to manufacturing tolerances; surface waves mitigation. However, solid dielectric filling and electrically small transverse sizes usually complicate placing any external controllable components inside the SIW. Due to this, the realization of active mmWave devices in SIW technology is limited.

Below we address the design of low-loss mmWave SIW switches. Previously reported designs employ mechanical SIW switches [4], the ferrite-loaded switches [5], PIN diode-loaded half-mode [6] and slotted SIW switches [7] — [9]. The slot-based concept solves the problem of DC and mmWave parts decoupling. However, it leads to insertion loss increase due to the parasitic slot radiation and reactances of PIN diodes and bonding wires [7]. Multilayer structures [8], [9] prevent the interference with control circuitry but require transitions between the layers, resulting in expensive designs and additional losses, especially at high frequencies.

Different types of switching [10] — [11] and reconfigurable structures [12] — [13] based on light-controllable photoconductive elements (PEs) have been studied recently. Thus far, photoconductive switches (PSs) have been demonstrated in microstrip and coplanar technologies. In the case of microstrips, the PE can be integrated into the line in series [11] or in parallel [13]. PSs for coplanar lines are usually shunt-integrated [10]. However, to the best of the authors' knowledge, no publically available results deal with SIW PSs.

In this paper, we report two SIW PS design examples. The basic building block of these designs is the PE, which represents a rectangular piece of intrinsic (high-resistivity) silicon wafer, with conductivity modulated by an external light source. This approach guarantees the separation of mmWave and control elements. Thus, decoupling circuits and matching components, as used in conventional switches, are not required. Therefore, switch insertion loss can be minimized over a wide frequency band, while maintaining high design simplicity.

II. Principle of Operation

A. Photoconductive Element

The switch operation is based on the photoconductive effect, i.e. the ability of the material to increase its conductivity by absorbing the radiation of a light source. The relationship between applied optical power P_{opt} and excited PE conductivity $\Delta\sigma$ can be described by the simplified formula [14]:

$$\Delta\sigma = q\mu \frac{P_{opt}(1-R)\xi\tau_{eff}\lambda_{opt}}{2\pi\hbar ctS}, \qquad (1)$$

where λ_{opt} is a wavelength of an optical source; R is the power reflection coefficient of light from the PE's surface; μ is the mobility of carriers; q is an elementary charge; ξ is the quantum efficiency of the PE; t and S are the thickness and the actuated surface area of the PE, respectively; τ_{eff} is the effective carrier lifetime; c is the speed of light in a vacuum; $\hbar$ is Plank's constant. Formula (1) assumes the uniform conductivity distribution inside the PE.

To provide a high PE impedance in the non-actuated state, we used the high-resistivity (~7 kΩ·cm) silicon wafer. In the

case of intrinsic silicon, the effective actuation is realized in the near infra-red spectrum, as, according to (1), it requires minimum optical power. However, the light penetration depth increases with the wavelength [15], thus care should be taken to ensure that the light power is fully absorbed by the PE. In our case, the thickness of the wafer is 205 um. This value is close to the optimum for the illumination by a light source with 940 nm wavelength [15]: light penetration depth at this wavelength is ~100 um and the PE absorbs more than 85 % of the power accepted by its surface. The estimated parameter values, chosen as the average for silicon wafers [14], are as follows: $\tau_{eff} = 1$ us, $R = 0.3$, and $\xi = 1$. Thus, according to (1), with the 50 mW of applied optical power, it is possible to get the conductivity value of 100 S/m.

B. Photoconductive switch for SIW

The basic controllable SIW block of the PS is depicted in Fig. 1. Two rows of metalized VIAs form the sidewalls of the SIW connecting two metal layers of the PCB substrate. The distance between VIAs is much smaller than the operating wavelength in the dielectric medium. This allows the structure approximation by a dielectric-filled rectangular waveguide [2]. The shunt VIA, whose upper pad is isolated from the top metal layer by the gap, is realized in the SIW center. The PE is placed right on the top pad, thus fully or partly covering the gap (Fig. 1). Being actuated (ON-state), the PE shunts the SIW, connecting the shunt VIA to the top metal layer. In this state, the PS fully reflects the incident SIW mode. To compensate for the gap capacitance C_{PE} in the non-actuated state (OFF-state), we used two additional VIAs placed in the same SIW cross-section as the shunt VIA (Fig. 1). These VIAs, forming the H-plane diaphragm, add the shunt inductance L_{DIA}. The equivalent circuits of the PS are shown in Fig. 2, where R_{PE} and L_{VIA} are the PE resistance in the OFF-state and the shunt VIA inductance, respectively.

According to the operation mechanism, the PS from Fig. 1 can be defined as the single-pole single-through (SPST) switch.

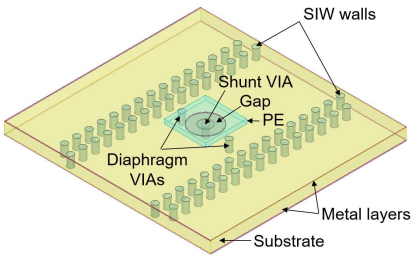

Fig. 1. The configuration of the SPST PS

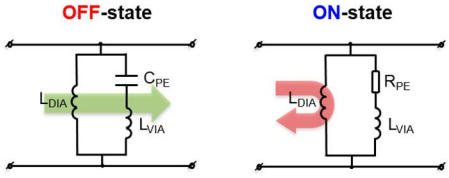

Fig. 2. Equivalent circuit of the SPST PS for OFF and ON states

III. Simulation and Experimental Results

A. SPST photoconductive switch with different sizes of PE

The proposed PS SIW structure was used for the development of a K-band SPST switch with 24 GHz central frequency. The geometry of the switch is presented in Fig. 3. The switch structure was optimized using a full-wave simulation model in Ansys HFSS. In the model, the PE element was considered as a silicon brick with conductivity σ. In this study, the following common parameters of the SIW are used for all design examples: $W_{SIW} = 4.1$ mm, $R_{VIA} = 0.15$ mm, $T_{VIA} = 0.6$ mm. Other dimensions of the SPST structures can be found in Table 1. All designs are performed on the 0.508 mm thick Rogers RO4003C substrate.

To investigate the performance for different PE sizes, we considered two PEs with different footprint areas: 1×0.5 mm^2 PE that covers the gap partially (Fig. 3); and 2×2 mm^2 PE, that fully covers the gap and centred relative to the shunt VIA (Fig. 1). Fig. 4 demonstrates the results of the parametric analysis, where the value of σ was varied from 0 to 100 S/m. Here, the asymptotic case of $\sigma = 5.8\times10^7$ S/m (copper conductivity) is also presented for comparison. It can be seen that the asymptotic levels of isolation ($1/|S_{12}|$, ON-state) for the 1×0.5 mm^2 and 2×2 mm^2 PEs are 10 dB and 24 dB respectively. However, the SPST with 2×2 mm^2 PE can provide higher isolation levels for some intermediate values of σ. We believe that this phenomenon is attributed to a resonance power dissipation inside the PE caused by a specific PE electric current distribution.

During fabrication, the PEs were mounted using silver-filled epoxy adhesive. Low-power light-emitting diodes (LED) were used as light sources. To prevent optical power loss, we mounted the LEDs right onto the top surfaces of the PEs. Note that in each case the PE area is larger than the LED area. Photos of the fabricated SPST prototypes are presented in Fig. 5.

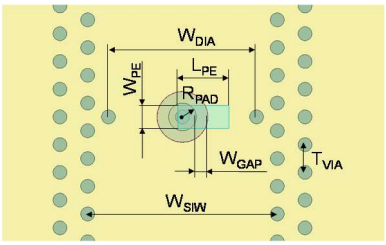

Fig. 3. Design parameters of the SPST PS

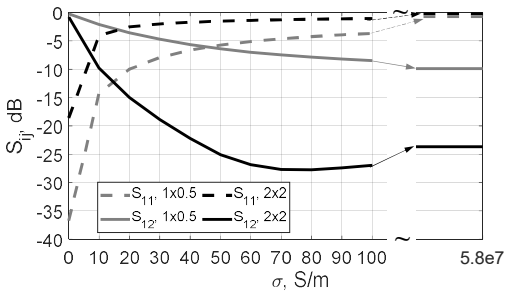

Fig. 4. Simulated *S*-parameters magnitudes of the SPST PS with different PE sizes versus σ at 24 GHz.

The SPST switch with the 1×0.5 mm^2 PE was actuated by the LED with lighting area 300×300 um^2 and 100 mW of DC power consumption, which is limited by the LED maximum forward current. The SPST switch with the 2×2 mm^2 PE was illuminated by the LED with 1×1 mm^2 lighting area. We varied the applied DC power in the range of 100 — 200 mW to investigate the isolation. In both cases, LED radiation efficiency was estimated as 40 % (accordingly with the manufacturer data).

The simulated and measured *S*-parameters for both SPST samples are shown in Fig. 6. Note that we used a SIW TRL setup to shift the measurement reference planes to 1 mm distance from the PE center. For the 1×0.5 mm^2 PE, the experimentally realized conductivity corresponds to 100 S/m in simulations, whereas for the 2×2 mm^2 PE we have a good agreement between 25 and 50 S/m in simulations and 100 and 200 mW DC in measurements, respectively. The PE volumes differ by eight times. According to (1), this should correspond to the eightfold difference in conductivity for the fixed value of applied optical power. However, from the experimental results, we observe only the fourfold difference (100 mW DC). It can be explained by different values of τ_{eff}, which are affected by the PE edges with excessive carriers recombination rate. Another possible reason is the non-uniform conductivity distribution inside the PE volume. The simulated radiation losses in the OFF-state are 23.7 and 20 dB for the 1×0.5 and 2×2 mm^2 PEs, respectively.

Table 1. Main parameters of SPST switches with different sizes of PE.

Parameters, mm	L_{PE}	W_{PE}	W_{DIA}	R_{PAD}	W_{GAP}
SPST 1×0.5	1	0.5	3.2	0.3	0.25
SPST 2×2	2	2	2.3	0.3	0.4

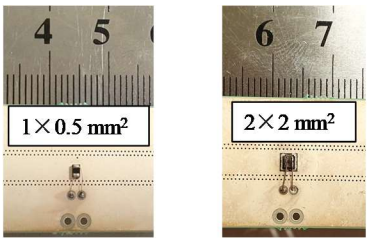

Fig. 5. Photographs of the fabricates SPST switches.

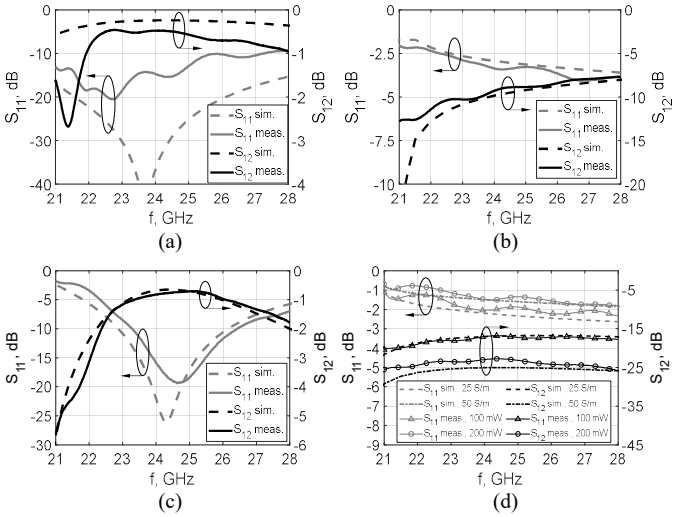

Fig. 6. *S*-parameters magnitudes of the SPST PS with different size of the PE: (a) 1×0.5 OFF-state; (b) 1×0.5 mm^2 ON-state; (c) 2×2 mm^2 OFF-state; (d) 2×2 mm^2 ON-state.

The measured performance of the SPST (OFF-state) with the 1×0.5 mm^2 PE demonstrates (21.5 — 27) GHz -10-dB impedance bandwidth, with the minimum insertion loss of 0.5 dB. However, the isolation level (ON-state) is relatively low (≥ 8 dB). This observation indicates weak shunting effects realized in the ON-state by the small actuated PE. On the other hand, the performance of the SPST with the 2×2 mm^2 PE is more promising in terms of isolation. The measured OFF-state –10-dB impedance bandwidth spans over (23.3 — 26.5) GHz range with the minimum insertion loss of 0.7 dB. The weakest isolation levels are 17 dB (100 mW DC) and 23 dB (200 mW DC). For both PSs, a small discrepancy between measured and simulated results can be explained by manufacturing and assembling tolerances. The measured switchings times are 3 us (OFF-to-ON) and 9 us (ON-to-OFF). Both PSs were successfully tested for up to 38 dBm of input power with 0.5 dB compression.

B. SPDT photoconductive switch

Because of the high isolation level, the 2×2 mm^2 PE was chosen for the development of a SIW single-pole double-through (SPDT) switch. The configuration of the switch is given in Fig. 7. The SPDT switch is based on two SPST blocks, connected to the input port (port 1, Fig. 7) through the H-plane SIW T-junction. At this stage, both PEs were placed at a relatively large distance $D/2$ = 8.15 mm from the T-junction center, which helps to provide input impedance matching using a single matching VIA compensating for the T-junction reactance (Fig. 7).

Fig. 8 presents photos of the fabricated SPDT prototype. Measurements were made in the two-port regime, i.e. two vector network analyzer's ports were connected to the PS ports

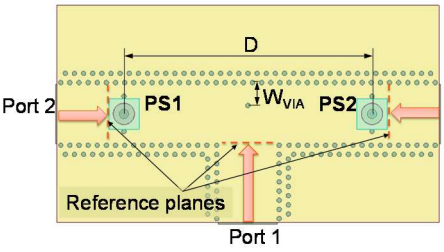

Fig. 7. SPDT switch geometry: D=16.3 mm, W_{VIA}=1.5 mm.

Fig. 8. Photo of the SPDT PS experimental prototype

Table 2. Comparison of different SIW switch technologies.

	[4]	[5]	[6]	[7]	[8]	[9]	**This paper**
Configuration	SPDT	SPST	SPDT	SPDT	SPST	SPST	SPST/SPDT
Technology	Mechanical	Ferrite-loaded SIW	Half-mode SIW with PIN diodes	SIW with PIN diodes	SIW with PIN diodes	SIW with PIN diodes	SIW with PEs
-10-dB imp. bandwidth, GHz	50 — 75 (40%)	9.5 — 10 (5%)	4.65 — 5.43 (15%)	8.24 —10.36 (23%)	20—24 (18%)	4— 4.2 (5%) 7—7.5 (7%)	23.3 — 26.5 (13%) / 23.0 — 24.8 (7.5%)
Ins. loss, dB	4.5	1	1.78	2.55	1.3	1—2	0.7 / 1.9
Isolation, dB	>45	>20	>28.5	>15	>10	>15	>22 / 25
Area, λ^2	1.14 × 0.58	0.53 × 0.33	1 × 1	0.9 × 0.9	1.13 × 0.38	0.4 × 0.4	0.328 × 0.16 / 1.464 × 0.328

1, 2 (Fig. 7), whereas the second SPDT output port was terminated with the matched load. The measurement reference planes are presented in Fig. 7. Fig. 9 shows the simulated and measured results. In simulations, we used σ = 50 S/m, whereas measurements were conducted with 200 mW DC power. A good agreement between simulated and measured return loss, insertion loss, and isolation can be observed inside the –10-dB impedance bandwidth. As before, some results discrepancies are attributed to the experimental prototype misalignments.

In Table 2, we summarized the main performance metrics of the developed PSs in comparison with the prior-art SIW switch designs.

IV. Conclusion

Three examples of the novel mmWave SIW switches based on the silicon PEs have been presented. The measured results evidence high performance of both SPST and SPDT switches in K-band. The main demonstrated advantages in comparison with the prior art are low insertion loss and design compactness. The future work will deal with further PSs size reduction and power consumption minimization. The latter can be addressed by the integrated LED-PE assembly and silicon wafer passivation.

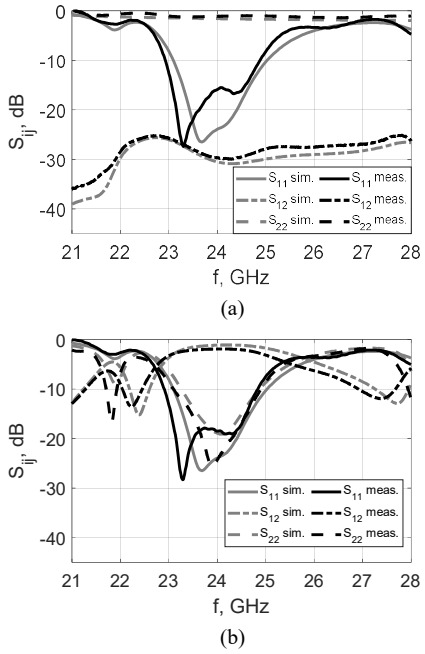

Fig. 9. *S*-parameters magnitudes of the SPDT PS: (a) State 1 (PS1 – ON-state; PS2 – OFF-state); (b) State 2 (PS1 – OFF-state; PS2 – ON-state).

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