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Wideband Slotline-to-Microstrip Transition for 210-375 GHz based on Marchand Baluns

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***Abstract*—This paper describes the design and cryogenic measurement of a novel slotline-to-microstrip transition based on Marchand baluns. The proposed transition is an attractive solution for numerous THz applications due to its remarkable broadband performance and compactness. For instance, such transition could be considered for wideband devices covering the frequency band 210-375 GHz. The suggested transition is designed on a thin silicon substrate and employs superconducting Nb as the electrode for the slotline and microstrip lines. In order to verify the performance of the designed transition, we fabricated a dedicated test structure consisting of two transitions connected back-to-back and integrated with E-probes at the waveguide interfaces. Due to the inherent bandwidth limitation of the E-probes, two different test structures for 210-295 GHz and 295-375 GHz were employed to characterize the proposed transition over the whole frequency band. The experimental verification performed at cryogenic temperatures showed results consistent with the simulation. Moreover, the cryogenic measurements indicated a remarkable 56% fractional bandwidth with an insertion loss as low as 0.3 dB for the fabricated slotline-to-microstrip transition.**

***Index Terms*—Broadband slotline-to-microstrip transition, Marchand balun, superconducting transition.**

I. Introduction

In the last decades, THz technology has experienced a rapid development driven by its numerous applications in radioastronomy [1], biomedical and medical science [2], material science [3], and THz wireless communications systems [4]. These applications often employ planar technology to integrate mixers, antennas, power dividers, amplifiers, and other various components, e.g. [5-10]. Furthermore, such components are frequently interconnected by microstrips lines which are the preferred transmission line in most modern Monolithic Microwave Integrated Circuits (MMIC) and thin-film technology chips employed in radioastronomy receivers [11-14]. Other transmission lines are occasionally used at the THz range, e.g., coplanar waveguides (CPW) and slotlines. In particular, slotlines are an attractive solution for implementation of planar devices [15], antenna feed [16], and finline transitions [17], [18]. Nevertheless, at THz frequencies, the realization of wideband and low loss slotline-to-microstrip transitions constitute a challenge that limits its applicability.

One of the main challenges in accomplishing a wideband and low loss slotline to microstrip transition is the inherent difference in their characteristic impedances, as analyzed in [15]. This problem is especially relevant for low impedances microstrip lines. While thin-film microstrip lines can reach an impedance of few Ω, thin-film slotlines cannot be fabricated with sufficient accuracy for impedances lower than 40 Ω [17], which hinders the application of classical solutions over large bandwidths, i.e., single-section 90° radial stubs [19] and double-Y baluns [20], where the best matching is found when the slotline and microstrip impedances are the same. The bandwidth limitation could be overcome through indirect transitions, where a piece of an auxiliary transmission line is placed between the slot and the microstrip [21]. Since the main requirements for the auxiliary line are a wide range of impedances and electromagnetic field compatibility with slotlines and microstrips, coplanar waveguides (CPW) are a widely adopted solution [15], [22]. Nevertheless, the overall fabrication complexity is further increased by suppressing the CPW parasitic mode through air bridges connecting both ground planes. Although indirect transitions reconcile the differences in the characteristic impedance of slotlines and microstrips and allow transitions with broader bandwidth, their fabrication complexity makes this solution less attractive.

Marchand baluns [22] could become an alternative solution for slotline-to-microstrip transitions. These baluns, commonly employed in low-frequency applications, combine different impedances to synthesize the transition response [22]. For instance, a Chebyshev passband response could be easily implemented. Moreover, the Chebyshev passband order is increased simply by adding more sections of the transmission line, which allows the selection of the bandwidth. Furthermore, this solution does not employ radial or circular stubs, thus reducing the required chip area. These features make the Marchand baluns a promising solution for the design of wideband low-loss transitions. However, to the authors' best knowledge, these baluns have not been previously considered for sub-mm applications.

This paper investigates Marchand baluns as a potential

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solution for wideband low-loss slotline to microstrip transitions for THz applications. In particular, the proposed cryogenic structure could be considered for the future design of a wideband mixer chip for radioastronomy applications in the 210-375 GHz frequency range. This particular frequency range combines band 6 (211-275 GHz) and band 7 (275 GHz-375GHz) of the Atacama Large Millimeter/submillimeter Array (ALMA) [23].

This paper is organized as follows: Section II-A describes the Marchand balun theory of operation, the design steps, and the electromagnetic simulation of the structure. Furthermore, section II-B details the integration of the designed balun in a back-to-back layout for experimental verification. Section III describes the fabrication process. Meanwhile, section IV addresses the measurement of the device at cryogenic temperatures, and section V discusses the results and their implications. Finally, Section VI presents the concluding remarks.

II. Theory and Design

A. Marchand Balun Design

The proposed transition depicted in Fig. 1 is based on a third-order Chebyshev Marchand balun. The balun consists of a microstrip and a slotline that are placed perpendicular to each other. In the suggested design, the balun is patterned on top of a 30 µm Si substrate. This material was selected due to its low loss at the temperature of operation of the structure, i.e., 4K [24]. The slotline is patterned in 450 nm thick superconducting Nb, which acts as the microstrip ground. Meanwhile, the microstrip is also formed by Nb patterned over 1.3 µm of SiO_2. This dielectric thickness was selected to achieve the desired impedance range while the microstrip width remains feasible for standard photolithography techniques.

Fig. 2 outlines the different impedances employed in the transition as an equivalent circuit diagram. It is important to remark that the employed Marchand Balun is one of the existing configurations detailed in [22] and other impedance arrangements could be implemented to achieve the slotline to microstrip transition. In the proposed design, the transition transforms a 45 Ω microstrip, denominated as Z_{0M}, into a 60 Ω slotline, referred to as Z_{0S}. The transformation is accomplished with an open circuit microstrip stub and a short circuit slotline stub, with Z_1 and Z_2 characteristic impedances, respectively. Besides, Z_3 is realized as a λ/4 slotline section that matches the intersection impedance to Z_{0S}.

The procedure to calculate the impedances Z_1, Z_2, and Z_3 can be found in [22]. Nevertheless, we present here a simplified set of equations:

$$Z_3 = Z_{0M}\sqrt{\frac{Z_{0S}}{Z_{0M}}} \tag{1}$$

$$Z_2 = \left[-\sqrt{\frac{Z_{0S}}{Z_{0M}}} + \left(\frac{Z_{0S}}{Z_{0M}} + \frac{\alpha^2+\beta^2}{(\alpha-1)\tan^2\theta}\right)^{\frac{1}{2}}\right] Z_{0M} \tag{2}$$

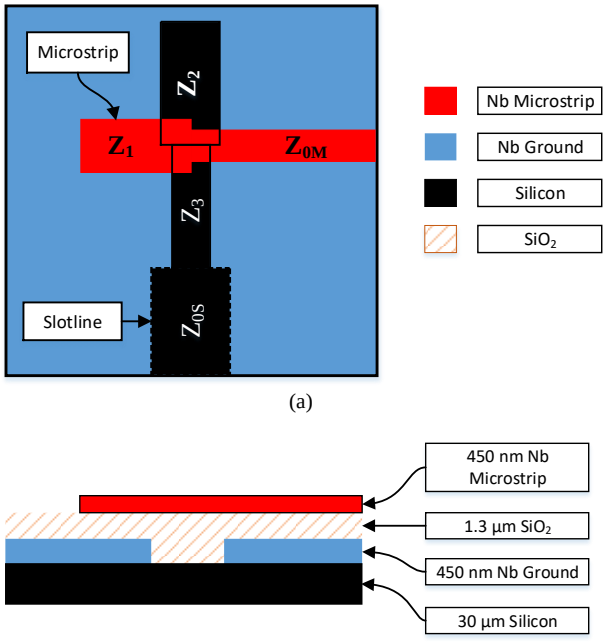

Fig. 1. Schematic picture of the proposed slotline-to-microstrip transition employing a third-order Chebyshev Marchand Balun. (a) Top view of the transition. Note that the SiO_2 layer is not displayed for clarity. The complete SiO_2 layout can be found in Fig.5. (b) Lateral view of the transitions where the different layers and thicknesses are detailed.

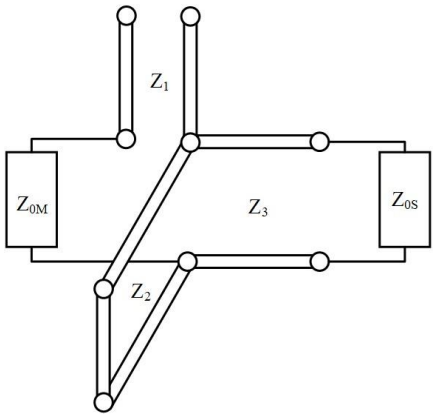

Fig. 2. Equivalent circuit diagram of the balun. The microstrip impedance Z_{0M} is 45 Ω, while the slotline impedance Z_{0S} is 60 Ω. Thus, the impedances Z_2 and Z_3 are realized with slotlines. Meanwhile, the short circuit stub with a characteristic impedance Z_1 is realized as a microstrip line.

TABLE I
Dimensions for Transmission Lines

	*Simulated Impedances [Ω]	Width [µm]		**Length [µm]	
		Calculated	Optimized	Calculated	Optimized
Z_{0M}	45	3	3	100	100
Z_1	23	8	8	143	126
Z_2	54	6	5	112.5	107.5
Z_3	51	2	4	110.6	122
Z_{0S}	~ 60	4	10	130	130

* The impedance values correspond to the optimized widths, taking the SiO_2 over layer into consideration. ** The calculated length of the transmission lines correspond to $\lambda_g/4$ at 293 GHz for Z_1, Z_2 and Z_3. The length of the microstrip and the slotline were selected to properly connect the back-to-back structure.

$$Z_1 = \left[\frac{\alpha^2 + \beta(\beta + \frac{Z_2}{Z_{0M}}\tan\theta)}{\alpha^2 + (\beta + \frac{Z_2}{Z_{0M}}\tan\theta)^2}\frac{Z_2}{Z_{0M}}\tan^2\theta\right]Z_{0M} \quad (3)$$

$$\alpha = \frac{Z_{0S}}{Z_{0M}}.\left(\frac{1+\tan^2\theta}{1+\frac{Z_{0S}}{Z_{0M}}\mathrm{Tan}^2\theta}\right) \quad (4)$$

$$\beta = \sqrt{\frac{Z_{0S}}{Z_{0M}}}\left(1-\frac{Z_{0S}}{Z_{0M}}\right)\frac{\tan\theta}{1+\frac{Z_{0S}}{Z_{0M}}\tan^2\theta} \quad (5)$$

The terms α and β are used solely to simplify the presentation of the equations. Meanwhile, the variable θ, expressed in degrees, determines the theoretical bandwidth of the Chebyshev response. The relation between the angle θ and the overall bandwidth of the transformer was numerically calculated in [22], showing an inverse non-linear relation between these two variables.

As a starting point for our Chebyshev design, we selected θ equal to 63.711°, which theoretically provides 50 % fractional bandwidth, to calculate the characteristic impedances detailed in Table I. In order to realize the slotline impedances Z_{0S}, Z_2, and Z_3 and compute their width and length, the approximations presented in [17] were employed. The length of the transmission lines was established to $\lambda_g/4$, where λ_g correspond to the guided wavelength at the center frequency, i.e. 293 GHz. Nonetheless, in the slotline impedance approximations, we did not consider the SiO_2 layer deposited over the slotline. In addition, the model did not take into account the proximity of the metallic walls of the cavity, which further reduced the slotline impedance. As a result, the slotline widths were corrected to account for these deviations. The correction was implemented by simulating a section of the slotline and adjusting its width to match the desired impedance. In particular, the width of the Z_{0S} slotline was widened to preserve the 60 Ω impedance. After the dimensions of the transmission lines were defined the complete Marchand Balun was simulated and optimized to obtain minimum insertion loss and the best possible reflection loss in the full-wave 3-D simulator Ansys HFSS [25].

The optimization process included variations in the widths and lengths of the transmission lines. The optimization aimed to improve the insertion loss and return loss of the structure, assuming constraints of the fabrication technology. In Fig. 3, it can be seen that the optimization was performed for a back-to-back layout, where both input and output are microstrips. This layout responds to the particular characteristics of the simulator, where microstrips are simpler to excite than slotlines. Moreover, the back-to-back arrangement is convenient for experimental verification. In the simulations, the superconducting Nb was assumed as a perfect conductor. This approximation was appropriate since the superconductor thickness is much thicker than the London penetration depth, i.e., $\lambda_L \approx 0.1$ µm [26]. The dielectric thickness of the microstrip is several times the thickness of Nb, i.e., 1.3 µm and 0.45 µm, respectively. Under these conditions, the superconducting

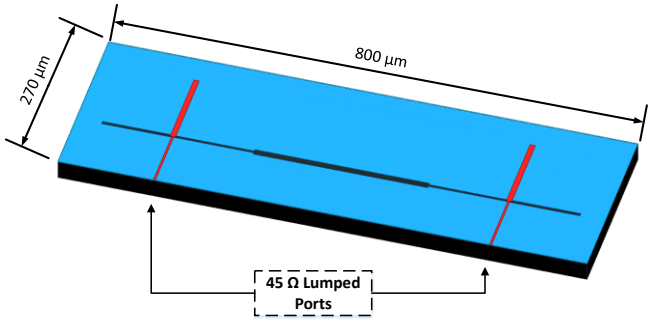

Fig. 3. Simulation model of the back-to-back structure where both input and output are microstrip lines. The microstrip was excited with 45 Ω lumped ports and centered in a metallic cabity of 800 µm in width and 200 µm in height.

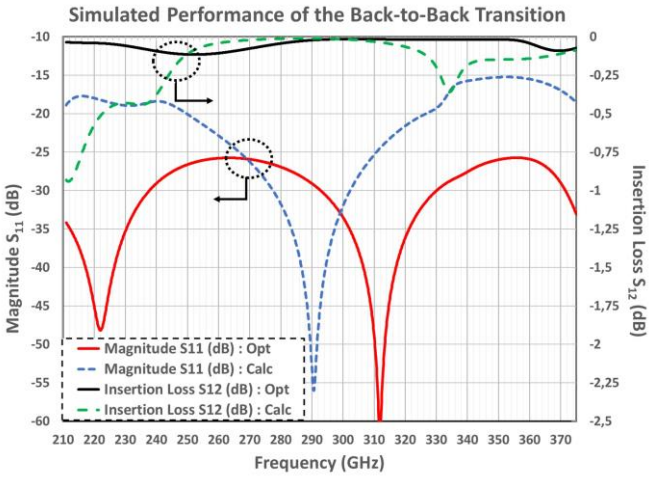

Fig. 4. Simulated S-parameters for the Marchand balun transition in a back-to-back arrangement as shown in Fig. 3. The simulation of the calculated and optimized parameters is shown for comparison.

microstrip impedance could be approximated to a microstrip with perfect conductor electrodes as investigated in [26], [27].

The simulation results for the back-to-back balun (Fig. 3) are presented in Fig.4, where the calculated and optimized transition can be compared. The graph shows that the simulated return loss for the optimized back-to-back Marchand balun is better than 25 dB over the whole band. Furthermore, the insertion loss is better than 0.1 dB over the entire frequency range.

B. Test Structure Design

With the purpose of measuring the suggested transition and comparing the results with the simulations, the balun was integrated into the test chip depicted in Fig 5 (a) and (b). The 30 µm thick chip integrates back-to-back structures composed of the Marchand balun and a pair of E-probes. However, a single E-probe cannot cover the entire operational bandwidth of the balun adequately, i.e., 210-375 GHz. Therefore, two different versions of the test chip were designed. The first version of the chip incorporated the probe shown in Fig.5(c) and covered 210-295 GHz lower frequency range. Meanwhile, a second version that integrates the probe depicted in Fig.5(d) covered the higher frequency range 295-375 GHz. Thus, the Marchand balun performance was evaluated by concatenating the low-frequency chip (LF) and high-frequency (HF) responses. It is important to remark that the LF differed from

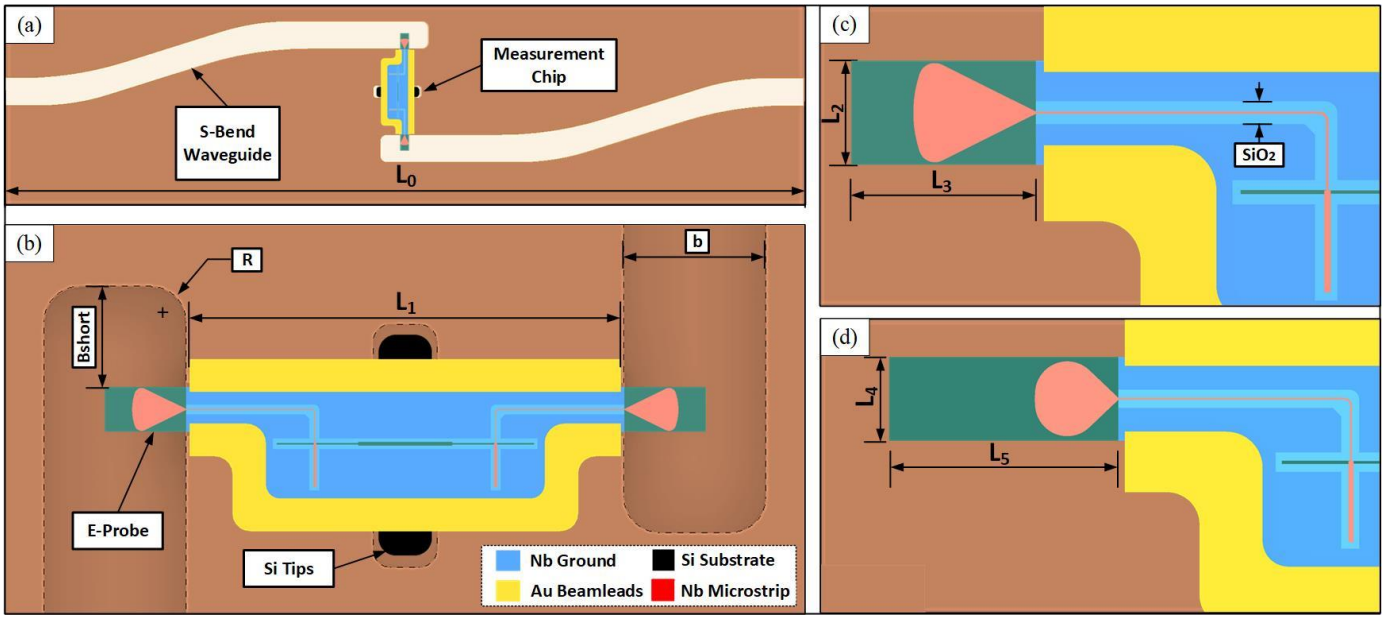

Fig. 5. Test structures and waveguide block. Two separate chips are employed to cover the full bandwidth of the proposed transition: A Low Frequency band chip (LF) for 210-295 GHz and a High Frequency band chip (HF) for 295-375 GHz (a) Test chip mounted in the lower half of the split block. The block incorporates S-bend waveguides to maintain the alignment of the input and output waveguides. L_0=11.47 mm corresponds to the length of the simulated block (b) Top view of the LF chip. The values are: L_1=1.211 mm, R=100 µm, Bshort=280 µm, b=400 µm. Note that the block for the HF chip in the backshort distance (Bshort), which is 132 µm. (c) Detail of the probe and the microstrip interconnection for the LF chip. The depicted values L_3=129 µm and L_4=229 µm correspond to the Si area that supports the probe inside the waveguide channel. For the sake of clarity, the SiO_2 is shown as a transparent layer. (d) Detail of the probe and the microstrip interconnection for the HF chip. The values of L_4 and L_5 are 130 µm and 356 µm, respectively.

the HF chip only in the probe shape and back-short distance of the waveguide. The back-short for the HF chip was naturally shorter since the structure was tuned for higher frequency operation.

The probes were designed and optimized in the full-wave 3D simulator Ansys HFSS [25]. The optimization included a straight section of microstrip that connects the probe with a 90° microstrip bend terminated in 45 Ω, i.e., Z_{0M}. The microstrip bend was introduced to accommodate the Marchand balun transition in a back-to-back layout. In Fig. 5(b), the simulated LF chip mounted in the lower half of the split block is shown. The block input and output waveguides are a=800 µm and b=400 µm, which were selected to adequately cover the entire frequency range (210-375GHz). In Fig 5(a), it is seen that the block incorporates S-bend waveguides to align the input and output waveguides properly. Moreover, the chip was grounded through a 5 µm thick Au beamleads that extend 80 µm beyond the silicon substrate. The beamleads provide an electrical connection between the niobium ground layer and the tellurium-copper block since the Au is clamped and smashed between the two waveguide halves. Furthermore, a pair of Si tips were included on both sides of the chip to facilitate the structure's handling and alignment. These Si tips fit inside specially made recesses, but they did not support the structure since the substrate was suspended on the beamleads over the lower half of the block. It is important to note that the SiO_2 layer was not deposited over the whole area, but rather it had been limited to certain specific regions below the microstrip and over the slotline, as depicted in Fig. 5c. In addition, the SiO_2 layer underneath the microstrip extended beneath the E-probes and covered the Si substrate hanging inside the waveguide, i.e., the

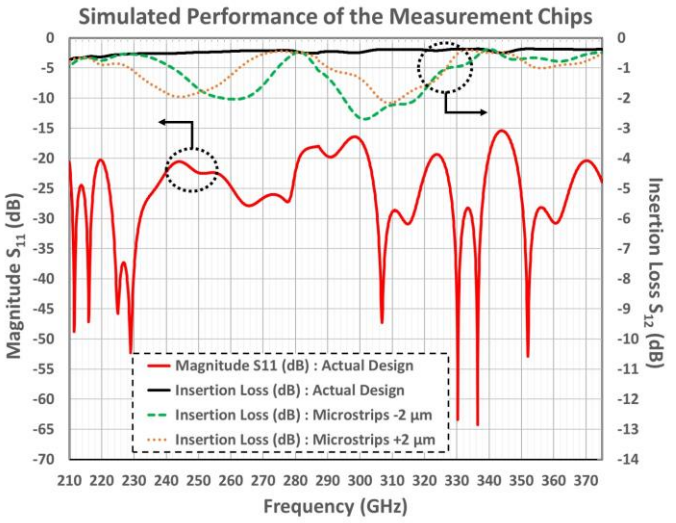

Fig. 6. Simulated S-parameters for the test structures depicted in Fig.5. For clarity, the graph combines the simulated performance of the LF and HF chips. Moreover, the insertion loss for inaccuracies of ±2 µm in the microstrip width is shown.

areas defined by L_2-L_3 in Fig. 5 (c) and L_4-L_5in Fig. 5 (d). The minimization of the SiO_2 area was motivated by the material stress that this layer may introduce into the structure.

The combined S-parameters performance of both chips is illustrated in Fig.6. The simulation includes the contribution of straight and S-bend copper waveguides, as depicted in Fig. 5 (a). Therefore, the total length of the simulated block was 11.47 mm. From the graph, it is clearly seen that the return loss is better than 15 dB in the entire band. Moreover, the insertion loss of the concatenated responses is less than 0.7 dB for the

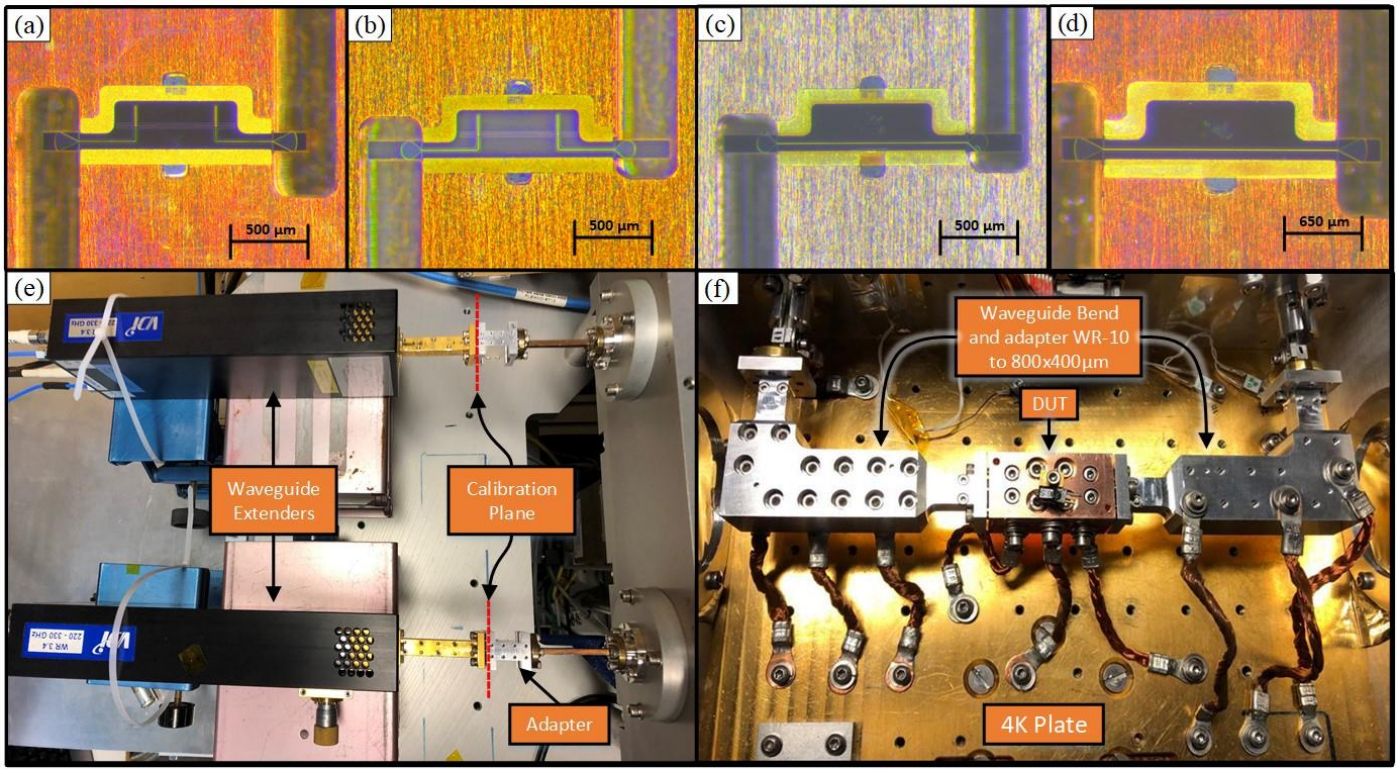

Fig. 7. Fabricated chips and Measurement setup. (a) Fabricated Low Frequency chip for 210-295 GHz. (b) Fabricated High Frequency chip 295-375 GHz. (c) Fabricated Low Frequency calibration chip for 210-295 GHz. (d) Fabricated High Frequency calibration chip for 295-375 GHz. (e) WR-3.4 frequency extension modules connected to the cryostat input. The calibration plane is located outside the cryostat. (f) Detail of the waveguide chain connected inside the cryostat.

whole band. In the produced structures, the microfabrication techniques employed to fabricate the structure might affect the overall performance due to inherent inaccuracies in the process. From the analysis of the fabricated devices, we have found out that our current process has an accuracy of ±2 µm. Moreover, the width of the thin-film microstrips seems particularly critical and more prompt to inaccuracies during fabrication than the slotline. Therefore, two different scenarios were simulated to evaluate a ±2 µm accuracy in the performance. As illustrated by Fig. 6, the insertion loss is degraded due to the impedance mismatch introduced by the imperfections in the microstrip widths. Nonetheless, it is worth noting that the insertion loss for a single balun transition and the integrated E-probe remains below 1.5 dB for the whole wide RF band.

III. Fabrication

The process employed for fabricating the test structures is similar to the one described in [17]. The samples were fabricated from a silicon-on-insulator (SOI) substrate with a 300 µm handle layer, 2 µm barrier layer SiO_2, and 30 µm device layer. The SOI structure facilitates handling the thin devices and provides a natural etch-stop layer for the Si etching.

The fabrication consisted of 2 stages: the front-side and the back-side processing. For the front-side processing, the 450nm Nb films of the superconducting lines were deposited by dc magnetron sputtering while the SiO_2 layer was deposited by a reactive RF magnetron sputtering. The microstrip and slotline were defined employing photoresist soft-masks and reactive ion etching (RIE) process. Meanwhile, the SiO_2 layer was dry-etched with the help of an Al hard mask. Moreover, the Au beamleads were created through electroplating process. Afterward, for the back-side patterning, the chip was mounted upside down on a 4-inch Si carrier wafer. The handle layer and buried oxide were removed through dry etching. Finally, a thick photoresist etch mask was created by photolithography. This soft mask is used for the final anisotropic etching that completes the device definition. Finally, the devices are released in a solvent.

Fig 7(a) and 7(b) show the fabricated LF and HF chips, respectively. It is important to note that calibration chips were fabricated for the high and low-frequency band, as depicted in Fig 7(c) and 7(d). The calibration chips do not include the back-to-back Marchand Balun structure, but they have a single microstrip that interconnects both E-probes. These chips were employed as a reference for cryogenic measurements.

IV. Cryogenic Measurements

The experimental verification of the fabricated devices was performed at 4K inside a cryostat with a closed-cycle refrigerator. The S-parameters were measured employing a Keysight PNA-X 5242A and frequency extension modules from Virginia Diodes Inc. [31]. Due to the considerable fractional bandwidth of the DUT, three pairs of extension modules for different frequency ranges were employed in the measurements, i.e., WR-5.1 (140-220 GHz), WR-3.4 (220-330 GHz), and WR-2.2 (330-500 GHz). However, the cryostat input

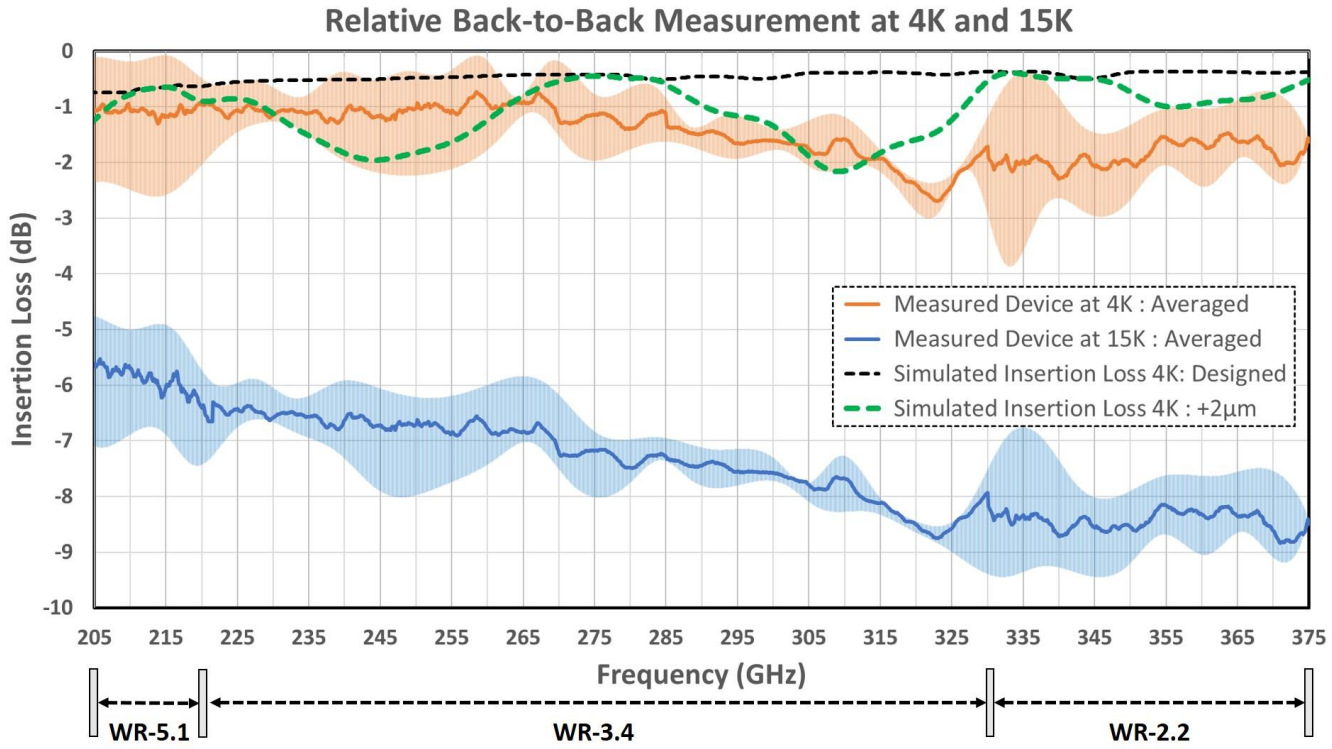

Fig. 8. Relative insertion loss at 4K and 15K for the fabricated back-to-back test structures depicted in Fig. 7a and 7b. The measurements are shown employing a waveguide thru at 4K as reference. The minimum and maximum insertion loss for each measurement point are plotted surrounding the average value. Note the relative measurements includes the contribution of the S waveguides and E-probe transitions. The frequency bands employed during the measurements are depicted. Furthermore, the graph shows the simulated insertion loss at 4K for two scenarios: designed microstrip and +2 µm wider microstrips.

waveguides were WR-10 (2.540 x 1.270 mm), hence a pair of adapters for each extension module were located at room temperature, as depicted in Fig. 7(e). These waveguide adapters convert the WR-10 dimensions into the waveguide size required by the extension modules. Furthermore, in Fig. 7(f), it is seen that a pair of adapters were located inside the cryostat as well, which allows to transition from WR-10 to the DUT waveguide dimensions, i.e., 800 µm in width and 200 µm in height. The DUT block was fabricated in tellurium copper by direct milling. In order to facilitate the block interconnection, straight waveguide sections were added to the design presented in Fig. 5(a) to complete an overall block length of 4 cm. Besides, six cooling straps were attached from the waveguide chain to the 4K plate to ensure adequate thermal contact.

The measurement of the complete set of S-parameters at cryogenic temperatures presents significant challenges. This is particularly relevant at higher frequencies where waveguide systems are employed. The main problem lies in the reduction of the waveguide chain losses during cooling and the geometry change due to the material thermal contraction. This phenomenon dramatically affects the reference planes calibrated at warm since the calibration overestimates the losses. The shift in the calibration planes might be corrected by measuring a short or open circuit standard at 4K, as analyzed in [28]. This method for cryogenic measurements is frequently applied at lower frequencies where coaxial cables are employed. Nonetheless, this procedure is not practical at higher frequencies due to the waveguide chain thermal contraction. The thermal shrinking is comparable to a guided wavelength and precludes an accurate correction of room temperature calibrations. Alternatively, a direct calibration could be applied inside the cryostat at 4K. Unfortunately, this measuring approach requires a cooling cycle for each calibration standard and the DUT measurement itself. A single cooling cycle starts with pumping the cryostat chamber to a proper vacuum level, followed by cooling it down to 4K. After the measurements are performed, the chamber is warmed up to room temperature once more. Since each cooling cycle takes between 7 to 8 hours, the complete calibration and measurement might take a significant amount of time to complete. During this period, the inherent drift of the VNA and the variability in the environmental conditions will severely degrade the calibration accuracy. Therefore, a straightforward approach presented in [17] was employed to measure the losses of the DUT. In this method, we consider that given the low insertion loss expected for the chip, the reflection loss should remain under an appropriate level. Furthermore, if the simulation and measurements of the insertion loss are consistent, then it could be concluded that the reflection of the chip should follow a similar pattern to the predicted by the simulations.

The cryogenic measurement method describe in [17] employs a standard warm thru, reflect, line (TRL) calibration at the input of the cryostat, as shown in Fig. 7(e). This calibration was later used to measure the DUT and a waveguide thru at 4K and 15K. The waveguide thru consists of a straight waveguide section with dimensions identical to the DUT block. The rest of the waveguide chain was identical for both measurements, which allows a direct comparison of the DUT insertion loss with the waveguide thru as reference. As a result, the relative insertion loss of the DUT could be obtained and compared with

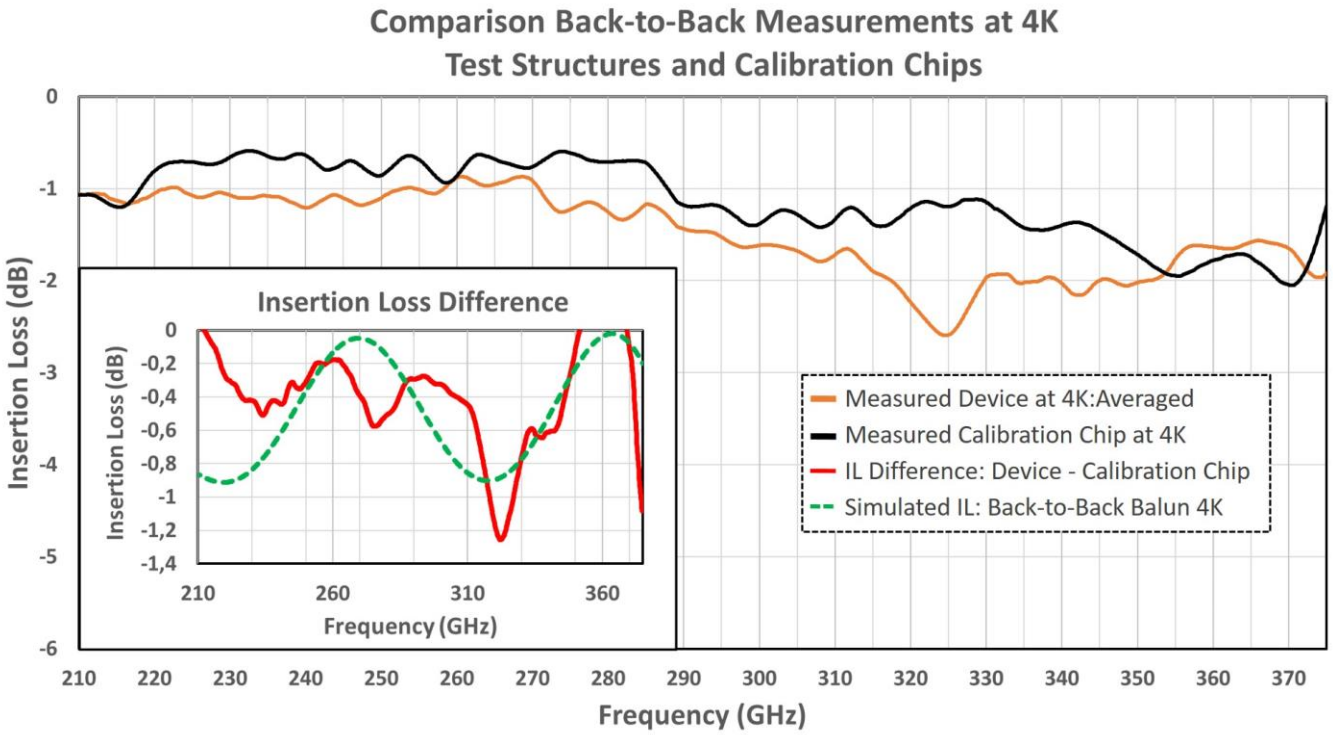

Fig. 10. Insertion loss comparison at 4K for the fabricated back-to-back test structures and the calibration chips. The measured transmission loss shown here is calibrated by using a waveguide thru at 4K as reference. The combined response of the calibration chips depicted in Fig. 7(c) and Fig. 7(d) is depicted. The inserted graph shows the insertion loss (IL) difference beween the fabricated back-to-back test structures and the calibration chips. The IL difference provides an approximation for the losses associated solely to the back-to-back Marchand Baluns without E-probes, S-waveguides and microstrip interconnections. Moreover, the inserted graph depicts a simulation of back-to-back Marchand Baluns with +2 µm wider microstrip.

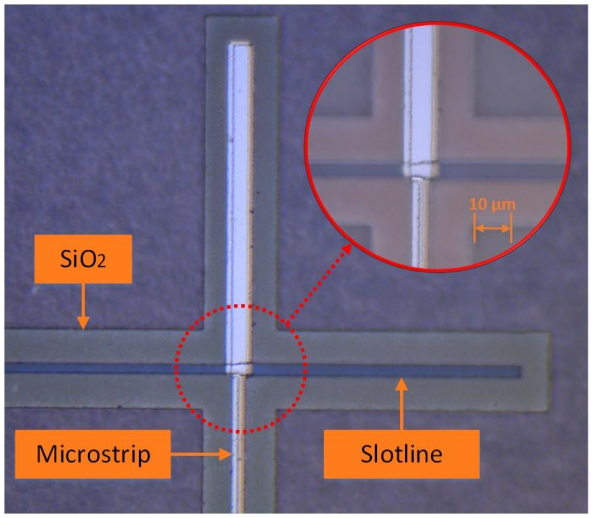

Fig. 9. Microscope image of the fabricated Marchand balun transition. The details of the microstirp, slotline and SiO_2 are appreciated. A close inspection confirms a +2 µm discrepancy in the widths of the microstrips .

the simulations. The same procedure was repeated for each of the frequency bands. Furthermore, the fabricated calibrations chips might be employed to de-embed the losses of the E-Probes and interconnection microstrips. Therefore, the losses associated solely with a single section of Marchand Balun could be extracted and analysed.

V. Results and Discussion

The simulation and measurement results of the fabricated chips are illustrated in Fig. 8. The results displayed in the graph were obtained from the measurement of multiple LF (Fig. 7(a)) and HF chips (Fig 7(b)). For these measurements, a waveguide thru at cryogenic temperatures was employed as reference. The chart shows the mean value of the relative insertion loss from the tested chips. Moreover, the graph depicts the minimum and maximum insertion loss values measured at each point. This variation accounts for microfabrication differences between the tested structures, chip mounting imperfections, block fabrication tolerances, and the inherent drift of the VNA and extender modules. In particular, multiple measurements were performed and compared on each measured chip to estimate the error solely due to the instrumentation. As a result, it was found that the mean error attributed to the instrumentation is ±0.02 dB. Therefore, the mean variation due to the fabrication differences between the tested DUTs could be estimated as ±0.58 dB. Thus, the error analysis indicates an accurate measurement and supports the good repeatability of the results.

As depicted in Fig. 8, the test structures were characterized at 4K and 15K to compare the insertion loss difference between the normal and superconducting state of Nb. It was found that the transition temperature of the Nb film occurs around 9K, which is consistent with values found in the literature for thin-film Nb layers [29].

From the graph, it is observed that the measured insertion loss for the test structure at 4K is less than 2 dB over most of the entire operating bandwidth. Nonetheless, the simulated design differs from the averaged measured performance. This difference could be quantified by the mean absolute error (μ_n)

between the simulated and experimental curves. In this case, μ_n takes a value of 1.045 dB. The difference between the curves might be explained by fabrication inaccuracies. The measured chips were carefully inspected under a microscope and it was found +2 μm discrepancy in the widths of the microstrips as shown in Fig. 9. The discrepancy was included in the simulation in Fig.8. An overall good agreement is observed between the +2 μm simulation and the experimental data with a considerably lower μ_n value of 0.68 dB. Nevertheless, the upper side of the band slightly deviates from the predicted behavior. Such deviation is believed to be related to minor differences between the DUT block and waveguide thru.

It is worth noting that the measured 2 dB insertion loss corresponds to test structures with the back-to-back arrangements of Fig. 7(a) and Fig7(b). Therefore, the insertion loss of the back-to-back Marchand balun could be estimated if the contribution of the E-probes, microstrip interconnections, and S-waveguides are known. The calibration chips depicted in Fig 7(c) and 7(d) were mounted under equal conditions as the test structures and measured at 4K. Fig. 10 shows the measurements comparison of the test structures and the calibration chips. It is seen that for the majority of the band the calibration chips present lower losses than the test structures as expected. Nonetheless, this is not the case for the 355 to 375 GHz frequency range. This phenomenon might be explained by a small difference in the calibration chip.

As depicted in the inserted graph in Fig.10, the insertion loss difference between the test structures and the calibration chip provides an approximation for the losses associated solely with the back-to-back Marchand Balun, i.e. without the contributions from E-probes, microstrip interconnections, and S-waveguides sections. The losses of the fabricated back-to-back balun were found to be 0.6 dB for most of the band. Therefore, the losses for a single slotline-to-microstrip transition were estimated to be 0.3 dB for most operational bandwidth. Moreover, the inserted graph shows a simulation of a back-to-back slotline-to-microstrip transition with a +2 μm discrepancy in the widths of the microstrips. The width discrepancy generates standing waves in the simulation curve due to impedance mismatch. It is seen that simulations and measurements are in a reasonably good agreement.

Most notably, the measured fractional bandwidth corresponds to 56 %, i.e., 210 - 375 GHz. Such notable bandwidth is a considerable improvement over earlier communicated THz slotline-to-microstrip transitions, as [30] that achieved 40% fractional bandwidth. In addition, the proposed transition stands out for its compactness since it does not require large radial stubs to accomplish a proper bandwidth, as is the case in [21]. Thus, when compared with existing designs for slotline-to-microstrip transitions at THz frequencies, it becomes clear that the Marchand Baluns are a promising solution for their outstanding fractional bandwidth, low loss, and compactness.

VI. Conclusion

In this paper, we have demonstrated a novel slotline-to-microstrip transition for 210-375 GHz based on Marchand baluns. Furthermore, we have described the design, simulation, and cryogenic characterization of the suggested balun. The proposed baluns were integrated with E-probes and characterized at cryogenic temperatures. From the experimental verification, it was estimated that the insertion loss of the slotline-to-microstrip balun was as low as 0.3 dB for the whole band. Moreover, the fabricated devices reach an outstanding 56% fractional bandwidth. The simulations showed good agreement with the measurements when the expected microstrip fabrication inaccuracies are considered. To the authors' knowledge, in this work, we have presented the first direct measurement of a slotline-to-microstrip transition at THz frequencies and cryogenic temperatures.

The proposed transition is especially suited for THz applications due to its large bandwidth and compactness. What is more, the design detailed in this paper might be easily employed for different frequency ranges as well, making the presented transition an attractive solution for a wide variety of applications.

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