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Enhancing mmWave On-Chip-Antennas Using In-Package Electromagnetic Bandgap Structures

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***Abstract* — We propose a silicon on-Chip-in-Package antenna design featuring a simulated radiation efficiency of $> 70\%$ and an S_{11} matching better than -10 dB in the 112–125 GHz frequency range. High radiation performance is achieved by: (i) thinning the silicon substrate down to 100 μm through wafer-level grinding; (ii) embedding the IC in-between two PCBs, one of which forms an electromagnetic bandgap structure that attenuates the EM leakage inside the silicon substrate. Furthermore, since the die-embedding concept employs the gap-waveguide packaging technology, a universal contactless waveguide interconnect is realized between the IC and the radiating gap waveguide in the package. This will also enable modular antenna designs.**

***Keywords* — Gap waveguide technology, millimeter-wave antennas, on-chip antennas, antenna-in-package.**

I. Introduction

In the antenna-on-chip (AoC) approach one co-integrates antennas with the RF electronics on a single integrated circuit (IC). Bringing the antennas closer to the active circuitry minimizes the mismatch and RF interconnection losses. AoCs become tractable above 100 GHz when the antenna does not occupy too much of the expensive chip area.

SiGe Bi-CMOS technologies promise both high performance and high integration density at sub-THz frequencies at relatively low cost [1]. Epitaxial layers are formed on top of the p-doped bulk silicon substrate that is often 0.3–0.8 mm thick and has low resistivity of 20–50 Ω cm [2]. Along with the high relative permittivity of silicon ($\epsilon_r \approx 11.9$), the AoC design becomes a challenging task; most of the radiation propagates in the substrate which leads to cross-talk effects between on-chip elements, field diffraction effects at the chip edges leading to pattern gain ripples and high Ohmic losses [3]. If these problems are left unattended, the radiation efficiency of the on-chip antennas will typically be less than 10 % [4].

The chip's back-end-of-line (BEoL) metalization layers can be used to shield-off the lossy silicon substrate. However, the BEoL is often very thin ($\approx 14\,\mu$m), and even at 100+ GHz the ground plane is too close to the radiating element. The fractional bandwidth in this case is typically 3–4 %. The radiation efficiency is improved, despite the conductor loss increases, but still is below 20 % [5]. Alternatively, an air cavity can be created under the antenna, which can result in a 50+ % radiation efficiency over a wide bandwidth [6]. However, the substrate waves (SW) problem is only partially solved, so that the antenna performance still depends on the chip size. In addition, micro-machining or localized etching are often used to form the cavity, and these post-processing steps increase the cost and the fabrication complexity. A third approach is to use metamaterials. With 2D-periodic structures, one can form an electromagnetic bandgap (EBG) to forbid SW modes from propagation [7]. A periodic structure in the IC's BEoL can be designed to act as an artificial magnetic conductor (AMC) that does not deteriorate the performance of an antenna as much as the regular ground plane. This can enhance the antenna gain by as much as 8 dB, but it limits the bandwidth to 3–4% [8]. Alternatively, SW modes can be cancelled through destructive interference by clever placement of the array elements [9].

This paper presents a novel EBG-based packaging approach, which is based on the gap waveguide packaging technology [10], that does not require expensive post-processing steps and will attenuate the SWs over a large bandwidth (60–150 GHz).

Key advantageous features of the EBG package are:

- Suppression of SW mode propagation in the silicon substrate of an AoC. This increases the radiation efficiency and decreases the chip-size dependence (e.g. decreases pattern gain ripples).
- Reduction of array mutual coupling and/or AoC-to-circuit coupling effects.
- Contactless standardized RF interface to open-ended radiating waveguide in the package constituting a universal connection between a base package and an Antenna-in-Package (AiP). (see also [11]).

Sec. II introduces our design and explains how the EBG is formed. In Sec. III we show the simulated performance with and without the EBG structure. In Sec. IV we summarize our findings.

II. Proposed Design

In our design, a silicon chip is sandwiched between two PCBs (embedded die packaging), each having two intermediate metal layers, see Fig. 1. A cross-section of the proposed antenna can be found in Fig. 2(a). A radiation-enhancing cavity is formed by vias in the bottom PCB. This ensures an optimal separation between the radiating elements that are located in the BEoL of the IC and the bottom ground plane of the PCB on which the whole device is resting. This forms the base package. The top PCB/package forms the gap waveguide EBG structure [12], where the vias and the lowest metal layers form the AMC, and the metal layers in

the silicon dioxide layer of the chip form the PEC surface [*cf.* Fig. 2(b)]. The two PCBs and the silicon chip effectively form a dielectric-filled waveguide, which can be excited in one of the desired polarizations by two opposite E-field probes [*cf.* Fig. 2(c)]. Each probe is $225\,\mu\text{m}$ long and $50\,\mu\text{m}$ wide. The cavity size and the open-ended waveguide aperture size is $1.1\times1.1\ \text{mm}^2$.

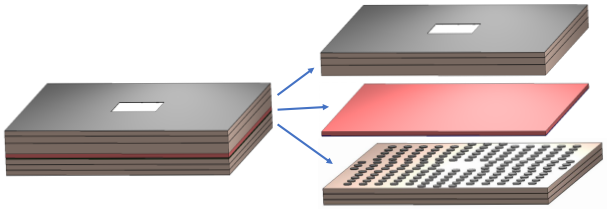

Fig. 1. Proposed structure: a silicon IC sandwiched between two PCBs.

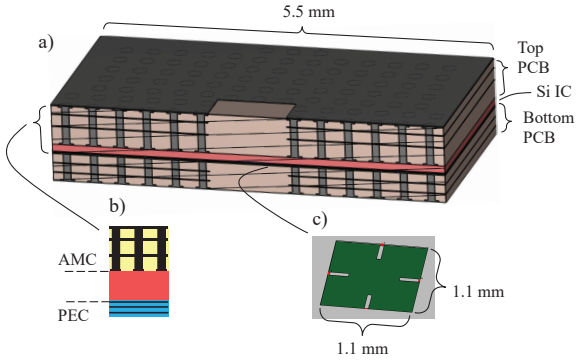

Fig. 2. (a) A cross-section of the proposed structure; (b) The bandgap structure is formed between the vias in the top PCB (AMC) and the bottom metal layers (M1-M7) of the silicon chip (PEC), and; (c) Dual-polarization feeding.

The silicon chip thickness in our simulations is $100\,\mu\text{m}$ (can be achieved by wafer-level grinding), the conductivity of the p-doped substrate is $\sigma = 2$ S/m and the relative permittivity $\epsilon_r = 11.9$. The silicon dioxide layer is $15\,\mu\text{m}$ thick, has the relative permittivity $\epsilon_r = 4.1$ and is assumed lossless. There are seven metal layers in the dioxide layer, all of them combined in a single $13\,\mu\text{m}$ thick metal layer for simplicity. The chip lies "face down" in order to use the flip-chip technology with Cu-pillars connecting the chip's BEoL to the vias in the bottom PCB. A $20\,\mu\text{m}$ thick epoxy layer with $\epsilon_r = 3$ and loss tangent $\tan\delta = 0.025$ is placed between the Si chip and the bottom PCB to represent the lossy underfill used is such interconnections for mechanical stability. We employ Astra MT77 PCBs, with loss tangent $\tan\delta = 0.002$ and $\epsilon_r = 3$. All metals are assigned the conductivity $\sigma = 2.5\cdot10^7$ S/m. The detailed layers stack-up is shown in Fig. 3.

The embedded die packaging technology considered in our design might be especially appealing for low to medium volume product lines. If high volume production is desired, the EBG structure can be formed in the mold compound on top of the IC or one could use wafer-level packaging approaches if also tighter tolerances are required.

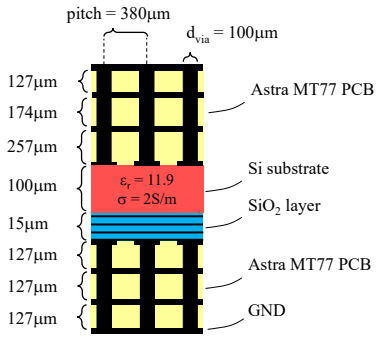

Fig. 3. Detailed layers stack-up and thickness.

III. Simulation Results

To calculate the dispersion diagram of the EBG periodic unit cell, the following setup was simulated in CST Microwave Studio [13] using the eigenmode solver (Fig. 4). PEC boundaries were set on the top and on the bottom surfaces of the cell, and periodic boundary conditions on the side surfaces. The cell is filled with $100\,\mu\text{m}$ of silicon, on top of which is $257\,\mu\text{m}$ of PCB. The planar size of the cell is $380\times380\ \mu\text{m}^2$. The diameter of the via is $100\,\mu\text{m}$. A periodic structure consisting of such cells will block in-silicon waves propagation in the 60–150 GHz range.

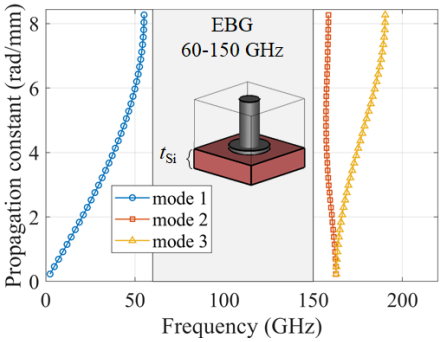

Fig. 4. Dispersion diagram of the EBG periodic unit cell.

To simulate the performance of the proposed antenna we used the full-wave finite-element time-domain (FDTD) 3D EM solver in CST Microwave Studio with 12 million+ mesh elements. Two opposite E-field probes were excited out of phase (differentially) for single-polarization radiation. The simulated radiation pattern is shown in Fig. 5. The broadside gain is $\approx$ 5 dBi between 114–126 GHz. The cross-polar components are below -30 dB in both the E- and H-plane cuts for all angles. Fig.6 shows the time-averaged E-field magnitude $|E|$ inside the antenna. Note the -40 dB attenuation inside the silicon substrate after the second row of pins. For comparison, Fig.7 shows the increased field strength in the substrate if no gap waveguide packaging is used.

The differential-mode S_{11} [14] is shown in Fig. 8. The S_{11} -10dB bandwidth is 112–128 GHz, which corresponds to

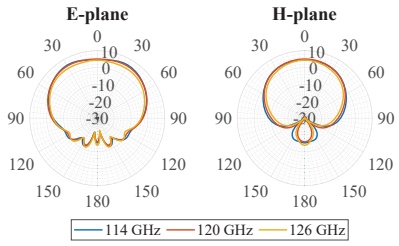

Fig. 5. Simulated Gain (IEEE) in dBi. The E-plane (left) and H-plane (right) cuts at 114, 120 and 126 GHz.

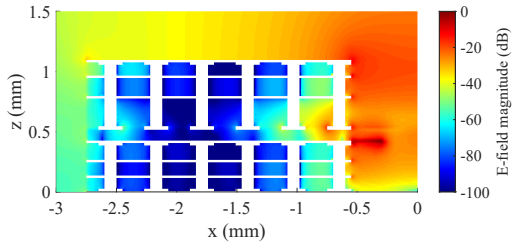

Fig. 6. Magnitude of the E-field $|E|$ calculated in CST. In dB, normalized to the maximum in-plane value.

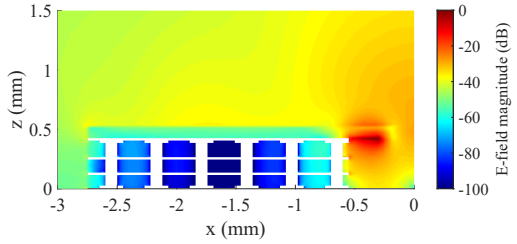

Fig. 7. Same as Fig. 6 but without gap waveguide packaging (top PCB).

the fractional bandwidth of $\approx 13\%$. It is a large improvement compared to the 2D metasurface solutions, and it is mainly due to the fact the gap waveguide-like EBG in our design only attenuates the substrate waves without affecting the matching of the E-field probes.

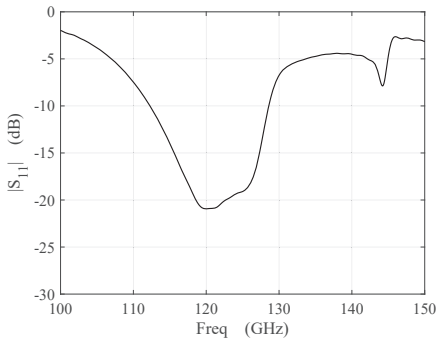

Fig. 8. Differential mode S_{11} parameter.

The simulated radiation efficiency is about 80% in the band of operation (Fig. 9). The EBG structure improves the radiation efficiency by about 10%. Most of the power is lost in silicon, and the metal losses (second largest source) are 4–5 times smaller in the whole 110–130 GHz frequency range. Epoxy underfill is the third largest source of losses, with about 10 times less power dissipated in it than in silicon. The losses in the PCBs are less than 1/20 of the silicon losses.

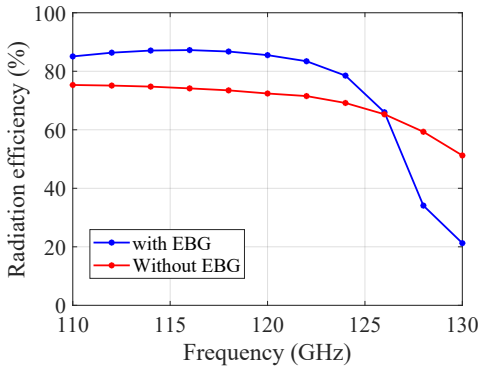

Fig. 9. Simulated radiation efficiency, with and without the EBG structure.

It is necessary to have at least two rows of EBG pins to sufficiently attenuate the substrate waves. It is then also the minimum number of rows between array elements. To see how much the design depends on the chip size we simulated single-element antennas with and without the EBG package for chip sizes from 3 to 5 millimeter with 0.1 mm step. Without the top PCB, the directivity changes from 2.6 dBi to 6 dBi when varying the chip size, while with the top PCB it changes from 4.7 dBi to 7.3 dBi. Higher directivity and less angular and chip-size dependant variations of the radiation pattern adds to the benefits of using the top PCB with the EBG structure with two rows of pins. An example of far-field patterns (directivity) for chip sizes 3.8 mm and 4.9 mm for the two cases is shown in Fig. 10. Without the EBG structure directivity differs by 3.3 dB, while with it the directivity only varies by 0.2 dB between these two chip sizes.

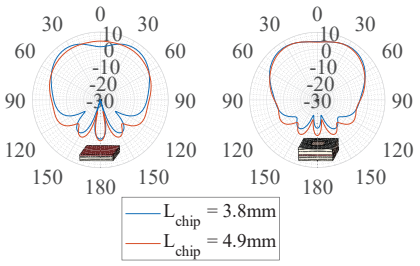

Fig. 10. Directivity for single-element antenna element with 2 rows of pins with (right) and without (left) the top PCB.

To further investigate how well the EBG structure attenuates the substrate waves in this case, we simulated a two-element array, the elements of which are separated by two rows of pins. One simulation was run with the top PCB (Fig. 11) and one excluding the top PCB (Fig. 12). Note that even just two rows of pins act as the EBG structure, resulting in reduced inter-element coupling. Also, as seen from the plots, the top PCB is also necessary to form the dielectric-filled waveguide of appropriate length to have the better S_{11} matching.

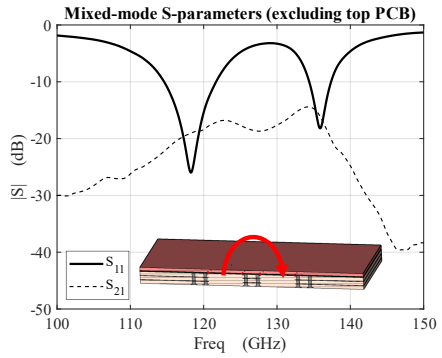

Fig. 11. The two-elements structure with EBG structure.

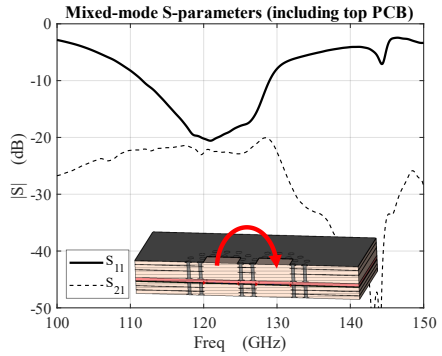

Fig. 12. The two-elements structure without EBG structure.

Table 1. Comparison with other antenna-on-chip designs at similar frequencies.

Type of design	**Bandwidth**	**Radiation efficiency**	**Gain**	**Ref.**
Cavity-backed slot above the ground plane in CMOS BEoL	-10 dB S_{11} 136–140 GHz (4%)	$< 20\%$	Single element -2 dBi	[5]
Two folded dipoles over micro-machined air cavity	3 dB Gain 122–140 GHz (14%)	$\approx 60\%$	Two elements 8.4 dBi	[6]
An array of zig-zag dipoles over AMC, spatial SW modes cancelling	3 dB equivalent isotropic radiated power (EIRP) 127–154 GHz (19%)	Single element 30%	Single element 2.3 dBi	[9]
Without EBG simulations only	-10 dB S_{11} 115–122 GHz (6%)	$\approx 70\%$	Single element $\approx$ 3 dBi	**This work**
With EBG simulations only	-10 dB S_{11} 112–128 GHz (13%)	$\approx 80\%$	Single element $\approx$ 5 dBi	**This work**

IV. Conclusion

We demonstrated that the performance of an Antenna-on-Chip design in flip-chip configuration can be enhanced by using an IC package incorporating an electromagnetic bandgap structure in conjunction with an in-package open-ended waveguide. CST simulation results show high radiation efficiency ($> 70\%$), 5 dBi gain and -10 dB S_{11} matching in the 112–125 GHz frequency range. In the absence of a measured prototype, we performed a relative comparison study on the antenna-on-chip performance with and without the EBG structure. We concluded that the EBG attenuates substrate waves, reduces the array inter-element coupling, and also reduces pattern gain ripples caused by field diffraction effects from the chip ends.

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