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Abstract: A novel hierarchical subcarrier rate and distribution matching has been implemented in an FPGA at 1.032 Tb/s. The implemented subsystem achieves seamless data flow among subcarriers at a resolution < 0.01 bit per channel use.

1. Introduction

Probabilistic shaping (PS) is a powerful tool in digital signal processing (DSP) based fiber-optic communications, especially in terms of capacity-approaching performance and rate adaptation [1,2]. In typical PS systems, distribution matching (DM) is placed outside forward error correction (FEC) coding for low-complexity implementation. The use of digital subcarrier enables waterfilling performance [3] or reduces impact from equalizer-enhanced phase noise [4].

An application specific integrated circuit (ASIC) for DSP with PS has been already reported, e.g., in [4]. However, there are only few reports detailing the DM implementation, which is still a challenging issue. Field programmable gate array (FPGA) implementations were reported in [5–7]. Real-time demonstrations of both DM encoding/decoding implementations were done in [5] only, and later verified at 400 Gb/s throughput in [8]. In contrast, only [6,7] implemented fine rate adaptation at 0.2 bit/channel use (bpcu) for 16- and 64-ary quadrature amplitude modulation (QAM). More precise rate adaptation and subcarrier rate matching are required in practical systems. To realize such rate adaptation, control of clock frequency or usage of dummy bits is essential, but it is rarely reported. Per-subcarrier PS was also implemented [4], but its signal processing architecture and granularity of subcarrier rate are still unclear.

Deployable high throughput and high baud rate fiber-optic communications [2,4,8] are constrained by transceiver signal-to-noise ratio (SNR) up to, e.g., around 20 dB with 256-QAM [9]. On the other hand, in recent years there have been several reports on hyper-scale constellations far larger than 256-QAM. Physical layer encryption was studied with 4,294,967,296-QAM [10], and SNR-adaptive radio-over-fiber transmission was demonstrated up to 1,048,576-QAM [11]. Ultra-high spectral efficiency was performed by PS-16384-QAM at 10 Gbaud [12]. A practically implementable DM for hyper-scale constellations will be needed for such alternative applications.

In this work, we propose and report subcarrier rate and distribution matching (SRDM) implementation for the first time to the best of our knowledge. The proposed hierarchical SRDM (HiSRDM) with a tree-structured architecture is suitable for implementation in high-throughput subcarrier-multiplexed fiber-optic communications. The achieved rate granularity is < 0.01 bpcu with a single FPGA at a system throughput up to 1.032 Tb/s. The implemented HiSRDM circuitry can also generate PS signals having hyper-scale base constellations up to 262,144-QAM.

2. Principle and architecture

To realize adaptive rates with a fixed circuit, we enable or disable bit lanes as needed, and fill the disabled lanes with dummy bits. In each subcarrier, we employ binary-tree-structured hierarchical DM (HiDM) [13] consisting look-up-tables (LUTs) in each layer. Thus the bit lanes are sequentially enabled until data bits enter each LUT. Fig. 1 depicts the (a) signal format and (b) block diagram of HiSRDM. The leftmost sub-figure in Fig. 1(a) shows the numbers of total lanes w and enabled lanes s (yellow), where $0 \le s \le w$. Dummy bits do not carry any meaningful information (can be fixed to '0' or *don't care*). Data bits are placed on the bottom lanes. The bits are demultiplexed into C subcarriers. Second left sub-figure in Fig. 1 (a) shows per-subcarrier bus width w/C and the number of enabled lanes s_j, where $j \in \{1,2,\ldots,C\}$ is the subcarrier index, and $0 \le s_j \le w/C$. The number of enabled lanes s_j can be unequally distributed over subcarriers with nonuniform SNRs. This is the subcarrier rate matching and is realized by a binary-tree demultiplexer shown in the right bottom sub-figure in Fig. 1(b). In each binary-tree demultiplexer, the bottom-side outputs the bottom v_b lanes having indices from 0 to $v_\mathrm{b} - 1$ of the input lanes. Among the v_b lanes, the bottom s_b lanes contain data bits. The top-side outputs are given by consecutive v_t lanes having indices from s_b to $v_\mathrm{b} - s_\mathrm{b} - 1$ of the input lanes. Among the v_t lanes, the bottom s_t lanes contain data bits.

Bits in the j-th subcarrier are demultiplexed into layers 1 to L and extra data bits. The bus widths for layer ℓ is $w_{\mathrm{lyr},\ell}$, and data bits are at the bottom $s_{j,\ell}$ lanes, where $0 \le s_{j,\ell} \le w_{\mathrm{lyr},\ell}$. The bus width for the extra bits is w_ex, and data bits are at the bottom $s_{j,\mathrm{e}}$ lanes, where $0 \le s_{j,\mathrm{e}} \le w_\mathrm{ex}$. The extra data bits will be used after the LUTs in layer 1.

Bits in the ℓ-th layer of the j-th subcarrier are further demultiplexed into each component for an LUT. An i-th LUT in layer ℓ (LUTℓ, $i \in \{1,2,\dots,I_\ell\}$) accepts a variable number of data bits $s_{j,\ell,i}$ with a fixed bus width of $w_{\mathrm{t},\ell}$ for information bits, where $0 \le s_{j,\ell,i} \le w_{\mathrm{t},\ell}$. The number of LUT$\ell$ ($= I_\ell$) equals $2^{L-\ell}$ in the HiDM. Such pre-processing helps to realize flexible-rate shaping. In the HiDM, output bits from an LUT in layer ℓ (LUTℓ) are fed into LUT$\ell-1$. As the LUT contents for HiDM can be software-defined, no additional memories are required in the hardware. After layer 1, bits for modulation symbols are generated with u_1 bits from LUT1 and $w_{\mathrm{t,e}}$ ($= w_{\mathrm{ex}}/2^{L-1}$) extra data bits, then subcarriers are multiplexed before FEC encoding. The extra data bits are non-shaped and can be used for separating a signal point into two or four signal points. The receiver-side processing is an inverse version of the transmitter's one.

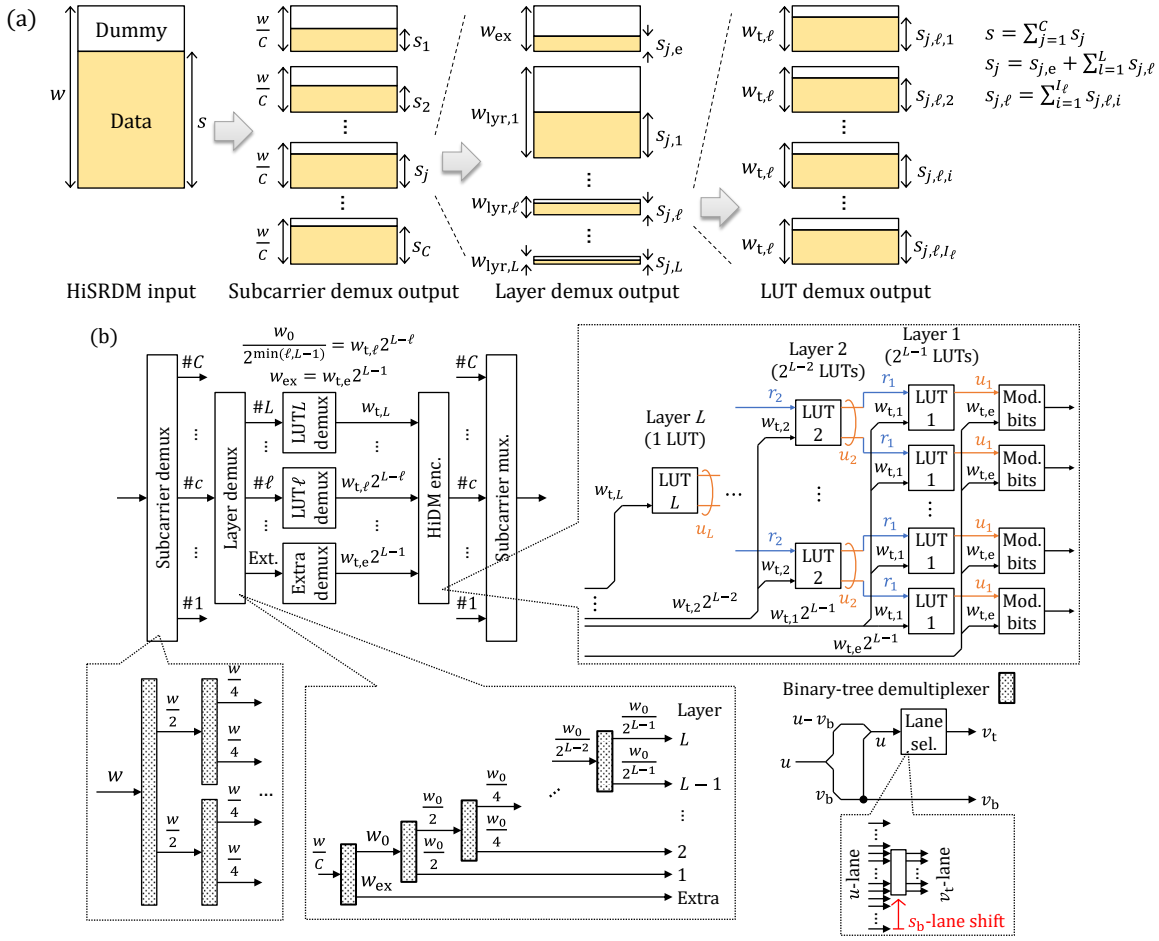

Fig. 1. Principle of HiSRDM; (a) signal formats and (b) block diagram. Paths for sign-bits are not shown because of space limitation.

3. FPGA implementation

We implemented both Tx and Rx subsystems of HiSRDM on a single FPGA of Xilinx® Virtex® Ultrascale+™ VCU118 XCVU9P. The number of subcarrier groups and the number of layers in the HiSRDM are flexible. At maximum, the number of subcarrier groups C is 16 (symmetric) and the number of layers L is 7. Processing of the sign bits was also implemented, which mainly adjusts for the latency.

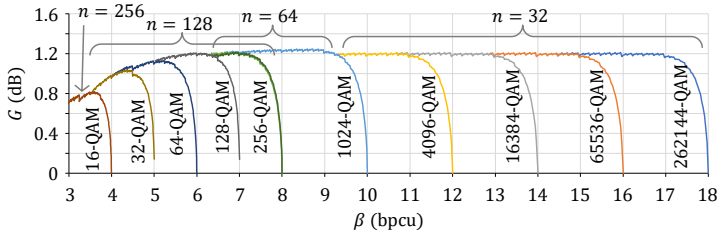

Fig. 2. Constellation gain G as a function of spectral efficiency $\beta = 2 + k/n$ for implemented shaping modes, where n denotes DM output block length (2d-symbols).

Fig. 2 shows the constellation gain $G = d_{\min}^2(2^\beta - 1)/(6E)$ [14] for available operation modes, where $d_{\min}$, β, and E denote minimum Euclidean distance, spectral efficiency, and average two-dimensional (2d) symbol energy, respectively. The largest base constellation is 262,144-QAM, and the rate granularity g_{R} is less than 0.01 bpcu (see

also Tab. 1) regardless of the chosen base constellation (or its combination among subcarriers). For a 90° rotational-symmetric QAM, $\beta = 2 + s_j/n$, where n denotes the number of DM output block length (in 2d-symbols). Shaped information bit rates s_j/n for j-th subcarrier and s/n in total are fully flexible. The gain G with a Maxwell-Boltzmann distribution is at maximum 1.53 dB for a high β [14]. For β = 9–17 bpcu, even with a reduced n of 32, 4096- or higher-order-QAM shows a good and flat G of 1.2 dB (around 0.3 dB gap to the theoretical limit). For β < 9 bpcu, the gap is < 0.3 dB. We have two 256-QAM modes with similar G; one is with 5 shaped bits and one *extra* non-shaped bit (see Sec. 2) per QAM symbol at n = 128 (marked (e) in Tab. 1), another is fully shaped at n = 64.

The FPGA fitting was successful at a clock frequency of 252 MHz. Parameters of the implemented HiSRDM are shown in Tab. 1, where M, B_s, R_spg, and R_tot denote the number of QAM constellation points, symbol rate (baud rate), shaped information bit rate, and total information bit rate including sign bits, respectively. The maximum R_spg and R_tot are 774.1 Gb/s and 1.032 Tb/s, respectively. Tab. 2 shows utilized resource elements and Fig. 3 illustrates the utilized area (cyan) in the FPGA consisting of three dies. We utilized mainly LUTs as logic and registers in configurable logic blocks (CLBs), and block random access memory (RAM). No DSP slices and ultra RAM were employed. The utilization of block RAM shows a relatively high value of 46%. There are several reasons why this is significantly larger than [5], where it was only 5%. Firstly, we employed dual-port read LUTs in [5], which reduced memory by 50%. On the other hand, in this work we did not do so to simplify the implementation. Thus, there is room to reduce the utilization in future work. Secondly, the supported information bit rate and base constellation are significantly larger than [5]. Thirdly, several LUTs in this work are larger than in [5]. There are 2160 instances of 36 kb RAMs in the FPGA. When an LUT size is less than 18 kb, half of an instance is utilized. Note that all block RAMs were utilized in DM encoding and decoding, and that the subcarrier rate matching employed CLB logics only.

Tab. 1. Parameters for implemented HiSRDM.

M	B_s (Gbaud)	max R_spg (Gb/s)	max R_tot (Gb/s)	g_R (bpcu)
16	129.024	516.096	1032.192	9.766E-4
32	64.512	387.072	645.120	1.953E-3
64	64.512	516.096	774.144	1.953E-3
128	64.512	645.120	903.168	1.953E-3
(e)256	64.512	774.144	1032.192	1.953E-3
256	32.256	387.072	516.096	3.906E-3
1024	32.256	516.096	645.120	3.906E-3
4096	16.128	322.560	387.072	7.813E-3
16384	16.128	387.072	451.584	7.813E-3
65536	16.128	451.584	516.096	7.813E-3
262144	16.128	516.096	580.608	7.813E-3

Tab. 2. Utilized resource elements.

Classification	Element	Used/Available	Utilization
CLB Logic	LUT as logic	364k/1182k	30.77%
	Register	781k/2364k	33.04%
RAM	Block RAM	1010/2160	46.76%

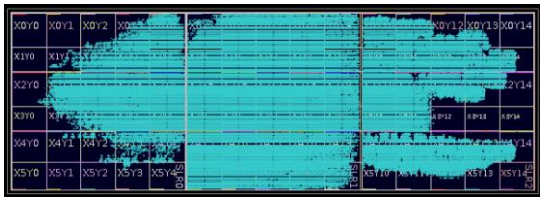

Fig. 3. Utilized area in FPGA (cyan).

4. Conclusions

Hierarchical subcarrier rate and distribution matching was proposed and implemented in a single FPGA. Its hardware architecture helped to realize key features; the highest throughput of 1.032 Tb/s, almost seamless rate granularity, and the largest base constellation of 262,144-QAM.

Acknowledgments

This work is in part supported by "Massively Parallel and Slice Optical Network," the commissioned research of National Institute of Information and Communication Technology (NICT), and "The research and development of innovative optical network technology as a new social infrastructure" (JPMI00316) of the Ministry of Internal Affairs and Communications, Japan. We also thank Prof. Kyo Inoue for assistance in the research.

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