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Influence of Spacer Thickness on the Noise Performance in InP HEMTs for Cryogenic LNAs

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***Abstract*— InP high electron mobility transistors (InP HEMTs) with different spacer thickness 1 to 7 nm in the InAlAs-InGaAs heterostructure have been fabricated and characterized at 5 K with respect to electrical dc and rf properties. The InP HEMT noise performance was extracted from gain and noise measurements of a hybrid low-noise amplifier (LNA) at 5 K equipped with discrete transistors. When biased for optimal noise operation, the LNA using 5 nm spacer thickness InP HEMTs achieved the lowest average noise temperature of 1.4 K at 4-8 GHz. The InP HEMT channel noise was estimated from the drain noise temperature which confirmed the minimum in noise temperature for the 5 nm spacer thickness InP HEMT. It is suggested that the spacer thickness acts to control the degree of real-space transfer of electrons from the channel to the barrier responsible for the observed noise variation in the cryogenic InP HEMTs.**

***Index Terms*— Cryogenic, InP HEMT, low-noise amplifier, noise, spacer thickness.**

I. Introduction

THE InP high electron mobility transistor (InP HEMT) is the workhorse device for the design of the cryogenic low noise amplifier (LNA) which offers the lowest noise temperature among all semiconductor-based circuits [1]. Applications are found in microwave and mm-wave receivers for radio astronomy and space communication [2]. At present, there is a rapid development of electronic devices used in quantum computing systems [3]. The cryogenic InP HEMT LNA has here become instrumental for the readout of microwave qubits at the 4 K stage [4], [5]. To further improve the qubit readout, the noise properties at low temperature for the InP HEMT are crucial.

It is well known that engineering of the InP HEMT epitaxial structure plays a decisive role for the device electrical performance [6] and this becomes even more critical under cryogenic operation [5]. Previous work demonstrated that the carrier concentration and the scattering of carriers in the HEMT channel were highly dependent on the location of the planar doping layer in relation to the heterojunction [7], [8]. Hence the choice of spacer thickness is expected to modify the properties of the two-dimensional electron gas (2DEG) which in turn is essential for the HEMT noise performance. To the authors knowledge, this has not been reported for the HEMT operating under the temperature conditions used in cryogenic LNAs.

In this study, we report on the optimum spacer thickness in the InAlAs-InGaAs heterojunction for lowest channel noise in the cryogenic InP HEMT LNA. The results suggest that the noise can be related to the amount of real-space transfer of electrons between channel and barrier in the InP HEMT.

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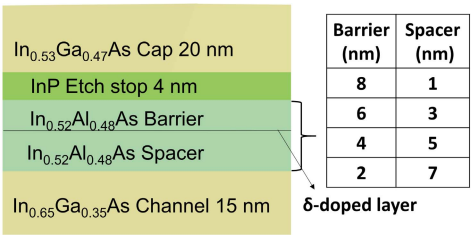

Barrier (nm)	Spacer (nm)
8	1
6	3
4	5
2	7

Fig. 1. Schematic of epitaxial stack used in HEMT fabrication. The table shows the investigated variation in spacer (and barrier) thickness.

II. Device Technology

The epitaxial layers were grown by molecular beam epitaxy on 3-inch diameter InP substrates. Starting from the bottom, the epitaxial stack consisted of a 500 nm thick $In_{0.52}Al_{0.48}As$ buffer and a 15 nm pseudomorphic $In_{0.65}Ga_{0.35}As$ channel layer. Fig. 1 shows a schematic of the InP HEMT epitaxial layers above the buffer. By growing an $In_{0.52}Al_{0.48}As$ layer with a Si δ-doped plane on top of the channel, a heterojunction with a 2DEG was formed. The spacer thickness was the distance between the top of the channel and the δ-doped layer. Four different samples with spacer thickness d_{sp} of 1, 3, 5 and 7 nm were grown. The δ doping level was calibrated to keep the sheet carrier concentration at a constant value of 2.5×10^{12} cm^{-2} for all four structures. The $In_{0.52}Al_{0.48}As$ barrier thickness above the δ-doped layer was adjusted accordingly so

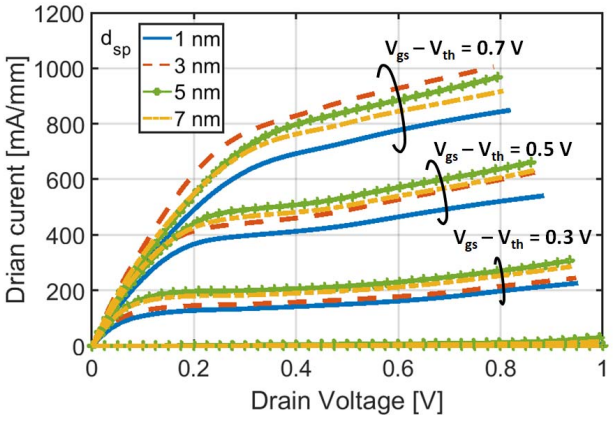

Fig. 2. Drain current versus drain voltage of InP HEMT with spacer thickness of 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K.

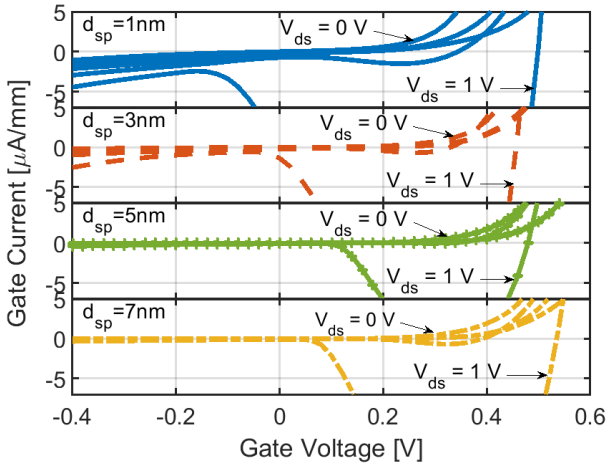

Fig. 3. Gate current versus gate voltage of InP HEMT with spacer thickness of 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K. V_{ds} = 0 – 1 V in steps of 0.25 V.

that the total thickness of the barrier and spacer layer was 9 nm for all four structures, see table insert in Fig. 1(a). To improve etching selectivity for the subsequent cap layer, a 4 nm thick InP etch stop layer was grown on the barrier [9]. The InP etch stop layer also served to passivate material-related defects in the gate recess region [10]. The epitaxial stack was finalized by growing a 20 nm thick n^+ $In_{0.53}Ga_{0.47}As$ cap layer.

The measured Hall electron mobility at 5 K for epitaxial structures without cap layer was 17,000, 39,000, 53,000 and 54,000 cm^2/Vs for structures with d_{sp} = 1, 3, 5 and 7 nm, respectively. The sheet carrier concentration at 5 K showed only a ±10% dependence on spacer thickness.

InP HEMTs using epitaxial structures with different d_{sp} were fabricated simultaneously employing the technology described in [2]. The transistor gate length and gate width were 100 nm and 4×50 μm, respectively.

III. Results

InP HEMTs with different spacer thicknesses were electrically characterized on-wafer at 5 K. The drain current versus drain voltage curves in Fig. 2 showed expected output behavior with no obvious kink effect previously reported for cryogenic InP HEMTs [2]. This is attributed to the efficient suppression of surface traps in the gate-recess region by the InP etch stop layer [9]. In saturation, all transistors displayed similar current driving ability except for InP HEMTs with d_{sp} = 1 nm where the drain current was lower. This was expected due to the relatively low Hall electron mobility and high sheet resistance at 5 K for d_{sp} = 1 nm.

The gate current I_g of the InP HEMTs with different spacer thickness is plotted in Fig. 3. All devices exhibited low gate current leakage <1 μA/mm with no impact ionization in the gate bias range between 0 and +0.2 V and drain-source bias lower than 0.5 V. Under such bias conditions, the InP HEMT is close to its optimum low-noise region. The amount of gate leakage shown in Fig. 3 is not expected to degrade the noise temperature in the LNA [11]. From the drain current versus gate voltage characteristics, the subthreshold swing (SS) at V_{ds} = 0.1 V was calculated to be 24, 20, 12 and 13 mV/dec for d_{sp} = 1, 3, 5 and 7 nm, respectively. The SS levels for d_{sp} = 5 nm is among the lowest reported for a field-effect transistor yet beyond the theoretical Boltzmann limit [12].

It was observed from the drain current versus gate voltage that the threshold voltage V_{th} varied with d_{sp}. For d_{sp} = 1, 3, 5 and 7 nm, the V_{th} was −0.2, −0.1, 0.1 V and 0 V, respectively. This was expected because V_{th} depends on the location of the δ-doped layer and the doping concentration [13]. With increased d_{sp} and decreased δ doping level, the V_{th} will show a positive shift and vice versa. Hence, there will be a maximum in V_{th}, here at 5 nm, when the spacer thickness was increased from 1 to 7 nm and the δ doping concentration was increased to keep the sheet carrier concentration in the channel constant.

Since the noise level of the InP HEMT at cryogenic temperature is too low to be accurately estimated from probed measurements [14], chips were diced into discrete InP HEMTs which were mounted in three-stage 4–8 GHz hybrid LNAs. By measuring the gain and noise of the amplifier at 5 K, the cryogenic transistor noise was possible to extract employing a methodology described in [14], [15]. All measurements were performed at the bias point for lowest amplifier noise using the same attenuator. As a result, the noise difference between the LNAs could be attributed to the noise difference for the InP HEMTs with different spacer thickness.

As seen in Fig. 4(a), the amplifier experimental data at 5 K revealed differences between the LNAs based on InP HEMTs with varying spacer thickness. All LNAs exhibited similar gain of around 40 dB which in turn meant high accuracy for the noise measurements. The noise temperature of the LNAs decreased with increased d_{sp} from 1 to 5 nm for InP HEMTs. Considering the relative differences in noise in Fig. 4(a), the LNA with 5 nm spacer InP HEMTs exhibited the lowest average noise temperature $T_{e,avg}$ of 1.4 K at 4-8 GHz. The noise level is on a par with the best result previously reported for this frequency band [2]. The $T_{e,avg}$ of LNAs with d_{sp} = 1, 3 and 7 nm was 1.9, 1.7 and 1.6 K, respectively. The optimum noise bias for the LNA was V_{DS} = 0.51 V, I_D = 12.0 mA for d_{sp} = 5 nm and V_{DS} = 0.61 V, I_D = 9.0 mA for d_{sp} = 7 nm. These biases were smaller

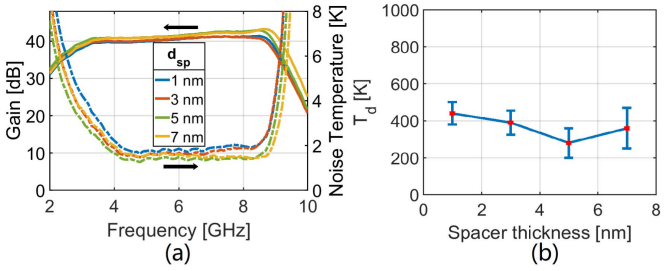

Fig. 4. (a) The measured gain (solid) and noise temperature (dashed) of three-stage 4-8 GHz hybrid LNAs integrated with the InP HEMT with $d_{sp} = 1$ (blue), 3 (red), 5 (green) and 7 nm (yellow) at the optimum noise bias of each LNA at 5 K. (b) The T_d as function of spacer thickness extracted at optimum noise bias for the InP HEMT at 5 K.

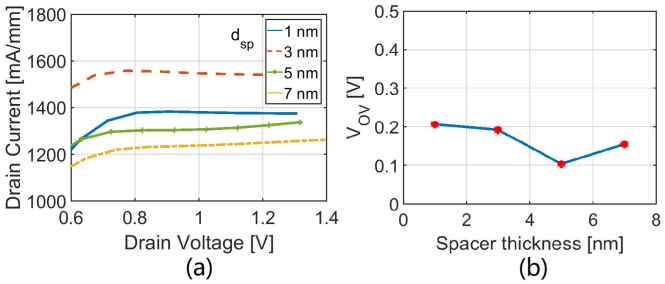

Fig. 5. (a) The drain current at 5 K for InP HEMT with $d_{sp} = 1$ (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot), V_{gs} = 1.14 V. (b) The overdrive voltage $V_{OV} = V_{gs} - V_{th}$ at optimum noise gate bias for the InP HEMT versus d_{sp} at 5 K.

than $V_{DS} = 0.75$ V, $I_D = 18.0$ mA for $d_{sp} = 1$ nm and $V_{DS} = 0.73$ V, $I_D = 16.8$ mA for $d_{sp} = 3$ nm. The corresponding optimum noise bias for the InP HEMTs was $V_{ds} = 0.475$ V, $I_d = 30$ mA/mm for $d_{sp} = 1$ nm, $V_{ds} = 0.475$ V, $I_d = 28$ mA/mm for $d_{sp} = 3$ nm, $V_{ds} = 0.325$ V, $I_d = 20$ mA/mm for $d_{sp} = 5$ nm and $V_{ds} = 0.475$ V, $I_d = 15$ mA/mm for $d_{sp} = 7$ nm.

The noise generated in the HEMT was quantified by the drain noise temperature T_d [16]. The T_d was extracted by comparing the measured gain and noise of the LNA with simulations [2] based on an equivalent small-signal HEMT model using the measured S-parameters [17]. The intrinsic small-signal parameters for the investigated InP HEMTs displayed similar values which is reasonable since they had identical geometries. The T_d of the InP HEMT extracted at its optimal noise bias are presented in Fig. 4(b). The error bars in T_d were estimated from the noise simulations through the frequency band 4-8 GHz. It is observed that T_d shows a minimum for InP HEMT with 5 nm spacer thickness. Even though the error bars in Fig. 4(b) are large in absolute numbers, the relative change in T_d suggests that noise in the transistor channel depends upon the spacer thickness of the cryogenic InP HEMT.

IV. Discussion

The high-frequency noise in the InP HEMT is connected to the degree of carrier fluctuations in the 2DEG channel. This will lead to a distribution in electrons velocities related to the noise spectrum of the InP HEMT [18]. The cryogenic InP HEMT is here well suited to probe the amount of noise since the intrinsic channel constitutes the dominant noise source in the full device [2]. Dopants serve as efficient scattering for electrons at spacer thicknesses below 5 nm as seen in the reduction of mobility. While the scattering mechanism of the 2DEG can be of several physical origins, impurities scattering is supposed to be significant at cryogenic temperature [19] which is consistent with the measured Hall mobility. Normally, one strives for a high-mobility channel for reducing noise in the HEMT as guided by well-known semi-empirical noise expressions such as the Fukui equation [20]. However, the channel electrons in the investigated InP HEMTs are expected to move at saturated velocity [21]. The Hall mobility reflects the average transport of the 2DEG at low electrical field and thus gives limited information on the expected noise level in the intrinsic InP HEMT at low temperature.

A recent theoretical study predicts that real-space transfer (RST) in the InP HEMTs is an important source for microwave drain noise [23]. RST is the emission of 2DEG carriers from the channel into the barrier prior to valley transfer [24]. RST noise has earlier been proposed for GaAs HEMTs [26] and InAlAs/InGaAs/InAlAs/InP quantum wells [27]. A well-known manifestation of RST in HEMTs is negative differential resistance (NDR) in the $I - V$ output curves at elevated gate voltage [25]. This is indeed observed (Fig. 5(a)) for our InP HEMTs at 5 K for d_{sp} = 1 and 3 nm. The absence of NDR for d_{sp} = 5 and 7 nm is due to the higher V_{th} of the InP HEMTs. Note that the NDR in Fig. 5(a) is far beyond the low-noise bias of the InP HEMT. RST may however also occur at low-bias operation and be detectable as increased noise in the HEMT [23], [26]. In Reference [23], it is proposed that the fraction of the electron transfer from the channel to barrier in a HEMT is determined by the conduction band offset ΔE_c and gate bias V_{gs}. However, a HEMT at a gate bias below V_{th} cannot have any RST. When comparing different devices, it is the overdrive voltage $V_{OV} = V_{gs} - V_{th}$ which controls the fraction of transferred electrons. If RST is responsible for noise in the HEMTs, with ΔE_c the same for all the structures, the noise must be minimized for the lowest V_{OV} at the optimum noise bias. This is confirmed in Fig. 5(b) where the V_{OV} shows a clear minimum for $d_{sp} = 5$ nm which is the InP HEMT with lowest T_d (Fig. 4). We therefore hypothesize that the channel noise probed by T_d is due to RST in the intrinsic InP HEMT at low temperature.

V. Conclusion

The channel noise estimated by T_d of the cryogenic InP HEMTs has been studied using a spacer thickness variation from 1 to 7 nm in the InAlAs-InGaAs heterostructure. It was found that the T_d versus d_{sp} exhibited a clear minimum at 5 nm. The electron mobility was a poor noise indicator. The correlation between T_d and V_{OV} at the optimum noise bias with d_{sp} suggests that RST noise can be important in cryogenic InP HEMTs. The result in this study shows the significance for epitaxial optimization of the HEMT for use in LNAs for quantum computing and will help to reduce the minimum noise temperature in the 4 K readout even further.

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