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Design of a Compact GaN Power Amplifier with High Efficiency and Beyond Decade Bandwidth

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***Abstract*—This letter presents a power amplifier (PA) design and network synthesis approach to achieve wideband and efficient performance with a very compact circuit size. A design method is presented in detail to convert a canonical filter-based high-order matching network to the proposed matching configuration with transistor parasitic and packaged elements absorption, and a compact passive network footprint. As a proof of concept, a prototype GaN HEMT PA is implemented. Starting from a fourth-order output network filter, the inductances and capacitance of the filter elements are re-organized to model, and thus absorb the output parasitics of the transistor, leading to a compact footprint with only four transmission lines. The measured results show that the prototype PA achieves an output power of 41.9-44.3 dBm and a 55-74% drain efficiency, over a record-high decade bandwidth (0.35-3.55 GHz).**

***Index Terms*—Energy efficiency, decade bandwidth, GaN, HEMT, power amplifier (PA), wideband matching networks.**

I. Introduction

THE increasing demand for higher data throughput has resulted in unprecedented challenges for the wireless communication infrastructure. To cope with the rising data capacity, the overall trend for communication systems is evolving towards more energy-efficient and frequency-agile. Those constraints are imposed on the power amplifier (PA) since it is a critical building block that governs many performance aspects of the wireless link. Consequently, it has been an important research topic to investigate the PA design with high efficiency over a wide range of frequencies.

The high-efficiency performance can be achieved by using harmonically tuned PAs [1], [2]. This technique reduces power dissipation by minimizing the current and voltage waveform overlap. However, the harmonic engineering approaches rely on achieving precise impedance values at harmonic frequencies, which makes them inherently difficult for beyond-octave operation. To obtain high PA efficiency over a wider bandwidth, the design in [3] uses artificial neural networks and an algorithm based on the simplified real frequency technique to obtain matching networks with desired bandwidth. Alternatively, design automation with particle swarm optimization is utilized for improved efficiency and bandwidth in the case of [4]. The high PA efficiency and wide bandwidth can be realized using system optimization approaches based on load-pull power and efficiency contour estimation [5] or simulation/characterization [6], [7]. Moreover, filter network synthesis techniques, including transformer-based [8] and load-tracking [9] networks, are used for wideband PA designs.

In this paper, a filter network synthesis technique is presented. By performing circuit transformation on the low-pass filter's lumped components, the method allows absorbing the output parasitic model of a 25 W packaged GaN HEMT transistor, which guarantees a wideband practice. Furthermore, an ultra-compact output network can be realized by reorganizing the lumped components to construct distributed elements. The measurement results of the fabricated prototype circuit show an ultra-wideband high-efficiency PA, with a record-high 163% fractional bandwidth and a drain efficiency of 54%-74%, for an output power of 41.9-44.3 dBm. When compared to the state-of-the-art high-efficiency PAs (shown in Table I), the designed PA exhibits excellent performance and thereby demonstrates the usefulness of the proposed approach.

TABLE I
Summary of state-of-the-art wideband PAs.

Ref.	BW (GHz)	BW (%)	P_{out} (dBm)	Gain (dB)	DE (%)
[1] 2021	3.05-3.85	23	39.9-41.4	11.0-12.4	70-78
[2] 2021	2.20-3.40	42	39.5-40.4	8.2-11.2	60-72
[3] 2021	2.00-3.00	40	43.5-45.0	15.2-16.0	53-74
[4] 2021	0.80-3.00	116	39.2-42.1	8.1-14.3	55-68
[5] 2020	0.45-3.40	153	41.5-44.3	8.0-10.5	54-70*
[6] 2018	0.85-5.40	146	43.5-45.0	8.0-9.5	45-55*
[7] 2021	0.80-3.20	120	46.8-48.1	9.5-13.1	57-71
This work	**0.35-3.55**	**163**	**41.9-44.3**	**8.1-9.6**	**55-74**

[a] DE stands for drain efficiency, [b] * PAE is reported

II. Design Methodology

The proposed design approach begins with a selection of the filter-based matching network. In this work, the low-pass matching filter [10] is selected because it can achieve a lower ripple within the desired bandwidth when compared to a conventional low-pass or band-pass filter. It should be stressed that the low-pass matching filter technique has been used in various

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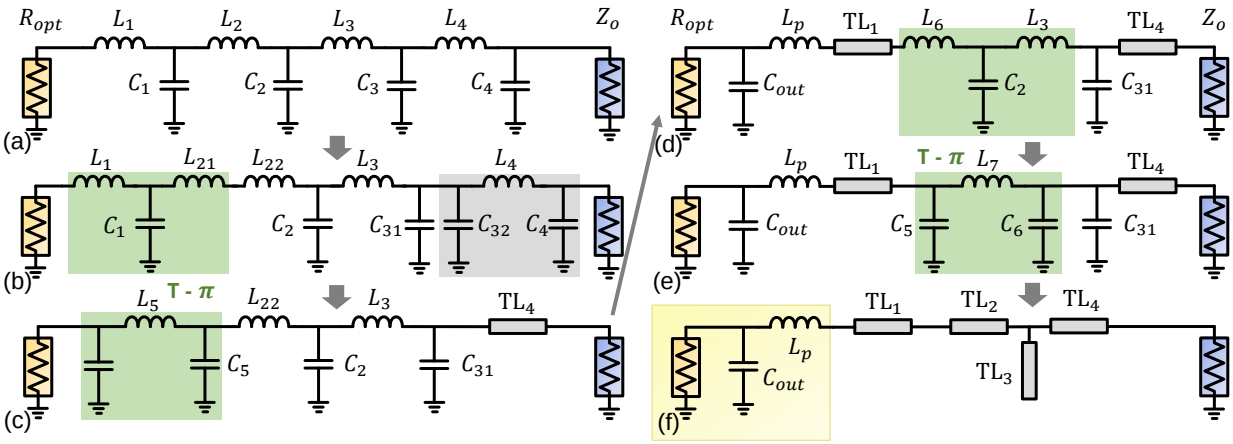

Fig. 1. Proposed modified low-pass matching network including transistor output parasitic and packaged elements. (a) A low-pass matching network with impedance transform ratio of Z_0/R_{opt}. (b) Reorganizing inductor for the T−Π circuit transformation. (c) T−Π circuit transformation. Modeling transmission lines with lumped Π-networks. (d) Reorganizing inductors to model the transistor output and modeling transmission lines with T-networks. (e) T − Π circuit transformation and reorganizing capacitors to model transmission lines. (f) Final matching network schematic including transistor parasitic capacitors (C_{out}) and package inductors (L_p).

designs, such as the class-E PA [11], the Doherty PA [12], and the load modulated balanced amplifier (LMBA) [13] etc. However, most of the previous work [11]–[13] relies on extensive network optimization since it functions only for a real-to-real impedance transformation. We demonstrate a design approach to synthesize the low-pass matching networks that include the model of the transistor output parasitics. Moreover, a more simplified and thus compact output network is also achieved by reorganizing, merging the lumped elements into distributed elements, and absorbing the parasitics.

It is also assumed that the packaged transistor output can be approximated by an ideal current source with a parallel resistor (R_{opt}) and capacitor (C_{out}) network, as well as a series inductor (L_p). Fig. 1 presents a step-by-step graphical illustration of the design procedure. Details of each step are shown below.

Step 1: A low-pass matching network with real-to-real impedance transformation is extracted from [10], based on the desired center frequency, fractional bandwidth, maximum acceptable in-band ripple, and an impedance transformation ratio of Z_0/R_{opt}.

Step 2: The $T-\Pi$ circuit transformation [14] is performed to generate a parallel capacitor C_{out} and a series inductor L_5, as shown in Fig. 1(c). It should be noted that the actual inductance (L_{21}) used for the $T-\Pi$ transformation should be carefully adjusted to obtain the desired C_{out}. Besides, it is possible to form a transmission line TL_4 from the C_{32}-L_4-C_4 based lumped Π-network in Fig. 1(b), considering that $C_{32} = C_4$. It is important to note that $L_2 = L_{21} + L_{22}$ and $C_3 = L_{31} + L_{32}$.

Step 3: Similarly, the inductor L_5 in Fig. 1(c) can be split into two inductors in series, L_{51} and L_{52}. Thus the package inductor $L_p = L_{51}$. In addition, transmission line TL_1 can be constructed using a L_{52}-C_5-L_{52} based lumped T-network. Therefore, $L_6 = L_{22} - L_{52}$ in Fig. 1(d).

Step 4: Transmission line TL_2 is modeled following a similar principle after $T-\Pi$ transformation and reorganizing the capacitors, with $C_5 = C_{61}$. The left shunt capacitance should be identical to $C_{31} + C_{61}$, which can be approximated by an open stub TL_3.

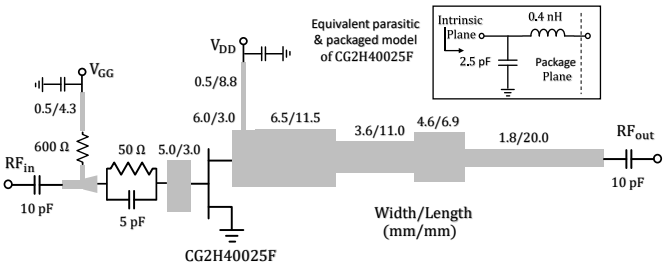

Fig. 2. Circuit schematic of the proposed wideband PA and the equivalent output parasitic and packaged model of the CG2H40025F transistor.

Based on the proposed synthesis, the fourth-order low-pass matching filter is modified to analytically include the parasitic capacitance and packaged inductance of the active device. Furthermore, the resulting output network consists of only four transmission lines, which is significantly more compact compared to a regular high-order filter. In the following section, a wideband and compact PA prototype circuit designed based on the method will be demonstrated.

III. Prototype PA Circuit

The complete schematic of the PA prototype circuit and the equivalent output parasitic and packaged model of the transistor, are illustrated in Fig. 2. The designed PA is implemented on a 20-mil Rogers 4350B substrate. A commercially available 25-W packaged GaN HEMT transistor from Wolfspeed (CG2H40025F) is selected to act as the active device. The output matching network is realized based on the proposed method. First, the equivalent output parasitic and packaged model of the CG2H40025F transistor, as shown in Fig. 2, can be extracted from de-embedded small-signal and load-pull simulations [15]. The optimum load resistance is

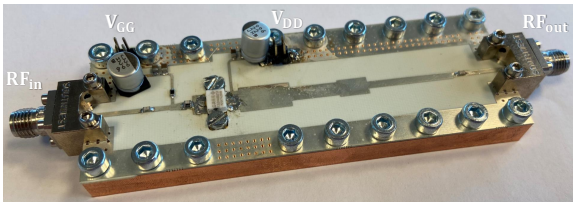

Fig. 3. Photograph of the fabricated wideband PA prototype circuit. The dimensions are 95 $\times$ 33 mm^2.

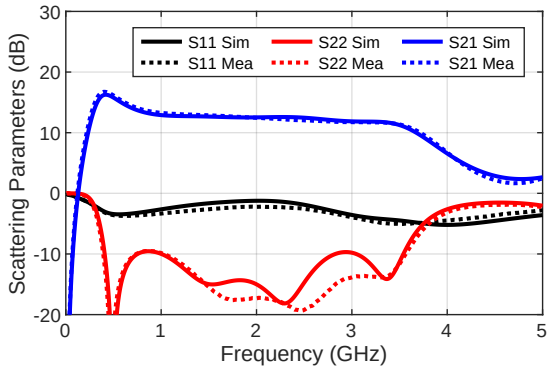

Fig. 4. Simulated and measured small-signal performance of the PA prototype.

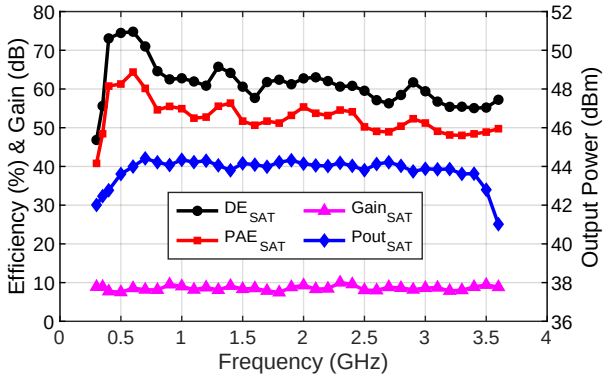

Fig. 5. Measured large-signal characterization results versus frequency of the PA prototype circuit. The index SAT refers to saturated power condition, while DE stands for the measured drain efficiency.

thereafter calculated from the transistor's IV curves, with an estimated value of 16 Ω. Then, a fourth-order real-to-real low-pass matching network is employed for wideband impedance matching. Finally, the output network is modified to include the transistor's output parasitic and packaged elements, with a compact and distributed form. The input network uses low-impedance open stubs connected to the gate pin to achieve wideband matching. Moreover, a series RC network at the input, together with a resistor at the gate bias path, is employed to maintain stability across the entire operating frequency bands. Fig. 3 shows a photograph of the implemented PA prototype circuit. For characterization, the PA is biased in class-AB mode to ensure good linearity and efficiency trade-off. A drain bias voltage of V_{DD} = 28 V, and a gate bias of V_{GG} = 2.75 V, are fixed for the prototype during the measurements.

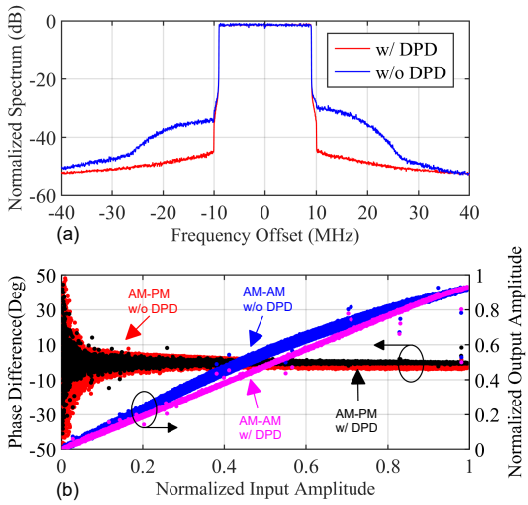

Fig. 6. Measurement results of the prototype PA circuit when applying digitally modulated signals. (a) Normalized power spectral density, (b) AM-AM and AM-PM characteristics, with and without applying DPD, for a 20-MHz 8.5-dB PAPR LTE signal at 2.1 GHz.

IV. Measurement Results

Fig. 4 presents the small-signal simulated and characterized results of the PA prototype circuit. It can be observed that the measured small-signal scattering parameters are in excellent agreement with the simulated results over an ultra-wide bandwidth. The continuous-wave (CW) characterization results in terms of drain efficiency, PAE, gain, and output power versus frequency are shown in Fig. 5. Across the $0.35-3.55$ GHz frequency band (over a fractional bandwidth of 163 %), the CW measurements demonstrate a peak drain efficiency between 55% and 74%, a saturated output power higher than 41.9 dBm, and an output 1-dB compression point greater than 40.1 dBm.

The performance of the prototype circuit is also characterized using a 20-MHz long-term evolution (LTE) signal with an 8.5 dB peak-to-average-power ratio (PAPR). Fig. 6 presents the measured output spectrum and the corresponding AM-AM and AM-PM characteristics, both with and without digital predistortion linearization (DPD) using the generalized memory polynomial model [16]. The measured average drain efficiency is 33% with an average output power of 35.2 dBm. In addition, the adjacent channel leakage ratio (ACLR) is improved from -32.7 to -47.4 dBc after applying DPD.

V. Conclusion

A decade-bandwidth, highly efficient PA is designed with a compact output network through a modified filter-based method. The obtained drain efficiency is higher than 55 % over a 163% fractional bandwidth (0.35-3.55 GHz), with an output power higher than 41.9 dBm. Compared to the state-of-the-art PAs, the performance of the designed PA stands out in terms of high efficiency over ultra-wideband frequencies. The presented PA also shows very good linearity performance with modulated signals, while meeting the requirements of modern wireless communication standards.

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