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An optimized parameter design method of SiC/Si hybrid switch considering turn-off current spike

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Abstract

In order to reduce the switching loss of SiC MOSFET/Si IGBT (SiC/Si) hybrid switch, the switching mode that turn off the Si IGBT prior to the SiC MOSFET is generally adopted to achieved the zero-voltage switching operation of IGBT. The minority carrier in N-base region of the IGBT are recombined in the form of exponential attenuation due to the conductivity modulation effect. When the SiC MOSFET is turned off, if the carrier recombination process of the IGBT is not finished, it needs to bear a large collector–emitter voltage change rate, resulting in apparent current spike. This current spike will increase the current stress of the device and produce additional turn-off loss. The equivalent model of double pulse test circuit of SiC/Si hybrid switch considering parasitic parameters is established, and the turn-off transient process is given analytically. The influence of turn-off delay time, circuit parameters and working conditions on current spike are analysed quantitatively. Combined with the consideration of device stress and comprehensive turn-off loss, an optimized circuit design method of SiC/Si hybrid switch considering turn-off current peak is proposed, which provides theoretical and design guidance for high reliability and high efficiency SiC/Si-based converters.

Peer-review under responsibility of the scientific committee of the 5th International Conference on Electrical Engineering and Green Energy, CEEGE, 2022.

Keywords: SiC MOSFET; Si IGBT; Hybrid switch; Switching loss; Parameter optimization

1. Introduction

Silicon (Si) Insulated-Gate-Bipolar Transistor (IGBT) is commonly used as power device in high power converter, but its high turning-off loss limits the development of the converter to high frequency and miniaturization. Silicon carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has the advantages of lower on-resistance, faster switching speed and higher temperature resistance, and has broad application prospects in the fields of electric vehicles, new energy power generation [1–4].

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However, due to the constraints of wafer fabrication and manufacturing process, the current level of existing SiC devices are still lower than that of Si IGBT [5,6]. Therefore, in order to take advantage of the conduction characteristics of Si IGBT under high current and the switching characteristics of SiC MOSFET, researchers have proposed a hybrid parallel structure based on SiC/Si devices [7]. At present, for SiC/Si hybrid switch, researchers have carried out research on their electrical characteristics, switching mode optimization, current level ratio and so on. Ref. [8] analysed the static and dynamic characteristics of SiC/Si switch, and proved that compared with the full SiC scheme, hybrid switch can increase short-circuit withstand capacity, reduce power loss and total cost. Ref. [9] combined variable switching mode and variable PWM frequency strategy, by reducing the switching frequency near the peak current region, it can not only ensure that SiC device does not bear overcurrent stress, but also reduce the switching loss introduced by IGBT, but did not consider the influence of different turn on/off delay time on the switching loss of SiC/Si hybrid switch. Junction temperature of SiC/Si hybrid switch realized balance by optimizing the switching control strategy [10] and multi-objective optimization control strategy based on the loss model [11]. However, the loss introduced by the turn-off current spike of Si IGBT is calculated by experimental fitting in [10,11], which is not accurate enough. In [12], the influence of parasitic inductance imbalance on the internal static current sharing time of the device was described, but no detailed loss modelling was performed for the switching process. In [13], researchers proposed the current ratio optimization design method of SiC/Si hybrid switch and pointed out that with the increase of turn-off delay time, the loss introduced by IGBT current peak will decrease, but the turn-off current peak value under different turn-off delay time was not given.

According to the turn-off current spike and circuit parameter design of Si IGBT, the presence of turn-off current spikes was pointed out in [14] by analysing the switching modes of SiC/Si hybrid switch, and [15] evaluated the turn-off current spikes at different turn-off delay time, but no studies were performed for other circuit parameters. In [16], the use of simple devices such as resistors and capacitors to achieve delay time regulation was proposed, but the effect of other parameters on the switching characteristics of SiC/Si hybrid switch was not considered. The active driving circuit was designed to optimize the switching characteristics by adjusting circuit parameters such as the switching delay time and the driving voltage of the hybrid switch, but the effect of the parameters on the IGBT turn-off current spikes was not addressed in [17]. Since the turn-off current spike of Si IGBT increases both the device current stress and the power loss of the hybrid switch, and also affect the setting of the dead time in the phase-leg configuration, it is important to evaluate the turn-off current spike to improve efficiency and ensure reliable converter operation.

Based on the above problems, this paper firstly considers the influence of parasitic parameters and analyses the turn-off transient process of SiC/Si hybrid switch. Secondly, the influencing factors of IGBT turn-off current spike are studied and analysed. Then, a parameter optimization design method is proposed by combining reliability and comprehensive loss optimization as the guideline. Finally, experiments are conducted by a double-pulse test platform to verify the correctness of the theoretical analysis and the proposed design method.

2. Turn-off transient modelling of SiC/Si hybrid switch

The schematic diagram of SiC/Si hybrid switch is shown in Fig. 1, in which: V_{DR_MOS}, V_{DR_IGBT} are the gate drive voltage of SiC MOSFET and Si IGBT; T_{on_delay}, T_{off_delay} are the turn-on delay time and turn-off delay time between SiC MOSFET and Si IGBT, respectively. In order to fully utilize the switching characteristic advantages of SiC MOSFET, the switching mode as shown in Fig. 1 is generally used. In this switching mode, since the turn-on speed of Si IGBT is slower than that of SiC MOSFET, Si IGBT can turn on at zero voltage when the turn-on delay time is zero. Also, since the Si IGBT turns off before the SiC MOSFET, the Si IGBT can achieve zero-voltage turn-off.

In order to analyse the turn-off process of SiC/Si hybrid switch thoroughly, we take the double-pulse test circuit shown in Fig. 2 as an example and models the turn-off transient for SiC/Si hybrid switch in segments considering the main parasitic parameters in the circuit. In the figure: V_{DC} is the bus voltage, I_L is the load current. D_H is the ideal SiC SBD, C_J is the junction capacitance; C_{GS}, C_{GD} and C_{DS} are the capacitance of SiC MOSFET. C_{GE}, C_{GC} and C_{CE} are the capacitance of Si IGBT. L_{D1}, L_{S1}, L_{C1}, L_{E1} are the parasitic inductors introduced by the device package, L_{G1}, L_{G2} are the gate loop parasitic inductors, $R_{G(int)1}$, $R_{G(int)2}$ are the gate internal resistance, $R_{G(ext)1}$, $R_{G(ext)2}$ are the external driving resistance; L_{h1}, L_{h2}, L_{D2}, L_{C2}, L_{S2}, L_{E2} are the stray inductors introduced by the PCB layout.

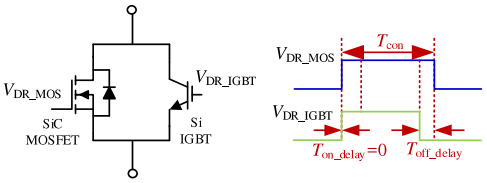


Fig. 1. Schematic diagram of SiC/Si hybrid switch.

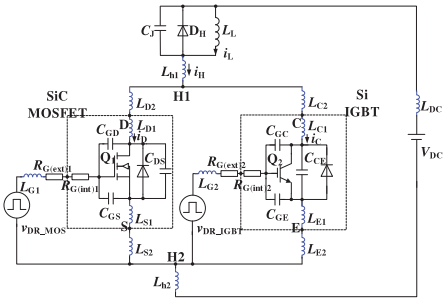


Fig. 2. Double pulse test circuit for SiC/Si hybrid switch considering parasitic parameters.

The turn-off waveform of the SiC/Si hybrid switch considering the parasitic parameters is shown in Fig. 3, from top to bottom: driving signal v_{DR_MOS} and v_{DR_IGBT}, gate voltage v_{GS_MOS} and v_{GS_IGBT}, drain current i_D and collector current i_C, and drain–source voltage v_{DS}. The turn-off process can be divided into nine stages according to the current–voltage variation.

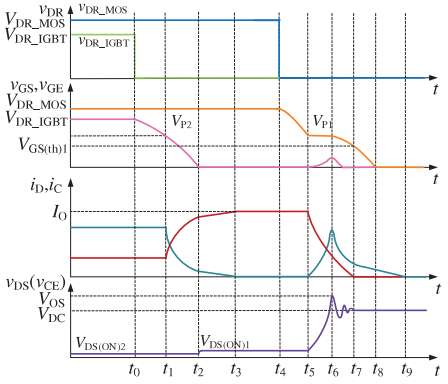


Fig. 3. Turn-off waveform of SiC/Si switch considering parasitic parameters.

Stage1[t_0~t_1]: At t_0, the Si IGBT driving signal steps to zero, and its equivalent input capacitance C_{ISS2} (= $C_{GE} + C_{GC}$) starts to discharge through the driving resistance R_{G2} (= $R_{G(int)2} + R_{G(ext)2}$), and the gate voltage v_{GE} starts to decrease. However, before v_{GE} decreases to V_{P2}, the IGBT works in the linear region, and the collector current i_C and the collector voltage v_{CE} remain unchanged. The time of this phase can be expressed as:

$$t_1 - t_0 = R_{G2} C_{ISS2} \ln\left(\frac{V_{TH2} + I_O/g_{fs}}{V_{DR\_IGBT}}\right) \tag{1}$$

Stage2[t_1~t_2]: At t_1, the gate voltage v_{GE} of the Si IGBT decreases to V_{P2}, the channel starts to shut down. The collector voltage v_{CE} is clamped by the on-state voltage drop $V_{DS(ON)2}$, so v_{CE} does not rise. The collector current i_C starts to fall, at which time the current is gradually transferred to the SiC MOSFET, and the drain current i_D starts to rise until the moment t_2, when the Si IGBT enters the turn-off trailing current phase.

Stage3[t_2∼t_3]: At t_2, the Si IGBT enters the turn-off trailing current phase and the equivalent MOSFET channel within the IGBT is completely shut down. Since there is only one carrier conducting in the IGBT, the low mobility of the minority carriers (holes) in the drift region can only disappear by compounding, so the collector current i_C decreases slowly, resulting in a trailing current phenomenon with a relatively long time. Obviously, the length of this period depends mainly on the life of the minority carriers in the drift region. At this time the hybrid device on-state voltage drop also rises to the on-state voltage drop of SiC MOSFET.

Stage4[t_3∼t_4]: At moment of t_3, the trailing current in the Si IGBT basically disappears and the SiC MOSFET undertakes the load current.

Stage5[t_4∼t_5]: At t_4, the SiC MOSFET driving signal steps to zero, its equivalent input capacitance C_{ISS1} (= $C_{GS} + C_{GD}$) starts to discharge through the driving resistance R_{G1} (= $R_{G(int)1} + R_{G(ext)1}$), and the MOSFET gate voltage v_{GS} starts to decrease. But before v_{GS} decreases to V_{P1}, SiC MOSFET works in the linear region, and the drain current i_D and the drain–source voltage v_{DS} remain constant. The time can be expressed as:

$$t_5 - t_4 = R_{G1} C_{ISS1} \ln\left(\frac{V_{TH1} + I_O/g_{fs}}{V_{DR\_MOS}}\right) \tag{2}$$

Stage6[t_5∼t_6]: At t_5, the voltage v_{GS} drops to the voltage V_{P1} and remains constant during this phase, the voltage v_{DS} rises slowly and the current i_D starts to drop, with the load current discharging the junction capacitance C_J and output capacitance C_{OSS2} (= $C_{CE} + C_{GC}$). At the same time, the remnant carriers in the IGBT need to withstand the high turn-off dv/dt of SiC MOSFET, so there will be a very high rate of carrier extraction, thus causing the current spike of the IGBT. The magnitude of its carrier compound extraction current is related to the lifetime of the remnant carriers. In addition, the displacement current of the C_{GC} charge causes a forward spike in the voltage v_{GE}. The time of this phase can be expressed as:

$$t_6 - t_5 = \frac{Q_{GD} \cdot R_{G1}}{V_{P1}} \tag{3}$$

Stage7[t_6∼t_7]: After the voltage v_{DS} stabilizes, the SiC MOSFET works in the saturation region. The current i_C and i_D continue to fall, the voltage v_{GS} continues to fall to $V_{GS(th)1}$, and the current i_D drops to zero at t_7. The duration of this phase is:

$$t_7 - t_6 = R_{G1} C_{ISS1} \ln \frac{V_{P1}}{V_{GS(th)1}} \tag{4}$$

Stage8[t_7∼t_8]: At t_7, the voltage v_{GS} continues to drop from the threshold voltage V_{TH1} and the SiC MOSFET is shut down. The carrier complex current of the Si IGBT continues to drop.

Stage9[t_8∼t_9]: At t_9, all the load current is transferred into the diode. The duration of this phase depends on the carrier compound rate of the IGBT.

The turn-off loss E_{off} of SiC/Si hybrid switch consists of three main components, which are SiC MOSFET hard turn-off loss E_{off_MOS}, SiC MOSFET additional conduction loss $\Delta E_{con\_MOS\_off}$ during the turn-off delay time, and the loss caused by Si IGBT turn-off current spike E_{off_IGBT}. The expression of each component loss are as follows.

$$E_{off} = E_{off\_MOS} + \Delta E_{con\_MOS\_off} + E_{off\_IGBT} \tag{5}$$

$$E_{off\_MOS} = \int_{T_{off\_delay}}^{T_{off\_delay}+t_{off\_MOS}} v_{DS} \cdot i_D \mathrm{d}t \tag{6}$$

$$\Delta E_{con\_MOS\_off} = \int_{0}^{T_{off\_delay}} v_{DS} \cdot i_D \mathrm{d}t \tag{7}$$

$$E_{off\_IGBT} = (E_{hard\_off\_IGBT} - E_{res\_off}) \cdot e^{-\tau \cdot t_{off\_delay}} + E_{res\_off} \tag{8}$$

where: t_{off_MOS} and t_{off_IGBT} are the turn-off time of SiC MOSFET and Si IGBT. $E_{off\_hard\_IGBT}$ is the hard turn-off loss of Si IGBT, E_{res_off} is the loss of parasitic capacitor charging when Si IGBT is subjected to bus voltage, τ is the time constant of Si IGBT turn-off loss, and the magnitude is related to the carrier lifetime in the Si IGBT, which can be obtained by fitting the double pulse experiment.

The analysis shows that the rise of the voltage v_{DS} causes the current spike due to the parasitic capacitance charging and carrier compounding. Since the degree of remnant carrier compounding in IGBTs is related to the operating conditions and compounding time, the turn-off delay time T_{off_delay} also affects the turn-off current spikes. The turn-off current spike is also affected by dv/dt, so the SiC MOSFET driving circuit parameters also affect the current spike.

3. Analysis of influencing factors on the turn-off current spike

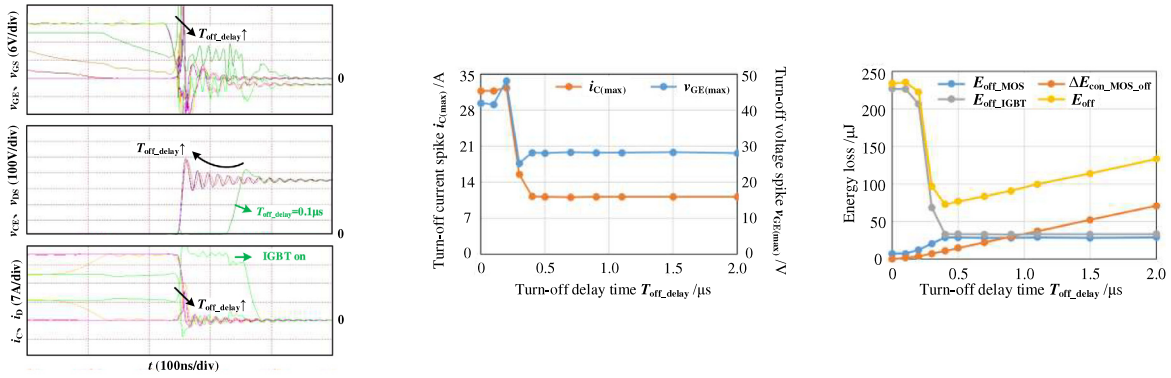
According to the analysis in the previous section, the influencing factors of the IGBT turn-off current spike include the remnant carrier compound degree and the drain–source voltage variation rate dv/dt. In this section, the LTspice simulation software is used to investigate the influence law of the influencing factors of the turn-off current spikes. The power devices used in the simulation are Rohm 650 V/27 A SiC MOSFET (SCT3060AL) and Infineon 600 V/40 A Si IGBT (IKW40N60H3), and the simulation parameters are set as shown in Table 1.

Table 1. Parameter values of SiC/Si hybrid switch simulation circuit.

Parameter	Value	Parameter	Value
Bus voltage V_{DC}/V	350	Driving voltage of MOSFET V_{DR_MOS}/V	18/−2
Load current I_O/A	25	Driving resistance of MOSFET R_{G1}/Ω	12
Turn-on delay time T_{on_delay}/μs	0	Gate parasitic inductance L_{G1}, L_{G2}/nH	40
Turn-off delay time T_{off_delay}/μs	0.5	Equivalent junction capacitance C_J/pF	80

3.1. Turn-off delay time

The turn-off waveforms of SiC/Si hybrid switch with different turn-off delay time T_{off_delay} are shown in Fig. 4(a). When $T_{off\_delay} = 0.1$ μs, due to the slower turn-off speed of Si IGBT, when the SiC MOSEFT is completely turn off, the load current is all transferred to the IGBT, which makes the Si IGBT produce hard switching loss, while the drain–source voltage v_{DS} change phase is delayed. As T_{off_delay} increases, the turn-off current spike decreases from 31.63 A to 11.16 A, at the same time, the voltage spike of v_{DS} increases and stabilizes at about 480 V.



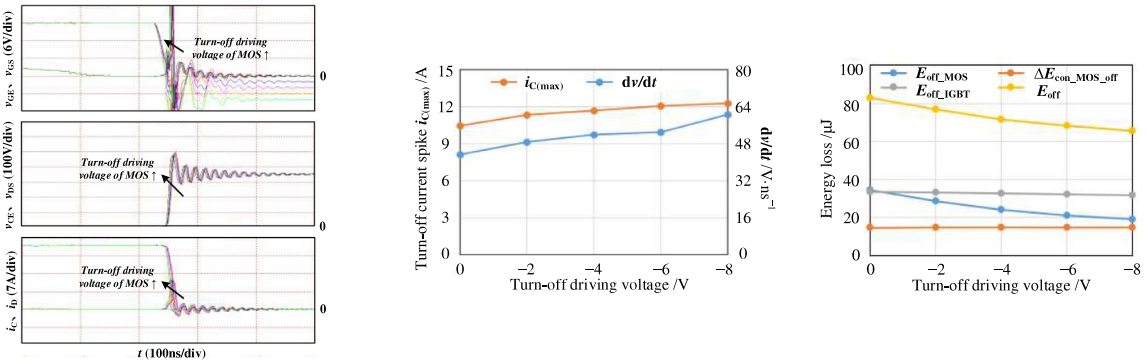
(a) Turn-off waveform (b) Turn-off current & voltage spike (c) Turn-off loss

Fig. 4. Effect of turn-off delay time on turn-off characteristics of SiC/Si hybrid switch.

As can be seen from Fig. 4, under the condition that dv/dt is basically constant, when T_{off_delay} ≤0.2 μs, the Si IGBT turns off after SiC MOSFET, the voltage drop generated by the common source parasitic inductance in the Si IGBT package with large di/dt interaction causes the peak of v_{GE}. When $T_{off\_delay} > 0.2$ μs, the SiC MOSFET turn off later and the peak of v_{GE} tends to be constant. When $T_{off\_delay} < 0.9$ μs, the current spike and its resulting loss E_{off_IGBT} decreases as T_{off_delay} increases. When $T_{off\_delay} > 0.9$ μs, the degree of Si IGBT carrier compound will be independent of time, the current spike and E_{off_IGBT} no longer decreases, but will increase the additional conduction loss of SiC MOSFET. According to the curve of turn-off loss E_{off} can be seen that there is a loss optimal point, comprehensive consideration of turn-off current spike and E_{off}, T_{off_delay} is recommended to be 0.4 μs.

3.2. Turn-off driving voltage of SiC MOSFET

The SiC/Si hybrid switch turn-off waveforms when the turn-off driving voltage of SiC MOSFET is taken as 0 V, −2 V, −4 V, −6 V and −8 V are shown in Fig. 5(a). As the absolute value of the turn-off driving voltage increases,



(a) Turn-off waveform (b) Turn-off current spike and dv/dt (c) Turn-off loss

Fig. 5. Effect of SiC MOSFET's driving voltage on turn-off characteristics of SiC/Si hybrid switch.

it has little effect on the turn-off current variation rate di/dt, and the turn-off drain–source voltage spike is basically unchanged. At the same time, the dv/dt of the voltage v_{DS} increases slightly and the remnant carrier extraction rate of the IGBT increases making the IGBT turn-off current spike increase from 10.45 A to 12.28 A.

As can be seen from Fig. 5, as the turn-off driving voltage of SiC MOSFET increases, the hard turn-off loss E_{off_MOS} decreases and the additional conduction loss $\Delta E_{con\_MOS\_off}$ remains essentially unchanged. Since the current spike of IGBT changes insignificantly, E_{off_IGBT} remains basically the same, and then the total turn-off loss E_{off} increases.

3.3. Turn-off driving resistance of SiC MOSFET

Considering that the SiC MOSFET device selected in this paper has 12 Ω gate internal resistance, the SiC/Si hybrid switch turn-off waveform is shown in Fig. 6(a) when its turn-off driving resistance is taken as 12 Ω, 17 Ω, 22 Ω, 27 Ω and 32 Ω, respectively. As the turn-off driving resistance increases, the voltage drop across the power loop inductor decreases and the turn-off drain–source voltage spike decreases from 500 V to 440 V due to the decrease of di/dt. At the same time, the variation rate dv/dt of turn-off drain–source voltage is significantly reduced, and the reduced rate of remnant carrier extraction for IGBT makes the IGBT turn-off current spike reduced from 11.32 A to 0.92 A.

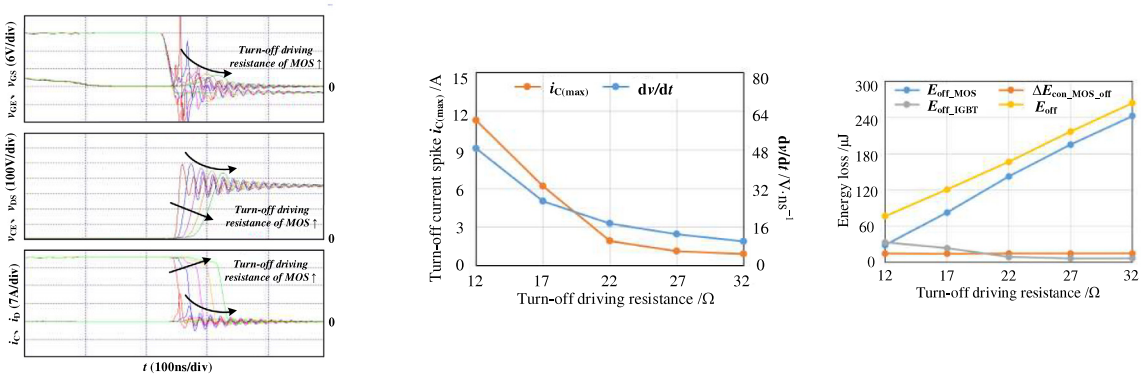
As can be seen from Fig. 6, the hard turn-off loss E_{off_MOS} increases significantly as the turn-off driving resistance increases, and the additional conduction loss $\Delta E_{con\_MOS\_off}$ remains essentially unchanged. Since the variation of the turn-off current spike decreases, E_{off_IGBT} will also decrease as the turn-off driving resistance increases. The total turn-off loss E_{off} increases because the driving resistance has a greater effect on the hard turn-off loss E_{off_MOS}.

4. Parameter optimization design method and experimental verification

In order to verify the effects of the parameter optimization design method on the Si IGBT turn-off current spikes and integrated losses, a double-pulse experimental platform as shown in Fig. 7 is built to test the turn-off characteristics of SiC/Si hybrid switch. The power devices used in the experiment are Rohm 650 V/27 A SiC MOSFET (SCT3060AL), Infineon 600 V/40 A Si IGBT (IKW40N60H3) and Rohm 600 V/40 A SiC SBD (SCS240AE).

4.1. Optimization design method of turn-off delay time

For SiC/Si hybrid switch, the increase of the turn-off delay time T_{off_delay} leads to a linear increase of the additional conduction loss $\Delta E_{con\_MOS\_off}$ of SiC MOSFET and a nonlinear decrease of the turn-off current spike loss E_{off_IGBT} of IGBT, so there is an optimal turn-off loss E_{off}, and the optimal turn-off delay time T_{off_delay} is selected based on the "comprehensive turn-off loss optimization principle".



(a) Turn-off waveform (b) Turn-off current spike and dv/dt (c) Turn-off loss

Fig. 6. Effect of SiC MOSFET's driving resistance on turn-off characteristics of SiC/Si hybrid switch.

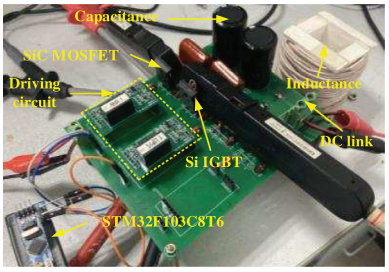
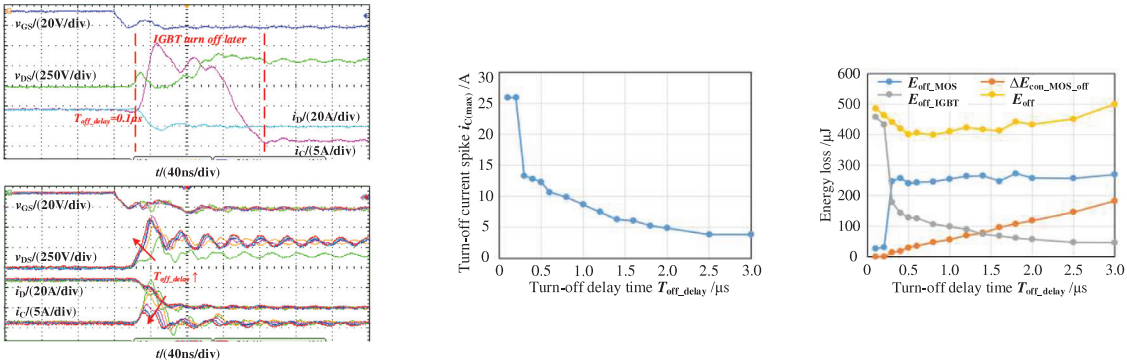


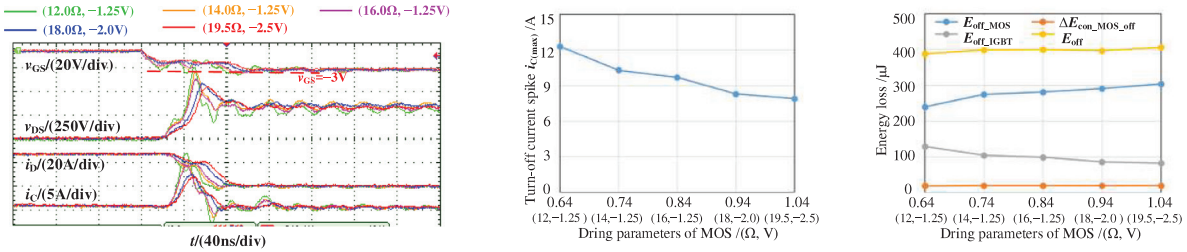
Fig. 7. Double-pulse experimental platform for SiC/Si hybrid switch.

Fig. 8 shows the turn-off characteristics when the turn-off delay time T_{off_delay} is 0.1 μs∼3.0 μs. Fig. 9(a) shows the turn-off waveforms when the turn-off delay is 0.1 μs, 0.5 μs, 1.0 μs, 1.5 μs, 2.0 μs, 2.5 μs, 3.0 μs, respectively. It can be seen that when the turn-off delay $T_{off\_delay} = 0.1$ μs, the IGBT turn-off time t_{off_IGBT} is less than 0.1 μs, so the IGBT turn off later and generates 450 μJ hard turn-off loss. With the increase of the turn-off delay time, the turn-off current spike decreases from 13.3A to 3.9 A, which reduces the loss caused by the IGBT turn-off current spike by 73.23%. Therefore, for the working condition of 350 V/25 A, a turn-off delay time of 0.5 μs is recommended for considering the comprehensive turn-off loss E_{off}, which is very close to the simulation results.



(a) Turn-off waveform (b) Turn-off current spike (c) Turn-off loss

Fig. 8. Experimental results with different turn-off delay time.



(a) Turn-off waveform (b) Turn-off current spike (c) Turn-off loss

Fig. 9. Experimental results with different driving parameters of SiC MOSFET.

4.2. Optimization design method of driving parameters

Due to the presence of parasitic inductance in the driving circuit of power devices, it will cause second-order oscillation. So reasonable driving resistance and driving voltage are required to ensure gate reliability. Therefore, the driving circuit parameters of SiC/Si hybrid switch need to be optimized considering gate reliability, IGBT turn-off current spike and turn-off loss. Since zero voltage switching is realized when SiC/Si hybrid switch is in the switching mode that the IGBT turn off firstly, the driving circuit parameters of IGBT has little effect on the turn-off characteristics of SiC/Si hybrid switch, we mainly optimize the driving circuit parameters of SiC MOSFET.

For the optimization design of the driving parameters, first, the maximum negative gate voltage $V_{GS(-max)}$ should be limited, then the driving circuit parameters are adjusted and the optimized parameters are selected according to the "comprehensive turn-off loss optimization principle". Obviously, as the driving resistance increases, the driving voltage can be increased accordingly.

For SiC MOSFET driving circuit parameters, increasing the turn-off driving resistance R_{G1} can be more effective to reduce dv/dt than increasing the turn-off driving voltage V_{DR_MOS-}, thus it should be more effective to suppress IGBT turn-off current spike and reduce E_{off_IGBT}, but will cause very large E_{off_MOS}. However, considering the comprehensive turn-off loss E_{off}, R_{G1} can still not be too large.

Similarly, while increasing the turn-off driving voltage V_{DR_MOS-} can reduce the loss caused by current spike E_{off_IGBT}, the low negative gate withstand voltage of the SiC MOSFET and the severe turn-off oscillations caused by the fast turn-off speed make it difficult to change the driving voltage significantly.

In order to find the optimal combination of driving parameters, the turn-off characteristics are shown in Fig. 9 when $V_{GS(-max)} = -3$V and the driving loop damping ratios of SiC MOSFET are set to be 0.64, 0.74, 0.84, 0.94 and 1.04, respectively, under the condition that L_{G1} is 42 nH. As the driving resistance increases, the turn-off speed of SiC MOSFET decreases, so the turn-off voltage peak decreases from 760 V to 530 V, which almost decreases by 30.3%, and the turn-off current peak decreases from 12.3 A to 7.9 A, which almost decreases by 35.8%.

Since the SiC MOSFET gate negative withstand voltage is −4 V, the absolute value of turn-off gate voltage spikes larger than 4 V when the driving resistance is less than 16 Ω, so a 16 Ω driving resistance is required to suppress the turn-off oscillation in order not to exceed $V_{GS(-max)}$. Although adjusting the driving parameters could ensure the gate reliability, increasing R_{G1} will make the SiC MOSFET turn-off loss E_{off_MOS} significantly larger, but at the same time it can reduce the spike loss E_{off_IGBT}. From the experimental results, it can be seen that the optimized combination of SiC MOSFET driving parameters that both to ensure reliability and the lowest turn-off loss is (18 Ω, −2V), and the driving circuit damping ratio is 0.94.

5. Conclusions

In this paper, the influencing factors of IGBT turn-off current spike in SiC/Si hybrid switch are evaluated, and an optimized circuit parameter design method of SiC/Si hybrid switch considering turn-off current spike is given:

(1) The turn-off current spike of Si IGBT is formed when the remnant carriers in the carrier storage region bear the high dv/dt during the turn off process of SiC MOSFET.

(2) The influencing factors of Si IGBT turn-off current spike include turn-off delay time and SiC MOSFET driving parameters. Among them, increasing the turn-off delay time, turn-off driving resistance of MOSFET and reducing turn-off driving voltage of MOSFET can effectively suppress the Si IGBT turn-off current spike.

(3) According to the “comprehensive turn-off loss optimization principle”, there is generally an optimal turn-off delay time, and 0.5 μs was selected as the optimal turn-off delay time of hybrid switch consisting of SiC MOSFET (SCT3060AL) and Si IGBT (IKW40N60H3).

(4) For the parameters of SiC MOSFET driving circuit, a damping ratio greater than 0.84 should be first confirmed to ensure the gate reliability, and then respective parameters of driving circuit should be optimized according to the “comprehensive turn-off loss optimization principle”.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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