Multi-Stage Gate Modulation of E-Band MMIC Power Amplifier for Efficiency Improvement

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***Abstract*—This work studies an efficiency improvement method of a 4 stage 1W GaAs E-band PA using multistage gate modulation. Using a behavioral modeling technique, we use simulations to investigate efficiency enhancement for different gate drive scenarios having one, two, or all stages of the PA modulated. Assuming an ideal pre-distortion and testing with a 64-QAM modulation signal an improvement of average PAE from 7.2% to 10.3% is achieved which corresponds to a reduction of average DC power consumption from 5.9W to 4W.**

***Index Terms*—MMIC, power amplifier, efficiency, gate modulation**

I. Introduction

Modern telecommunication systems aim for modulation schemes with greater spectral efficiency, which results in signals with a high peak to average power ratio (PAPR). Moreover, at mm-wave bands, transistor power, and gain are limited, and efficiency is low. To both overcome linearity and output power limitations, power amplifiers (PA) of the front ends are usually biased for class A or AB operations with high quiescent currents. Unfortunately, at backed-off output power levels, this high quiescent current results in excessive power consumption and heat. To overcome this problem, in this paper, we propose a dynamic gate bias modulation technique for multi-stage MMIC PAs and investigate the possible PAE improvements as well as gain and linearity behaviour for modulated signals depending on the chosen gate modulation configuration.

The theory of adaptive gate bias based on the envelope of the input signal to improve power added efficiency (PAE) was studied in [1]. In [2] gate bias modulation of the carrier and peaking amplifier of a Doherty PA was shown to improve in PAE and output power compared to conventional Doherty and class AB amplifiers under the same linearity. In [3] quiescent current of HBT devices was modulated to both extend linear gain range before compression at high input power, and reduce the quiescent current at low input power. Finally, in [4], [5] gate modulation was used to flatten the amplitude and phase response of a PA which allowed it to operate at higher output powers before they exceed specific linearity specifications so that overall efficiency with modulated signal was improved.

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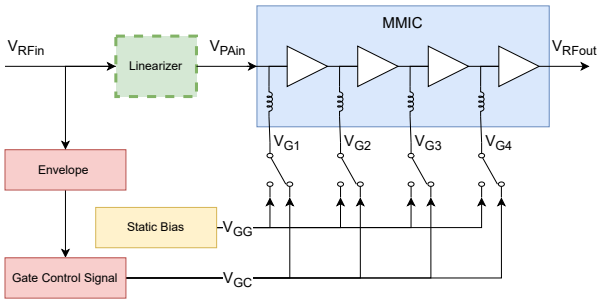
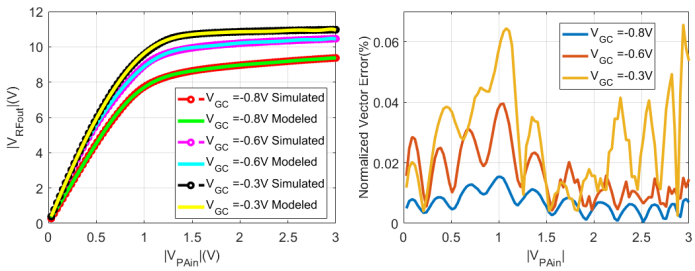


Fig. 1. Functional schematic of dynamic multi stage gate bias controlled power amplifier

Fig. 1 illustrates the proposed architecture, where we study the effects of gate modulating one or several stages of a power amplifier. To keep the system complexity low, a common gate modulation signal (V_{GC}) was used to gate modulate one or several of the stages $(V_{\mathrm{G}(1-4)})$. We investigate three scenarios: 1) gate modulation of the last stage where only V_{G4} was connected to V_{GC}, 2) gate modulation of the last two stages where both V_{G4} and V_{G3} were connected to V_{GC} and 3) gate modulation of all stages where all gate biases connected to V_{GC}. In each case, the rest of the gate biases were connected to static gate bias voltage (V_{GG}) which was kept at its default value -0.46 V. Finally, we added an ideal pre-distortion stage to demonstrate the maximum efficiency improvement possibilities.

II. Behavioral Modeling for Gate Modulated Power Amplifiers

In this work, to investigate the potential of gate modulation of an existing PA and test our result with quasi-static simulation, we developed a behavioural model based on Harmonic Balance (HB) simulations at 83.5 GHz of Gotmic AB's 1 W E-band GaAs PA gAPZ00092. The gate bias voltage was swept from -0.8 V to -0.3 V for different gate modulation scenarios. The lower limit was set to the pinch-off voltage -0.8 V. This will guarantee class B/AB/A operation. The maximum gate voltage was set to -0.8 V, beyond which the transconductance starts to decrease and no improvement



(a) (b)

Fig. 2. Last stage gate modulated power amplifier's (a) magnitude of output voltage, (b) and normalized vector error magnitude with respect to V_{PAin} at different V_{GC} levels.

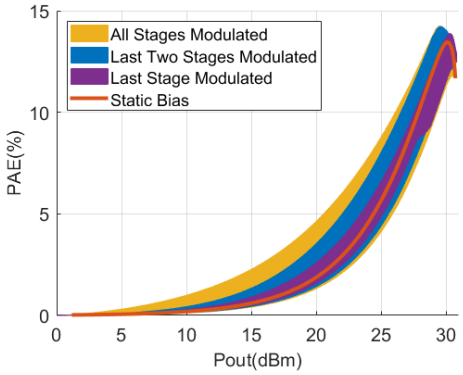


Fig. 3. Achievable PAE with different gate modulation scenarios

is possible. For each gate voltage setting, the input power was swept from -20 dBm to 20 dBm to both observe linear and the saturated response of the PA.

For different scenarios, we modeled the complex output voltage($V_{\mathrm{RFout_m}}$) as an odd order polynomial expansion of the input voltage of PA (V_{PAin}) and represented its complex coefficients (c_{p}) as function of V_{GC} as below

$$V_{\mathrm{RFout_m}} = \sum_{p=0}^{P} V_{\mathrm{PAin}} |V_{\mathrm{PAin}}|^{2p} c_p(V_{\mathrm{GC}}), \tag{1}$$

where P is the highest polynomial order.

Similarly, modeled DC power consumption ($P_{\mathrm{DC_m}}$) is

$$P_{\mathrm{DC_m}} = \sum_{q=0}^{Q} V_{\mathrm{PAin}}^{q} c_q(V_{\mathrm{GC}}), \tag{2}$$

where (c_q) are the coefficients and Q is the highest polynomial order.

The complex coefficients c_p and c_q are themselves represented by a polynomial expansion of V_{GC}

$$c_p(V_{\mathrm{GC}}) = \sum_{r=0}^{R} V_{\mathrm{GC}}^{r} c_r. \tag{3}$$

where again c_r are the coefficients and R is the highest polynomial order.A similar equation can be also written for c_q.

By using the least square method, these polynomial models were fitted to the PA simulation results. Fig. 2a compares modeled and simulated $|V_{\mathrm{RFout}}|$ for the selected V_{GC} range. Fig. 2b shows NVE(normalized vector error) described as

$$\mathrm{NVE} = |V_{\mathrm{RFout_M}} - V_{\mathrm{RFout_S}}| / |\widehat{V_{\mathrm{RFout_S}}}|, \tag{4}$$

where ($V_{\mathrm{RFout_M}}$) is the modeled and ($V_{\mathrm{RFout_S}}$) is the simulated output voltage and $|\widehat{V_{\mathrm{RFout_S}}}|$ is the maximum $|V_{\mathrm{RFout_S}}|$. For all models and all modulation scenarios, this value does not exceeded 0.09%. This allows us to use this model for our later investigations trusting its accuracy.

III. Efficiency Optimised Drive Profiles

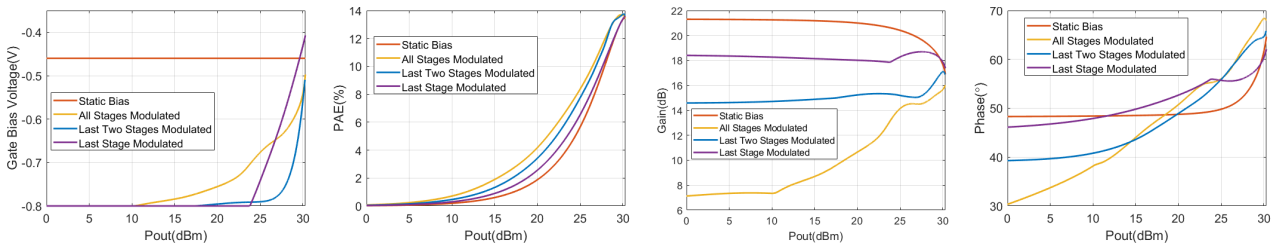
The achievable PAE regions for different modulation scenarios are shown in Fig.3. We observe that the range of PAE increases with the increased number of gate modulated stages. For each configuration and each output power (P_{out}) value, an optimum gate voltage can be found that maximises PAE. To find these PAE optimized gate drive functions we use the previously explained polynomial model and select optimum V_{RFin} and V_{GC} pairs for each P_{out} value. While V_{GC} was selected to maximise PAE, Referring to Fig. 1, V_{PAin} was selected to provide a linear relationship between V_{RFin} and V_{RFout}, similar to the static splitter function described in [6]. The resulting gate drive functions and PAE characteristics of the gate modulated PAs can be seen in Fig. 4a and Fig. 4b, respectively. Fig. 4c and Fig. 4d shows the gain and phase relation between V_{PAin} and V_{RFout} after the gate drive signal was applied to the PA. These figures show the gain variance of modulation of the last and last two stages is significantly smaller compared to modulation of all stages and could be linearized easier. However, modulating two or more stages promises larger PAE improvement.

IV. Simulation Results With Modulated Signal

The quasi-static gate modulated power amplifier models were tested with the same, randomly generated 64QAM signal shaped with raised-cosine-filter with the roll-off factor of 0.25, To investigate the requirements of the predistortion linearizer, and the achievable PAE performance for different gate modulation schemes.

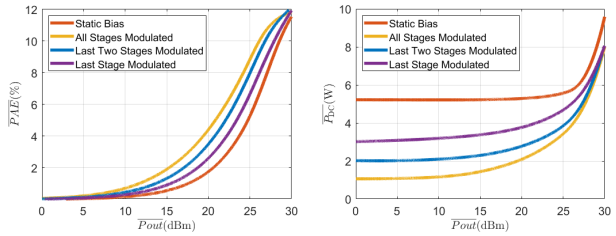
First, gate modulated but not linearized PAs were tested with increasing signal power levels to study the complexity of the required pre-distortion. Fig. 6a shows error vector magnitude (EVM) with increasing average output power level ($\overline{P_{\mathrm{out}}}$). Considering the average PAE ($\overline{PAE}$) and DC Power consumption($\overline{P_{\mathrm{DC}}}$) given in Fig. 5a and Fig. 5b, it is clear that the more number of stages are gate modulated, the more complex pre-distortion is required but in return larger $\overline{PAE}$ improvement is acquired.

Second, the input power level was increased until the gate modulated PAs' output spectrum reach the limitations of the applicable ETSI spectrum emission mask shown in Fig. 6b.



(a) (b) (c) (d)

Fig. 4. Modelled PA behavior for different gate modulation scenarios (a) gate drive functions , (b) power added efficiency, (c) gain and (d) phase variation with respect to output power



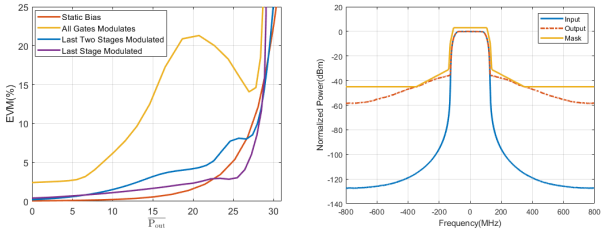
(a) (b)

Fig. 5. Under modulated signal, (a) realized average PAE(%) (b) average DC power consumption with respect to average output power.

For each scenario, EVM, $\overline{PAE}$, $\overline{P_{\text{out}}}$ and maximum output power $(\widehat{P_{\text{out}}})$ were populated in Table I at spectrum mask limit. The first columns of the table show that, without a pre-distortion, the derived gate drive profiles will not offer any performance improvement over static bias. However, when used in combination with an ideal pre-distortion, and with the output power clipped at the maximum output power of the PA, 30.3 dBm, we observe a promising improvement in PAE. Table I shows that $\overline{PAE}$ can be improved from 7.1% to 8.2% , 9.5% and 10.3% with different modulation scenarios. These improvements correspond to the reduction of average DC power consumption from 5.88W to 5.11W, 4.30W and 4.01W, respectively.

V. Conclusion

In this work, we studied the potential of gate modulation of the different numbers of stages of a millimeter-wave PA with a single gate control signal. We show that PAE optimized drive provides promising improvement when used in collaboration with pre-distortion. It is shown that, depending on the realizable pre-distortion, gate modulation of more stages promises larger PAE improvement. However, gate modulation of all stages requires a significantly more complex pre-distortion to be realized compared to other cases. In conclusion, in collaboration with pre-distortion, PAE optimized gate modulation of multi-stages is a promising technique to reduce the overall power consumption of front-ends.



(a) (b)

Fig. 6. (a) Error vector magnitude at different average output power levels of gate modulated power amplifiers without pre-distortion. (b) Spectrum of the V_{RFin} and V_{RFout} and emission mask

TABLE I
Quasi-Static Simulation Results at Spectrum Mask Limit

Gate Modulation Mode	Without pre-distortion				With pre-distortion			
	EVM	$\overline{PAE}$	$\overline{P_{\text{out}}}$	$\widehat{P_{\text{out}}}$	EVM	$\overline{PAE}$	$\overline{P_{\text{out}}}$	$\widehat{P_{\text{out}}}$
Static Bias	2.75	3.27	22.5	28.6	1.81	7.2	26.3	30.3
Last Stage	2.33	2.49	19.8	28.2	1.81	8.2	26.3	30.3
Last Two Stages	2.79	1.11	13.91	21.52	1.81	9.5	26.3	30.3
All Stages	2.47	0.13	1.5	9.5	1.81	10.3	26.3	30.3

EVM and $\overline{PAE}$ in %, $\overline{P_{\text{out}}}$ and $\widehat{P_{\text{out}}}$ in dBm

Acknowledgment

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