THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Study of charge carrier transport in field-effect transistors

with two-dimensional electron gas using geometrical magnetoresistance effect

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Cover:
An artistic interpretation of a transistor in a magnetic field. The zoom-in sequence shows the gate region and how the magnetic field affects the electrons.

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Abstract

During the last decades, significant efforts have been made to exploit the excellent and promising electronic properties exhibited by field-effect transistors (FETs) with two-dimensional electron gas (2DEG) channels. The most prominent representatives of this class of devices are high-electron-mobility transistors (HEMTs) and graphene field-effect transistors (GFETs). Despite the relative maturity of the HEMTs and considerable efforts recently applied to develop the GFETs, a better understanding of the charge carrier transport mechanisms is required for their further development. This thesis work is focused on studying the charge carrier transport in the InGaAs/InP HEMTs and GFETs using the geometrical magnetoresistance (gMR) effect.

The angular dependencies of output characteristics of the InGaAs/InP HEMTs oriented in a magnetic field (B) up to 14 T at 2 K were investigated. A strong angular dependence as a function of the B-field was identified. It was shown that the gMR effect governs the observed performance of the HEMTs, and the measured dependencies were accurately described by gMR theory. Additionally, the carrier velocity in InGaAs/InP HEMTs was studied using the gMR effect in the wide range of the drain fields at a cryogenic temperature of 2 K. The velocity peak was observed experimentally for the first time, and it was found that the peak velocity and corresponding field decreased significantly with the transverse field. The relevant scattering mechanisms were analyzed, and it was further demonstrated, that the low-field mobility and peak velocity reveal opposite dependencies on the transverse electric field, indicating the difference in carrier transport mechanisms dominating at low and high electric fields.

It was demonstrated, that the mobility in the GFETs can be directly characterized and analyzed using the gMR and that the method is free from the limitations of other commonly used approaches requiring an assumption of constant mobility and knowledge of the gate capacitance. This allowed for interpretation of the measured dependencies of mobility on the gate voltage, *i.e.*, carrier concentration, and identifying the corresponding scattering mechanisms. The charge carrier transport in the GFETs, characterized using the gMR method in combination with the drain-source resistance model, was also studied by applying a model of the quasi-ballistic charge carrier transport and transfer formalism. The charge carrier mean free path was found to be in the range of 374-390 nm. GFETs with a gate length of 2 μm were shown to have $\approx$ 20 % of the charge carriers moving ballistically, while at the gate length of 0.2 μm this number increases to above 60 %.

Keywords: high-electron-mobility transistor, graphene field-effect transistor, low noise and high frequency applications, geometrical magnetoresistance, charge carrier transport, charge carrier scattering mechanisms, velocity saturation, velocity peak, low-field mobility, two-dimensional electron gas, quasi-ballistic charge carrier transport

List of publications

This thesis is based on the work contained in the following appended papers:

Paper A **Isabel Harrysson Rodrigues**, David Niepce, Arsalan Pourkabirian, Giuseppe Moschetti, Joel Schleeh, Thilo Bauch, and Jan Grahn, "On the Angular Dependence of InP High Electron Mobility Transistors for Cryogenic Low Noise Amplifiers in a Magnetic Field", *AIP Advances* **9**, 085004, 2019.

Paper B **Isabel Harrysson Rodrigues**, Andrei Vorobiev, "Low-field mobility and high-field velocity of charge carriers in InGaAs/InP high-electron-mobility transistors", *IEEE Transactions on Electron Devices*, **69**(4), pp. 1786-1791, 2022.

Paper C **Isabel Harrysson Rodrigues**, Andrey Generalov, Anamul Md Hoque, Miika Soikkeli, Anton Murros, Sanna Arpiainen, Andrei Vorobiev, "Geometrical magnetoresistance mobility in graphene field effect transistors", *Applied Physics Letters*, **121**, 013502, 2022.

Paper D **Isabel Harrysson Rodrigues**, Niklas Rorsman, Andrei Vorobiev, "Mobility and quasi-ballistic charge carrier transport in graphene field-effect transistors", *Under revision for publication in J. Appl. Phys.*, 2022.

Other publications:

Paper I André Dankert, Priyamvada Bhaskar, Dmitrii Khokhriakov, **Isabel Harrysson Rodrigues**, Bogdan Karpiak, M. Venkata Kamalakar, Sophie Charpentier, Ion Garate, and Saroj P. Dash, "Origin and evolution of surface spin current in topological insulators", *PHYSICAL REVIEW B* **97**: 125414, 2018.

Paper II **Isabel Harrysson Rodrigues**, Arsalan Pourkabirian, Giuseppe Moschetti, Joel Schleeh, Per-Åke Nilsson and Jan Grahn, "Magnetic Influence on Cryogenic InP HEMT DC Characteristics", *Compound Semiconductor Week* 2018.

Paper III **Isabel Harrysson Rodrigues**, David Niepce, Arsalan Pourkabirian Giuseppe Moschetti, Joel Schleeh, Thilo Bauch, and Jan Grahn, "Angular Dependence of InP High Electron Mobility Transistors for Cryogenic Low Noise Amplifiers under a magnetic field", *Compound Semiconductor Week* 2019.

Paper IV **Isabel Harrysson Rodrigues**, Andrei Vorobiev, Jan Stake, "Evaluation and Study of Mobility in GFETs by geometrical magnetoresistance", *Graphene week 2021*, Conference contribution, September, 2021.

Paper V **Isabel Harrysson Rodrigues**, Andrei Vorobiev "Charge carrier transport in graphene field-effect transistor scaled down to submicron gate lengths", *Compound Semiconductor Week* 2022.

Parts of the research work in this thesis have already been published in the Licentiate thesis:

Paper VI **Isabel Harrysson Rodrigues**, "Cryogenic InP High Electron Mobility Transistors in a Magnetic Field", *Chalmers University of Technology*, Licentiate thesis, September 27, 2019.

Contents

To my beloved parents,
who always believed in me, and with kindness and care, taught me to believe in myself and observe the world around me with eyes of curiosity.

Abbreviations

2D	=	two-dimensional
2DEG	=	Two-dimensional electron gas
3D	=	three-dimensional
AlGaAs	=	Aluminum gallium arsenide
B	=	Magnetic flux (with unit Tesla), also referred to as B-field
CI	=	Charged impurities
Cr	=	Chromium
CVD	=	chemical vapor deposition
dc	=	direct current
DCL	=	diamond-like carbon
DUT	=	device under test
F	=	electric field (E in Paper B)
FET	=	field-effect transistor
FFT	=	fast Fourier transform
FOMs	=	figures of merit
FTICRMS	=	Fourier-transform ion cyclotron resonance mass spectroscopy
GaAs	=	Gallium arsenide
GFET	=	graphene field-effect transistor
gMR	=	Geometrical magnetoresistance
hBH	=	Hexagonal boron nitride
He	=	helium
HEMT	=	High-electron-mobility transistor
InAlAs	=	Indium aluminium arsenide
InGaAs	=	Indium gallium arsenide
InP	=	Indium phosphide
IPA	=	Isopropanol or Isopropyl alcohol
LAO	=	Local anodic oxidation
LC-network	=	electric circuit made of an inductor (L) and a capacitor (C)
LNA	=	Low noise amplifier
MIM	=	metal-insulator-metal
MMIC	=	Monolithic microwave integrated circuit
MOD	=	Modulation-doped
MODFET	=	Modulation-doped field-effect transistor
MOSFET	=	metal-oxide-semiconductor field-effect transistor
MR	=	magnetoresistance
MRI	=	magneto-resonance imaging
N	=	nitrogen
Ni	=	nickel
OPs	=	optical phonons
PMMA	=	polymethyl methacrylate
pMR	=	physical magnetoresistance

PPMS	=	Physical property measurement system
QD	=	Quantum Device
RF	=	Radio frequency
RRF	=	Relative reduction factor
rpm	=	Rotations per minute
RS	=	Resonant scatterers
SdH	=	Shubnikov de haas
S	=	Scattering
Si	=	Silicon
SiO_2	=	Silicon-dioxide
SPP	=	surface polar phonons
SRS	=	Surface roughtness scattering
T	=	Temperature (Kelvin)
TG	=	top-gate
TFR	=	Thin film resistor
VNA	=	vector network analyzer
III-V	=	”three-five”; materials from period 3 to 5 in the periodic table

Parameters & Symbols

a	=	Fitting parameter
c	=	speed of light
C_{g}	=	Gate capacitance per unit area
C_{gd}	=	Gate-drain capacitance
C_{gs}	=	Gate-source capacitance
C_{pad}	=	Gate pad capacitance
d	=	Total thickness of barrier and spacer layers
ϵ	=	(*epsilon*) Effective dielectric constant of barrier and spacer layer
ϵ_0, κ_{vacc}	=	Vacuum permittivity
e	=	Electron charge
E_{C}	=	conduction band energy
E_{F}	=	energy at Fermi level
E, E_{int}	=	intrinsic electric field
E_{T}	=	transfer field
E_{peak}	=	Peak field (kV/cm)
E_{T}	=	Transfer field (kV/cm)
f_{max}	=	maximum frequency
f_{T}	=	transit frequency
$f_{\mathrm{T,ext}}$	=	extrinsic transit frequency
$f_{\mathrm{T,int}}$	=	intrinsic transit frequency
F_i^2	=	Fröhlich coupling constant
$g_{\mathrm{m,ext}}$	=	extrinsic transconductance
$g_{\mathrm{m,int}}$	=	intrinsic transconductance

γ	=	(*gamma*) fitting parameter
$\hbar$	=	(*h-bar*) reduced Planck's constant
I	=	Current
I_{ds}	=	Drain-source current
I_{gs}	=	Intrinsic gate-source current
I_{GS}	=	Extrinsic gate-source current
k	=	Fitting parameter
k_{B}	=	Boltzmann's constant
L, L_{g}	=	Gate length
λ	=	(*lambda*) mean free path
m	=	particle mass
m_{e}	=	electron mass
m^*	=	effective mass
n	=	charge carrier concentration
n_0	=	residual charge carrier concentration
N_{CI}	=	density of charge impurities
N_{OP}	=	Phonon occupation
N_{RS}	=	density of resonant scattering
$N_{\mathrm{SPP,i}}$	=	SPP phonon occupation number
N_{sq}	=	number of squares of top-gated area
p	=	momentum
π	=	(*pi*) mathematical constant
q	=	Elementary charge
R_0	=	Effective radius of resonant scattering
R_{j}	=	resistance of the gate-metal junction
R_{channel}	=	channel resistance
R_{contact}, R_{C}	=	contact resistance
R_{D}	=	Extrinsic drain resistance
R_{DS}	=	Extrinsic drain-source resistance
R^0_{gated}	=	Resistance in the gated region without B-field
R^B_{gated}	=	Resistance in the gated region with B-field
R_{DS}	=	Extrinsic drain-source resistance
R^0_{series}	=	Series resistance without B-field
R^B_{series}	=	Series resistance with B-field
R^0_{total}	=	Total resistance without B-field
R^B_{total}	=	Total resistance with B-field
R^0_{ungated}	=	Resistance in the ungated region (access region) without B-field
R^B_{ungated}	=	Resistance in the ungated region (access region) with B-field
σ	=	(*sigma*) conductivity
T	=	Transmission coefficient
τ	=	(*tau*) scattering time
τ_{ch}	=	channel charging delay time
τ_{d}	=	drain delay time
τ_{eff}	=	effective scattering time

τ_{ext}	=	extrinsic delay time
τ_{imp}	=	impurity relaxation time
τ_{int}	=	intrinsic delay time
τ_{pad}	=	delay time due to gate pad capacitance
τ_{th}	=	thermal relaxation time
τ_{tot}	=	total current delay time
τ_{tr}	=	transit time
v	=	Charge carrier velocity
v_{F}	=	Fermi velocity
v_{d}	=	Drift velocity
V	=	Voltage
V_{app}	=	applied voltage
V_{ds}	=	Intrinsic drain source voltage
V_{gs}	=	Intrinsic gate source voltage (*i.e.,* transverse field)
v_{sat}	=	Saturation velocity
v_{peak}	=	Peak velocity
V_{DS}	=	Extrinsic drain source voltage
V_{GS}	=	Extrinsic gate source voltage
V_{GSO}	=	Extrinsic gate source voltage overdrive
V_{GS_0}	=	Extrinsic gate source voltage at zero extrinsic drain source current
V_{T}	=	Threshold voltage
V_{TG}	=	top-gate voltage
W, W_{g}	=	Gate width
$\hbar w_{\text{OP}}$	=	optical phonon energy
Z	=	new charge of impurity (assumed to be 1)
z_0	=	(≈ 0.35 nm) separation between polar substrate and graphene
μ	=	mobility
μ_0	=	low-field mobility (in the thesis and in **Paper B**)
μ_{c}	=	diffusive mobility or collision mobility (μ_0 in **Paper D**)
$\mu_{\text{B(0)}}$	=	electron mobility at low fields
μ_{B}	=	Ballistic mobility
μ_{d}	=	drift mobility
μ_{e}	=	electron mobility
μ_{eff}	=	effective mobility
μ_{FE}	=	field-effect mobility
μ_{gMR}	=	mobility from geometric magnetoresistance
μ_{H}	=	Hall mobility
μ_{imp}	=	impurity dependent mobility
μ_{th}	=	thermal dependent mobility
θ	=	(*theta*) angle of rotation in degrees
ϕ	=	(*phi*) angle of deflection

Thesis

1 Introduction

This introductory chapter will briefly describe the main theoretical concepts and previously published discoveries related to the behavior of transistors based on high electron mobility materials in a magnetic field (B).

It is crucial in today's most sensitive detection systems to read out tiny microwave signals with the highest achievable accuracy. A high-electron-mobility transistor (HEMT) is a critical device in many of these read-out systems. The HEMT is usually included as an active component of an LNA. Some of these systems also rely on the presence of a strong B-field, *e.g.*, in mass spectrometry [1] or detection of dark matter, *e.g.*, in the first results from the HAYSTAC axion search [2, 3]. Magnetic resonance imaging (MRI) is another potential application for cryogenic LNAs in a B-field and is of immense importance in medical diagnostics [4]. It has long been known that the sensitivity of the cryogenic LNA is affected by the presence of a B-field: When aligned perpendicular to the B-field, the noise temperature of a cryogenic AlGaAs-GaAs (GaAs) HEMT LNA was shown to be degraded with increasing B-field [5, 6]. However, reports on the electrical behavior in a B-field for the cryogenic InGaAs-InAlAs-InP (InP) HEMT LNA - the standard component used in today's most sensitive microwave receivers – have so far been absent.

For current transport in a B-field, it is well known, already since 1879, that the Hall effect occurs when applying a B-field in the electric characterization of conducting materials. When a charged particle travels with a velocity in a perpendicular B-field, it will experience a force known as the Lorentz Force, giving rise to the Hall effect [7]. For the Hall effect to occur in a sample, the structure must be longer or equal to its width ($L \geq W$). In the case where the sample structure is much wider than its length ($L << W$), another phenomenon called the geometrical magnetoresistance (gMR) effect occurs. Looking at the geometry of a HEMT layout, with gate length L_g << gate width W_g in a B-field, it is clear that gMR will also occur here.

Measurements of gMR can be used to extract the mobility (μ) of a transistor, as in Ref [8], without the influence of series resistance effects. Another example of μ-extraction using gMR measurements can be found in Ref. [9], where a sub-100 nm n-type metal-oxide-semiconductor field-effect transistor (MOSFET) device was investigated in a B-field up to 10 T. The μ could be measured independently of the charge carrier concentration (n), and the results strongly depended on the geometry of the current flow. The gMR effect is relatively small in low-μ silicon-based field-effect devices [8]; hence very high B-fields are required. In contrast, III-V HEMT devices such as GaAs and InP HEMTs exhibit large gMR already at 1 T [10]. A GaAs HEMT was used in an experiment published in 1997, examining a cryogenic GaAs HEMT low-noise amplifier (LNA) in a B-field [5]. Their investigation was conducted by measuring the LNA, and no data on the actual transistor was shown. When exposed to a B-field, the InP HEMT cryogenic LNA degradation can only be understood by measuring the individual InP HEMT at low temperatures. The effect of a strong static B-field on the dc characteristics of a HEMT alone has never been reported before.

For many scientific and future commercial applications, μ is an important figure of merit (FOM). Commonly a test structure is fabricated to obtain μ, *e.g.*, via hall measurements. However, such measurements can give an incomplete picture of the expected performance of an actual device. Compared to creating a test structure, the fabrication and contacting of an actual device are more destructive. The final device will unlikely represent the initial state of the unprocessed heterostructure or film. Therefore, another approach to obtaining true μ in a device would be preferable for electronic applications, such as the gMR method.

Future development in modern electronics relies on progress made with novel two-dimensional materials, which have cutting-edge performance. Here graphene is a promising candidate. Due to the high μ in graphene, 100 000 cm^2/Vs for a single layer at room temperature [11], much faster electronics would be possible compared to traditional semiconductors possibilities, but also to understand the phenomena occurring when scaling down reaches a limit an no longer improves the performance. Despite the excellent properties of graphene, there are still a lot of challenges and unknowns related to how we can benefit from and take advantage of these properties in an actual device without a significant reduction in performance. A criterion for graphene to compete with existing technology is the possibility of scaling down devices while maintaining high performance. During the fabrication processing of a graphene device, charged impurities are introduced in the substrate, *e.g.*, created by the diffusion of metallic ions present in the solvents or etching solutions used [12], which can significantly reduce μ due to the associated long-range Coulomb-scattering centers [11, 13]. When impurities are present, they often ionize and can form centers of charge scattering. It will result in further degradation of mobility.

To conclude, the thesis aims to clarify the charge carrier transport mechanisms in the FETs with two-dimensional electron gas (2DEG) channels. In turn, this allows for the development of state-of-the-art transistors and devices for advanced electronics applications in the emerging areas of high-speed communication, quantum computing, terahertz sensing, imaging, etc. The gMR effect in the HEMTs and GFETs was used as a powerful tool to study and analyze the charge carrier transport mechanisms effectively.

The thesis is organized as follows: Chapter 2 introduces concepts and theory regarding the charge transport in field-effect transistors (FETs) with two-dimensional electron gas (2DEG) channels, such as scattering mechanisms, velocity overshoot, and velocity saturation in HEMTs and GFETs

Chapter 3 contains descriptions of the layouts and fabrication of HEMTs and GFETs for advanced cryogenic low noise and high-frequency applications, respectively, and the specific considerations made. The minute details of microfabrication recipes have been relegated to Appendix A and B. This chapter also presents the technology of encapsulating graphene by hBN layers developed at Stanford University, which includes dividing graphene flakes via ripping/tearing, anodic oxidation or laser cutting prior to stacking graphene with hBN layers.

Chapter 4 discusses models and methods for evaluating various transistor parameters, *e.g.*, μ, series resistance, and drift velocity. It also presents the experimental setups and procedures for measuring dc characteristics.

Chapter 5 discusses the experimental results related to studying the charge carrier transport in the measured devices using the method of geometrical magnetoresistance. Here angular dependence of dc characteristics on the B-field is presented, and the phenomena of physical and geometrical magnetoresistance. This chapter also contains results on GFETs when scaling down the gate lengths to submicron size and the transmission probability approximating the quasi-ballistic transport contribution.

Chapter 6 presents a summary of the appended papers, followed by Chapter 7, providing an outlook for the future.

In Appendix A and B, a detailed microfabrication recipe for InP HEMTs and GFETs, respectively, can be found. Appendix C presents an error and reliability study related to **Paper B** and **Paper C**.

At the end of the thesis, **Paper A, B, C** and **D** are appended.

2

Charge carrier transport in field-effect transistors with 2DEG channels

This chapter reviews the charge carrier transport and scattering mechanisms in semiconductors, specifically in the 2DEG FETs. Furthermore, the scattering mechanisms governing the charge carrier transport observed in the HEMTs and GFETs studied in the appended papers are discussed. The Coulomb scattering, resonant scattering (RS), and scattering by substrate surface polar phonons (SPP), typical for GFETs at low fields, and the carrier velocity saturation by remote optical phonons (OPs) governing the carrier transport in GFETs at high fields, are considered. The low-field scattering mechanisms, typical for HEMTs, including scattering by alloy disorder, polar OPs, ionized impurity, interfacial scattering, and screening of the Coulomb potential, are reviewed.

The velocity peak phenomena in the InGaAs/InP HEMTs at high fields are analyzed, mainly using the model of the electron quantization and subband formation caused by the transverse field.

2.1 Intrinsic mobility in 2DEG of HEMTs and GFETs

The main similarities and differences in mobility phenomena in the 2DEG of HEMTs and GFETs are here discussed. Both HEMTs and GFETs exploit the 2DEG as the transistor channels, *i.e.*, an electron gas with charge carriers that are free to move in two dimensions but tightly confined in the third one. Both HEMTs and GFETs benefit, at least, potentially in the case of GFETs, from their superior intrinsic carrier mobility and velocity for emerging and advanced applications *e.g.* in high-frequency electronics. However, the origin and nature of the high intrinsic mobility in HEMTs and GFETs are essentially different and not related directly to the 2DEG properties. In the HEMTs, the formation

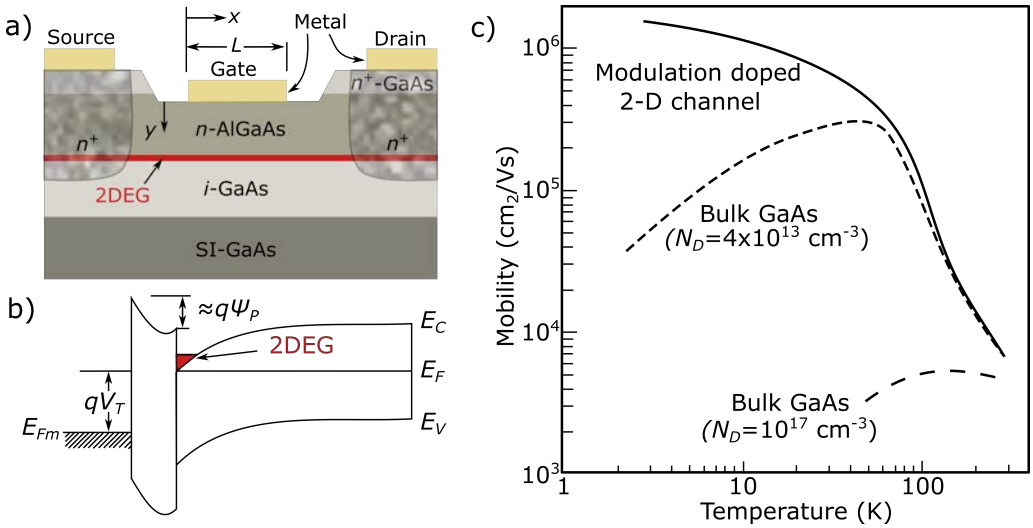

Figure 2.1: *a) Typical structure of an HEMT, using the basic AlGaAs/GaAs system. b) Energy-band diagrams for an enhancement-mode HEMT at onset of threshold. c) Comparison of low-field electron mobility of modulation-doped 2-D channel to bulk GaAs at different doping levels. (Modified Fig. from Ref. [14], p.402-403)*

of the 2DEG channel is used just as a tool for spatial separation of the channel from the doped regions allowing for minimizing associated impurity scattering and, hence, resulting in effective mobility enhancement. Fig. 2.1 a) shows the typical structure of a HEMT using the basic AlGaAs/GaAs system. Considering the electrons transferring from the doped AlGaAs barrier to the undoped GaAs, a triangular quantum well with the 2DEG is formed at the heterointerface, as shown in Fig. 2.1 b), which is locally separated from the doped region thus mitigating the effects of direct impurity scattering. Fig. 2.1 c) compares the low-field electron mobility in HEMTs (Modulation-doped 2D channel) with bulk GaAs at different doping levels. At cryogenic temperatures, the mobility in HEMTs can be above 10^6 cm^2/Vs, which is approx. ≈ 2 orders of magnitude more than in bulk GaAs.

The intrinsically high electron mobility in graphene, up to 2×10^5 cm^2/Vs at room temperature, is not associated directly with the 2DEG but arises from the effective masslessness of electrons in the Dirac band structure and relatively larger relaxation time. Explanations of high electron mobility in graphene usually invoke seminal work [15] which has demonstrated that the electron transport in graphene is governed by the Dirac equation, with the charge carriers acting like relativistic particles with zero rest mass. Unlike the parabolic-band semiconductor (Fig. 2.2 a), the Dirac band structure holds a linear dispersion relation $E = v_\mathrm{F} p$, (see Fig. 2.2 b) equivalent to a constant electron speed $v = \frac{\partial E}{\partial p} = v_\mathrm{F}$, which is independent of the momentum (p). Here, the Fermi velocity of graphene, *i.e.*, the velocity of electrons at the Fermi energy up to which states are filled with electrons [16], is $v_\mathrm{F} = 8.3 \times 10^5$ m/s. In the relativistic picture, linear dispersion

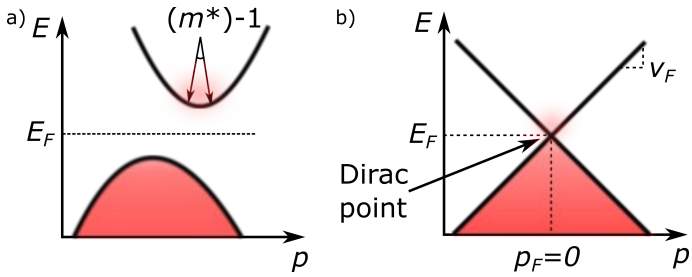

Figure 2.2: *a) Schematic band structure of a parabolic-band semiconductor and b) undoped graphene, with band velocity (E vs p slopes) and effective mass (inverse E vs p curvature) annotated. The shading denotes the Fermi occupation factors of electrons. (First published in Ref. [18], Copyright ©2019, AIP Publishing).*

corresponds to massless carriers since $E^2 = (mc^2)^2 + (pc)^2$ for a particle of mass m reduces to $E = pc$ when $m = 0$. However, this analogy obviously does not apply for graphene since the electrons in graphene have a constant velocity $v_{\mathrm{F}} \approx 8.3 \times 10^5$ m/s$\sim c/400$, instead of the speed of light c [17]. Recently, an alternative approach was presented for derivation and explanation of the unusual effective mass and mobility in graphene using only basic concepts from semiconductor theory and the linear band structure of graphene [18]. In this approach, the effective electron mass in graphene can be expressed as [18]

$$m^* = \frac{4\ln(2)k_B T}{v_{\mathrm{F}}^2}, \tag{2.1}$$

where T is temperature and k_B is Boltzmann's constant.

Table 2.1 (from Ref. [18]) compares the typical effective masses m^*, momentum relaxation time, and mobility of electrons in a prototypical metal (silver), semiconductor (silicon), and both doped and undoped graphene. The values for silver and silicon are based on experimental measurements, while that for graphene is based on derivation. It can be seen that the relative effective mass of the electron in graphene is ≈ 10 times lower, and relaxation time is ten times larger than in Si, which results in 100 times larger intrinsic mobility.

Table 2.1: Comparison of typical relaxation time, effective mass, and electron mobility for metals, semiconductors, doped graphene and (undoped) graphene at room temperature. (First published in Ref. [18], Copyright ©2019, AIP Publishing)

Material	τ (fs)	$m*/m_{\mathrm{e}}$	μ (cm^2/V·s)
Silver	30	1.0	50
Silicon	200	0.26	1400
Graphene with $E_{\mathrm{F}} = 0.1$ eV	700	0.063	2×10^4
Undoped graphene	2000	0.018	2×10^5

2.2 Low-field scattering mechanisms in HEMTs at cryogenic temperatures

The low-field scattering mechanisms and associated effects in a 2DEG are here considered with a focus on phenomena in HEMTs at cryogenic temperatures, *i.e.* devices, and conditions related to LNA applications. Comprehensive analysis and modeling of the relevant low-field scattering mechanisms were published in Ref. [19] by the example of the 2DEG confined in the channel region of the InGaAs/InAlAs heterostructures in the temperature range from 15 K to 300 K. Fig. 2.3 a) shows the results of numerical calculations of the temperature dependence of electron mobility together with experimental data obtained by Hall effect measurements. It can be seen that below ≈ 100 K, the charge carrier transport is defined by the combined effect of the alloy disorder, ionized impurity, and interface roughness scattering. The interface roughness scattering has a minor contribution compared to the scattering by ionized impurities and alloy disorder. The phonon scattering can be neglected.

At low temperatures, ionized impurity scattering can play an important role in limiting the mobility of HEMTs. In particular, it can be associated with the scattering by unintentional donors in the channel and unintentional donors at the channel interfaces [21]. The significant contribution of the ionized impurity scattering in HEMTs manifests via the accompanying screening effect. Fig. 2.3 b) shows dependencies of the electron drift mobility (μ) of the 2DEG in the channel of HFETs on gate voltage (V_G). The rise in μ_d with increasing V_G can be accounted for by stronger screening of the scattering by ionized impurities and dislocations in the 2DEG. Similar dependencies

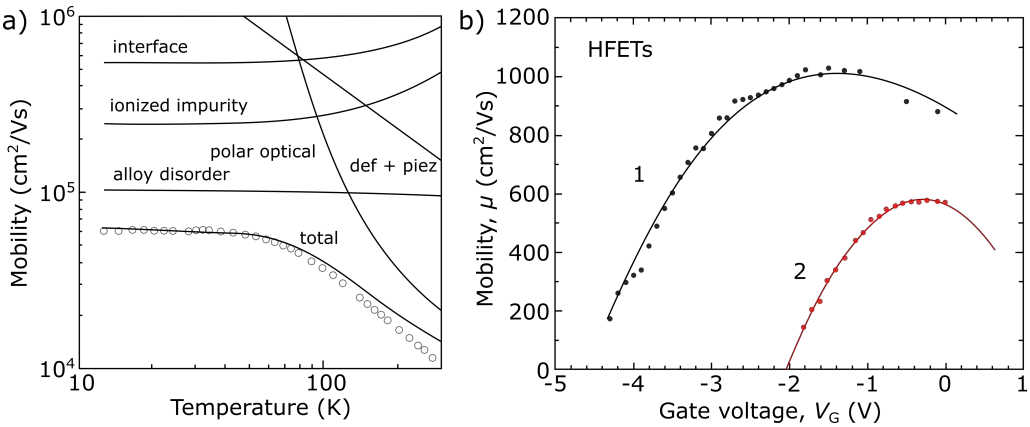

Figure 2.3: *a) Results of numerical calculations of temperature dependence of electron mobility, together with experimental data obtained by Hall effect measurements (closed circles). (First published in Ref. [19], Copyright ©Semiconductor Science and Technology 2003, Institute of Physics Publishing.) b) Dependences of the electron drift mobility of the 2DEG in the channel of HEMTs (HFETs) on gate voltage. (First published in Ref. [20], Copyright ©IOP Publishing on behalf of the Japan Society of Applied Physics (JSAP))*

were reported in Refs. [22] and [23]. In **Paper B**, the observed increase of the low-field mobility with the carrier concentration is also explained by an increased screening of the Coulomb potential of the ionized impurities responsible for the carrier scattering. It can be seen from Fig. 2.3 b) that with V_G increasing further, the μ starts to decrease. This decrease can be attributed to a spillover of electrons from the 2D-channel to a parallel low electron-drift-mobility 'parasitic conduction channel' [20]. Since the channel region of InGaAs/InAlAs consists of a ternary random alloy of InAs and GaAs, electrons in the channel are scattered by the alloy disorder potential, shown to be dominant at low temperatures [19].

2.3 Charge carrier velocity peak in HEMTs

Theoretically, charge carrier transport in bulk InGaAs has been studied using models for GaAs [24]. However, for the InGaAs/InP HEMTs, particularly at cryogenic temperatures, there is an apparent lack of theoretical and experimental studies, where no previous work on v has been published. Though, Ref. [25] presents an evaluation of the electric field-dependent drift velocity in the ultra-thin films of $In_{0.53}Ga_{0.47}As$ at room temperature using Monte Carlo simulations. Fig. 2.4 a) shows electron velocity versus electric field curves in trap-free $In_{0.53}Ga_{0.47}As$ an ultra-thin film with 4 nm quantum well, demonstrating the importance of the different scattering mechanisms. It can be seen that without the effects of screening and surface roughness scattering (SRS), the model reveals a velocity peak comparable with that in the bulk material. In Ref. [25], formation of the peak was associated with two main effects: i) the transfer of electrons from the Γ-valley with low effective mass and high drift velocity to L-valleys with high effective masses and low drift velocity and (ii) the increase of the scattering probability of carriers at a high electric field. In case ii), the increase of scattering rates leads to a randomization of the carrier direction, which reduces the drift velocity and, therefore, the appearance of the velocity peak. It was found that the velocity peaks in InAs would also manifest in the case of a single sub-band (*i.e.*, no intervalley carrier transfer) and without including any satellite valley, just because the group velocity saturates. At the same time, the scattering rates increase with the electric field.

Paper B reports on the first experimental observation of the peak of the carrier velocity in InGaAs/InP HEMTs using the gMR effect. Fig. 2.4 b) (from **Paper B**) shows the effective drift velocity (v) and the corresponding intrinsic transit frequency (f_T) as a function of intrinsic drain field (E) for different intrinsic gate-source voltages (V_{gs}). The peak velocity (v_{peak}) and corresponding field (E_{peak}) appears to be strongly dependent on V_{gs}, *i.e.*, transverse field, where both v_{peak} and E_{peak} are decreasing with increased V_{gs}. The velocity overshoot indicates that v and E are distributed along the channel [26]. The observed decreases in v_{peak} and E_{peak}, with the intrinsic gate voltage (see Figs. 4 and 5 in **Paper B**), are most likely associated with the electron quantization and subband formation caused by the transverse field. In the electron quantization model, the subband energies are proportional to the transverse electric field [27–30]. Therefore, a change in the proportion of carriers in the upper valleys can be expected, which, due to the band structure of InGaAs, exhibit a higher effective mass at higher energies and subsequently

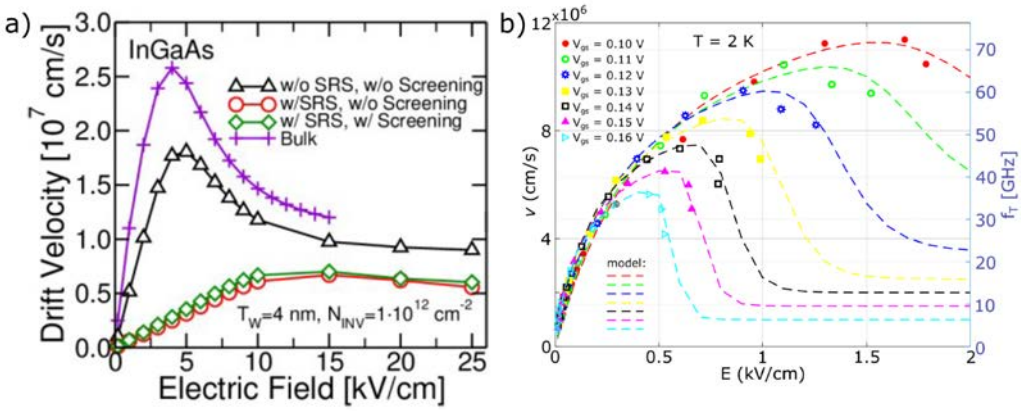

Figure 2.4: *a) Importance of the different scattering mechanisms. The bulk case is shown for reference. (Fig. and caption from Ref. [25] ©2017 IEEE) b) Effective drift velocity (v) and corresponding intrinsic transit frequency (f_T) versus intrinsic drain field (E) at different intrinsic gate voltages (V_{gs}), at 2 K. The lines represent dependencies calculated using Eq. (2.2). (From* ***Paper B****. ©2022 IEEE. Reprinted, with permission, from I. Harrysson Rodrigues and A. Vorobiev, "Low-Field Mobility and High-Field Velocity of Charge Carriers in InGaAs/InP High-Electron-Mobility Transistors," in IEEE Transactions on Electron Devices, vol. 69, no. 4, pp. 1786-1791, April 2022, doi:10.1109/TED.2022.3147733* `https://ieeexplore.ieee.org/document/9714140`*.)*

a corresponding decrease in v, with higher gate voltages. Extrapolation of dependencies in Fig. 2.4 b) down to $V_{gs} - V_T = 0$ points to a peak velocity as high as 2.7×10^7 cm/s with a peak field up to 4.4 kV/cm, which corresponds well with the simulated values for ultra-thin InGaAs films in Ref. [25]. The analysis in Ref. [24] shows that v-models developed for bulk GaAs do not accurately reproduce the shape of the dependencies and significantly overestimate the velocity. Instead, a more accurate correlation can be obtained as in **Paper B**

$$v = \frac{\mu_0 E + v_{sat}\left(\frac{E}{E_T}\right)^k}{1 + \left(\frac{E}{E_T}\right)^k + a\left(\frac{E}{E_T}\right)} \tag{2.2}$$

where the saturation velocity (v_{sat}), low-field mobility (μ_0), transfer field (E_T), and coefficients k and a are fitting parameters. The dashed lines in Fig. 2.4 b) represent v calculated using Eq. (2.2) for different V_{gs}.

2.4 Low-field scattering mechanisms in GFETs

The effects of imperfections on low-field dc graphene properties, and corresponding scattering mechanisms, have been extensively studied experimentally [31–35] and theoretically [36–39] and are currently well understood. For comparison, $\mu > 10^5$ cm^2/Vs and micrometer electron mean free path (λ) have been measured in suspended graphene

or graphene encapsulated between hBN layers. However, much lower μ values, below 10^3 cm^2/Vs, are typically reported in graphene on common substrates, *e.g.*, SiO_2, used for device fabrication [34]. Current electronic transport models in graphene suggest only a few mechanisms that can explain the common experimentally observed proportionality between conductivity (σ) and carrier concentration (n) at low n [34]. Among them, charged-impurities (CI) scattering [39] (or Coulomb scattering) and resonant scattering (RS) [40] are currently considered as the most probable candidates to influence μ and λ. The inhomogeneous distribution of such scattering sources in graphene is responsible for nanoscale lateral inhomogeneities in the electronic properties [34]. The interaction of graphene 2DEG with surface polar phonons (SPPs) of the substrate has been indicated as a strong degradation mechanism for λ in graphene [41]. In Ref. [34], the above scattering mechanisms were studied theoretically and experimentally using scanning capacitance microscopy/spectroscopy. It is assumed that λ obeys Matthiessen's rule as

$$\frac{1}{\lambda} = \frac{1}{\lambda_{\mathrm{RS}}} + \frac{1}{\lambda_{\mathrm{CI}}} + \frac{1}{\lambda_{\mathrm{SPP}}}. \tag{2.3}$$

The CI term λ_{CI} is expressed as [42]

$$\lambda_{\mathrm{CI}} = \frac{16\kappa_0^2\kappa^2\hbar^2 v_{\mathrm{F}}^2}{Z^2 q^4 N_{\mathrm{CI}}}\left(1 + \frac{q^2}{\pi\hbar v_{\mathrm{F}}\kappa_0\kappa}\right)^2\sqrt{\pi n} \tag{2.4}$$

where v_{F} is the electron Fermi velocity in graphene (=1×10^6 m/s), Z is the net charge of the impurity (assumed to be 1), N_{CI} is the CI density, and κ is the average between the permittivity of the substrate κ_{sub} and the vacuum permittivity ($\kappa_{\mathrm{vac}} = 1$).

The RS term λ_{RS} is expressed as [42]

$$\lambda_{\mathrm{RS}}(n) = \frac{\sqrt{\pi n}}{\pi^2 N_{\mathrm{RS}}}[\ln(\sqrt{\pi n}R_0)]^2 \tag{2.5}$$

where N_{RS} is the RS density and R_0 the effective radius of RS, which is commonly assumed as $R_0 \approx 2a$, where $a \approx 0.14$ nm is the bond length in graphene [43].

The λ_{SPP} associated to scattering by a SPP mode with energy E_i is expressed as [44, 45]

$$\lambda_{\mathrm{SPP,i}} = \sqrt{\frac{\beta}{E_i}}\frac{\hbar v_{\mathrm{F}} 4\pi\kappa_0}{q^2}\frac{q v_{\mathrm{F}}}{F_i^2}\frac{\exp(k_0 z_0)}{N_{\mathrm{SPP,i}}}\frac{\hbar\sqrt{\pi}}{q} \tag{2.6}$$

where $\kappa_0 \approx [(2E_i\hbar^{-1}v_{\mathrm{F}}^{-1})^2 + \chi n]^{1/2}$, $\chi \approx 10.5$, $\beta \approx 0.153 \times 10^{-4}$ eV [44], and $z_0 \approx 0.35$ nm is the separation between the polar substrate and graphene. $N_{\mathrm{SPP,\,i}}$ is the SPP phonon occupation number given by the Bose-Einstein statistics. F_i^2 is the Fröhlich coupling constant which gives the magnitude of the polarization field and depends on the substrate permittivity [46].

Fig. 2.5 a) shows the experimental λ versus n (circles) and a fit (red line) at a fixed position in graphene on SiO_2. The λ_{CI}, λ_{RS}, and λ_{SPP} contributions to λ are also shown. Fig. 2.5 b) show the corresponding map of λ, and as a guide for the eye, the positions of representative maxima and minima in the λ map are indicated by green and red circles,

respectively. It can be seen from Fig. 2.5 a) that the CI scattering dominates. The μ can be expressed via λ and n as [34]

$$\mu = \frac{q\lambda}{\hbar(\pi n)^{-\frac{1}{2}}} \tag{2.7}$$

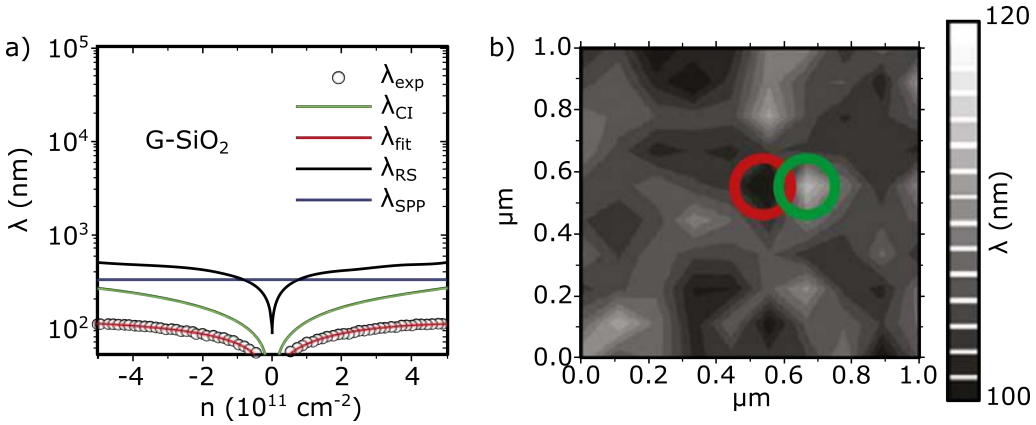

Figure 2.5: *Experimental mean free path vs carrier concentration (circles) at fixed position in G-SiO_2 (a) and to guide the eye, the positions of representative maxima and minima in the λ maps are indicated by green and red circles, respectively, in (b). (Fig. and caption from Ref. [34]. Reprinted with permission from Filippo Giannazzo, Sushant Sonde, Raffaella Lo Nigro, Emanuele Rimini, and Vito Raineri Nano Letters 2011 11 (11), 4612-4618 DOI: 10.1021/nl2020922 https://doi.org/10.1021/n12020922 ©2011 American Chemical Society.)*

Analysis using Eqs. (2.4), (2.5) and (2.6) indicates that the CI scattering is the only mechanism at which μ does not depend on n. This feature is used to distinguish CI scattering from other scattering mechanisms in this thesis work. Additionally, this allows for applying the drain-source resistance model for evaluation of μ using it as a fitting parameter to the experimental transfer characteristics of the GFETs, see Chapter 4 and **Paper D**.

The CI scattering in graphene is described theoretically in a self-consistent theory for graphene transport [36]. Fig. 2.6 a) shows a schematic illustration of this concept. The theory predicts that the product of μ_0 and residual concentration of charge carriers (n_0) is constant, and for graphene on the SiO_2 substrate, $n_0 \times \mu_0 \approx 1.5 \times 10^{15}$ 1/(Vs) [47]. As an example, Fig. 2.6 b), adapted from Ref. [48], shows the n_0 versus the inverse μ_0 of the GFETs located at various positions on the Si chip for 4 different L_g. It can be seen that at mobilities above ≈ 1000 cm^2/Vs, the product $n_0 \times \mu_0$ is close to $1.5{\times}10^{15}$ 1/(Vs). This confirms that the Coulomb scattering dominates. The mobilities below ≈ 1000 cm^2/Vs (data points within the dashed curve area) are reduced, which indicates additional contributions of the other charge-carrier scattering mechanisms, *e.g.*, "short-range" or "resonant" scattering [34, 47].

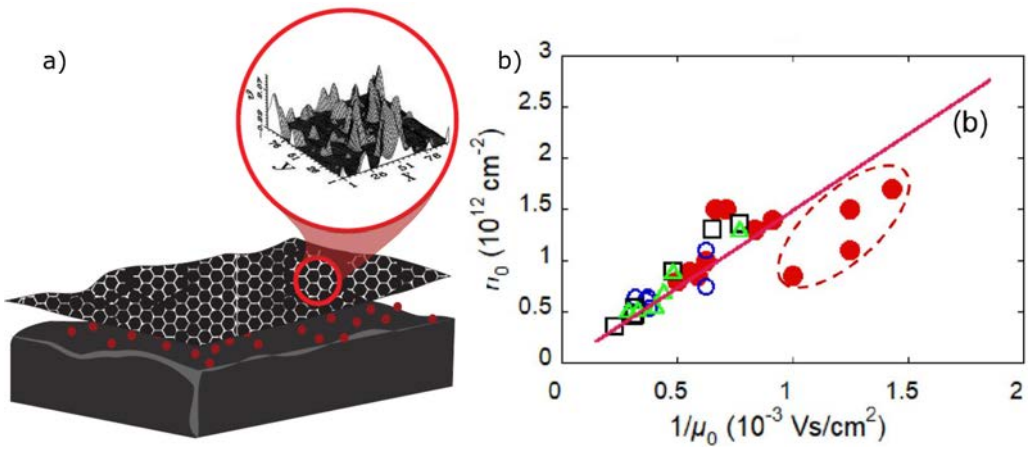

Figure 2.6: *(a) Main panel shows cartoon of the model where charged impurities in the substrate at a distance d away from the graphene sheet create a spatially inhomogeneous screened Coulomb potential. At low carrier density, the system breaks up into puddles of electrons and holes. The inset is used here just to illustrate the voltage fluctuations schematically, where it is understood that the presence of both electron and hole carriers implies that both positive and negative voltages are screened. (First published in Ref. [36]). Residual charge-carrier concentration versus inverse low-field mobility in the GFETs of gate lengths 0.5 μm (filled circles), 0.75 μm (open circles), 1 μm (squares), and 2 μm (triangles), located at different positions on the Si chip. The line corresponds to the product* $n_0 \cdot \mu_0 = 1.5 \cdot 10^{15}\ V^{-1}\ s^{-1}$. *(From Ref. [48]. First published by M. Asad et al., "The Dependence of the High-Frequency Performance of Graphene Field-Effect Transistors on Channel Transport Properties," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 457-464, 2020, doi: 10.1109/JEDS.2020.2988630. Reprinted with CC BY 4.0-permission.)*

2.5 Charge carrier velocity saturation in GFETs

Graphene was proposed and already demonstrated high potential for application as a channel material in advanced GFETs developed for high-frequency applications [49, 50]. However, fully realizing the high-frequency GFETs requires a better understanding of the charge carrier transport mechanism, specifically at high drain fields, which will allow for optimization of design/dimensions and operational conditions. In previous work, the high-frequency performance of GFETs was analyzed using the drift-diffusion theory of charge carrier transport, assuming that the intrinsic (cutoff) transit frequency ($f_{\mathrm{T,int}}$) is limited by v_{sat} as [51–53]

$$f_{\mathrm{T,int}} = \frac{v_{\mathrm{sat}}}{2\pi L_{\mathrm{g}}}. \tag{2.8}$$

It was shown theoretically and experimentally that in the typical GFET structures, v_{sat} is limited by the remote optical phonons (OPs) of the adjacent dielectrics, *e.g.*, SiO_2 of the substrate, which phonon energy is significantly below the 160 meV of the longitudinal

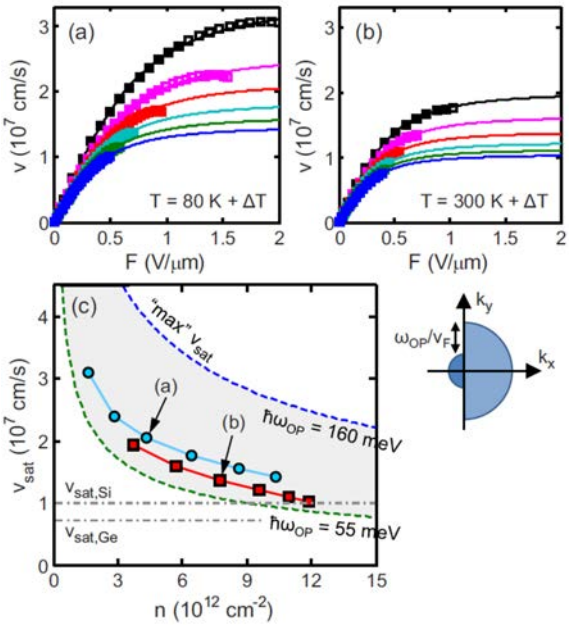

Figure 2.7: *Electron saturation velocity. (a) Background temperature T_0 = 80 K with V_{G0} = 10.5–60.5 V, and (b) T_0 = 300 K with V_{G0} =23.5-73.5 V (in 10 V steps from top to bottom). Squares represent data, lines are empirical fits (c) Saturation velocity vs. electron density at F = 2 V/μm. Side panel shows carrier distribution assumed for analytic model. Dashed lines correspond to $\hbar w_{OP}$=55 meV (SiO_2) and 160 meV (graphene), the latter suggesting the maximum v_{sat} that could be achieved in graphene. (From Ref. [55]. First published by Vincent E. Dorgan, Myung-Ho Bae, and Eric Pop, "Mobility and saturation velocity in graphene on SiO2", Appl. Phys. Lett. 97, 082112 (2010) https://doi.org/10.1063/1.3483130, ©2010 American Institute of Physics.)*

zone boundary phonon of intrinsic graphene [52, 54, 55]. The concept of the μ and v in graphene at high fields was developed and summarized in Ref. [55]. In that work, v was calculated from current measured on four-probe graphene structures on SiO_2 with a highly doped Si substrate as the back-gate. Figures 2.7 a) and b) show the velocity-field relationship at the two background temperatures, indicating saturation tendency at fields F >1 V/μm. Here, v was fitted by

$$v(F) = \frac{\mu F}{[1 + (\mu \frac{F}{v_{sat}})^{\gamma}]^{\frac{1}{\gamma}}} \tag{2.9}$$

where γ=2 provides a good fit. For comparison, a similar model was applied for high-field v in GFETs found using delay time analysis and demonstrated good fitting; however, with γ = 3 [52]. Figure 2.7 c) shows extracted v_{sat} as a function of n [55]. The experimental results were compared with an analytic model, which approximates the high-field distribution with the two half-disks shown in the Fig. 2.7 c) right-hand inset, suggested by previous simulations [56]. This model assumes that v_{sat} is limited by inelastic emission of OPs [55] and leads to

$$v_{sat}(n,T) = \frac{2}{\pi}\frac{w_{OP}}{\sqrt{\pi n}}\sqrt{1 - \frac{w_{OP}^2}{4\pi n v_F^2}}\frac{1}{N_{OP}+1}, \tag{2.10}$$

where $\hbar w_{OP}$ is the OP energy and $N_{OP} = \frac{1}{\exp(\hbar w_{OP}/k_B T)-1}$ is the phonon occupation.

Analysis indicated that both graphene zone-edge OPs and the remote OPs of the SiO_2 substrate play a role in limiting v_{sat}, but that substrate phonons are dominant. Therefore,

for further increasing v_{sat} and, hence, f_T, selecting the dielectric materials with higher phonon energies was suggested [52, 54]. This approach was verified experimentally using encapsulation by hBN, Al_2O_3 buffer layer and diamond substrate in the GFETs resulting in increased v_{sat} and f_T [51, 57, 58]. The approach reaches its limit in the GFETs based on graphene encapsulated by diamond-like carbon (DLC) layers since the DLC surface phonon energy (165 meV) is even slightly higher than that of graphene [59]. Finally, it should be noted that recent studies in this thesis work, presented in **Paper D** indicate that the above analysis and conventional relationship between the f_T and L_g, *i.e.*, derived using the drift-diffusion theory, might not be valid for GFETs with relatively short L_g (below ≈ 1 μm) due to contribution of the ballistic mode in the charge carrier transport. In particular, in the purely ballistic mode, the v_{sat} in the above relationship should be replaced by v_F or virtual source injection velocity [60, 61].

3

Design and fabrication of state-of-the-art HEMTs and GFETs

This chapter presents aspects of the design, layout, and fabrication of InGaAs/InP HEMTs and GFETs developed for advanced low-noise and high-frequency applications. The focus will be on the details and specifics of layouts and fabrication flow steps developed at Chalmers University of Technology and applied for fabrication of the HEMTs, and GFETs reported in the appended papers. Additionally, this chapter presents the technology of encapsulating graphene by hBN layers developed at Stanford University, which can be used in GFETs with extremely improved high-frequency performance.

3.1 Design and layouts of HEMTs for advanced low noise applications

A generic process flow was followed for fabrication of the InP HEMT devices used in this work, where a more detailed list of the fabrication recipe can be found in Appendix A. All fabrication steps were performed in a cleanroom facility[1].

A conventional top-down approach has been used, relying on the patterning of thin films via planar lithography and wet etching of an InP-based heterostructure. The heterostructure used in this thesis is presented in Fig. 3.1. It has previously been shown to give excellent transistor performance [62] and was, therefore, the material of choice for this study. The barrier was thin enough to permit modulation of the transistor current in a 100 nm L_g technology. Shown in Fig. 3.2 are scanning electron microscopic images

[1] Laboratory size: 1000 m^2, Fed. Std.209 E Class: 10-100, ISO 14644-1 Class: 4-5

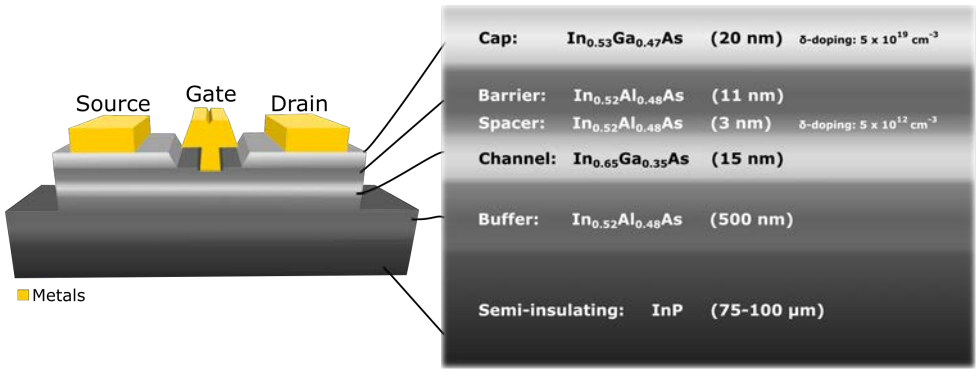

Figure 3.1: *InP HEMT investigated in this thesis where the active channel was a 15 nm thin* $In_{0.65}Ga_{0.35}As$.

of a dual-gate-finger device and a zoomed-in view on the cross-section of the gate area, where the metal contacts are highlighted in yellow, and L_g is indicated with an arrow. At the same time, the barrier was thick enough to suppress gate leakage current, which is well-known to be detrimental to the noise figure in the InP HEMT LNA. The channel, show in Fig. 3.3, contained 65 % of indium. The buffer was 500 nm thick, which was twice the value used in [62]; however, this is judged not to influence the active part of the device. The 4-inch wafers were purchased from an epitaxy foundry, growing the material using molecular beam epitaxy.

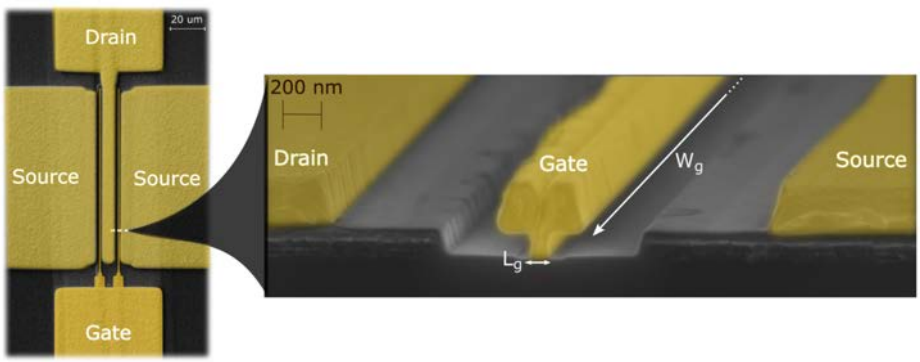

Figure 3.2: *Scanning electron microscopic images of a dual-gate-finger device and a zoomed-in view on the cross section of a gate area, where the metal contacts are highlighted in yellow.*

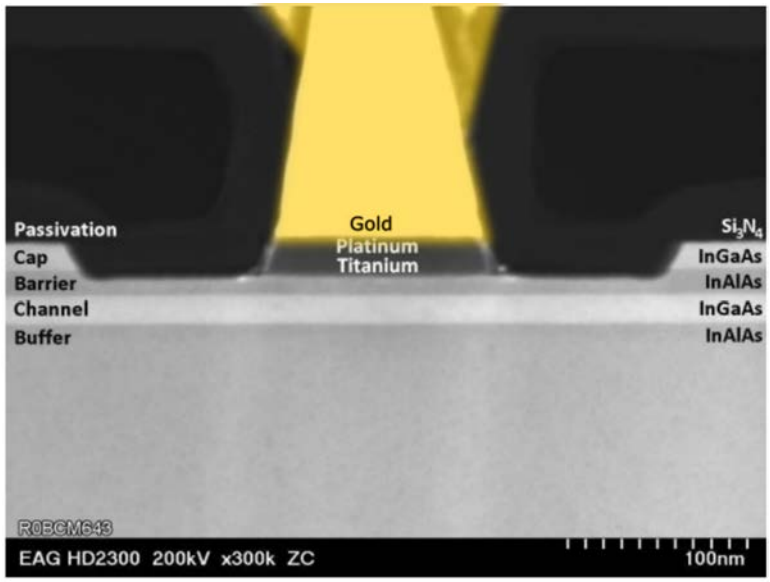

Figure 3.3: *Modified cross sectional STEM image of the gate region of the 130 nm InP HEMT developed in Ref. [63].*

3.2 Fabrication of low noise InP HEMTs

The most critical parts of the InP HEMT fabrication are to achieve a low access resistance, a selective gate recess etching, and a T-gate process. As for this thesis, a brief schematic illustration of a process flow can be seen in Fig. 3.4.

Below is a description of the most critical fabrication steps, i)-v), whereas the complete recipe details can be found in Appendix A. Device fabrication started with preparing a substrate, a 17 mm x 17 mm chip, which was diced from a 4-inch wafer with an InGaAs-InAlAs-InP heterostructure, followed by a cleaning process. i) **MESA**: Creating the mesa was done by wet etching of the InGaAs and InAlAs layers in a solution of H_2O_2:H_3PO_4:H_2O (1:1:25), to electrically isolate the individual devices from the other ones on the same chip or wafer. The mesa was prepared using laser lithography, chemical wet etching, and photoresist stripping. The mesa was verified to have the specified height of 80-110 nm using a surface profilometer. ii) **source** & **drain contacts**: Forming the source and drain ohmic contacts was done through electron-beam lithography, oxide removal, and metal deposition of the combination Ni-Ge-Au, followed by lift-off and rapid thermal annealing. The rapid thermal annealing was done to create a metal alloy, optimizing contact resistance. The transmission line method (TLM) was then used to measure the contact resistance, with a typical value around 0.03 Ω·mm at 300 K. iii) **Gate contact**: The different gate geometries were determined by design in the AutoCAD mask exposed during the gate electron beam lithography. Several dose tests were performed to make the actual gate as similar as possible to the drawn gate. After the exposure, the

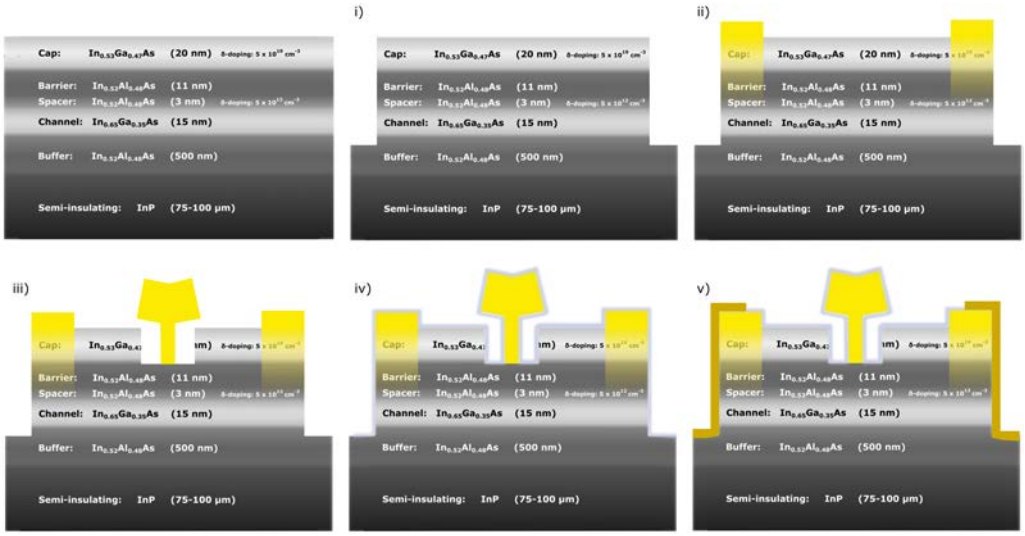

Figure 3.4: *Schematic of fabrication processes for the InP HEMT.*

gate recess was done, and oxide removal and metal deposition created the physical gate after a final lift-off step. The gate material used was titanium, platinum, and gold. iv) **Passivation**: All samples were passivated with a layer of 60 nm thick Si_3N_4 through thin film deposition to protect the surface of the samples and prevent contamination in the sensitive gate area. The passivating layer had to be removed above the contacts, which was done with laser writing, wet etch, and photoresist stripping. v) **Pad metalization**: Larger pads, for improved adhesion when contacting, were then added through laser lithography, oxide removal, metal deposition, and the last lift-off. Both one- and two-finger device layouts were fabricated, with W_g ranging from 20 to 200 μm (2x10 to 2x100 μm) and L_g from 60 to 250 nm.

3.3 Design and layouts of GFETs for advanced high-frequency applications

The GFETs in this work were developed and optimized for high-frequency performance using the formation of planar top gates in a dual-gate-finger design to minimize the parasitic gate-source and gate-drain capacitances. Fig. 3.5 shows an SEM image of such a device. Typical FOMs for characterizing high-frequency performance of RF FETs are f_T and maximum frequency of oscillation (f_{max}). These FOMs can be expressed using small-signal equivalent circuit models, such as the one presented in Ref. [14]. To achieve high FOMs, the conditions important to consider for high-frequency GFETs are well described in Ref. [57], with the same design as in this work.

When analyzing Eq. (3.1) and (3.2) in Ref. [57], it is clear that the high frequency aspects of the GFET design put the following requirements. i) The relatively large gate

width and two gate fingers should be used to minimise effects of the pad capacitances. ii) The top gate configuration should be used with the aim to minimise the parasitic gate-source and gate-drain capacitances. iii) In the planar gate technology, rather thick gate electrode of 0.3 μm Ti/Au should be used to minimise the limiting effect of the gate resistance on extrinsic f_{max}. iv) The ungated regions should be as short as possible to minimise the effect of the total series resistance. It should be noted here, that the lowest limit achievable by the e-beam lithography (ungated region of ≈ 100 nm) has been reached in the current process flow (see Fig. 3.5 for region indication). To further reduce the access area and related resistance, a self-aligned gate technology could be a possible solution.

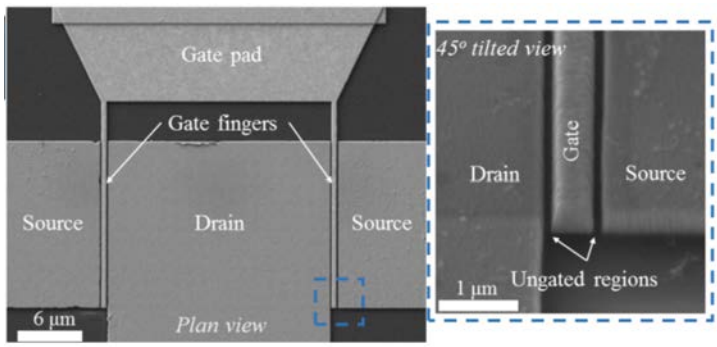

Figure 3.5: *(a) SEM image of a GFET. (b) Magnified and 45° tilted view of the gate area in (a) corresponding to the dashed line box. (From Ref. [48]. First published by M. Asad et al., "The Dependence of the High-Frequency Performance of Graphene Field-Effect Transistors on Channel Transport Properties," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 457-464, 2020, doi: 10.1109/JEDS.2020.2988630. Reprinted with CC BY 4.0-permission.).*

3.4 Fabrication of high-frequency GFETs

Since the GFET technology is still immature, the quality of the materials is relatively more crucial. In addition to highlighting the importance of using high-quality clean graphene, it is just as essential to keep it preserved throughout the entire fabrication process, avoiding contamination and maintaining its inherent properties to achieve optimal performance.

The processing steps developed for state-of-the-art GFETs are similar to that described in Ref. [48] and are presented in detail in Appendix B. Below, the four main distinguishable stages of the GFET fabrication are reported [48]. In stage (i), via the *Easy Transfer* approach [64], a transfer of the chemical vapor deposition (CVD) graphene film is done onto a silicon/silicon oxide (Si/SiO_2) substrate with high resistivity, where the SiO_2 had a thickness of 1 μm. Subsequently, the first layer of the gate dielectric is made, where the transferred graphene film is covered by an ≈ 8 nm thick Al_2O_3 layer.

The layer is created by a six-time repetition of the process of depositing 1 nm thick Al film and oxidizing it on a hotplate at 160° C for 5 min. In this technology, the first gate dielectric layer encapsulates graphene in the transistor channel, which prevents contamination during further processing, thereby reducing the concentration of impurities at the graphene/gate dielectric interface. In stage (ii), the graphene/dielectric mesa and, subsequently, the openings in the Al_2O_3 layer for the drain/source contacts are patterned by e-beam lithography. The drain/source contacts are formed by deposition of 1 nm Ti/15 nm Pd/250 nm Au layered structure and using a standard lift-off process. In stage (iii), a second gate dielectric layer is formed, now by a ten times repetition of the deposition of the 1 nm thick Al film and its oxidation, as previously described. The second gate dielectric layer becomes ≈ 14 nm thick, resulting in a total gate dielectric thickness of ≈ 22 nm. The second dielectric layer covers the graphene edges exposed at the mesa sidewalls and prevents short-circuiting by the overlapping gate fingers. In stage (iv), via e-beam lithography, the gate electrodes/contact pads and the drain/source contact pads are fabricated. Using e-beam evaporation depositing 10 nm Ti/290 nm Au, followed by a lift-off process, finally constituted the electrodes.

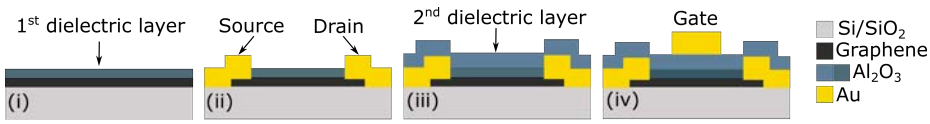

Figure 3.6: *Main steps of the GFET fabrication. (i) Formation of the 1st dielectric layer, (ii) patterning of the dielectric/graphene mesa nd formation of the source and drain contacts, (iii) deposition of the 2nd dielectric layer, and (iv) formation of the gate electrodes and source, along with the drain contact pads. Labels S, D and G indicate source, drain and gate electrodes, respectively.*

3.5 Fabrication of hBN encapsulated graphene stacks

Obtaining a high saturation velocity in graphene is vital for practical applications, especially in radio frequency amplifiers [65] and high-current graphene interconnects [66]. However, the intrinsic transit frequency of a transistor is limited by the saturation velocity, which is an issue that could be addressed by encapsulating graphene with hBN. Encouraging values of saturation velocities have been reported at room temperature in graphene in contact with hBN and SiO_2 substrates [55] and velocities approaching the Fermi velocity in graphene have been estimated in suspended samples [67]. There are many good reasons for using hBN as a candidate substrate to enhance graphene saturation velocity: its surface optical phonon (OP) energy, high thermal conductivity, increased mobility, and greater Fermi velocity, which are further described in Ref. [51], where they investigate high-field electric transport behavior in high-mobility graphene encapsulated by hBN. Stacking two graphene sheets at a specific angle can result in a moiré superlattice, which can be superconducting. Ref. [68] presents that researchers have found superconductivity in four- and five-layer graphene moiré stacks.

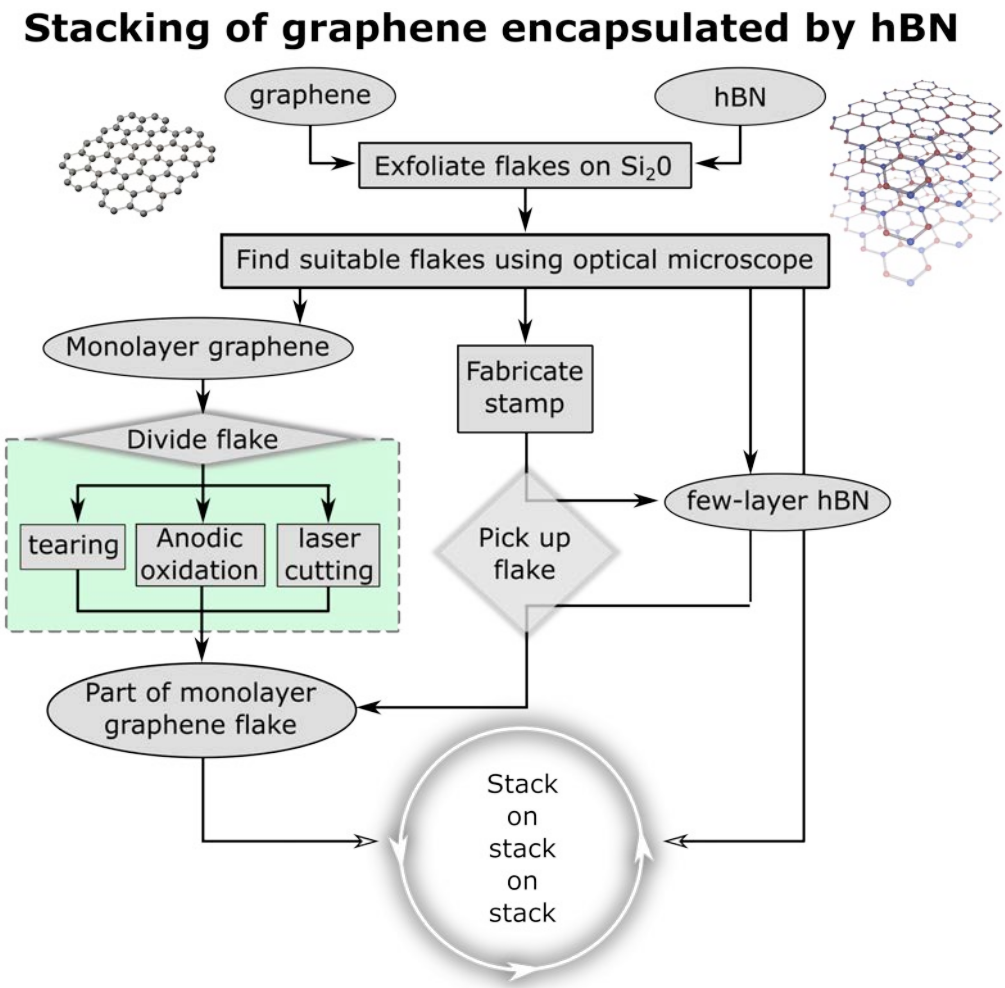

Figure 3.7: *Flowchart presenting steps in the fabrication of moiré heterostructures, based on graphene encapsulated by hBN, from exfoliation to multi-stacking.*

The increasingly demanding development in today's technology and electrical components requires increasingly delicate processes to keep the quality of materials at a continued high level, specifically for enabling groundbreaking research. Fig. 3.7 shows a flowchart of different paths one can take from exfoliation to a stack of the desired combination, which is the step before a device can be completed with electrodes for measurements.

The technology of encapsulating graphene by hBN layers developed at Stanford University, including dividing graphene flakes via ripping/tearing, anodic oxidation, and laser cutting, was characterized mainly via atomic force microscopy (AFM). Both hBN

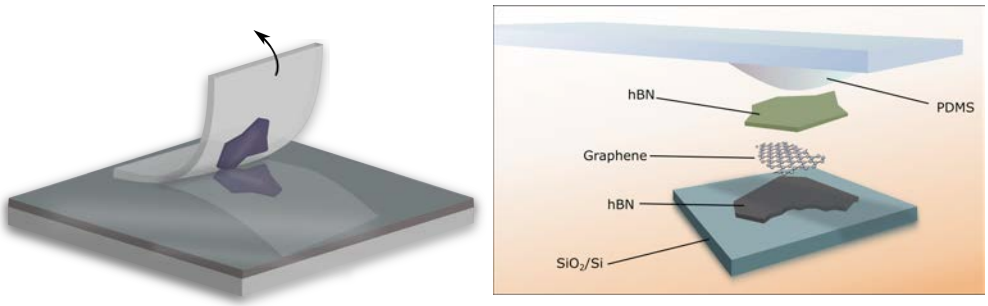

Figure 3.8: *Schematic illustration of exfoliation using the scotch tape method (left) and encapsulation of graphene using the stacking method with PDMS-stamp (right).*

and graphene stacks were further investigated through piezoelectric force microscopy (PFM), finding moiré patterns. The hBN encapsulated graphene can be used in GFETs with extremely improved high-frequency performance. However, to eventually build graphene-based components aimed at industry, a controlled and reproducible process is needed to create the desired amount of devices with correct geometry and high-quality graphene on an industrial scale.

Usually, graphene is grown via CVD, but it is also possible to directly exfoliate graphene from graphite crystals, which is often the first step in fabricating a graphene device for research. Fig. 3.8 a) illustrates this relatively simple process; to exfoliate a monolayer of graphene using scotch tape. There are many discussions about the angle and speed of exfoliation, as well as at what temperature and with what material/tape is optimal for exfoliation, but there are no clear or concrete guidelines. It can help to warm the tape before exfoliation to avoid residues and to ensure that a proper van der Waal's (VdWs) force is established. When creating a heterostructure of single-layer graphene, it is essential to have very clean interfaces, which can be achieved by using hBN to encapsulate graphene, ideally with a more robust few-layered hBN-flake.

A robust and relatively novel technique to use as a nanolithography tool is the scanning probe lithography based on local anodic oxidation (LAO). The method enables in situ patterning of low-dimensional materials. At first, a conventional LAO driven by a direct current required prefabricated microelectrodes to drive the electrical current, making it a less attractive alternative. However, in recent years, it has been shown that an electrode-free LAO can be used [69], driven by a high-frequency alternating current above 10 kHz, applied through capacitive coupling. The method has shown high etching quality without oxide residues, which opens up great opportunities for fabricating ultraclean nanoscale devices. The LAO method was performed on monolayer graphene flakes using conductive atomic force microscopy (AFM) tips, as schematically illustrated in Fig. 3.9 together with optical microscope images of the flake, pre-cut and post-cut.

The many limitations of the tear-and-stack method, *e.g.*, yield, strain, and non-reproducibility, make it less attractive for further research. In contrast, both anodic oxidation and laser cutting are promising for industrial scaling and high-quality research [70].

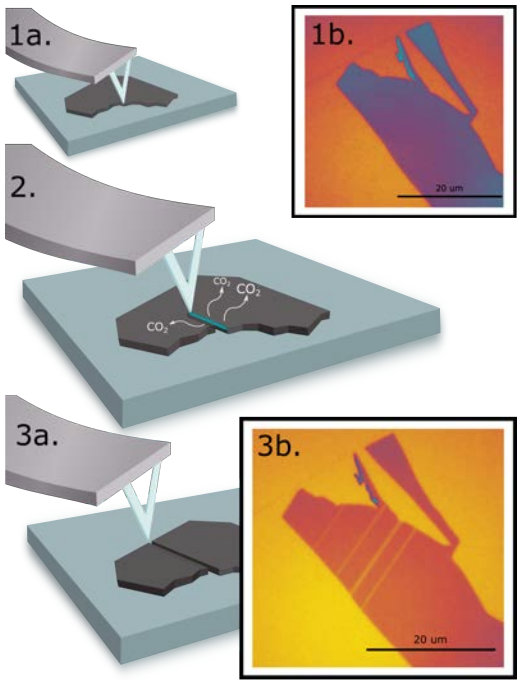

Figure 3.9: *1a) AFM-tip above flake on sample, pre-anodic oxidation, 1b) Optical microscope image of a monolayer graphene flake. 2a) Schematic illustration of the anodic oxidation method, cutting the flake. 3) Post-anodic oxidation and 3b) A post-cut optical microscope image of a monolayer graphene flake.*

Future fabrication developments could involve tailoring CVD-grown Graphene on Cu, possibly by laser cutting, enabling a more pristine graphene-device fabrication on a much larger scale.

4

Selected methods of characterization of HEMTs and GFETs for evaluation of carrier mobility and velocity

There are numerous methods used for characterization of μ and v in different electronic devices. These methods evaluate μ through various approaches, hence there are several types of μ, *e.g.* conductivity mobility, effective mobility (μ_{eff}), field-effect mobility (μ_{FE}), Hall effect mobility (μ_{H}), magnetoresistance mobility (μ_{gMR}), time-of-flight drift mobility etc. [61]. In this chapter, selected methods of evaluation of μ and v are reviewed, *i.e.*, those methods directly used in this work for characterization and analysis of HEMTs and GFETs. In the last section, the corresponding experimental setups and procedures are considered. In the analysis below, it is assumed that μ and v are coupled by the following relation $\mu = \frac{\partial v}{\partial E_{\mathrm{int}}}$, where E_{int} is the intrinsic field.

4.1 Delay time analysis

The delay time analysis can be considered as a high-frequency version of the time-of-flight drift mobility method [61]. The method was applied to analyze the v in GFETs [52]. An advantage is that it allows for studying v in high-frequency GFETs under actual application-like conditions. The general outline of the developed method is as follows. The f_{T} values are calculated from the measured scattering (S) parameters. To obtain v, the S-parameters are converted into delay times via the delay time analysis. The total

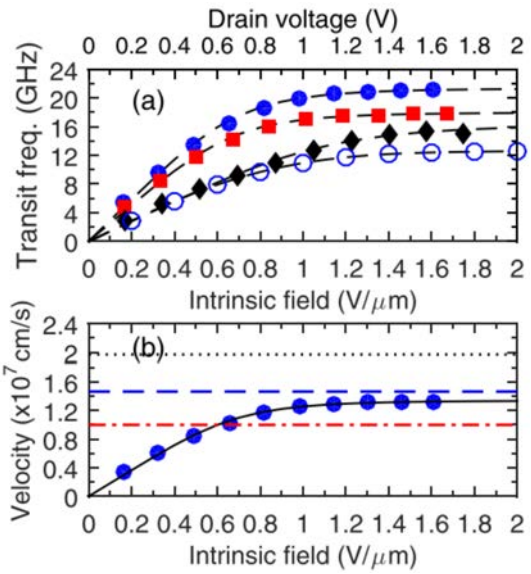

Figure 4.1: *a) Intrinsic transit frequency vs electric field in the channel for devices with* $n_0 = (1.7, 1.9, 2.8) \times 10^{12}\ cm^{-2}$ *(circles, squares, and diamonds) at* $V_g = -2$ *V. The extrinsic transit frequency vs drain voltage for the device with* $n_0 = 1.7 \times 10^{12}\ cm^{-2}$ *is indicated in the same graph by open circles. Dashed lines are polynomial fitting curves and serve as a guide to the eye. (b) The carrier velocity for the device with* $n_0 = 1.7 \times 10^{12}\ cm^{-2}$ *was calculated using Eq. (4.1) and fitted by the empirical expression of Eq. (2.9) (solid line) using* $\gamma = 3$, $\mu_0 = 1920\ cm^2/Vs$, *and* $v_{sat} = 1.4 \times 10^7\ cm/s$ *vs the electric field in the channel. The effective saturation velocities calculated using Eq. (2.10) for graphene with* Al_2O_3 *OPs (dotted), graphene with* SiO_2 *OPs (dashed), and graphene with* SiO_2 *and* Al_2O_3 *OPs are also shown (dashed-dotted). (Fig. from Ref. [52]. First published by Bonmann, M. et al., "Charge carrier velocity in graphene field-effect transistors", Appl. Phys. Lett. 111, 233505 (2017), doi: https://doi.org/10.1063/1.5003684. Reprinted with CC BY 4.0-permission.)*

current delay through the device is expressed as

$$\tau_{tot} = \frac{1}{2\pi f_{T,ext}} = \tau_{int} + \tau_{ext} + \tau_{pad} = \tau_{int}\left(1 + \frac{R_{series}}{R - R_{series}}\right) + \frac{C_g \cdot W \cdot L}{2} R_{series} + \frac{C_{pad}}{g_{m,ext} W}, \quad (4.1)$$

where τ_{int} is the intrinsic transit delay, τ_{ext} is the delay time associated with charging the parasitic parts of the active device region, τ_{pad} is the delay time required to charge the gate pad capacitance (C_{pad}), $f_{T,ext}$ is the extrinsic transit frequency calculated from the measures S-parameters, and $g_{m,ext}$ is the extrinsic transconductance normalized per unit width [52]. Since the GFETs operate in the linear regime $C_{gs} = C_{gd} = C_g \cdot W \cdot \frac{L}{2}$, where C_{gs} and C_{gd} are the gate-source capacitance and the gate-drain capacitance, respectively, and C_g is the gate capacitance per unit area [54]. The fringing field effect is neglected here. De-embedding of τ_{pad} is done by extrapolating the dependence $\tau_{tot}(\frac{1}{W})$ to $\frac{1}{W} = 0$ [71]. The τ_{ext} and τ_{pad} can be found via analyzing the dc transfer characteristics and dependence of τ_{pad} on L_g. After subtracting τ_{ext} and τ_{pad}, the v of the charge carriers and field dependent μ can be calculated as [52]

$$v = \frac{L}{\tau_{int}} \quad \text{and} \quad \mu = \frac{L}{\tau_{int} E_{int}} \quad (4.2)$$

Fig. 4.1 a) shows the intrinsic transit frequency $f_{T\text{-}int}$ vs E_{int} in the channel of GFETs with different n_0. Fig. 4.1 b) shows v calculated using Eqs. (4.1) and (4.2). For fields

above E_{int} = 1–1.5 V/μm, it can be seen that v saturates. The solid line in Fig. 4.1 b) is fitting by the empirical expression of Eq. (2.9). Fig. (4.1) also shows the effective saturation velocities calculated using analytic model assuming that v_{sat} is limited by inelastic emission of OPs, Eq. (2.10) (in Chapter 2).

4.2 Drain-source resistance model

At the current level of the GFET technology development, there is typically a strong surface distribution of μ measured in the GFETs located at different positions on a wafer caused by the spatially inhomogeneous Coulomb potential associated with CIs [36, 48]. Therefore, for further development of graphene-based high-frequency electronics, methods of accurate evaluation of μ directly based on the measured characteristics of the specific device, *i.e.*, without involving different test structures, should be developed and applied. To date, the μ in a specific GFET is generally characterized using a drain-source resistance model applied to the measured transfer characteristics [72–74], which is an approach that does not require any additional test structures.

The approach using the drain-source resistance model can be considered as a version of the field-effect mobility method adapted for GFETs. It was introduced in Refs. [54], and [73]. According to the model, the total drain-source resistance is given by [73]

$$R_{\text{tot}} = R_{\text{contact}} + R_{\text{channel}} = R_{\text{contact}} + \frac{N_{\text{sq}}}{n_{\text{tot}} e\mu} = R_{\text{contact}} + \frac{N_{\text{sq}}}{\sqrt{n_0^2 + n[V_{\text{TG}}^*]^2 e\mu}}, \tag{4.3}$$

where, as defines in Ref. [73], R_{channel} is the resistance of the graphene channel covered by the top-gate electrode, the contact resistance R_{contact} consists of the uncovered graphene section resistance and the metal/graphene contact resistance, and N_{sq} represents the number of squares of the top-gated area.

The expression for carrier concentration depending on the top-gate voltage $n[V_{\text{TG}}^*]$ is obtained from the following equation relating V_{TG}, oxide capacitance per unit area (C_{ox}), and the quantum capacitance of the 2DEG in graphene:

$$V_{\text{TG}} - V_{\text{TG, Dirac}} = \frac{e}{C_{\text{ox}}} n + \frac{\hbar v_{\text{F}} \sqrt{\pi n}}{e}. \tag{4.4}$$

Fig. 4.2 shows the measured (R_{tot}) versus V_{TG} (symbols), along with the model of Eq. (4.3) (solid lines). It can be seen that the modeling results agree well with the experimental data. By fitting this model to the measured data, the relevant parameters n_0, μ, and R_{contact} have been extracted. When the thickness of the Al_2O_3 gate dielectric is approximately 20 nm, it can be shown that the contribution of the quantum capacitance to the model can be ignored. Therefore, for this thesis work, the total drain-source resistance of a GFET can be expressed as in [48]:

$$R_{\text{total}} = R_{\text{series}} + \frac{L_{\text{g}}}{W_{\text{g}}} \frac{1}{e\mu_0} \frac{1}{\sqrt{n_0^2 + \left(V_{\text{GS}} - V_{\text{Dir}}\right)\frac{C_{\text{ox}}}{e}\Big)^2}}, \tag{4.5}$$

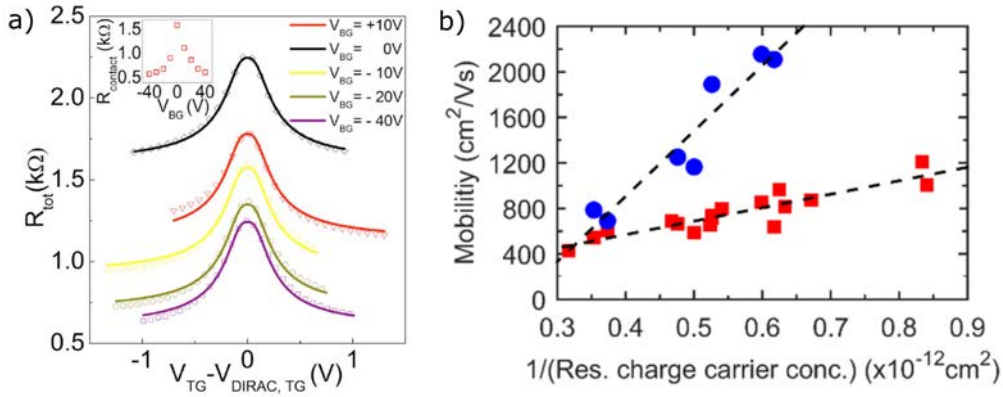

Figure 4.2: *a) R_{tot} vs $V_{TG} - V_{Dirac,TG}$ at selected V_{BG} values (symbols) along with modeling results for each data set (lines). The inset shows the extracted contact resistance $R_{contact}$ vs V_{BG}." (Fig. from Ref. [73]. First published by Seyoung Kim, et al. "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric", Appl. Phys. Lett. 94, 062107 (2009); https://doi.org/10.1063/1.3077021). b) "Low-field μ of holes in GFETs found by fitting the drain-source resistance model (μ_R, Eq. (S1), squares) and using delay time analysis (μ_0, circles) vs the inverse of the residual charge carrier concentration n_0. Dashed lines are polynomial fitting curves and serve as guide for the eye. (Fig. from Supplementary of Ref. [52]. First published by Bonmann, M. et al., "Charge carrier velocity in graphene field-effect transistors", Appl. Phys. Lett. 111, 233505 (2017), doi: https://doi.org/10.1063/1.5003684. Reprinted with CC BY 4.0-permission.)*

where R_{series} is represents all series resistances except $R_{channel}$, and n is defined as

$$n = \sqrt{n_0^2 + \left((V_{GS} - V_{Dir})\frac{C_{ox}}{e}\right)^2} \tag{4.6}$$

However, the analysis made in this thesis work indicated that the drain-source resistance model, in the commonly used approach, has several limitations, including the assumption of constant μ, requiring knowledge of n, and the uncertainty of C_g, which could be significantly modified by interfacial states [75]. These assumptions and uncertainties may result in significant errors in the μ-evaluation. For example, Fig. 4.2 b) shows the low-field μ of holes in GFETs found by fitting the drain-source resistance model and using delay time analysis versus the inverse n_0. It can be seen that the μ values calculated using the drain-source resistance model, compared to what was found from the delay time analysis, are 2–3 times lower in the same GFETs [52]. The results of the evaluation of the GFET μ using the gMR effect presented in **Paper C** also indicated that the μ found using the drain-source resistance model is 2–3 times lower than the corresponding gMR mobility. In earlier studies, using the delay time analysis and capacitance-voltage characteristics, it has been explicitly shown that the drain-source resistance model, in its commonly used approach, *i.e.*, using only C_{ox} as C_g, can underestimate μ. Therefore, the gMR method to extract μ can be considered more accurate compared to the commonly

used drain-source resistance model. Characterization of μ and v using the gMR effect is considered in more detail in section 4.3. A study of drift-diffusion and quasi-ballistic charge carrier transport in HEMTs and GFETs using the gMR effect is considered in Chapter 5.

4.3 Characterization of mobility and velocity using gMR effect

In the early years of the HEMT development, it has been proposed that the carrier μ and v can be found and studied using the gMR method [60, 76]. The gMR effect arises when the B-field alters the path of the charge carriers, causing them to deviate from their original straight line, increasing the sample resistance [61]. Compared to other methods of evaluation of v, the advantage of this method is that no knowledge of n, C, L_g, $R_{ungated}$, or threshold voltage ($V_{threshold}$) is required [77]. Evaluating μ_{eff} and μ_{FE} from the output and transfer characteristics usually approximate n from the simple parallel-plate capacitance model, which may result in large errors. On the contrary, the gMR method directly measures and allows for an accurate v analysis. Despite this advantage, the number of publications on v in HEMTs studied using the gMR is very limited. In the Refs. [77, 78], the dc and ac magnetoresistance measurements of Si MOSFETs and AlGaN/GaN HEMTs were used, respectively, for analysis of the low-field μ and quasi-ballistic charge carrier transport. The ac gMR method preserves the most important advantages of the dc gMR method while eliminating the parasitic contribution of R_{series} via modulation of V_G by square pulses and measuring the derivative of the transistor resistance [77].

As shown in **Chapter 5**, under the conditions of a negligible physical magnetoresistance effect (pMR), and $L/W < 0.4$, the μ_{gMR} is given by Ref. [61] as

$$\mu_{gMR} \approx \frac{1}{B}\sqrt{\frac{R^B_{gated}}{R^0_{gated}} - 1}, \tag{4.7}$$

where R^B_{gated} and R^0_{gated} are the resistances of the gated region with and without applied B-field, respectively.

Detailed analysis of the gMR phenomenon and examples of studies of low-field μ and high-field v in HEMTs and GFETs are given in **Chapter 5**. In this thesis work, the gMR effect has been applied for studies of the drift-diffusion and quasi-ballistic charge carrier transport reported in **Paper B**, **Paper C** and **Paper D**.

4.4 Methods of extraction of series resistance

The series resistance (R_{series}) in HEMTs and GFETs is made up of resistances associated with the junctions (contacts) and ungated regions of the channel ($R_{contact}$ and $R_{ungated}$), that together with R_{gated} constitutes the total resistance (R_{total}), which can be used to

calculate the gMR μ as

$$\mu_{\mathrm{gMR}} = \frac{1}{B}\sqrt{\frac{R^{B}_{\mathrm{total}} - R^{B}_{\mathrm{series}}}{R^{0}_{\mathrm{total}} - R^{0}_{\mathrm{series}}} - 1}. \tag{4.8}$$

According to analysis in this thesis work, the R_{series} can be comparable with R_{ungated} and depend on both E and B-fields. Therefore, for accurate μ_{gMR} evaluation, the R_{series} should be found and de-embedded from R_{total}. Additionally, when studying the charge carrier transport in the ranges of lateral and transverse E-fields, the knowledge of R_{series} is also required to find the intrinsic gate-source voltage (V_{gs}) and the intrinsic drain-source voltage (V_{ds})

$$V_{\mathrm{gs}} = V_{\mathrm{GS}} - I_{\mathrm{ds}}\frac{R_{\mathrm{series}}}{2} \tag{4.9}$$

$$V_{\mathrm{ds}} = V_{\mathrm{DS}} - I_{\mathrm{ds}} \cdot R_{\mathrm{series}}. \tag{4.10}$$

where I_{ds} is the drain-source current.

There are several dc methods of extraction of R_{series} in FETs, which can be distinguished into two groups of approaches I) parameter extraction and II) exploiting the asymmetry between drain and source resistances [79]. The most used methods from the first approach are: i) direct fitting of the drain current, ii) constant μ at two small drain biases, and iii) V_{D} versus V_{G} at constant current. The common drawback of all the above methods for the gMR evaluation is that they require applying a certain transfer and output characteristics model, which, according to analysis in this thesis work, results in significant errors. For this reason, approaches that do not require pre-knowledge of certain models have been selected in this work. For evaluation of the R_{series} in HEMTs the method presented in Refs. [80] and [81] has been applied. Fig. 4.3 a) shows the total resistance R_{total} (V_{DS} = 1 V) as a function of V_{G} for AlGaN/GaN MOS-HEMTs with unpolarized and (± 120 V) polarized P(VDF-TrFE) gating. It is assumed that for a very large gate-overdrive $V_{\mathrm{GS}} - V_{\mathrm{th}}$ ($V_{\mathrm{GS}} - V_{\mathrm{th}} >> V_{\mathrm{DS}}$) with a small fixed V_{DS}, R_{channel} becomes very small compared to R_{series}, and R_{series} can be estimated from the plot R_{total} versus V_{GS}. This method was successfully applied in **Paper B**. However, this method cannot be applied for GFETs used in this work because the relatively larger L_{g} and lower gate-break-down field do not allow for saturating the total resistance dependence fully. For evaluation of R_{series} in GFETs, the approach presented in Ref. [78] has been applied.

The μ_{gMR} can be calculated using Eq. (4.7), after subtracting the corresponding R_{series} from the measured R_{total}). To find R_{series}, an approach similar to that published previously [78], was applied. In the GFETs, at high gate voltage overdrive, $V_{\mathrm{GSO}} = V_{\mathrm{GS}} - V_{\mathrm{Dir}}$, where V_{Dir} is the Dirac voltage, *i.e.*, under the condition where the gate induced n is much larger than n_0, R_{total} with (and without) B-field can be expressed as

$$R^{B(0)}_{\mathrm{total}} = R^{B(0)}_{\mathrm{series}} + \frac{L}{We n \mu_{\mathrm{FE}}} \tag{4.11}$$

where e is the elementary charge, and n is the charge carrier concentration proportional to V_{GSO} [55]. In support of previous studies, it can be assumed that in the limited range of n, the carrier transport is being governed by the Coulomb scattering with μ independent

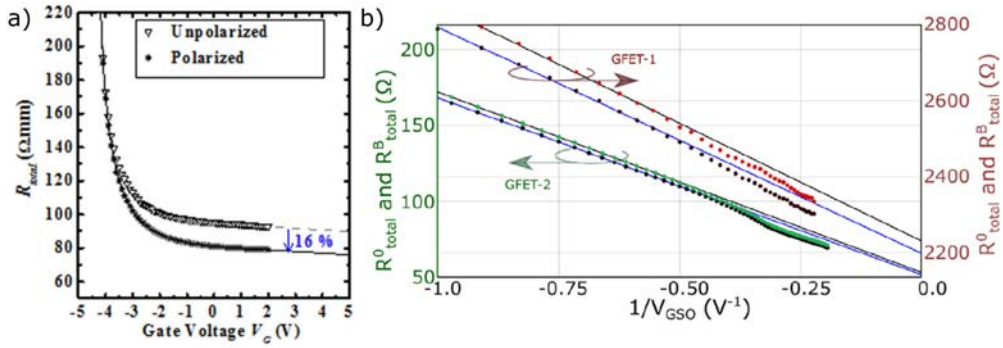

Figure 4.3: *a) "Total resistance R_{Total} (V_{D} = 1 V) as a function of gate voltage V_{G} for AlGaN/GaN MOS-HEMTs with unpolarized and (± 120 V) polarized P(VDF-TrFE) gating." (Fig. from Ref. [80]. First published by Liu, X. et al. AlGaN/GaN Metal-Oxide-Semiconductor High-Electron-Mobility Transistor with Polarized P(VDF-TrFE) Ferroelectric Polymer Gating. Sci. Rep. 5, 14092; doi: 10.1038/srep14092 (2015). Reprinted with CC BY 4.0-permission.) b) "The drain resistances of GFET-1 and GFET-2, with and without the transverse B-field, plotted vs $\frac{1}{V_{\mathrm{GSO}}}$ in the hole conductivity branch above -1 V^{-1}. The straight lines are linear fits in the ranges of constant mobility." (Fig. from* ***Paper C****, Ref. [82]. First published by Harrysson Rodrigues, I et al, "Geometrical magnetoresistance effect and mobility in graphene field-effect transistors" Appl. Phys. Lett. 121, 013502 (2022); https://doi.org/10.1063/5.0088564. Reprinted with permission .)*

of n [48]. For comparison, analysis of n_0 in the graphene test structures showed that μ is relatively constant in the range of n: 2–3×10^{12} cm^{-2} [55], which is explained by the dominating Coulomb scattering. It was shown that the Coulomb scattering is the only mechanism resulting in μ being independent of n [34, 36, 55]. Under these conditions, R^0_{total} and $R^{\mathrm{B}}_{\mathrm{total}}$ given by Eq. (4.11) are linear functions of $\frac{1}{V_{\mathrm{GSO}}}$, and R^0_{series} and $R^{\mathrm{B}}_{\mathrm{series}}$ can be found by linear fitting of the corresponding dependencies. In the analysis below, only the hole branch of the transfer characteristics was considered, *i.e.*, at $V_{\mathrm{GSO}} < 0$, since the data obtained in the electron branches was not sufficient for a reliable fitting. Additionally, R_{series} in the electron branch is typically higher due to the formation of the pn-junction in the ungated regions [83]. Figure 4.3 (b) shows R^0_{total} and $R^{\mathrm{B}}_{\mathrm{total}}$ of GFETs with sufficiently different R^0_{series} and $R^{\mathrm{B}}_{\mathrm{series}}$, plotted vs $\frac{1}{V\mathrm{GSO}}$ in the hole conductivity branch above -1 V^{-1} together with the linear fits made in the ranges of constant μ. It can be seen that the dependencies are relatively linear up to approximately -0.5 V^{-1}, manifesting that μ is constant. Deviations from the linear dependencies above -0.5 V^{-1}, *i.e.*, higher n, can be explained by a decrease in μ due to the increasing contribution of phonon scattering [55]. Analysis indicated that higher R_{series}, for sample GFET-1, was caused by incomplete removal of the Al_2O_3 layer in the openings for the drain/source contacts.

4.5 Experimental setups and procedures for measuring dc characteristics

This section presents the experimental setups used for dc measurements to characterize state-of-the-art InP HEMTs and various geometries of GFETs, with and without a *B*-field present.

The dc characterization of the InP HEMTs has been carried out in a Quantum Design Physical Property Measurement System (PPMS), see Fig. 4.4, using a Keithley 2604B source meter controlled via LabView to bias the samples. The PPMS setup contains a superconducting magnet enabling measurements up to 14 T in an ambient temperature of 2 K. The transistors were electrically connected through wire bonding to an impedance-matched LC-network to stabilize the measurement and avoid oscillations in the output current. The sample was then mounted on an adjustable sample holder, allowing for sample rotation, and placed in the vacuum chamber of the cryostat. The data sets measured in this setup were obtained on various occasions over six months, where no fluctuations were observed, and the result was reproducible.

Measurements of the fabricated device were done at room and cryogenic temperatures to confirm the quality of the HEMT. The essential device parameters for a low-noise transistor were initially measured, with obtained values comparable with those measured in Ref. [62], and further used.

Due to setup limitations, microwave measurements could not be done on individual HEMTs. However, RF measurements on an LNA containing three of these HEMTs were

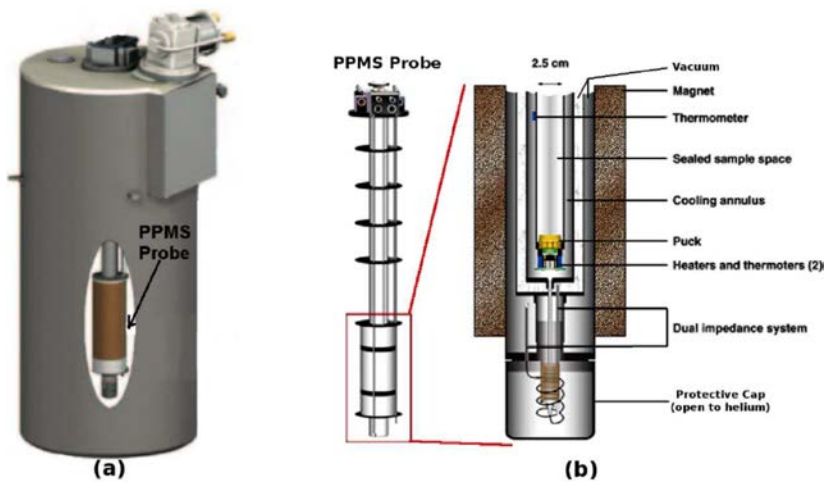

Figure 4.4: *"QD PPMS dewar and probe. Shown are the PPMS dewar (a) and PPMS probe (b) with cross-section of the probe's sample region, SC magnet, and dual impedance system. Source: Q. Design, Physical Property Measurement System: User's Manual (Quantum Design, Inc., San Diego, CA, 2002)." (Fig. from Ref. [84]. First published by Melinda Toth, "Magnetic Properties of Sr2YRu1-xIrxO6 Compounds" (May, 2013))*

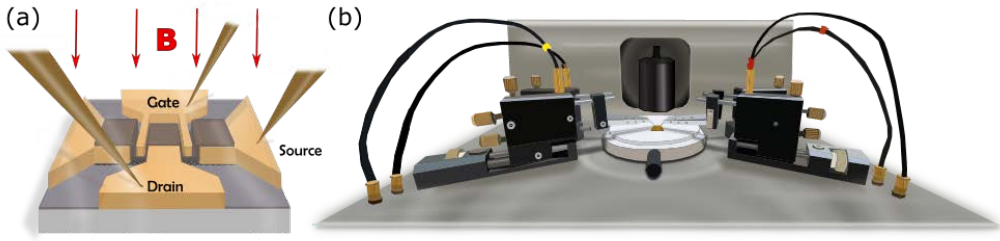

Figure 4.5: *a) Schematic illustration of probed GFET. b) "Illustration of the experimental set-up with a permanent magnet visible in the middle, used for measurements of the GFET transfer characteristic." (From the supplementary material of* ***Paper C****)*

evaluated, with and without a perpendicularly applied B-field.

The dc characteristics of the GFETs, with the design as in Fig. 4.5 (a), were obtained using a standard probe station. See **Paper C** and **Paper D** for a complete image of a transistor obtained using an optical microscope.

For measurements involving a B-field when characterizing GFETs in this study, a standard Hall measurement setup was used; see Fig. 4.5 (b) for a depicted illustration. The Hall setup was equipped with dc microprobes and a movable permanent magnet with B=0.33 T. μ_{gMR} in the GFETs could be obtained from the transfer characteristics via a Keithley 2612B dual-channel source meter and a semiconductor parameter analyzer without and with a transverse B-field. Various devices were examined and contacted using dc microprobes and via wire bonding.

The measurements were performed in daylight and in a dark and illuminated environment to estimate the possible effects of the persistent photoconductivity traps [60].

A B-field sweep was performed to verify the expected B^2-dependence in the device resistance. The verification was done by exposing the sample to a B-field swept between -0.8 to 0.8 T.

5

Study of drift-diffusion and quasi-ballistic charge carrier transport in HEMTs and GFETs using geometrical magnetoresistance effect

This chapter briefly reviews different phenomena of the charge carrier transport in 2DEG FETs arising under an external B-field, namely: the Hall effect, the physical magnetoresistance effect (pMR), and the geometrical magnetoresistance effect (gMR). The focus will be on the gMR effect being the method of analysis of the carrier transport reported in the appended papers. Examples of evaluation of the low-field mobility and high-field velocity in HEMTs and GFETs using the gMR effect are reviewed. The advantages and limitations of the gMR method are analyzed in comparison with other methods. A portion of this chapter is also devoted to the concept of the quasi-ballistic charge carrier transport in HEMTs and GFETs, introducing transmission formalism and ballistic mobility (μ_B). It shows how the gMR effect, combined with the drain-source resistance model, can be used to evaluate the collision mobility and μ_B accurately.

5.1 Physical and geometrical magnetoresistance phenomena

In general, the magnetoresistance effect is associated with the phenomenon of an increase in resistance in the presence of a magnetic field. It can result from the combined action of several independent mechanisms and effects. At conditions used in this work for studies

of carrier transport in HEMTs and GFETs, the following two mechanisms can be relevant: (1) a physical magnetoresistance (pMR) effect and (2) geometric magnetoresistance (gMR) effect [14, 61]. The original cause of the pMR effect is that the velocity, or energy, of the ensemble of carriers, instead of being the same for each carrier, is distributed around the average value. The carriers with velocities that differ from the average would be deflected and deviate from the shortest path, increasing resistance. The gMR effect occurs in samples with small L/W ratios. In this case, the Hall voltage is not fully developed to balance the Lorentz force, and carriers near the contacts move at an angle to the applied electric field. The longer path again leads to higher resistance. Due to their specific layout, *i.e.* $L/W << 1$, the gMR effect in the high-frequency HEMTs and GFETs always dominates over the pMR effect.

In Ref. [85], the gMR effect is analyzed in detail by an example of a MOSFET as follows. It is assumed that the longitudinal electric field E is given by $\frac{V_{DS}}{L}$. Furthermore, when applying a B-field, the electrons in the channel fields experience the Lorentz force $F_L = -q \cdot E - q \cdot v \times B$. The energy gain of the electron with F_L is transferred in to the silicon lattice due to scattering, resulting in a energy equilibrium, which leads to an average v that is proportional to F_L as $v = \frac{\mu_n}{q} \cdot F_L = -\mu_n \cdot E - \mu_n \cdot v \times B$. As a result, the current density can be calculated as

$$J = n \cdot q \cdot v = n \cdot q \cdot \mu_n \cdot E - \mu_n \cdot j \times B. \tag{5.1}$$

Supposing the response to the Lorentz force is the same as for an electric field, the carrier velocity v is given by:

$$\mathbf{v} = \mu(\mathbf{E} + \mathbf{v} \times \mathbf{B}). \tag{5.2}$$

Eq. (5.2) leads to the solution for v as

$$\mathbf{v} = \frac{\mu}{1 + (\mu B)^2}(\mathbf{E} + \mu \mathbf{E} \times \mathbf{B} + \mu^2 (\mathbf{B} \cdot \mathbf{E})\mathbf{B}), \tag{5.3}$$

where the effective reduction in mobility due to the perpendicular B-field is apparent. Electric current will decrease with an increasing B-field, so the resistance of the device will increase. Due to the scalar product relation: $(U \times V) \bullet W = (U \bullet V) \cdot V - (V \bullet W) \cdot U$, Eq. (5.1) can be solved for perpendicular B-field, *i.e.*, $E \bullet B = 0$, which leads to:

$$j = \frac{\sigma_n \cdot E + \mu_n \cdot \sigma_n \cdot (E \times B)}{1 + \mu_n^2 \cdot B^2} \tag{5.4}$$

where $\sigma_n = n \cdot q \cdot \mu_n$ is the silicon conductivity. As seen in Fig. 5.1 a), for a short channel, the drift electric field in the channel, E, remains along the x-axis. Eq. (5.4) shows that the drift current is no longer parallel to E. It is deflected with the angle ϕ, where $\tan(\phi) = \mu_n \cdot B$ and can be decomposed as a longitudinal component, j_x, and a perpendicular component, j_y:

$$j_x = \frac{\sigma_n \cdot E}{1 + \mu_n^2 \cdot B^2} \quad \text{and} \quad j_y = \frac{\mu_n \cdot \sigma_n \cdot (E \times B)}{1 + \mu_n^2 \cdot B^2} \tag{5.5}$$

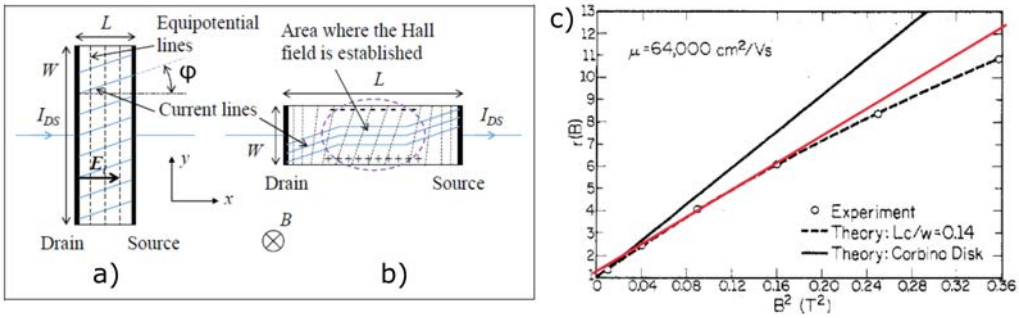

Figure 5.1: *a) short transistor, b) long transistor, under B. [From Ref. [85]]. c) The reduced resistance* $r(B) = \frac{R(B)}{R(0)}$ *for a structure with 100 μm channel width and 14 μm channel length as a function of B-field along with the calculated* $r(B)$ *for electrons with a mobility of 64 000* cm^2/Vs*. The measurement was made with no sample illumination at 77 K in an electric field less then 1 V/cm. Also shown is the* $r(B)$ *relation for the Corbino disk geometry with the same mobility. [From Ref. [76]]*

When the channel is short, as in a transistor with a small L/W ratio, the electrons will tend to accumulate on the lateral side, as depicted in Fig. 5.1 a), and instantly flow back to the source and drain ohmic contacts. This is not the case for longer transistors when L/W is high. Due to this geometry, the resistivity of the channel is too high for the electrons to flow back to the source and drain, which leads to an accumulation of electrons on one side, causing a negative net charge. In contrast, there will be a deficit of electrons on the opposite side, resulting in a positive net charge. This imbalance in charge gives rise to a Hall field and an electric force opposite the Lorentz force. Ultimately, a charge balance will take place, and the current remains along the x-direction in the center of the long channel, as depicted in Fig. 5.1 b), while E no longer is aligned with x [86].

The only current density component leading to a drain-source current I_{ds} is j_x. So, for a small L/W transistor, the expression of j_x in Eq. (5.5) shows that under a B-field, the channel conductivity, respectively the carrier mobility, is reduced to an effective conductivity $\sigma_n(B)$, respectively an effective mobility $\mu_n(B)$, given by:

$$\sigma_n(B) = \frac{\sigma_n}{1 + \mu_n^2 \cdot B} \quad \text{and} \quad \mu_n(B) = \frac{\mu_n}{1 + \mu_n^2 \cdot B} \tag{5.6}$$

Ref. [87] gives the exact solution for gMR, taking into account the lateral edge effect, shown in Fig. 5.1 c) from Ref. [76]. It is sublinear in B^2-format, starting approximately around 0.4 T. This is in good agreement with what was observed in **Paper C**, where the dependence can be considered relatively linear up to $B \approx 0.55$ T, indicating that the approximation in Eq. (4.7) is valid below this B-field. The approximation for relatively large L/W is as follows [60]

$$R(B) = R(0)\Big(1 + \mu^2 B^2 (1 - 0.543 L/W)\Big) \tag{5.7}$$

If the error in the determination of μ_{gMR} is less than 10 %, then the aspect ratio L/W must be less than 0.4 [61]. For typical FET structures with $L/W << 1$, Eq. (5.7), originating

from measurements on a Corbino disk, is a close approximation to Eq. (4.7), which makes it suitable in gMR measurements.

5.2 Angular dependencies of dc characteristics in magnetic field

In many sensitive detection systems, FET and HEMT-based components are used. Several such systems depend on strong B-fields, *e.g.*, various imaging techniques. Nuclear Magnetic Resonance (NMR) is commonly used in analytical chemistry and its application to MRI for medical diagnostic. In analytical NMR, fields up to 28.2 T are used, and in brain research, static fields up to 10.5 T [88]. Although typical MRI scanners for humans are between 1.5 T to 3 T and biomedical and preclinical MRI and MR-Spectroscopy on animal models are 7 T and 14.1 T [88]. Therefore, it is of immense importance that electronics can withstand strong B-fields.

A problem prevalent in, for example, detectors is that amplifier properties such as gain and noise figure are negatively affected by the B-field, specifically for LNAs oriented perpendicular to a B-field, as shown in **Paper A**. Mounting the LNA away from the B-field, using coaxial cables, or aligning the LNA perfectly parallel to the B-field lines could be a solution. However, the former is not preferable due to losses and reduced sensitivity, and the latter gives rise to potential issues in the degree of alignment of the LNA in the field. There is a limited number of publications on the topic, where one example is Ref. [89] examining a junction field effect transistor (JFET) in an applied B-field up to 30 T.

In the results of **Paper A**, the I_{ds} full angular dependence for the cryogenic InP HEMT was demonstrated from 0 to 14 T. Figure 5.2 shows a schematic illustration of the rotation of the transistor and Fig. 5.3 a) shows the obtained data from full angular sweeps. The current limiting mechanism was identified to be gMR, where the semi-empirical I_{ds}-V_{ds} equation

$$I_{\mathrm{ds}}(\theta, B) = \frac{V_{\mathrm{ds}}}{R_0(1 + \mu^2 B^2 \sin^2\theta)} \tag{5.8}$$

captures the θ and B dependence in the experimental data well, where R_0 is a resistance term consisting of resistance of gated regions without a B-field. It can be seen from Fig. 5.3 a) that experimental angular dependencies can be fitted by the model in Eq. (5.8) using $R_0 = 11\ \Omega$ and $\mu = 10500\ \mathrm{cm}^2/\mathrm{Vs}$. Note that extrinsic parameters were used and no de-embedding was done at this stage, hence a lower μ than what is presented in **Paper B**, for the same type of devices, was obtained. Regardless of the model used, the Relative Reduction Factor (RRF) is proportional to $\mu_n^2 \cdot B^2$:

$$RRF = \frac{I_{\mathrm{DS}}(B) - I_{\mathrm{DS}}}{I_{\mathrm{DS}}} \approx -\mu_n^2 \cdot B^2 \tag{5.9}$$

RRF depends on the carrier mobility, which also depends on V_{GS} and V_{DS}; therefore, the effect of B-field on MOSFETs depends on the transistor biasing. The mobility dependence on V_{GS} and V_{DS} needs to be considered to derive a model of the transistor behavior. RRF

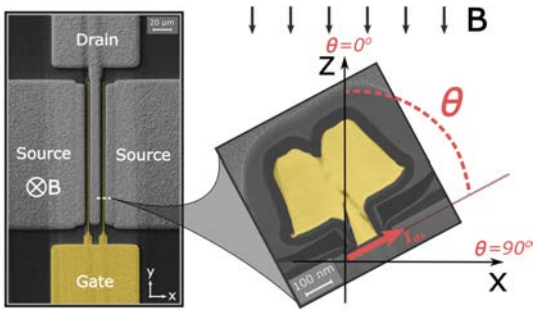

Figure 5.2: *The two-finger InP HEMT is shown in the top view (by scanning electron microscopy) and side view (by cross-sectional transmission electron microscopy) perspective. The T-shaped gate is marked in yellow. The static B-field was applied in the z-direction. The device was rotated from $\theta = 0^0(180^0)$ to 90^0 corresponding to parallel and perpendicular orientation, respectively, of the HEMT output current with respect to the B-field. (First published in **Paper A**)*

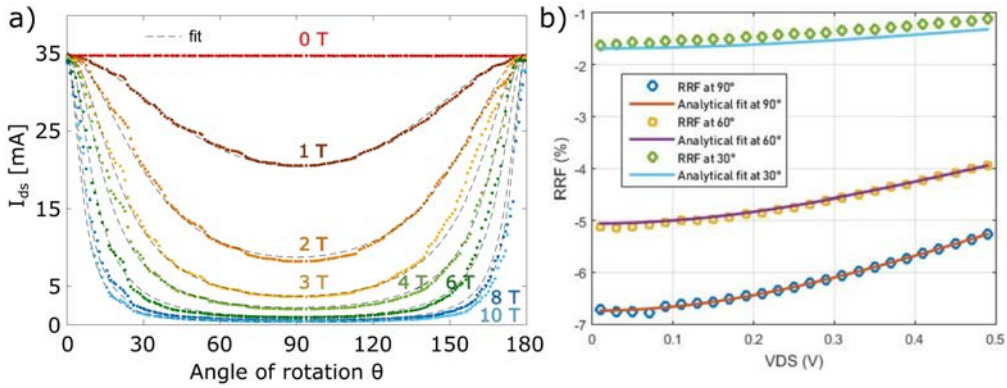

Figure 5.3: *a) Rotation sweep (θ from 0^o to 180^o) showing I_{ds} (absolute values) for various externally applied B-fields 0, 1, 2, 3, 4, 6, 8 and 10 T at a fix V_{gs} and V_{ds} of 0.4 V in an ambient temperature of 2 K. The dashed lines (black) are fitting of Eq. (5.8) to the experimental data points (colored). Device size $W_g = 2x50$ μm and $L_g = 100$ nm. [From **Paper A**]. b) shows RRF for the chip at $\beta = 90^o$ computed versus $V_{GS} - V_{TH}$ at $V_{DS} = 10$ mV, as well as its fitting by the analytical expression $-\mu_n^2 \cdot B^2$ where Eq. (6), in Ref. [85], is used for $\mu_n(V_{GS})$. Here again, the model is in excellent agreement with the experimental data. [From Ref. [85]].*

for a MOSFET is presented in Fig. 5.3 b). The main reason for observing much stronger angular dependence in HEMTs, can be explained by using Eq. (4.7) originating from the theory given in section 5.1, and is because the mobility in the examined HEMTs is 100 times larger than that of the MOSFET. In Ref. [90], prior to Ref. [85], they only observe mobility on the order of 500 cm^2/Vs.

In conclusion, HEMTs are perfect for *B*-field sensing and imaging; even at room temperature. The strong angular field dependence demonstrated in Fig. 5.3 a) for the cryogenic InP HEMT output current suggests that even a tiny misalignment of the cryogenic InP HEMT LNA in a *B*-environment can be detrimental to read-out sensitivity.

5.3 Low-field mobility evaluated via gMR effect

The gMR allows for in-depth studies of mechanisms affecting mobility in the full range of charge carrier concentrations, as demonstrated in **Paper B** and **Paper C**, where the charge carrier mobility in InP HEMTs and GFETs have been investigated using Eq. (4.7). Previous publications using the gMR effect for evaluating low-field mobility are Ref. [77, 78] and [91]. In Fig. 5.4 a), Lusakowski *et al.* presents magnetoresistance mobility in a series of bulk Si n-type MOSFETs for a range of concentrations ($n = 5\times10^{12}$ cm^{-2} down to 5×10^{10} cm^{-2}), as a function of L_g. The devices were measured using direct current biasing to obtain the magnetoresistance (dc MR), keeping the transistor in a B-field perpendicular to the inversion layer plane. The dc MR method is also used in Refs. [9, 92, 93] and gives a correct value of the mobility once R_{series} is properly subtracted from R_{total}. However, subtracting R_{series} is quite ambiguous, limiting the applications of the dc MR method. In Ref. [77], they propose an alternating current magnetoresistance (ac MR) method. By measuring the ac MR, while simultaneously modulating the gate potential, this method allowed the determination of n and μ in a HEMT under the gate, avoiding the influence of R_{series}. Fig. 5.4 b), from Ref. [77], shows μ for several transistors investigated using the ac MR method. To determine n, a Fourier transform of Shubnikov-de Haas oscillations was performed. The obtained ac MR μ was validated by comparing it to μ_H measurements on gated Hall bars adjacent to the transistors.

In **Paper B**, a study of the low-field μ and high-field v in state-of-the-art InGaAs/InP HEMTs found via the gMR effect is presented. Regarding graphene and graphene-based devices, *e.g.*, GFET, mobility is typically significantly reduced compared to mobility in single-layer graphene, which can reach above 100 000 cm^2/Vs. For room tempera-

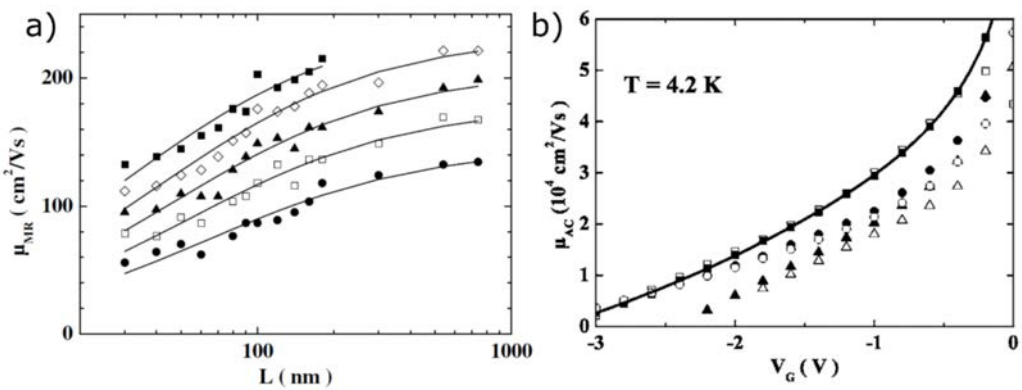

Figure 5.4: *a) Magnetoresistance mobility, μ, as a function of the gate length, L, for $n = 5\times10^{12}$ cm^{-2} (solid squares), 2×10^{12} cm^{-2} (diamonds), 10^{12} cm^{-2} (triangles), 5×10^{11} cm^{-2} (open squares) and 5×10^{10} cm^{-2} (circles). Solid lines are fits to Eq. (5). b) The ac mobility for the transistors investigated at 4.2 K. Wafer T799: T2-solid triangles; T3-open triangles. Wafer T854B: T1-solid circles; T3-open circles. Wafer T1077B: T4-solid squares; T3-open squares. Solid line: Fit of Eq. (1) to T4 data. [Figures from Ref. [78] and [77], respectively].*

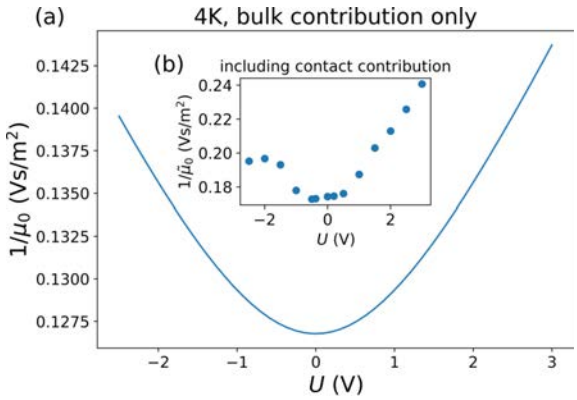

Figure 5.5: *(a) Electron-hole averaged inverse mobility, Eq. (19), derived using the parameters extracted from the 4 K MR data. (b) Mobility naively extracted from the scaled shifted MR as $R(B)/R(0) = 1 + \mu_0^2 B^2$: this includes the contribution of the contact resistance. [Figure from Ref. [91]].*

ture, the mobility in GFETs, with the highest reported high-frequency performance, is below 5000 cm^2/Vs [58, 94]. The apparent degradation in μ is most likely associated with material imperfections, partly introduced during the device processing, and the vicinity of dielectrics in the device structure. Moreover, strong surface distribution is typically observed in the measured mobility of GFETs located at different positions on the wafer [36]. A method of direct measurement of the mobility of a specific device, *i.e.*, without involving different test structures, is therefore crucial for accurately characterizing such devices. Generally, the mobility in a specific GFET is characterized using a drain-source resistance model applied to the measured transfer characteristics [54, 73], and no test structures are required for this approach. Nevertheless, it has several limitations, mainly; the assumption of constant mobility and uncertainty of the gate capacitance, where the latter can be strongly modified by the interfacial states [75], which further can result in significant errors in the mobility evaluation. This can lead to 2-3 times lower mobility values than those found from the delay time analysis in the same GFETs [52]. The advantages of the gMR method for the evaluation of the mobility are the same for GFETs; it does not require knowledge of the carrier concentration or the transistor's C, L_g, R_{ungated}, and $V_{\text{threshold}}$ [77]. However, despite the apparent advantages, the only demonstration of μ_{gMR} in graphene devices so far is that in Ref. [91]. They measured MR of suspended graphene in the Corbino geometry at B-fields up to 0.15 T, *i.e.*, in a regime uninfluenced by Shubnikov–de Haas oscillations, see Fig. 5.5

5.4 High-field velocity studied using gMR effect

To obtain an accurate representation of the charge carrier velocity in the channel of a MODFET at higher fields, precise and effective models are crucial. One can start reviewing previous studies with a method for determining electron velocities at high fields in bulk semiconductors [95, 96]. The method is based on measuring the time of flight using an oscilloscope when injecting electrons with a pulsed electron beam to reverse biasing a p-n junction. Another way to determine the velocity is through the standard method of measuring the current as a function of the field by knowing the constant carrier concentration. This can be done in samples where the geometry

prevents carrier injection via the contact [97, 98]. In 1984, the methodology of using Hall measurements was adapted to determine velocity by finding μ in AlGaAs/GaAs heterostructures at electric fields up to 750 V/cm [99]. In the same study, they also investigated electron temperature using photoluminescence. This, together with the earlier results [100], also agreed with studies of μ and temperature of 2DEGs at low and moderate fields [101]. In Ref. [101], they describe the method of gMR, enabling direct measurements of v. In Ref. [76], they demonstrate a method for measuring μ, v, and n in MOD structures, using the gMR effect, where several advantages of the gMR-method are brought up, *i.e.*, no assumption of constant carrier concentration is required. Instead, the method allows studying the carrier concentration in detail for each field strength; hence carrier injection in FET structures can straightforwardly be studied. In addition, oscillation issues related to Hall measurements at high electric fields can, to a large degree, be avoided because of the short channel lengths compared to standard FET channels, *e.g.*, MOSFETs. At low fields, they observe drastically decreasing mobility with increasing electric field. Additionally, the velocity and 2DEG concentration were studied. Their work points out that the gMR method would be well suited for studying velocity characteristics in FETs since the geometry of their structures is the same as that of a typical FET. Their prediction agrees well with what was observed in **Paper B**. Moreover, the method presented in **Paper B** should also be applicable for studying short-channel MOSFETs and other types of FETs with the appropriate geometry. Further validation of the results presented in **Paper B** can be made by a more detailed analysis of Ref. [76] and Ref. [60], where the electric field is given by

$$E = \frac{V_{\text{app}} - R_{\text{series}} \cdot I}{L} \tag{5.10}$$

Here, the V_{app} is the applied voltage, R_{series} is the series resistance due to the two contacts and is given by $R_{\text{series}} = 2\frac{R_C}{W}$, and I is the channel current. The velocity is

$$v(E) = \mu(E) \cdot E. \tag{5.11}$$

As described in Ref. [60], the measured $\mu(E)$ and $v(E)$ are representative of the electrons in the 2DEG. They present $\mu(E)$ characteristics and calculations of $v(E)$, see Fig. 5.6. It can be seen that the velocity is almost linear with the field at low fields and continues to increase at higher fields, to eventually saturate gradually. The velocity saturation is contrary to the results presented in **Paper B**, and the expected negative differential velocity observed in bulk GaAs, where $\frac{\delta v}{\delta E} < 0$. However, they state that their experimental technique is likely not reliable in fields greater than those at which negative differential velocity would be observed, thus a need for further studies of this phenomenon. Ref. [76] and [60] do provide a report on high-field velocity measurements in MODFETs (HEMTs) using gMR, where Eq. (3) in Ref. [60] is the exact solution for gMR. However, it should only be used for small L_g/W_g. This originates from Ref. [87], where a more thorough discussion of correction factors is presented.

In **Paper B**, the two key findings are i) higher low-field mobility does not lead to a higher high-field velocity; therefore, low-field mobility is not a vital parameter for characterizing a transistor. ii) first experimental observation of velocity peaks. The μ at

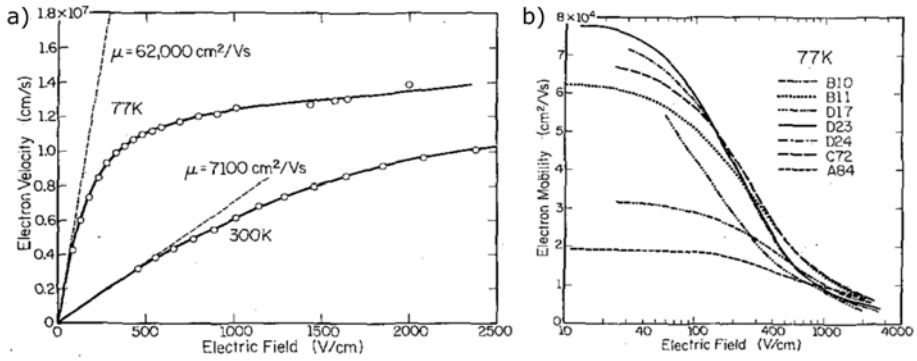

Figure 5.6: *a) The 2DEG velocity as a function of electric field for sample at 77 K and b) the 2DEG mobilities as functions of electric field for the seven structures studied (from Ref. [60]).*

low-field and v_{peak} reveal opposite dependencies on the transverse field; hence the peak velocity is a more appropriate parameter for characterization and development of the low-noise HEMTs. These findings are relevant for further developing high-performance HEMTs, particularly for applications in the LNAs.

In Ref. [60], they do not observe any velocity peaks, referred to as negative differential velocity. Their simulations predict a much smaller decrease in the v_{peak} and corresponding E_{peak} than what is presented in *Paper B*. According to the study in **Paper B**, the most probable reason for their observation is that they did not apply high enough fields at a high enough charge carrier concentration. Comparing the lowest charge carrier concentration in **Paper B** (Fig. 4), where $V_{\text{gs}} = 0.10$ V, it is clear that at higher drain fields the E_{peak} is less pronounced. For the charge carrier concentrations used in Ref. [60] they would need drift velocities above the 2 kV/cm mark, however, from Fig. 5.6 it is clear that more data points would be needed, alternatively higher concentration.

5.5 Quasi-ballistic charge carrier transport

In this section, the concept of μ_B and the transmission formalism to study the charge carrier transport in GFETs with different L_{g} in the range 0.2-2.0 μm is applied. Comparative analysis of μ_{c} and μ_B parameters clearly illustrates the transition of the charge carrier transport from the scattering regime through the quasi-ballistic to the purely ballistic regime. This analysis is specifically relevant for graphene, which already has demonstrated high potential as a channel material in advanced graphene field-effect transistors (GFETs) for high-frequency applications [50, 102]. Theoretically, it was shown that in GFET structures, the saturation velocity is limited by the remote optical phonons of the adjacent dielectrics [52, 55, 72]. Therefore, for further increasing f_{T}, selecting the dielectric materials with higher phonon energies was suggested [52, 72]. However, when this approach reaches its limit, the remaining obvious way of further increasing f_{T} is to continue scaling down L_{g}. Though, the above analysis and conventional relationship

between the f_T and L, *i.e.* derived using the drift-diffusion theory, might not be valid for GFETs with relatively short L_g due to the contribution of the ballistic mode in the charge carrier transport [103]. In particular, in the purely ballistic mode, the saturation velocity in the above relationship should be replaced by a Fermi velocity or virtual source injection velocity. [103, 104] For comparison, it was predicted that in short channel (submicron) HEMTs, the effective, *i.e.*, measured mobility must be much smaller than that in long channel devices, which was related to the ballistic transport. [105]

A relatively limited number of publications analyze the ballistic charge carrier transport in GFETs. Refs. [104, 106–108] reported the reduction of the effective mobility in the GFETs with L_g shorter than 1-2 μm. In Refs. [104, 107] the observed reduction of the mobility was associated with the quasi-ballistic transport, and by using the concept of μ_B [105], λ was found to be in the range of 175-400 nm, which can be seen in Fig. 5.7 a). However, the reported data and analysis do not allow for a conclusion to which extent the ballistic motion contributes to the total charge carrier transport in the GFETs. In comparison, in Ref. [78], μ in quasi-ballistic Si MOSFETs was analyzed using the concept of μ_B and the transmission formalism, which allowed for the evaluation of the transmission probability and estimation of the fraction of the total number of ballistic electrons [109], as shown in Fig. 5.7 b.

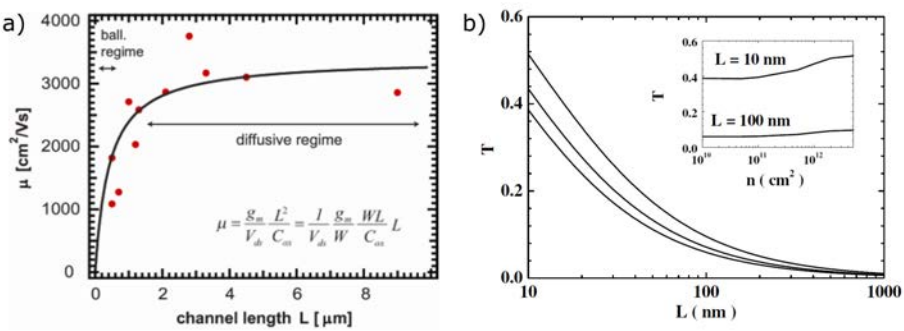

Figure 5.7: *a) Mobility versus channel length extracted for various graphene FETs assuming diffusive transport conditions [107]. b) Transmission coefficient, T, as a function of gate length L, for the electron concentration equal to 5×10^{10} cm^{-2}, 5×10^{11} cm^{-2} and 5×10^{12} cm^{-2} (from bottom to top). Inset shows T as a function of n for $L = 100$ nm (bottom) and 10 nm (top) transistor. [Figure from Ref. [78]]*

In **Paper D**, different gate geometries of GFETs were examined in the absence of a B-field, which shows typical dependencies of R_{total} on V_{GS} of the GFETs with $L_g = 0.2$ μm and 2 μm. Here the measured dependencies of the R_{total} on V_{GS} was used to evaluate μ_{eff} via fitting the dependencies by the drain-source resistance model, Eq. (4.5) presented in Ref. [73]. To evaluate if the μ in the transistors with different L_g show any L_g-dependence, and potentially ballistic transport, a model developed in Ref. [78] has been used. Initially, Eq. (4.5) can be used to calculate μ_{eff}. Then the model proposed in Ref. [78] can be used:

$$\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{c}}} + \frac{1}{\mu_{\text{B}}}, \tag{5.12}$$

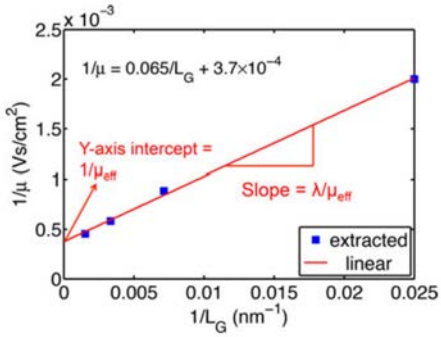

Figure 5.8: *Inverse of extracted mobility versus inverse of L_g. The extracted mobility is fit with a straight line. [Figure from Ref. [104]].*

where μ_c is the diffusive mobility (or collision mobility), *i.e.* the mobility that would be measured on long transistors, and is determined by all scattering mechanisms that are responsible for the diffusive motion of electrons in the channel. The μ_B can be expressed as

$$\mu_B = \frac{2eL_g}{\pi m v_F}. \tag{5.13}$$

One can rewrite Eq. (5.12) as

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_c}\left(1 + \frac{\lambda_B}{L}\right), \tag{5.14}$$

where $\lambda_B = \frac{\mu_c \pi m v_F}{2e}$ is characteristic length corresponding to L_g on which the ballistic motion becomes important for the mobility reduction: *e.g.*, if $L_g = \lambda_B$ then $\mu_{eff} = \frac{\mu_c}{2}$.

According to the theory of ballistic transport, one can define a transmission coefficient (T) that is equal to the probability that an electron moves between the source and the drain without being scattered, as

$$T = \frac{\lambda_B}{L + \lambda_B} \tag{5.15}$$

This coefficient is equal to the fraction of the total number of ballistic electrons and is a measure of the ballistic performance of a device [78].

Based on the discussion above, the following method of analysis of the ballistic transport in GFETs has been proposed: i) Plotting μ versus L, to demonstrate a dependence. ii) Plotting $\frac{1}{\mu}$ versus $\frac{1}{L}$ to find the μ_c at the intersection by extrapolating to $\frac{1}{L} = 0$, for Eq. (5.14), as in Fig. 5.8. iii) Find λ_B from the slop (see Eq. (5.14)). iv) Finding μ_B for each L_g using Eq. (5.12) and plotting μ_B versus L. v) Finally calculating T using Eq. (5.15) to plot T versus L_g, as in Fig. 5.7 b). This strategy gives a potential estimate of ballistic transport. The transmission for the devices in this study is presented in **Paper D** (in Fig. 5), where qualified predictions of ballistic transport for even shorted L_g can be made [49].

The dependencies of $f_{T\text{-ext}}$ and maximum frequency f_{max} on L_g have previously indicated that GFETs are very promising for down-scaling, particularly for developing amplifiers operating in the mm-wave frequency range. Though, little attention has been brought to the fact that down-scaling will eventually force us to enter the quasi-ballistic transport regime.

6

Summary of appended papers

This chapter presents a brief summary of the content of the appended papers, with a short description of my contribution to each paper.

Paper A

On the angular dependence of InP high electron mobility transistors for cryogenic low noise amplifiers in a magnetic field

In this paper, for the first time, it is demonstrated that the output drain current I_{ds} of a InP HEMT, when placed in a high magnetic field, can be significantly reduced due to strong geometrical magnetoresistance. We have investigated the angular dependence of the InP HEMT when oriented in a magnetic field up to 14 T at 2 K ambient temperature. A sharp angular dependence as a function of the magnetic field was measured for the output current of the InP HEMT. This was accurately described by a geometrical magnetoresistance expression for all angles and magnetic field strengths.

My contribution includes design, fabrication, and characterization of the HEMTs, interpretation of the results, and writing the manuscript.

Paper B

Low-field mobility and high-field velocity of charge carriers in InGaAs/InP high-electron-mobility transistors

In this paper, we report on study of the low-field mobility and high-field carrier velocity in InGaAs/InP HEMTs found via geometrical magnetoresistance in the wide range of

the drain fields, up to 2 kV/cm, at cryogenic temperature of 2 K. We observed, for the first time experimentally, the velocity peaks with peak velocity and corresponding field decreasing significantly with the transverse field. The low-field mobility and peak velocity are found to be up to 65000 cm^2/Vs and 1.2×10^6 cm/s, respectively. We also demonstrated, for the first time, that the low-field mobility and peak velocity reveal opposite dependencies on the transverse field, indicating the difference in carrier transport mechanisms dominating at low- and high-fields.

My contribution includes design, fabrication, and characterization of the HEMTs, analysis, and interpretation of the measured data, development of the model of the charge carrier velocity in the InP HEMTs, and writing the manuscript.

Paper C

Geometrical magnetoresistance mobility in graphene field effect transistors

In this paper, we present a study on low-field charge carrier transport, e.g., the mobility, of a graphene field effect transistors using the method of geometrical magnetoresistance. Complete transistors were measured at room temperature and under a perpendicular magnetic field. We show that measuring the geometrical magnetoresistance can be a method of choice for accurate direct evaluation of mobility in GFETs. We also compare our findings with already existing and commonly used models for field effect transistor mobility.

My contribution includes design, fabrication, and characterization of the GFETs, interpretation, and modeling of the results, error analysis, and writing the manuscript.

Paper D

Mobility and quasi-ballistic charge carrier transport in a graphene field-effect transistor.

In this paper we present a study on charge carrier transport in GFETs with gate lengths ranging from 2 μm down to 0.2 μm applying a model of the quasi-ballistic charge carrier transport. The analysis, in particular, indicates that at the gate length of 0.2 μm the fraction of the carriers moving ballistically can be up to 60 %. Our findings can be used as a guide for further development of the GFETs with submicron gate length for high-frequency applications.

My contribution includes design, fabrication, and characterization of the GFETs, analysis of the measured data, applying the quasi-ballistic transport model, and writing the manuscript.

7 Outlook

Paper A reports on studies of angular dependencies of the dc characteristics of the HEMTs in the inclined B-field. As it is shown in Section 5.2 by comparison with MOSFETs, the HEMTs reveal superior performance as a magnetic field sensor, mainly because of inherently high mobility. Therefore, an important continuation of the research would be further development of the HEMTs, specifically as magnetic field sensors for various advanced and emerging applications.

The findings of studies of the low-field mobility and high-field velocity of the charge carriers in HEMTs reported in the **Paper B** can play an essential role in further development of the high-performance HEMTs, in particular, for applications in the LNAs. The predicted dependence of the transit frequency on the longitudinal and transient fields is important to confirm experimentally via microwave measurements. In future work, the gMR method can be applied to analyze the InGaAs/InP HEMTs with different gate lengths, down to 60 nm, to study quasi-ballistic charge carrier transport, analyzing both dc and microwave performance.

Studies reported in **Paper C** showed that the mobility in the GFETs can be directly characterized and studied using the gMR effect. The method is free from the limitations of other approaches since it does not require an assumption of constant mobility and the knowledge of the gate capacitance. Further development of graphene field-effect transistors (GFETs) for high-frequency electronics requires accurate evaluation and study of the high-field carrier velocity, which directly defines the high-frequency performance of the GFETs. Therefore, future research can extend the gMR method for evaluating the saturation velocity in GFETs, *i.e.*, similarly as in **Paper B**.

Paper D reports on the study of the charge carrier transport in GFETs with gate lengths ranging from 2 μm down to 0.2 μm by applying a quasi-ballistic transport model. It is shown that at the gate length of 2 μm approximately 20 % of the charge carriers

are moving without scattering, while at the gate length of 0.2 μm this number increases to above 60 %. It was concluded that the conventional relationship between the transit frequency and gate length, *i.e.*, derived using the drift-diffusion theory, might not be valid for GFETs with relatively short gate lengths due to the contribution of the ballistic mode in the charge carrier transport. In particular, in the purely ballistic mode, the saturation velocity should be replaced by a Fermi velocity or virtual source injection velocity. Therefore, an important continuation of this work would be the development of theory and experimental investigation of the effect of the quasi-ballistic charge carrier transport on the high-frequency performance of the GFETs. Similar work should be done on HEMTs.

A

Fabrication of AlGaAs/InGaAs InP HEMT

A conventional top-down approach has been used, relying on the patterning of thin films via planar lithography and wet etching of an InP-based heterostructure. Fabricating an InP HEMT requires numerous process steps. This chapter briefly describes the various micro- and nanofabrication techniques used in this work. It is finalized with a description of the consecutive order of fabricating an InP HEMT device.

The specific transistors used in this thesis were all fabricated from the same type of heterostructure. The main results are on a heterostructure with a channel thickness of 15 nm. However, devices with 7 nm were also fabricated to investigate the influence of channel thickness on the output and transfer characteristics.

The gate materials for most components were Titanium, Platinum, and Gold, and for the contacts, a metal alloy of Nickel, Germanium, and Gold. Although, additional experiments were done varying these materials to investigate the potential of using non-alloyed contacts.

Cleaning Process: The first step of the fabrication process consists of adequately cleaning the substrate. It is also essential that the substrate surface is kept as clean as possible in between fabrication steps to avoid possible contamination and impurities compromising the device's performance.

An essential and crucial first step is to place the chip in warm Acetone, 60-65^{o}C, for 5-10 minutes, which will dissolve and remove old resist often used as a protection, *e.g.* when stored, during transport, or dicing. After dissolving the resist in Acetone, the chip is rinsed in IPA (isopropanol or isopropyl alcohol) to avoid leftover stains from Acetone. The chip should be blow-dried with nitrogen immediately after IPA rinsing, which dries the surface fast and homogeneously. One should examine the chip in an optical microscope to ensure the surface is cleaned correctly; if not, this process must be

repeated.

Lithography

The fabrication process of nano-devices heavily relies on lithography due to the need for patterning thin films to create small structures. There are two more common lithography techniques based on the source of exposure: electron-beam lithography and photolithography using deep UV light. In both cases, the chip is spin-coated with a polymer resist and then exposed to the electron beam or UV radiation. The resist goes through a chemical change when exposed to light or electron beam, either by forming or disrupting cross-links, allowing detailed patterns to form. This project used laser and electron beam lithography and is described further down. Subsequently, parts of the resist should be developed, enabling the creation of the desired pattern.

Spin Resist: Before patterning, the first step in any lithography process is adding the proper resist(s): Chip is placed on a spinner and held down by a vacuum. 2-3 droplets of resist (depending on sample size) are added to the surface using a pipette. The chip is spun for 30-60 seconds, with a chosen speed set in rotations per minute (rpm) and acceleration time in milliseconds (ms). For a thinner layer of resist, the rpm value should be higher. The resist will ideally be equally distributed on most of the surface, leaving a slightly thicker layer of resist at the edges due to surface tension. An extra exposure of the edges can remove this. Although, keeping the pattern concentrated in the middle of the chip circumvents this problem, and no extra exposure is needed. After being spun, the chip must be baked on a hot plate to solidify the spun resist and increase the adhesion.

The thickness of the spun resist must be greater than the device height (mesa[1] and contacts included) or else there will be a risk for short cuts and high risk of lift-off failure later on.

Resists: In the critical step of creating the gate pattern, the spin resist process needed to be done twice, once with resist *ZEP520 1:1* followed by resist *UV60 0.75*. The reason for using two different resists is to create an undercut when developing one resist after another, as described and illustrated in Fig. A.1. The two resists also vary in properties such as viscosity, thickness, and sensitivity.

Patterning: The area to expose is determined by the designed mask, which can be drawn and converted from a suitable software *e.g.* AutoCAD. The masks drawn in this project were based on the same template, only varying the gate geometry. The mask was designed to have two layers for the gate. One for high current and one for low, to not overexpose the fine area for the gate foot, enabling higher precision L_g of down to 60 nm.

[1] mesa = Latin for table and refers to the structure that the device stands on, up above the substrate, *i.e.*, the substrate is etched back to leave the transistor isolated from surrounding material.

Maskless Laser lithography: Maskless laser lithography is a direct write system and is an excellent alternative to mask aligners for optical lithography, where a high-resolution laser is used to expose the photoresist. The minimum achievable feature size is comparable to standard UV contact lithography ($\sim 1\,\mu m$), which can be a limitation if more minor, more accurate patterns are required. The benefits, however, are flexibility and faster writing time.

Electron Beam Lithography: An electron beam lithography system can be used to overcome the resolution limit of fast photolithography. The system consists of an electron gun, magnetic lenses, a collimator, a beam blanker, and deflecting coils, enabling smaller and more accurate patterning. In the electron gun, steam of electrons is extracted from a filament and accelerated by an electric field. The magnetic lenses and the collimator then focus the electrons. The position of the focused electron beam can then be controlled by using the deflecting coils. Vector scanning the beam over the substrate surface covered with a resist sensitive to electrons will create the wanted pattern. It can be directly "written" without the need for any mask. Dose tests can be performed to obtain optimal feature sizes, specifically important for gate lithography. A range of different electron beam intensities is then evaluated based on how close the lithography results are to the drawn features.

Developing Resist: When the chip, covered by resist, has been exposed and patterned in a lithography step, it needs to go through a development step, where the exposed (or unexposed if inverted/negative mask was used) areas are developed and removed. Depending on what resist was used and what details the recipes of the lithography steps contained, the solvents for developing can differ, but the process is the same.

For developing UV60 and ZEP520, creating the pattern for the gate, MF-CD26 and O-Xylene were used. The bottom resist is more sensitive; hence is developed with an enhanced undercut, *i.e.* the top layer extends past the opening in the bottom layer. Creating an undercut ensures an easier lift-off process later on, as well as a precise vertical slop if the next step is a metal deposition. This can be seen in Fig. A.1 (c) to (e).

Thin Film Deposition:

After resist-development, the sample is ready for metal deposition. The sample is mounted in a vacuum chamber of an electron beam multi-material evaporator. Then the metal of choice can be evaporated onto the chip, as shown in Fig. A.1 (e).

The tool used in this fabrication process step was *Evaporator - Lesker PVD 225 nr1 (451*, a multi-material evaporator.

Lift-Off: When the chip has been under deposition in the evaporation chamber, the whole surface is covered with a metallic layer. Underneath the metallic layer, areas of resist can be left, which should be removed to remove the excess metal. This process is called lift-off. The schematics of the steps included in a Lift-off process are illustrated in Fig. A.1 (f) below. Like the cleaning process, the chip is put in warm Acetone, which will

dissolve the resist layer on the substrate and lift off the excess metal. The chip should be rinsed in IPA and blow-dried with a nitrogen gun as a final step.

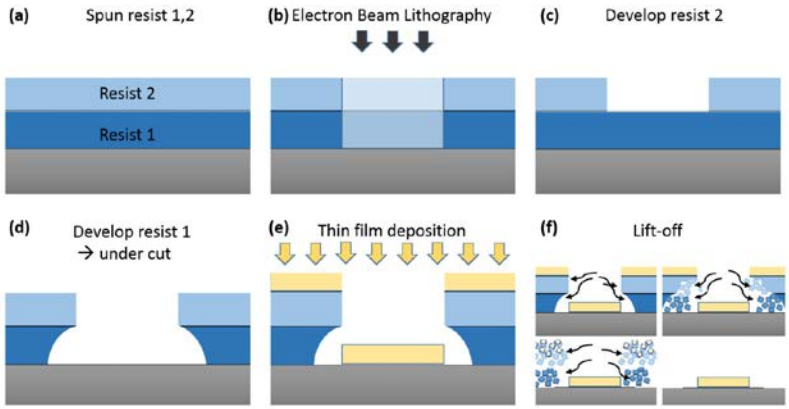

Figure A.1: *Schematic illustration of (a) prepared substrate spun with two different resists and (b) patterned via electron beam lithography. In (c) the top resist, resist 2, has been developed, followed by (d) where the second resist has been developed, leading to a undercut. (e) shows when a thin metal film has been deposited on the substrate and (f) illustrates the lift-off process, the final step in the fabrication.*

Dry Etch; Reactive Ion Etch: The final step in the cleaning process is resist-stripping. The chip should be put in a reactive ion etcher that uses oxygen plasma to clean the chip. The plasma produces energetic neutrally charged free radicals that react at the surface of the substrate. When the plasma contains oxygen, it oxidizes the material and facilitates removal.

Process summary of process steps for InP HEMTs:

- Laser lithography (MESA)
- Wet etching (MESA)
- Photoresist stripping (MESA)
- Measurement (MESA step height)
- Ebeam lithography (OHM)
- Oxide removal and Metal deposition (OHM)
- Lift-off (OHM)
- Annealing (OHM)

- Electron Beam Lithography (GATE)
- Gate recess (GATE)
- Oxide removal and Metal deposition (GATE)
- Lift-off (GATE)
- Thin film deposition (PASSIVATION)
- Laser lithography (PASSIVATION)
- Etch (PASSIVATION)
- Photoresist stripping (PASSIVATION)
- Laser lithography (MET1)
- Oxide removal and Metal deposition (MET1)
- Lift-off (MET1)
- Laser lithography (SPAN)
- Metal deposition (SPAN)
- Laser lithography (MET2)
- Metal deposition (MET2)
- Photoresist and seed layer removal (PLATING)

B

Fabrication of GFETs

This chapter presents the main recipe for fabrication of the GFETs in this study, with reservation for minor changes or adjustments as this process is under constant development.

1. prepare graphene

- After easy transfer, dry graphene on hotplate, first low temp. Approx 47 deg. C until color change, then increase to 150-160 deg. C to get rid of water bubbles.
- Place graphene in vacuum chamber for 2-3 days to dry more and get rid of the final water under or on top
- 45 min- acetone 70 deg. C, then 45 min. in IPA 70 deg. C

2. Oxide layer

- Aluminum oxide layer in lesker #1, with settings: 10 Å of Al, preasure 2-1.4e-6
- Oxidation 5 min 160deg. C
- REPEAT the steps above 5 times.
- Chip on hotplate for 1,5 h to oxidize the Al.

2. E-beam MARKS

- Spin resist step 1) MMA (8.5) EL10, 1 min, 3000 rpm (400 nm)

- Bake 5 min at 160 deg. C
- Spin resist step 2) ARP6200.13 1:1, 1 min, 3000 rpm (150 nm)
- Bake 5 min at 160 deg. C

– EXPOSE –

- Develop exposed resist step 1) N-Amylacetate 45s + blow dry with N_2 gun
- Verify alignment in microscope
- Develop resist step 2) MIBK:IPA 1 min.+20s + blow dry
- Verify alignment in microscope
- Remove resist in RIE plasma etch 50 W, 10s
- Remove Al2O3 in 1:10 BOE:H2O for 5 sek, rinse in H_2O and blow dry with N_2.
- Remove graphene with RIE plasma etch 50 W, 5s
- Evaporate (marks) Ti/Au 100Å/1800Å
- Lift-off in Acetone 10 min. at 75 deg. C
- Rinse in new acetone, then Rinse in IPA

3. E-beam CONTACTS

- Spin resist as previously (e-beam MARKS)
- Develop 1) n-amylacetate 45s + blow dry with N_2
- 2)) MIBK:IPA 1:1 for 1 min. 10s
- Verify alignment in microscope
- Boe:H_2O 1:10 20s
- Rinse in water for 20-30 sek
- Evaporate Ti/Pd/Au:10Å/150Å/2500Å for contacts
- lift-off over night in Acetone

4. MESA

- Rinse in IPA
- spin resist ma-N2403 1 min. 3000 rpm (acc 1500)
- bake on hot-plate 1 min. at 90 deg.C

– E-beam exposure: dose 170, step size 20, 10nAap7 –

- Develop MF-24A; 30 s immediately wash in H2O for some time 1 min.
- Clean from resist in RIE plasma etch 10 s
- BOE:H2O 1:10 9-10 s to etch aluminum oxide
- removal of graphene with RIE plasma etch 50 W, 10 s
- Wash off resist in warm (70deg. C) Acetone 5min.
- wash off acetone with IPA (also warm) 2 min.
- Repeat 5x evaporation of Al 10Å put on hotplate for 5 min. at 160deg. C to for gate oxide
- again repeat 5x evaporation of Al 10Å put on hotplate for 5 min. at 160deg.C

5. Gate lithography

- spin resist 1) MMA(8.5)EL10 1 min. 2900rpm (410 nm)
- Bake 5 min. at 160 deg. C
- spin resist 2) ARP6200.13 1:1 1 min. 3000rpm (150 nm)
- Bake 5 min. at 160 deg. C

– READY for e-beam; GATE, dose 390 and 10Aap7 –

- Develop 1) N-Amylacetate 45s + blow dry with N2
- develop 2) MIBK:IPA 1:1 120s + blow dry + N2
- Evaporate Ti/Au 100Å/2900Å for gate
- Lift-off: acetone for 10 min at 75 deg. C
- Rinse in acetone, then rinse in IPA

C

Repeatability analysis and error analysis

This chapter follows an error analysis of the dc data, parameter extraction, and de-embedding methods used in **Paper B** and **C**, as well as some abundant material related to **Paper D**.

Error propagation in results of Paper B

To calculate the error propagation in the InP HEMT results of **Paper B** the following analogy have been used. Considering

$$x = \frac{a^l b^m}{c^n}, \tag{C.1}$$

it can be proved that:

$$\frac{\Delta x}{x} = l\frac{\Delta a}{a} + m\frac{\Delta b}{b} + n\frac{\Delta c}{c} \tag{C.2}$$

Applying this to the gMR method with the main equation:

$$\mu_{gMR} = \frac{1}{B}\sqrt{\frac{R_B}{R_0} - 1}, \tag{C.3}$$

where R_B (and R_0) can be calculated as $R_{B(0)} = R_{DS} - R$, where $R = \frac{V_D}{I_D}$ is the series resistance at $V_G = 0.4$ V. Which, for

$$\delta\mu_{gMR} = \frac{\Delta\mu_{gMR}}{\mu_{gMR}} = \frac{1}{2}(\delta R_B + \delta R_0), \tag{C.4}$$

and the highest $V_{DS} = 0.35$ V , gives

$$\delta R_B = \frac{\Delta R_B}{R_B} = \frac{10.52 - 10.3}{10.52} = 0.021 \tag{C.5}$$

$$\delta R_0 = \frac{\Delta R_0}{R_0} = \frac{9.22 - 9.0}{9.22} = 0.024 \tag{C.6}$$

$$\delta \mu_{gMR} = \frac{1}{2}(0.021 + 0.024) = 0.0225. \tag{C.7}$$

Using μ at $V_g = 0.16$ V then results in: $\Delta\mu_{gMR} = \delta\mu_{gMR} \times \mu_{gMR} = 0.0225 \times 0.78 = 0.01755$ m^2/Vs, *i.e.*, the absolute error is comparable or less than the marker size in Fig. 2 and Fig. 3 in **Paper B**.

Doing the same for the lowest $V_{DS} = 0.05$ V gives:

$$\delta R_B = \frac{\Delta R_B}{R_B} = \frac{9.5 - 9.3}{9.5} = 0.021 \tag{C.8}$$

$$\delta R_0 = \frac{\Delta R_0}{R_0} = \frac{6.496 - 6.496}{6.496} = 0 \tag{C.9}$$

$$\delta \mu_{gMR} = \frac{1}{2}(0.021 + 0) = 0.0105, \tag{C.10}$$

Which together with μ at $V_g = 0.16$ V results in: $\Delta\mu_{gMR} = \delta\mu_{gMR} \times \mu_{gMR} = 0.0105 \times 6.5 = 0.06825$ m^2/Vs, *i.e.*, the absolute error is also here comparable or less than the marker size in Fig. 2 and Fig. 3 in **Paper B**.

Error analysis of results in Paper C

Since several different GFETs on both samples have been measured in **Paper C**, a comprehensive error analysis could be made and is presented in this section, with subsections of 1) assuming that variations between measurements were the only source of error, 2) error propagation in the gMR mobility considering both deviations between measurements as well as parameter extraction, and 3) the influence of light versus dark environment on measurements.

Error propagation in mobility only considering measurement deviations

For error analysis on sample 1, in **Paper C**, 60 sweeps on the same device were done, enabling thorough sensitivity analysis of the device and the absolute error. This could be done using the standard deviation, in Eq. (C.11)

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n}(\overline{x} - x_i)^2}{n}} \tag{C.11}$$

where $\overline{x}$ is the mean value, x_i is a single value of R_{DS}, and n is the number of observations, in our case, the number of sweeps. After obtaining the standard deviation, the standard error of the mean can be calculated as $SEM = \frac{\sigma}{\sqrt{n}}$, which is required to find the confidence interval $CI = \overline{x} \pm z * \frac{\sigma}{\sqrt{n}}$, where z is the confidence level, here set to 95 %. The confidence

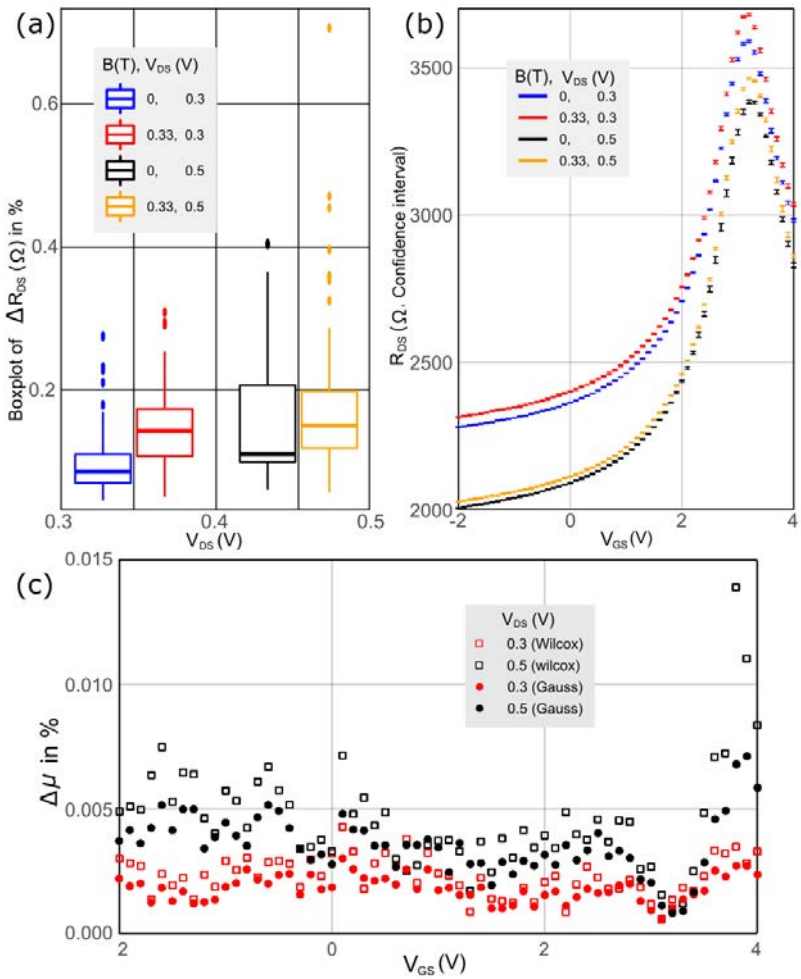

Figure C.1: *a) Shows a box-plot of the relative error* $\frac{\Delta R_{DS}}{R_{DS}}$ *as a function of drain voltage 0.3 and 0.5 V, respectively. b) presents the measured data with error-bars in CI and c) the propagated error from R in mobility in percentage.*

interval[1] could then be used to find the error of propagation in mobility, as in Eq. (C.12) below:

$$\Delta\mu = \frac{\delta\mu}{\delta R^B_{DS}}\Delta R^B_{DS} + \frac{\delta\mu}{\delta R^0_{DS}}\Delta R^0_{DS} \tag{C.12}$$

where ΔR^0_{DS} was found by taking the highest values of the CI and subtracting the mean (or vice versa for the lowest values of the CI).

Fig. C.1 a) shows a box-plot of $\frac{\Delta R^0_{DS}}{R^0_{DS}}$ considering the data as a non-symmetric distribution, using a non parametric test, *Wilcox test* of the confidence interval, in percentage. Fig. C.1 b) shows the measured data presented with error bars of the confidence interval, and Fig. C.1 c) shows the error propagation of R_{DS} in mobility, in percentage. This analysis shows that the reproducibility in sample 1 is very high, and the measurement error is tiny.

Error propagation in gMR mobility due to measurement deviations and uncertainties in parameter extraction

Assuming that the error in the gMR mobility is defined mainly by errors in the resistances of the gated regions of the GFET channel and that the errors with and without magnetic field are equal, *i.e.*, $\delta R^B_{ds} = \delta R^0_{ds}$. Uncertainty in the magnetic field is assumed to be relatively low. The δR^0_{ds} is composed of the errors in drain resistance (δR_{0DS}) and series resistance (δR_0) and assuming propagation of errors can be expressed as

$$\delta R^0_{ds} = \sqrt{(\delta R_{0DS})^2 + (\delta R_0)^2}. \tag{C.13}$$

The drain current instabilities cause an error in the drain resistance due to the trapping/de-trapping of the charge carriers. The error in the series resistance is caused by uncertainty in the linear fitting by a software algorithm.

It is assumed that the uncertainties in magnetic field and intrinsic channel resistance are: $B \pm \delta B$, $R^B_{ds} \pm \delta R^B_{ds}$ and $R^0_{ds} \pm \delta R^0_{ds}$, then the partial contributions are as follows:

$$|\delta\mu_{B(0)}| = \left|\frac{\partial\mu}{\partial B}\right|\delta B = \frac{\delta B}{B^2}\sqrt{\frac{R^B_{ds}}{R^0_{ds}} - 1} = \frac{\delta B}{B}\mu \tag{C.14}$$

$$|\delta\mu_{R^0_{ds}}| = \left|\frac{\partial\mu}{\partial R^B_{ds}}\right|\delta R^B_{ds} = \frac{\delta R^B_{ds}}{2BR^0_{ds}}\frac{1}{\sqrt{\frac{R^B_{ds}}{R^0_{ds}} - 1}} = \frac{\delta R^B_{ds}}{2(R^B_{ds} - R^0_{ds})}\mu \tag{C.15}$$

$$|\delta\mu_{R^B_{ds}}| = \left|\frac{\partial\mu}{\partial R^0_{ds}}\right|\delta R^0_{ds} = \frac{\delta R^0_{ds}}{2B}\frac{R^B_{ds}}{(R^0_{ds})^2}\frac{1}{\sqrt{\frac{R^B_{ds}}{R^0_{ds}} - 1}} = \frac{\delta R^0_{ds}}{2(R^B_{ds} - R^0_{ds})}\frac{R^B_{ds}}{R^0_{ds}}\mu \tag{C.16}$$

[1] The confidence interval is the range in which a new mean would fall, with a probability of 95 % (i.e., z = 1.96) provided an identical set of measurements are performed (i.e., using the same amount of sweep under the same conditions)

Thus the relative error of propagation:

$$\frac{\delta\mu}{\mu} = \sqrt{\left(\frac{\delta\mu_{B(0)}}{\mu}\right)^2 + \left(\frac{\delta\mu_{R^B_{ds}}}{\mu}\right)^2 + \left(\frac{\delta\mu_{R^0_{ds}}}{\mu}\right)^2}, \tag{C.17}$$

together with Eq. (C.14), (C.15) and (C.16) is calculated as:

$$\sqrt{\left(\frac{\delta B}{B}\right)^2 + \left(\frac{\delta R^B_{ds}}{2(R^B_{ds} - R^0_{ds})}\right)^2 + \left(\frac{\delta R^0_{ds}}{2(R^B_{ds} - R^0_{ds})}\frac{R^B_{ds}}{R^0_{ds}}\right)^2} \tag{C.18}$$

Here, the relative error in the magnetic field is assumed small compared to the uncertainty in intrinsic channel resistances and possible error obtained during the linear fitting of series resistance. Also, assuming $\delta R_B = \delta R_0$, the uncertainty and relative error in gMR mobility due to propagation of errors from variations in measurements and parameter extraction can be expressed as

$$\frac{\delta\mu_{gMR}}{\mu_{gMR}} = \frac{\delta R^0_{ds}}{R^0_{ds}} f\left(\frac{R^B_{ds}}{R^0_{ds}}\right) \approx \frac{\delta R^0_{ds}}{2(R^B_{ds} - R^0_{ds})}\sqrt{1 + \left(\frac{R^B_{ds}}{R^0_{ds}}\right)^2}. \tag{C.19}$$

In specific, the raw data and the linear fitting for sample 2 gave $\delta R^0_{ds} = 0.22\ \Omega$. From sample 1, the δR_{0DS} values were calculated from standard deviations via statistical analysis of 60 gate voltage sweeps and found to be below 0.2 % in the whole range of the gate voltage. Through the error analysis above, using Eqs. (C.13) and (C.19), the relative error in the gMR mobility could be calculated to less than 6 % for the worst-case scenario of sample 2 and less than 8 % for the worst case scenario of the more scattered data from sample 1, in the whole range of gate voltages.

Light versus dark measurements

As part of the error analysis for sample 2 in **Paper C**, many sweeps were repeated under identical conditions to investigate reproducibility. See Fig. C.2 (a)-(b) showing the largest deviation between identical sweeps. These repeated sweeps confirm the largest deviations between measurements being significantly smaller than the variation observed when introducing a magnetic field; hence our measurements on sample 2 have high reproducibility.

As another part of the error analysis, sample 2 was measured under various light settings to investigate the impact of the degree of illumination on the dc characteristics. See Fig. C.2 (c)-(d) for R_{DS} as a function of V_{GS} where sample 2 was measured in an environment with three different light settings: 0, 1 and 2. Measurement sweeps with no light are denoted as 0 (zero), sweeps exposed to light only from the lit-up room are denoted as 1, and sweeps exposed to very bright light where sample 2 was illuminated by the optical microscope above are denoted as 2. Forward and backward sweeps have also been done, confirming the hysteresis is negligibly small, indicating very stable devices.

The comparative measurements of the transfer characteristics in the dark and illuminated environment showed that variations of the drain resistance remain within the

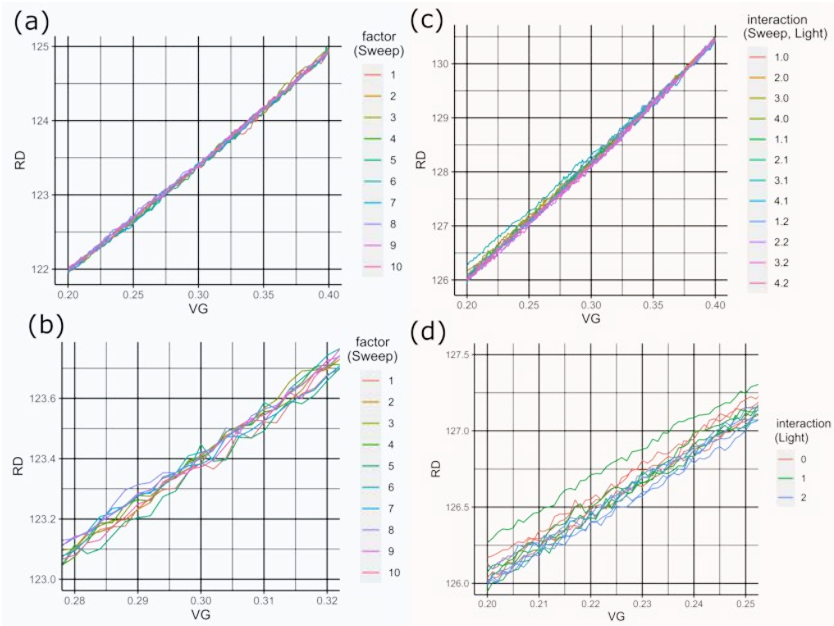

Figure C.2: *Error analysis (a) 10 sweeps, same device (b) 10 sweeps same device, zoomed in. (c) Dark/room light/illuminated by microscope, 12 sweeps (4 of each). (d)Dark/room light/illuminated by microscope, 12 sweeps (4 of each), but zoomed in.*

errors of measurements. This allowed for excluding the possible effects of the persistent photo-conductivity traps, [60] caused by screening the light by the magnet and confirms that the charge carrier transport under magnetic field is governed mainly by the gMR effect.

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